TEXAS INSTRUMENTS

Modeling the ADS61XX family of components through IBIS

Texas Instruments

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IBIS modeling of buffers in ADS61XX family

This document describes the method used to model the I/O buffers in ADS61XX family of products through IBIS. (Sections 1-5 describe the model creation methodology and section 6-7 illustrates spice decks for use in simulations. Section 8 describes the contents of the model file)

The buffers modeled are:

1. 3-state-CMOS output buffer at the output data pin
2. 3-state-CMOS output buffer at the output clock pin
3. Input buffer for external clock input
4. 3-state- LVDS (DDR) output buffer at the output data and clock pins

The CMOS and the LVDS output buffers are 3-state buffers so that only one of them is activated depending on what mode of output is chosen.

1. 3-state CMOS buffer

3-state CMOS buffer output is available for both clock as well as data at different drive current strengths. There are 4 drive strength modes

1. default strength
2. low strength
3. high strength mode 1
4. high strength mode 2

The supply voltage range permissible for the CMOS buffer is wide (1.8V to 3.6V). Hence for better results this range has been split and 2 sets of models are generated for each drive strength mode, namely 1.8-2.7 and 3.0-3.6. The methodology for generating the CMOS buffer models for various modes is described below.

The structure of the CMOS buffer in ADS61XX family of products is shown in Figure 1.1. The structure can be directly mapped to the structure of a 3-state output buffer as specified by the IBIS standard. So its model shall consist of

1. I-V characteristics of Power and Ground clamp as well as the pull-up and pull-down circuits.
2. V-t characteristics of output pin

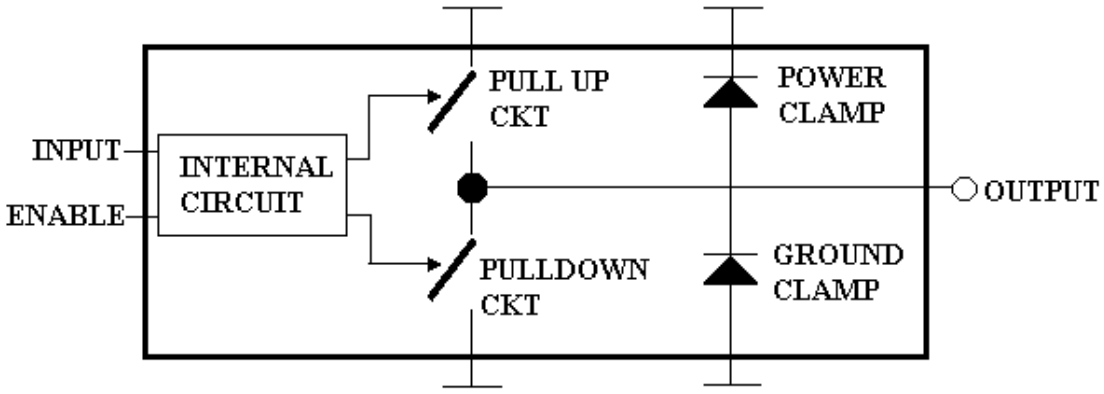

Figure 1.1 3-state CMOS output buffer structure

Voltage levels of 0 Volts and 1.8 Volts correspond to logic levels of '0' and '1' at HI and LO at the input of the buffer.
In following description VDD values at typ, min and max corners are (2.5, 1.8, 2.7) and (3.3, 3.0, 3.6) for the 2 sets of models respectively

1.1 V-I tables for Pull-up and Power clamp

The Circuit setup used to extract the pull-up and power clamp data is shown in Fig. 1.2 Two sets of measurements is taken.

1Measurement (a)

- Input is at HI
- Enable pin is at LO to deactivate output
- The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0).
- The current flowing through VPIN is tabulated

2Measurement (b)

- Input is at HI
- Enable pin is at HI to activate output
- The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0), where VDD = 3.3V, 3.0V or 3.6V (for typ, min and max corners).
- The current flowing through VPIN is tabulated

The current measurements in (a) (for VPIN = VDD to 2VDD) are the Power clamp data, as only clamp circuits are active. The current measurement in (b) is sum of clamp circuit current and pull-up circuit current. So (b) - (a) gives the pull-up data.

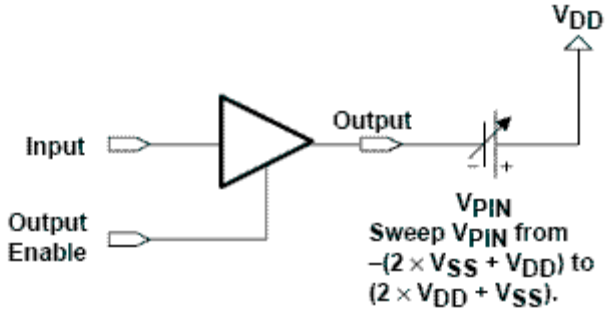

Figure 1.2 Circuit setup to extract Pull-up and Power clamp data

1.2 V-I tables for Pull-down and Ground clamp

The Circuit setup used to extract the pull-down and ground clamp data is shown in Fig. 1.3. Two sets of measurements are taken.

1.Measurement (a)

- Input is at LO
- Enable pin is at LO to deactivate output
- The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0)
- The current flowing through VPIN is tabulated

2.Measurement (b)

- Input is at LO
- Enable pin is at HI to activate output
- The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0)
- The current flowing through VPIN is tabulated

The current measurements in (a) (for VPIN = -VDD to VDD) are tabulated as the Ground clamp data, as only clamp circuits are active. The current measurement in (b) is sum of clamp circuit current and pull-down circuit current. So (b) - (a) gives the pull-down data.

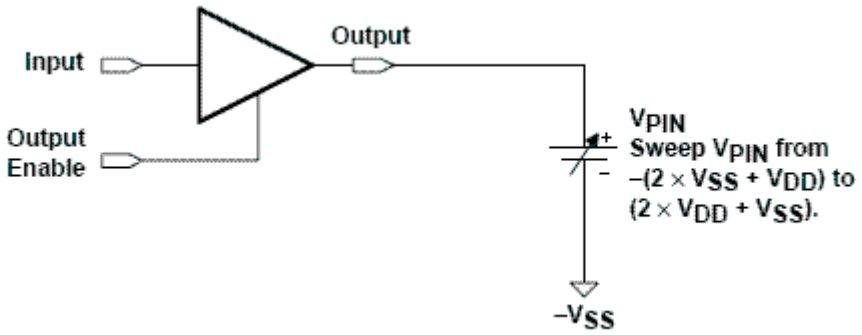

Figure 1.3 Circuit setup to extract Pull-down and Ground clamp data

1.3 Generating the V-t Data

Four V-t tables are generated using the setup shown in Figure 1.4. A step signal is given at input at voltage waveform at output is tabulated

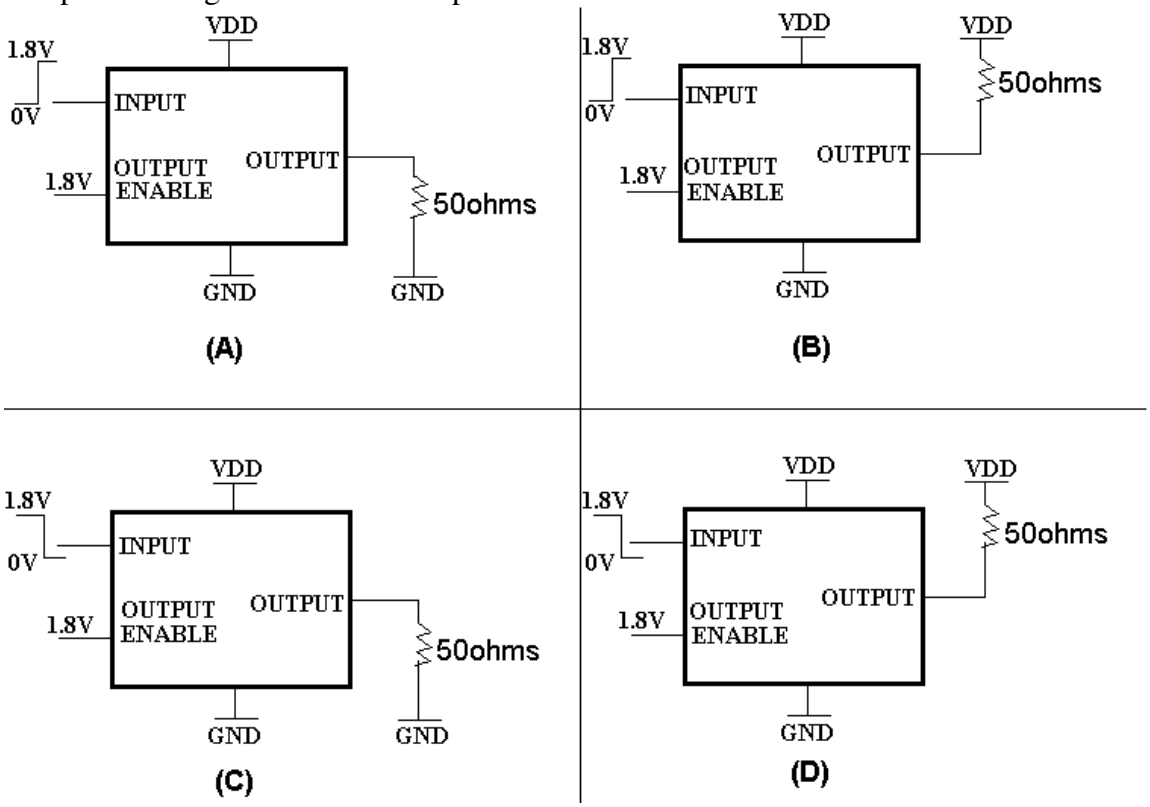

Figure 1.4 Circuit setup to extract the four V-t tables

1.4 Comparison of IBIS model with the actual circuit

To check how well the IBIS models shall model the actual circuit, the following SPICE simulations were done. The circuit set up is shown in Figure 1.5. In the first simulation the SPICE netlist of the buffer is used and in the second simulation the IBIS model of the buffer is used.

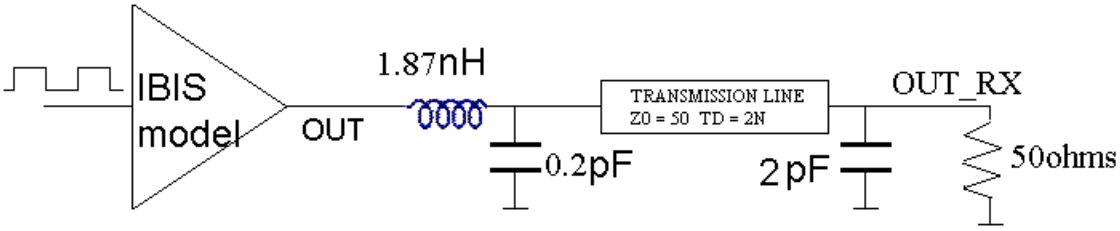

Figure 1.5 Circuit set up used in simulations for validation of the model

Simulations were done with different values of the delay for the transmission line.

Figure 1.6 shows a comparison of the HSPICE simulation results obtained from the IBIS model with those from the actual circuit.

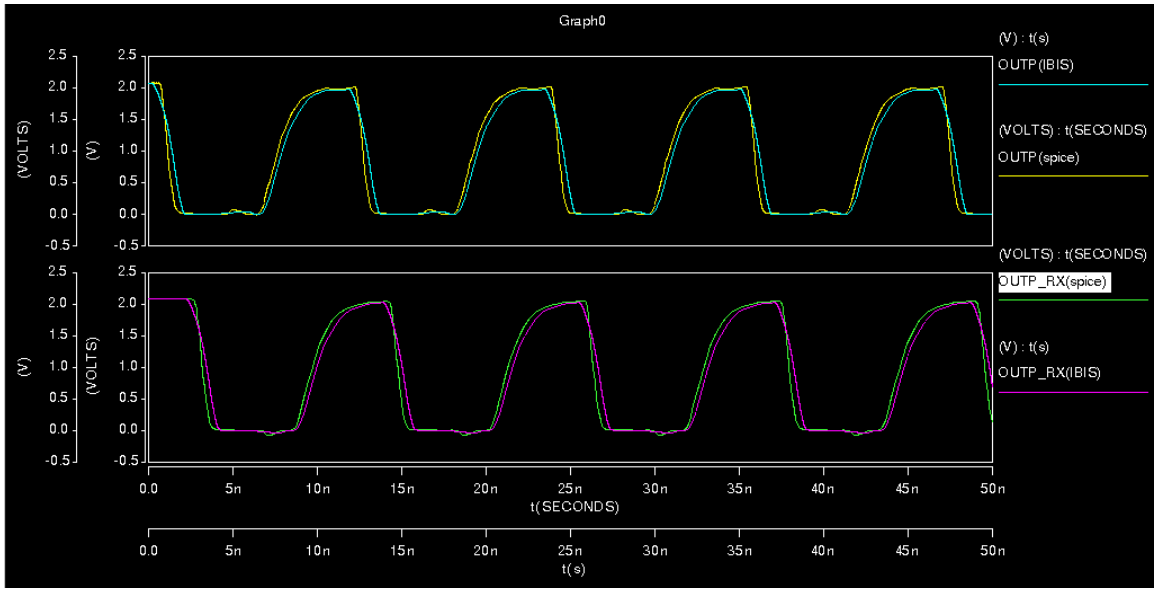

Figure 1.6 Output waveforms of simulation with IBIS model vs. full-transistor net list

As is observed, there is a close match between the actual circuit and its IBIS model.

2. LVDS BUFFER (3-state)

Since the LVDS buffer has differential inputs and differential outputs, some additional considerations are involved while modeling it through IBIS.

2.1 LVDS buffer architecture

The internal structure of the LVDS buffer in ADS61XX family of products is shown in Figure 2.1. For simplicity the enable pin has not been shown. HI and LO refer to the differential input to the buffer. Voltage levels of 0 Volts and 1.8 Volts correspond to logic levels of '0' and '1' at HI and LO. LOUTP and LOUTM are the differential output of the buffer. The buffer consists of two current sources (one NMOS and one PMOS) and a set of four switches to change the direction of the current flowing into the external load.

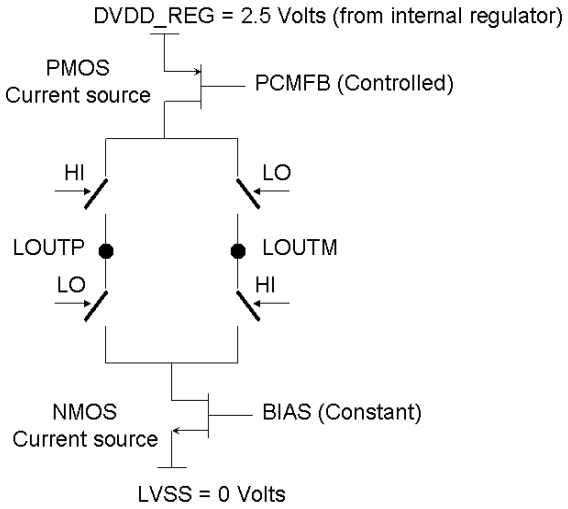

Figure 2.1 Internal structure of LVDS buffer

While the NMOS current source is a constant current source (its value set by one of the eight current mode settings), the PMOS current source is controlled through a feedback loop as shown in Figure 2.2.

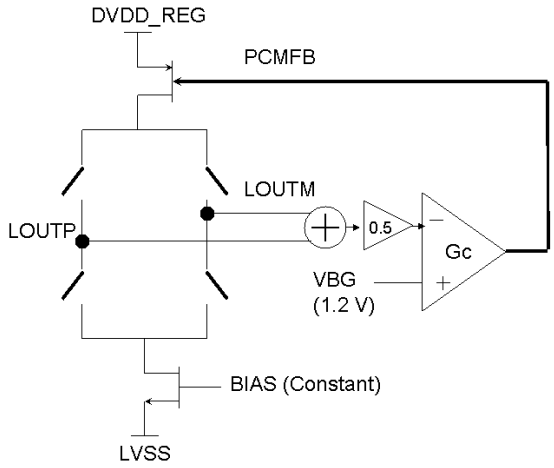

Figure 2.2 Controlling the PMOS current source

The PMOS current source is controlled so as to maintain the output common mode voltage of the buffer equal to a reference voltage of 1.2 Volts.

2.2 Extracting V-I tables

The setup for the pull-down and ground clamp data is as shown in Figure 2.3. A 50 Ohm resistor connects LOUTM to the common mode voltage of VBG=1.2 Volts. The measurements used for extracting the pull-up, pull-down, power clamp and the ground clamp data are very much similar to the method described for CMOS 3-state buffer in section 1.1 .

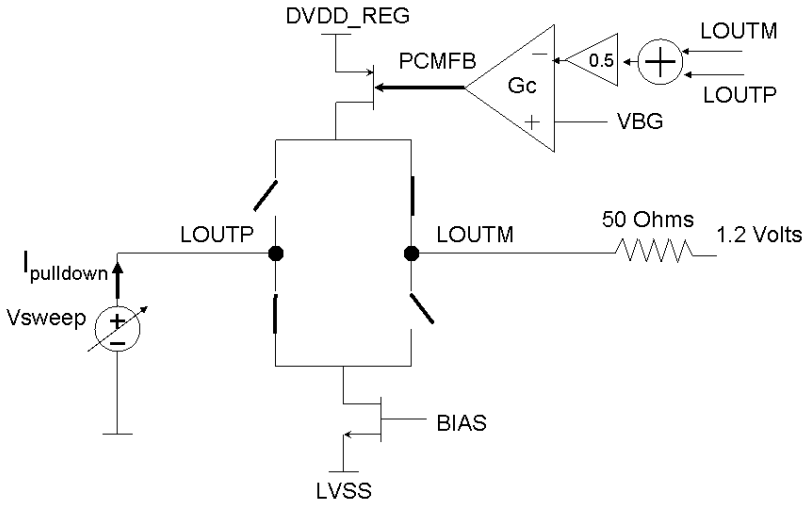

Figure 2.3 Circuit set up for extracting pull-down and ground clamp data

Since the NMOS current source is a constant current source, the pull-down current is fairly a constant for an output voltage between 0.5 V to 1.9 V.

The pull-up and power clamp data is generated by the method shown in Figure 2.4. Refer to section 1.2 for a description of the method used. In this case however, because of the P-side current source being a controlled current source, the pull-up current source varies *even* around an output voltage of 1.2 Volts.

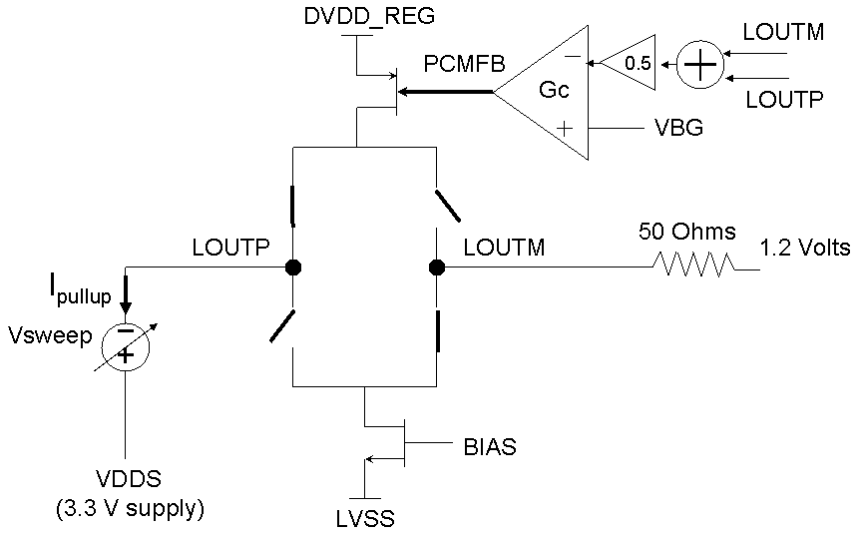

Figure 2.4 Circuit setup to extract pull-up and power clamp data

2.3 Generating the V-t table

The V-t tables are generated using the setup shown in Figure 2.5.

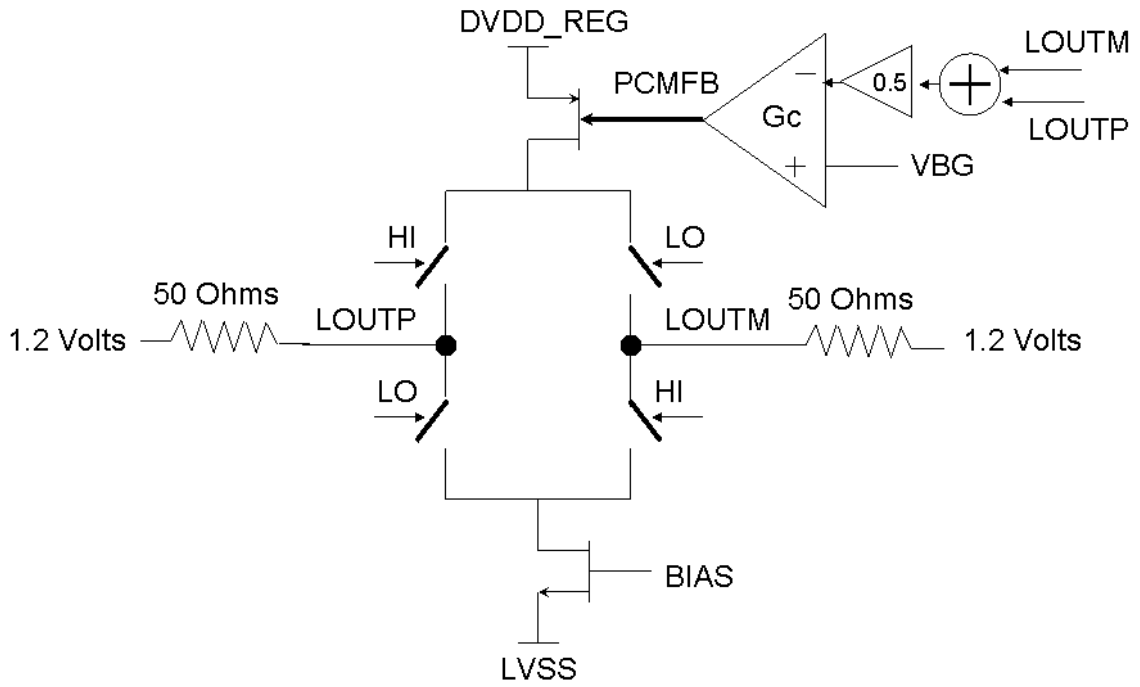

Figure 2.5 Circuit set up used to extract V-t table

2.4 Modeling the internal termination resistances

There are 3 internal termination resistances between the 2 output pins of the lvds buffer that can be turned on or off individually. These resistances have been modeled in the IBIS model file as series switch model. This model consists of a V-I table in which the current flowing in the resistor is tabulated (at the 3 corners) for a range of voltage across it. There are 3 separate models for the 3 individual resistances

1.series_res_166
2.series_res_200
3.series_res_333

2.5 Comparison of IBIS model with the actual circuit

The IBIS models were generated and compared with the actual circuit through SPICE simulations. Figure 2.6 shows the simulation environment for the actual LVDS buffer, while Figure 2.7 shows the identical environment used for the IBIS model.

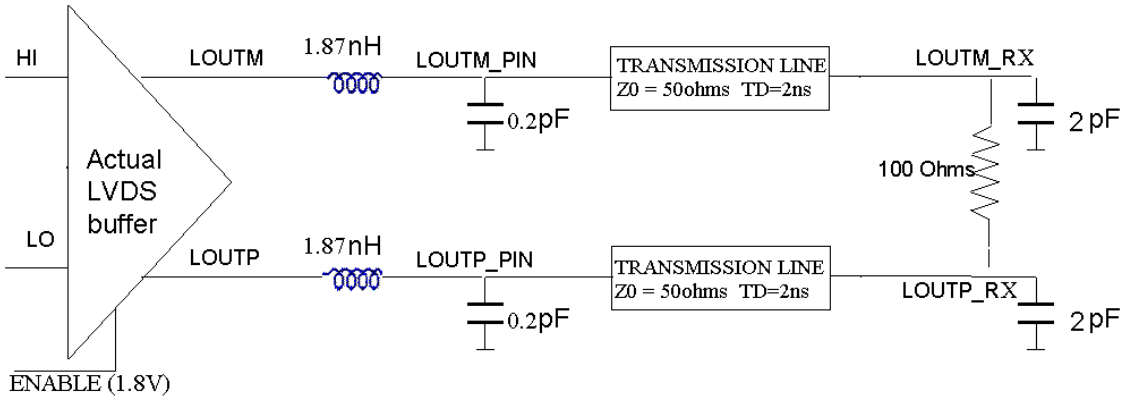

Figure 2.6 Circuit set up of the full transistor spice deck

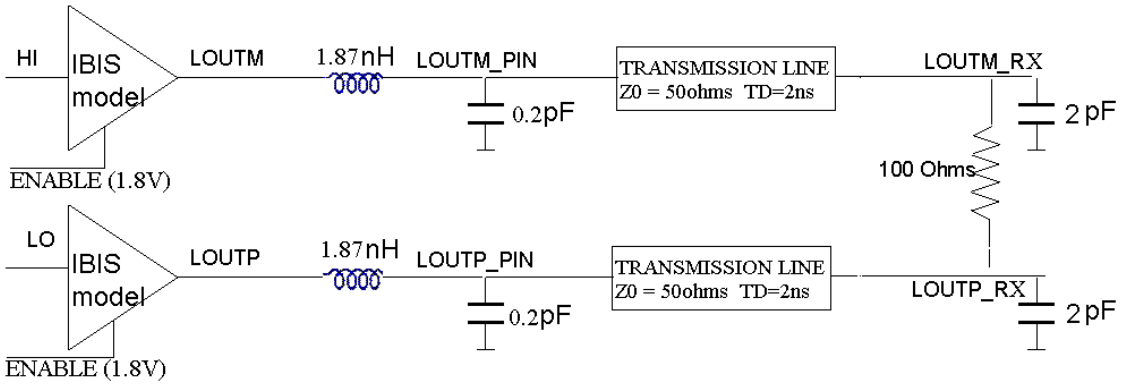

Figure 2.7 Circuit set up of spice deck using IBIS models

Simulations were done with different values of the delay for the transmission line.

Figure 2.8 shows a comparison of the SPICE simulation results obtained from the IBIS model with those from the actual circuit. The delay of the transmission line was set to 2.0ns. There are 2 sets of waveforms

1.LOUTP and LOUTM : waveforms at the buffer output

2.LOUTP_RX and LOUTM_RX: Waveform at the receiver end.

The test circuits shown in Figure 2.6 / 2.7 have the lvds buffer without the internal load terminations. When internal load terminations are used there is a very small shift in the common mode of the output wave forms (~ 0.05 V). But the shape of the waveforms as well as the differential signal shall well correlate with SPICE results. This is due to the inherent inability of IBIS modeling to model feedback (As mentioned in section 2.1 the common mode is set using a feedback loop).

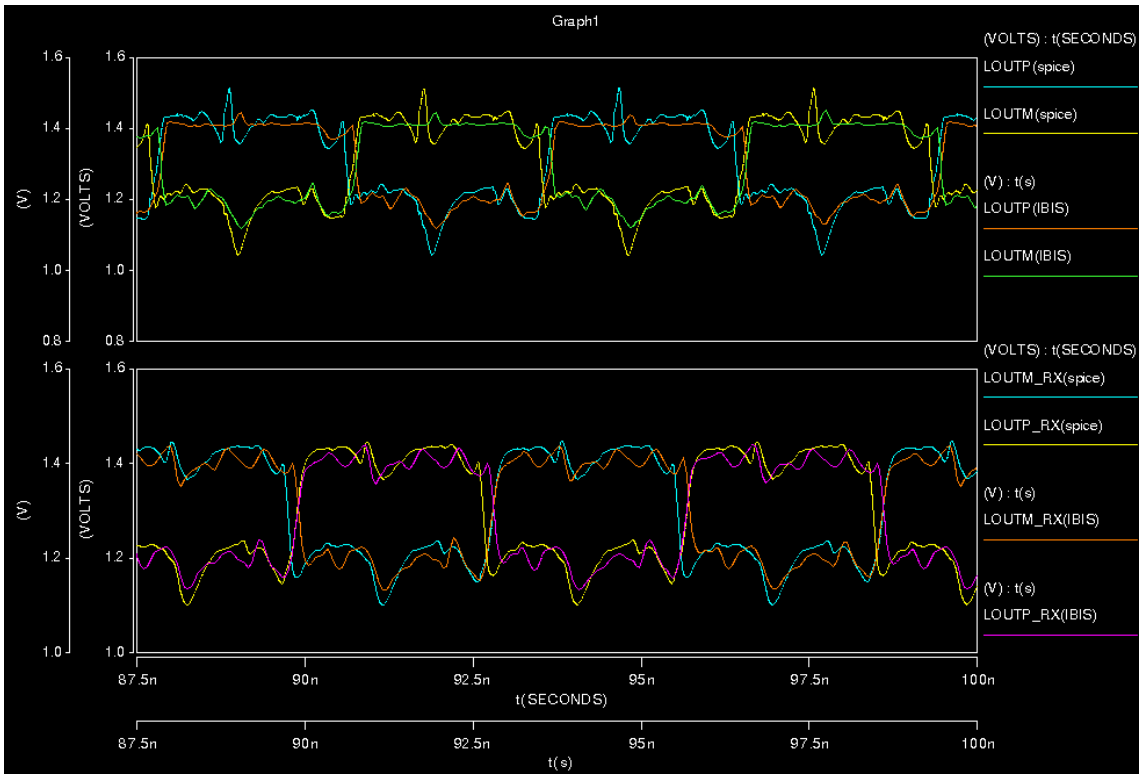

Figure 2.8

As can be observed, there is a close match between the actual circuit and its IBIS model.

3. Input buffer for clock

The structure of the input buffer in ADS61XX family of products is shown in Figure 3.1. The inputs to the buffer are differential and internally it consists of clamping circuits and pull-up/pull-down circuits (as in any input buffer). In addition to them, there is a termination consisting of a capacitance C and 2 equal resistances R1 and R2 from each input to a common mode voltage of 1.5V.

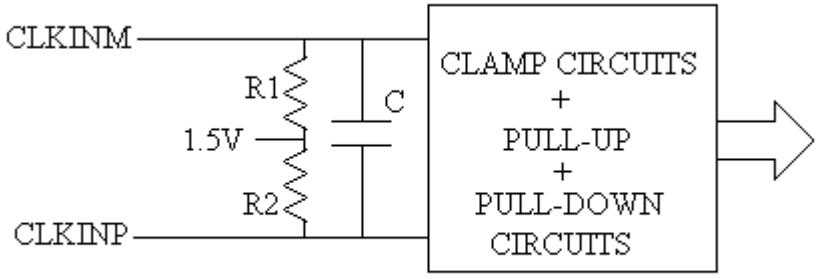

Figure 3.1 Structure of the input buffer in ADS61XX family

As it is an input buffer the pull-up/pull-down circuits shall not be characterized in the IBIS model. The differential input buffer plus R1 and R2 is modeled as combination of 2 single-input buffers and termination capacitance C is modeled as a series element. So the IBIS model file consists of:

1. A model for characterizing clamp circuits + termination resistance. Model type used is Terminator
2. A model for the termination capacitance. Model type used is Series

The input file to the simulator shall consist of 2 instances of the 1st model to represent the differential input and 1 instance of 2nd model to represent the capacitive termination between the differential inputs

3.1 Model for characterizing clamp circuits and termination resistance

The clamp circuit together with termination resistance (R1 or R2) shall be modeled using buffer type Terminator. The model name in the ibis file is ‘input’.

3.1.1 Extracting power clamp and ground clamp data

The setup for the CLAMP data extraction is as shown in Figure 3.2.

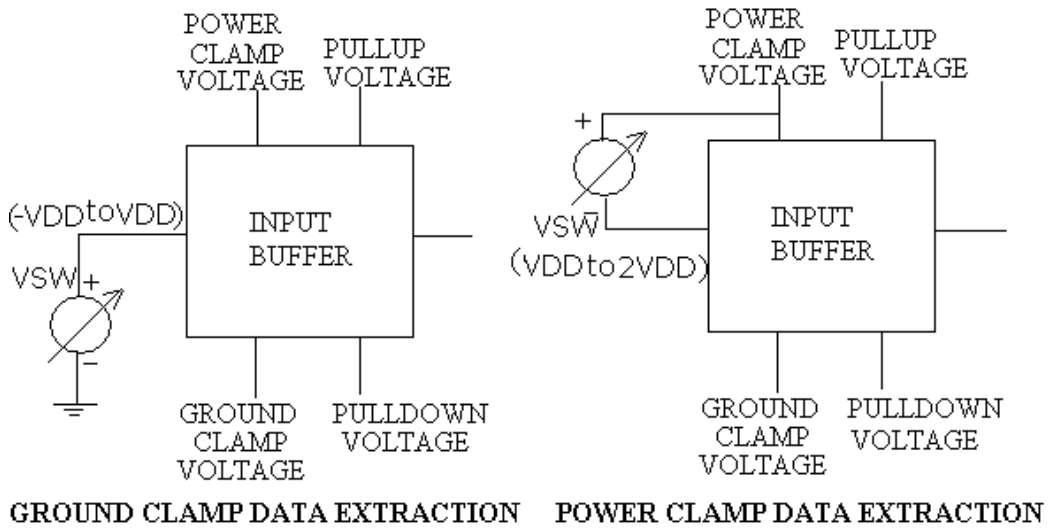

Figure 3.2 Circuit setup used to extract V-I tables

3.1.2 Termination resistance

As shown in Figure 3.1 the termination resistance is connected between input pin and a constant voltage of 1.5V. The Terminator buffer model has keywords [Rpower] and [Rgnd] to specify resistance between the pin to supply voltage and ground respectively. So we split the termination resistance into 2 parts ; one each to the supply and to the ground. The values of Rpower and Rgnd are obtained by solving

VDD*Rpower / (Rpower + Rgnd) = 1.5

Rpower*Rgnd / (Rpower + Rgnd) = R1 (= R2)

This calculation is done for ‘typ’, ‘min’ as well as ‘max’ values of R1(=R2) to get the Rpower and Rgnd at the 3 corners.

From the above discussion, it follows that the ‘Terminator’ model can be represented diagrammatically as in Figure 3.3

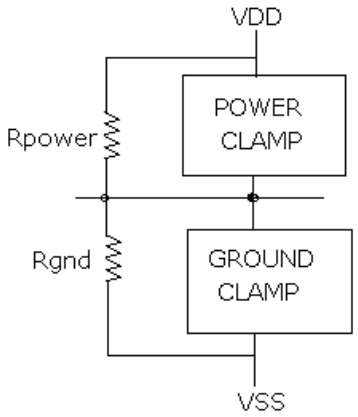

Figure 3.3 The equivalent terminator model of the termination resistance

3.2 Termination Capacitance

The termination capacitance (C) between the pins of the differential input is captured in the IBIS model as 'Series' buffer type. The [C Series] keyword is used to specify its value at the 3 corners.

3.3 Comparison of IBIS model with the actual circuit

The IBIS models were generated and compared with the actual circuit through SPICE simulations. Figure 3.4 shows the simulation environment.

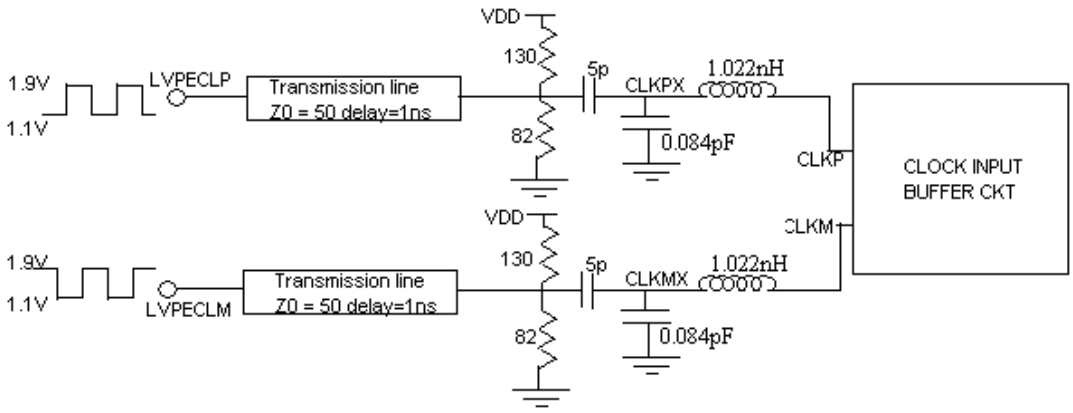

Figure 3.4 Circuit set up used in simulations to validate the IBIS model

Two simulations are performed. The first one uses the full transistor spice netlist of the input buffer circuit. The second simulation uses the IBIS model representation of the buffer as shown in Figure 3.5. A sample spice deck for this configuration is given in section 7.3 of the document.

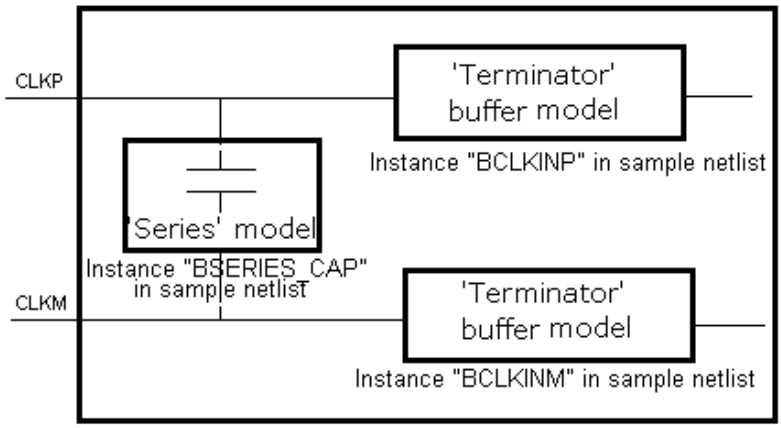

Figure 3.5 The "clock input buffer" block in Fig 3.4 was replaced with this setup of model instances for simulation with IBIS model

Simulations were done with different values of the delay for the transmission line.

Figure 3.6 shows a comparison of the SPICE simulation results obtained from the IBIS model with those from the actual circuit. The transmission line used has Z0 = 50 ohms and delay = 1ns.

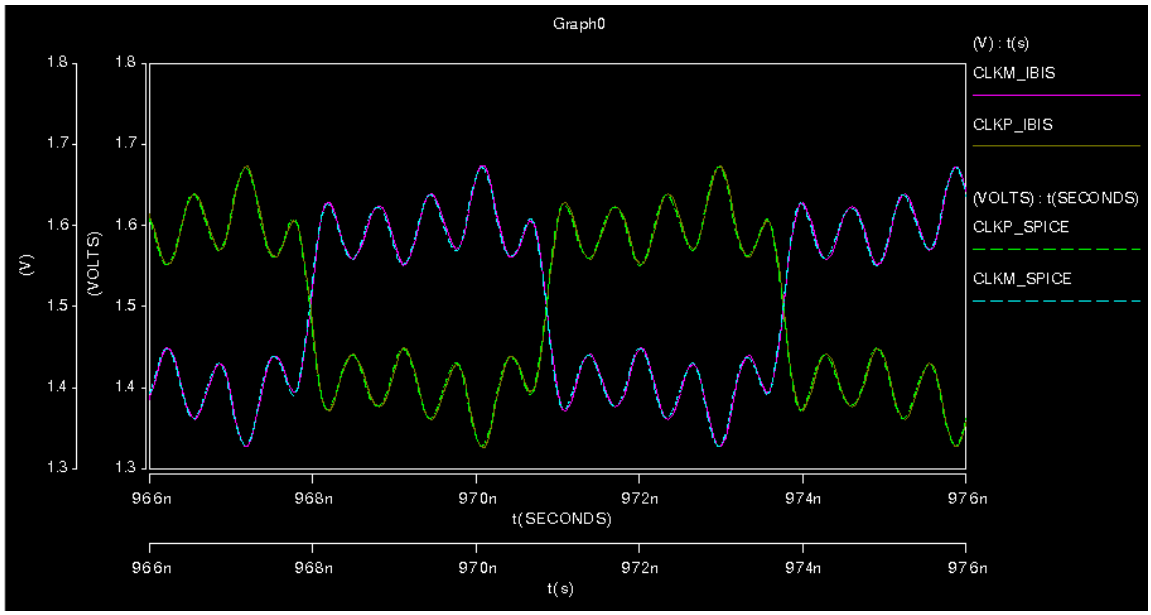

Figure 3.6 Waveforms of simulation with IBIS model Vs full transistor net list

There is a close match between the output waveforms of simulation using actual circuit netlist and its IBIS model.

4. **MODEL SUMMARY**

Component name - ADS61XX *
Model types - Tristate, Terminator, series switch, series cap
Filename - ads61xx.ibs *

Modeling conditions:

Condition	typ/ min/ max
VDD	3.3 V/ 3.0 V/ 3.6 V 2.5 V/1.8 V/2.7 V
VCM (Common mode voltage for LVDS mode)	1.5V
Junction temperature (Tj)	27/ 125/ -40 (degree C)
Process setting	nominal/ weak/ strong
Drive strength modes for CMOS buffers	1.default strength 2.low strength 3.high strength mode 1 4.high strength mode 2
Drive strength modes for LVDS buffers	1.1.95 mA 2.2.5mA 3.3.5mA 4.3.9mA 5.4.5mA 6.5.0mA 7.7.0mA 8.9.0mA

Package characteristics :

Characteristics	typ/ min/ max
R_pkg:	0.1107 / 0.08455 / 0.17649 (ohms)
L_pkg	1.39nH /1.04nH / 2.28nH
C_pkg	0.192pF /0.1545pF / 0.2472pF

Please Note: Models for the buffer have been generated at various differential load terminations like 100, 75 and 50 ohms. Please refer to [Notes] keyword in the model file for details of the termination used for creating the model.

5. Quality Checks:

The created IBIS models are verified as follows:

1. Visual check of each characteristics using the s2iplt tool
2. Syntax check by IBISCHK4
3. Behavior of IBIS models and actual circuit compared using SPICE

6. Sample instantiation of the IBIS models in HSPICE:

6.1 CMOS DATA OUTPUT BUFFER

```
BOUTPUTP PU 0 DOUT IN OBE
+FILE='ads61xx.ibs' MODEL='cmos_low_data_1'  TYP = TYP BUFFER =
THREE_STATE +POWER = ON RAMP_RWF = 1 RAMP_FWF = 1 INTERPOL = 1


*ENABLE SIGNAL FOR THE BUFFER
VEN_CMOS OBE 0 1.8
```

6.2 CMOS CLOCK OUTPUT BUFFER

```
BOUTPUTP PU 0 COUT CLK OBE
+FILE='ads61xx.ibs' MODEL='cmos_clk_low_1' TYP = TYP BUFFER =
THREE_STATE +POWER = ON RAMP_RWF = 1 RAMP_FWF = 1 INTERPOL = 1


*ENABLE SIGNAL FOR THE BUFFER
VEN_CMOS OBE 0 1.8
```

6.3 LVDS OUTPUT BUFFER (SAME FOR BOTH DATA AND CLOCK) ALONG WITH A TERMINATION RESISTANCE

```
BOUTPUTP PU 0 LOUTP INP EN_LVDS
+FILE = 'ads61xx.ibs' MODEL = 'lvds_obuf_1.95'
+TYP = TYP POWER=ON
+BUFFER = THREE_STATE
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1

BOUTPUTM PU 0 LOUTM INM EN_LVDS
+FILE = 'ads61xx.ibs' MODEL = 'lvds_obuf_1.95'
+TYP = TYP POWER=ON
```

+BUFFER = THREE_STATE
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1

VEN_LVDS EN_LVDS 0 3.3

*INTERNAL LOAD TERMINATION OF 166 OHM
BSERIES166 LOUTP LOUTM
+FILE = 'ads61xx.ibs' MODEL = 'series_res_166'
+TYP = TYP
+SS_STATE = ON
+BUFFER = SERIES_SWITCH
+INTERPOL = 1

6.4 INPUT BUFFER FOR CLOCK ALONG WITH TERMINATION CAPACITANCE

VAVDD AVDD 0 3.3
VAVSS AVSS 0 0

BCLKINP AVDD AVSS CLKP
+FILE ='ads61xx.ibs' MODEL = 'input'
+TYP = TYP POWER=OFF
+BUFFER = TERMINATOR
+INTERPOL = 1

BCLKINM AVDD AVSS CLKM
+FILE ='ads61xx.ibs' MODEL = 'input'
+TYP = TYP POWER=OFF
+BUFFER = TERMINATOR
+INTERPOL = 1

*The following line may also be replaced with a capacitance
*Of value as specified against the [C Series] keyword in IBIS model
BSERIES_CAP CLKP CLKM
+FILE ='ads61xx.ibs' MODEL = 'series_cap'
+TYP = MIN
+BUFFER = SERIES
+INTERPOL = 1

7. Sample SPICE deck for simulation of the buffer in HSPICE

7.1 CMOS DATA OUTPUT BUFFER at “low” drive-strength mode , 3.3V supply

```
.TEMP 27
* INPUT TO THE BUFFER
VIN IN 0 PULSE (0 1.8 0.2N 0.2N 0.2N 5.8N 12.5N)

**********************
* Buffer *
**********************
BOUTPUTP PU 0 DOUT IN OBE

+FILE='ads61xx.ibs' MODEL=’cmos_low_data_1’ TYP = TYP BUFFER =
THREE_STATE POWER = ON RAMP_RWF = 1 RAMP_FWF = 1 INTERPOL = 1


*ENABLE SIGNAL FOR THE BUFFER
VEN_CMOS OBE 0 1.8

** TRANSMISSION LINE LOAD

TDATALINK DOUT 0 DOUT_RX 0 Z0=50 TD=300e-12

** CAPACITANCE AT RECEIVER END
COUTP_RX DOUT_RX 0 200e-15

** PIN CAPACITANCE
COUTP DOUT 0 500e-15


.OPTION POST
.OPTION DELMAX=1PS
.TRAN 10PS 30NS
.PLOT TRAN  V(IN) V(DOUT) V(DOUT_RX)
.END
```

7.2 CMOS CLOCK OUTPUT BUFFER at low drive strength , 2.5V supply

```
.TEMP 27
* INPUT TO THE BUFFER
VCLK CLK 0 PULSE (0 1.8 0.2N 0.2N 0.2N 5.8N 12.5N)

**********************
* Buffer *
**********************
BOUTPUTP PU 0 COUT CLK OBE

+FILE='ads61xx.ibs' MODEL='cmos_clk_low_2' TYP = TYP BUFFER =
THREE_STATE POWER = ON RAMP_RWF = 1 RAMP_FWF = 1 INTERPOL = 1


*ENABLE SIGNAL FOR THE BUFFER
VEN_CMOS OBE 0 1.8

** TRANSMISSION LINE LOAD

TDATALINK COUT 0 COUT_RX 0 Z0=50 TD=300e-12

** CAPACITANCE AT RECEIVER END
COUTP_RX COUT_RX 0 200e-15

** PIN CAPACITANCE
COUTP COUT 0 500e-15


.OPTION POST
.OPTION DELMAX=1PS
.TRAN 10PS 30NS
.PLOT TRAN  V(CLK) V(COUT) V(COUT_RX)
.END
```

7.3 LVDS OUTPUT BUFFER (FOR DATA and CLOCK) ALONG WITH A TERMINATION RESISTANCE

```
.TEMP 27

* INPUT TO THE BUFFER
VINM INM 0 PULSE (0 1.8 0N 0.2N 0.2N 5.8N 12.5N)
VINP INP 0 PULSE (1.8 0 0N 0.2N 0.2N 5.8N 12.5N)

**********************
*     Buffer         *
**********************
BOUTPUTP PU 0 LOUTP INP EN_LVDS
+FILE = 'ads61xx.ibs' MODEL = 'lvds_obuf_1.95'
+TYP = TYP POWER=ON
+BUFFER = THREE_STATE
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1

BOUTPUTM PU 0 LOUTM INM EN_LVDS
+FILE = 'ads61xx.ibs' MODEL = 'lvds_obuf_1.95'
+TYP = TYP POWER=ON
+BUFFER = THREE_STATE
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1

VEN_LVDS EN_LVDS 0 3.3

*INTERNAL LOAD TERMINATION OF 166 OHM
BSERIES166 LOUTP LOUTM
+FILE = 'ads61xx.ibs' MODEL = 'series_res_166'
+TYP = TYP
+SS_STATE = ON
+BUFFER = SERIES_SWITCH
+INTERPOL = 1

* PIN INDUCTANCE
LOUTP LOUTP_EXT LOUTP 1.87N
LOUTM LOUTM_EXT LOUTM 1.87N
** PIN CAPACITANCE
COUTP LOUTP_EXT 0 0.2PF
```

```
COUTM LOUTM_EXT 0 0.2PF

** TRANSMISSION LINE LOAD
TDATALINKP LOUTP 0 LOUTP_RX 0 Z0=50 TD=2N
TDATALINKM LOUTM 0 LOUTM_RX 0 Z0=50 TD=2N

** LVDS TERMINATION AT RECEIVER END
RLOAD LOUTP_RX LOUTM_RX 100
*
** CAPACITANCE AT RECEIVER END
COUTP_RX LOUTP_RX 0 2PF
COUTM_RX LOUTM_RX 0 2PF

.OPTION POST
.TRAN 10PS 100NS
.PLOT TRAN V(LOUTP) V(LOUTM)
+ V(LOUTP_EXT) V(LOUTM_EXT)
+ V(LOUTP_RX) V(LOUTM_RX)
+ V(LOUTP_RX,LOUTM_RX)

.END
```

7.4 INPUT BUFFER FOR CLOCK ALONG WITH TERMINATION CAPACITANCE

```
.TEMP 27
VAVDD AVDD 0 3.3
VAVSS AVSS 0 0

BCLKINP  AVDD AVSS CLKP
+FILE ='ads61xx.ibs' MODEL = 'input'
+TYP = TYP POWER=OFF
+BUFFER = TERMINATOR
+INTERPOL = 1

BCLKINM AVDD AVSS CLKM
+FILE ='ads61xx.ibs' MODEL = 'input'
+TYP = TYP POWER=OFF
+BUFFER = TERMINATOR
+INTERPOL = 1

*The following line may also be replaced with a capacitance
*of value as specified against the [C Series] keyword in IBIS model
```

```
BSERIES_CAP CLKP CLKM
+FILE ='ads61xx.ibs' MODEL = 'series_cap'
+TYP = MIN
+BUFFER = SERIES
+INTERPOL = 1


VCLKP LVPECLP 0 DC 0
+PWL 0 1.1 1n 1.1 1.3n 1.9 3.9n 1.9 4.2n 1.1 6.8n 1.1 R=1n

VCLKM LVPECLM 0 DC 0
+PWL 0 1.9 1n 1.9 1.3n 1.1 3.9n 1.1 4.2n 1.9 6.8n 1.9 R=1n

T1 LVPECLP 0 CLKP1 0 Z0=50 TD=1N
T2 LVPECLM 0 CLKM1 0 Z0=50 TD=1N

R1P AVDD CLKP1 130
R2P AVSS CLKP1 82
CC1P CLKP1 CLKPX 5pF

R1M AVDD CLKM1 130
R2M AVSS CLKM1 82
CC1M CLKM1 CLKMX 5pF

C1 CLKPX 0 0.084pF
L1 CLKPX CLKP 1.022n

C2 CLKMX 0 0.084pF
L2 CLKMX CLKM 1.022n

.TRAN 0.01n 1000n
.OPTIONS POST
.plot tran V(CLKP CLKM)
.END
```

8. A brief description of contents of the model file: ads61xx.ibs

The list of pins of the device and corresponding model names for them are tabulated under the key word [Pin]. The names clockoutp, clockoutm and dataoutput represent model selectors. i.e. The pins corresponding to them have multiple modes of operation and there are separate models for each mode of operation. The various models corresponding to each model selector is specified under the keyword [Model Selector].

8.1 DATA OUTPUT BUFFER

There are 2 forms of output: lvds buffer and cmos buffer modes. The lvds buffer has 8 modes of operation, which correspond to different drive strengths for the output transistors. The cmos data buffer is modeled for two supply voltage ranges and each for 4 modes of drive strengths. Hence there is a total of 8 + 8 = 16 models specified under [Model Selector] dataoutput. (The circuit for cmos buffers is different for clock and data because clock rate is double of data rate; but the lvds buffer is identical as in that mode it is DDR. Hence lvds buffer names are same for both whereas cmos buffer model name is different). Also the lvds buffers have 3-termination resistances b/w the 2 output pins, which can be turned on or off. They have been separately modeled (see section 8.4 below)

8.2 CLOCK OUTPUT BUFFER

There are 2 forms of output: lvds buffer and cmos buffer modes. The lvds buffer has 8 modes of operation, which correspond to different drive strengths for the output transistors. The cmos clock buffer is modeled for two supply voltage ranges and each for 4 modes of drive strengths. Hence there is a total of 8 + 8 = 16 models specified under [Model Selector] clockoutp. And for 2nd pin there are 8 lvds models specified under [Model Selector] clockoutm (In the CMOS buffer mode it is not used). Also the lvds buffers have 3-termination resistances b/w the 2 output pins, which can be turned on or off. They have been separately modeled (see section 8.4 below)

8.3 Clock input buffer

The clock input buffer has model name “input”. It also has a terminating capacitance between the 2 input pins which has been separately specified as model series_cap (see section 8.4)

8.4 Termination resistances for lvds buffers and capacitance for input buffer

The lvds buffers have 3 termination resistances between the 2 output pins, which can be turned on or off. Their model name is series_res_<value>. Also there is a termination capacitance between the input pins of clock buffer. It is captured under the model name series_cap.

The keyword [Series Pin Mapping] lists the pairs of pins across which these termination elements are present