Application Report
SLAA648–October 2014

Migrating From the MSP430F4xx Family to the MSP430FR4xx/FR2xx Family

Lixin Chen *MSP430 Applications*

ABSTRACT

This application report enables easy migration from MSP430F4xx flash-based MCUs to the MSP430FR4xx/FR2xx family of FRAM-based MCUs. It covers programming, system, and peripheral considerations when migrating firmware. The intent is to highlight key differences between the two families. For more information on the use of the MSP430FR4xx/FR2xx devices, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

Contents

List of Figures

List of Tables

1 Introduction

The purpose of this application report is to highlight the key differences between the MSP430F4xx families and the MSP430FR4xx/FR2xx family to ensure a smoother migration. It is divided into:

- Changes when handling nonvolatile memory
- System-level considerations such as power management and hardware
- Peripheral modifications

With respect to the instruction set, the MSP430FR4xx/FR2xx family is completely backward code compatible with all other MSP430™ families. Any code migration is therefore impacted only by register or peripheral feature changes and slight variations in instruction cycle times, while the instruction set remains the same. For any specific information, see the device-specific data sheet and errata.

NOTE: For the purpose of this application report, the term *F4xx* indicates the MSP430F4xx families, and the term *FR4xx* indicates the MSP430FR4xx/FR2xx family.

2 In-System Programming of Nonvolatile Memory

2.1 Ferroelectric RAM (FRAM) Overview

In contrast to the F4xx family, which uses flash memory, FR4xx family devices use FRAM nonvolatile memory. Using FRAM is similar to using static RAM (SRAM). FRAM's first introduction as an embedded memory in a general-purpose ultra-low power MCU was on Texas Instruments 16-bit MSP430 product line, the MSP430FR57xx family.

Some of the key attributes of FRAM are:

- FRAM is nonvolatile; that is, it retains its contents on loss of power.
- The embedded FRAM on MSP430 devices can be accessed (read or write) at up to a maximum speed of 8 MHz. Above 8 MHz, wait states are used when accessing FRAM.
- Writing to FRAM and reading from FRAM requires no setup or preparation such as pre-erase before write or unlocking of control registers (unless write protection is used to protect the FRAM against write access).
- FRAM is not segmented and each bit is individually erasable, writable, and addressable.
- FRAM segments do not require an erase before a write.
- FRAM write accesses are low power, because writing to FRAM does not require a charge pump.
- FRAM writes can be performed across the full voltage range of the device.
- FRAM write speeds can reach up to 8 MBps with a typical write speed of approximately 2 MBps. The high speed of writes is inherent to the technology and aided by the elimination of the erase bottleneck that exists in other nonvolatile memory technologies [6]. In comparison, typical MSP430 flash write speed including the erase time is approximately 14 kBps [6].
- FRAM has far greater write endurance compared to flash: practically unlimited 10^{15} write cycles of FRAM compared to 10^{5} write cycles of flash.

2.2 FRAM Cell

A single FRAM cell can be considered a dipole capacitor that consists of a film of ferroelectric material (ferroelectric crystal) between two electrode plates. Storing a 1 or 0 (writing to FRAM) simply requires polarizing the crystal in a specific direction using an electric field. This makes FRAM very fast, easy to write to, and capable of meeting high-endurance requirements.

Reading from FRAM requires applying an electric field across the capacitor similar to a write. Depending on the state of the crystal, it may be repolarized, thereby emitting a large induced charge. This charge is then compared to a known reference to estimate the state of the crystal. The stored data bit 1 or 0 is inferred from the induced charge. In the process of reading the data, the crystal that is polarized in the direction of the applied field and loses its current state. Hence, every read must be accompanied by a write-back to restore the state of the memory location. With TI's MSP430 FRAM MCUs, this is inherent to the FRAM implementation and is completely transparent to the application. The write-back mechanism is also protected from power loss and completes safely under all power-fail events.

The FR4xx power management system achieves write-back safety by isolating the FRAM power rails from the device supply rails in the event of a power loss. The FRAM power circuitry also uses built-in low dropout regulator (LDO) and a capacitor that stores sufficient charge to complete the current write-back in the event of a power failure.

More information about FRAM and FRAM controller is discussed in Section 6.5.

2.3 Protecting FRAM Using the Memory Write Protection Bits

Because FRAM is very easy to reprogram, it also makes it easy for erroneous code execution to unintentionally overwrite application code, just as it would if executing from RAM.

To safeguard against erroneous overwriting of FRAM, memory write protection is provided. FR4xx provides two separate write protection bits:

- SYSCFG0.PFWP – User Program FRAM protection
- SYSCFG0.DFWP – User Data FRAM (1800h to 19FFh) protection

When a write protection bit is set, any write to the protected FRAM is blocked but does not generate an illegal interrupt or reset.

NOTE: FRAM write protection should be enabled at all times except a necessary write operation is required. The write operation is recommended to be accomplished within a short period with interrupts disabled to reduce the risk of unintended write operations. After the write operation completes, it is highly recommended to enable the FRAM write protection again as soon as possible to reduce the risk of unintended writes.

Code examples on how to write the FRAM are provided in the MSP430FR4133 product folder at www.ti.com/product/msp430fr4133.

2.4 FRAM Memory Wait States

The maximum FRAM memory access speed is 8 MHz. If the MCLK is operating faster than 8 MHz and FRAM access is required, wait states are necessary to set to ensure reliable FRAM access. When using MCLK ≥ 8 MHz, configure the FRAM wait states in software before configuring the MCLK frequency.

1. Configure the appropriate wait states.

```
FRCTL0 = FRCTLPW | NWAITS_x
```

2. Configure MCLK ≥ 8 MHz.

For more information, see the Wait State Control section of the FRAM Controller (FRCTRL) chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

2.5 Bootstrap Loader (BSL)

The BSL is software that is used to reprogram the MCU; for example, during field firmware updates. On the F4xx family of devices, the BSL uses a Timer_A-based UART and is located in ROM. The BSL is not erasable or customizable by the user.

The FR4xx family follows a similar approach in which the BSL software is located in ROM. It occupies the address range 1000h to 13FFh and cannot be erased or reprogrammed. The communication interface of the FR4xx is also based on the UART protocol similar to the F4xx devices. However, it uses the hardware eUSCI_A module to implement UART communication instead of using Timer_A. Hence, the module pins UCA0TXD and UCA0RXD are used for BSL communication. The RST/NMI/SBWTDIO pin and TEST/SBWTCK pin are used for BSL entry sequence.

Disabling the BSL is possible with the FR4xx family by programming a specific signature to the BSL signature location. For detailed setting, see Table 1. Note that the location and length of the BSL signature is different from the F4xx family.

This process is documented in the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

2.6 JTAG and Security

On F4xx devices, the JTAG port is secured by blowing a physical fuse on one of the JTAG lines by subjecting it to a high voltage through a special procedure. This action is irreversible, and further access to the device is only possible through the BSL.

On the FR4xx devices, there is NO physical fuse. The JTAG/SBW is locked by programming a specific signature into the device's FRAM memory at JTAG/SBW signature address of FF80h to FF83h.

When JTAG/SBW is locked by programming the JTAG/SBW signature, access to the device is only possible through the BSL (using the BSL password). However, when the BSL is not disabled and the BSL password is supplied, it is possible to clear the JTAG/SBW signature and make JTAG communication available once again. Hence, on the FR4xx devices, locking the JTAG/SBW is reversible if the BSL password is known and BSL is not disabled. See Table 1 for information about the FR4xx device password, BSL signature, and JTAG/SBW signature.

Table 1. FR4xx Device Password, BSL Signature, and JTAG/SBW Signature

Name	Address	Value	Device Security	BSL/SBW Behavior After Reset
Device Password	FFE0h-FFFFh	Depending on vector table configuration		The value is used to protect BSL.
BSL Signature	FF84h-FF87h	5555_5555h	Secured, password not required	BSL is bypassed. User code starts immediately.
		Any Other Values	Secured, password required through the BSL	BSL is invoked before user code starts if BSL is triggered.
JTAG/SBW Signature	FF80-FF83h	FFFF_FFFFh	Not Secured	JTAG/SBW is not locked.
		0000_0000h		
		Any Other Values	Secured	JTAG/SBW is locked.

2.7 Production Programming

MSP-GANG430 does not support the FR4xx devices . This production programmer has been superseded by MSP-GANG (www.ti.com/tool/msp-gang).

3 Hardware Migration Considerations

- For JTAG and SBW connections on the FR4xx devices, see the *MSP430 Hardware Tools User's Guide* (SLAU278). Note that the parallel capacitor on the pin RST/NMI/SBWTDIO should be less than 1.1 nF when using SBW for debug or firmware download.
- The FR4xx devices provide an internal pullup resistor on the reset line, which eliminates the need for an external reset resistor. The internal pullup resistor is enabled by default. For details, see the Reset Pin (RST/NMI) Configuration section in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).
- The FR4xx devices assign the BSL pins to P1.0 and P1.1. For the pin numbers of any given package, see the device-specific data sheet.

- The FR4xx devices do not provide internal load capacitors on the LFXT oscillator as in the F4xx family. Hence, it is required to have external load capacitors if the LFXT oscillator is used. For layout, the external crystal should be as close as possible to FR4xx pins XIN and XOUT, and the capacitor values should be matched with crystal specification and PCB layout. For more guidance about crystal selection, layout concerns and crystal oscillator testing, see the application report *MSP430 32-kHz Crystal Oscillators* (SLAA322).
- The FR4xx devices do not support a high-frequency clock source on the LFXT oscillator. Note that the FLL reference divider FLLREFDIV is fixed as 0 for FR4xx.
- Compared to the F4xx family, the FR4xx clock system is a little different. There is an internal REFO in FR4xx devices that can generate the REFO clock at 32.768 kHz with an accuracy of ±3.5%. For detailed information, see Section 6.2.2 and the Clock System of the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).
- Instead of having analog voltage supply pins (AVCC and AVSS) and digital voltage supply pins (DVCC and DVSS) as in F4xx devices, there is only one pair of power supply pins (DVCC and DVSS) in FR4xx devices.

4 Device Calibration Information

Unlike most F4xx devices, FR4xx devices provide a TLV structure. The TLV structure contains calibration values that can be used to improve the measurement capability of various functions. The calibration values available on a given device are shown in the TLV structure of the device-specific data sheet. In FR4xx data sheet, DCO frequency, ADC offset and gain calibration data, and temperature sensor calibration data are provided.

The TLV information on FR4xx devices is stored in protected FRAM area where it cannot be erased by unintended write operation. For details on the location and access of the TLV, see the device-specific data sheet.

For more information about how to use the TLV in the FR4xx devices, see Device Descriptor Table in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

5 Important Device Specifications

Table 2 shows important differences in device-level electrical specifications [3][4].

Table 2. Device Specifications

Parameter	FR4xx	F4xx
Supply voltage range	1.8 V to 3.6 V(1)	1.8 or 2.2 V to 3.6 V
Maximum system frequency, f_{SYSTEM}(2)	16 MHz at VCC = 1.8 V	4 MHz at V_{CC} = 1.8 V 8 to 12 MHz at V_{CC} = 2.7 V 8 to 16 MHz at V_{CC} = 3.3 V
Minimum supply voltage for nonvolatile memory programming	1.8 V	2.2 V
Minimum analog supply voltage for ADC operation	2.0 V	2.2 V

(1) The minimum operating voltage depends on the SVSH voltage levels.
(2) See the device-specific data sheet for the specified operating conditions.

Note that the most significant impact that migrating to an FR4xx device brings to your system is in terms of the power consumption. The FR4xx demonstrates significant improvement in active and standby power consumption, during both typical conditions and across the voltage and temperature range of the device. The same is also true for peripherals in the FR4xx family, such as the ADC, which show significant power improvements when compared to their F4xx counterparts. For details on the power consumption for each peripheral and of the device in active and standby modes, see the device-specific data sheet.

6 Core Architecture Considerations

6.1 Power Management Module (PMM)

6.1.1 Core LDO and LPM3.5 LDO

The F4xx family devices use DVCC and AVCC to power the chip and the AVCC should not power up prior to DVCC. However the FR4xx family devices use a single power rail to supply both the analog peripherals and the digital core on the chip. There are NO AVCC and AVSS pins – only DVCC and DVSS. The external voltage supply on the DVCC pin is fed to an internal low-dropout voltage regulator (LDO) (see Figure 1).

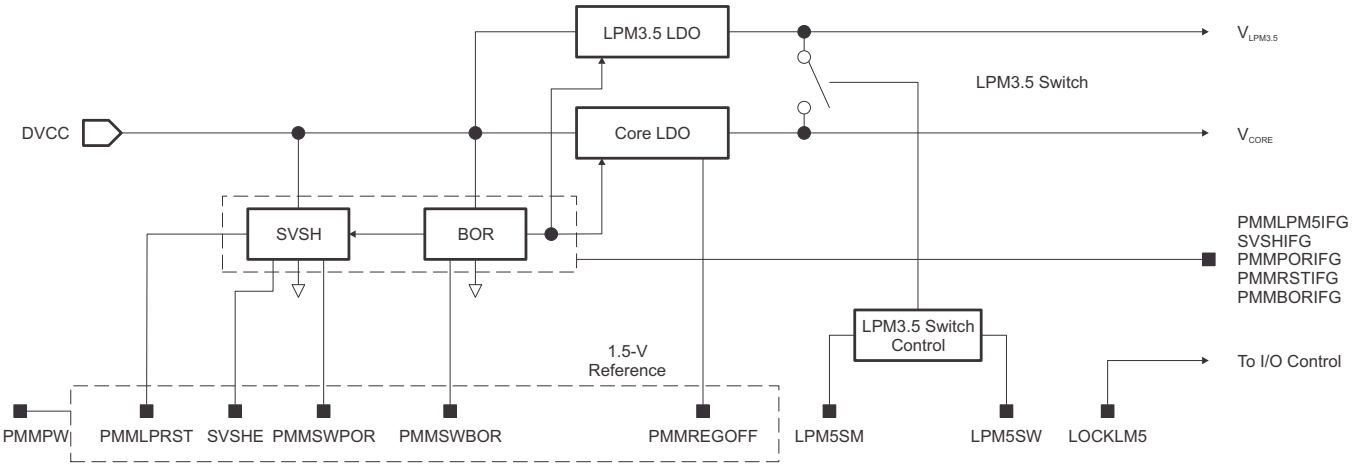

Figure 1. PMM Block Diagram

The PMM manages all functions related to the core voltage and its supervision. Its primary functions are, first, to generate a supply voltage for the core logic and, second, to provide several mechanisms for the supervision of both the voltage supplied to the device (DVCC) and the voltage generated for the core (VCORE).

Using the PMM is especially advantageous as it allows the core to operate at a lower voltage, which brings significant power savings. It also ensures that the core receives a stable and regulated voltage over a wide supply range.

This allows the FR4xx devices to operate across the entire voltage range of the device at the maximum device frequency of 16 MHz. In comparison, F4xx devices have a relationship between system frequency and supply voltage that must be followed to ensure proper operation of the device (see Table 2).

There is a second LDO integrated in FR4xx, the LPM3.5 LDO. This LDO supplies the current for the LPM3.5 power domain logic, which contains the RTC and LCD modules. In LPMx.5 low-power modes, the core LDO is turned off. When entering LPM3.5, the LPM3.5 switch is turned off to save power consumption; when exiting LPM3.5 power mode, the LPM3.5 switch is turned on so that the core LDO can supply power to the LPM3.5 domain logic to support high-frequency operation (see Figure 1).

6.1.2 SVS

Because supply voltage supervision (SVS) is an important aspect of providing a stable supply or a notification in case of power failure, the FR4xx provides a high-side supply voltage supervision (SVSH) block. The SVSH handles the supervision of the external chip supply (DVCC), and the low-side supervision of the core is handled internally by the PMM.

In FR4xx devices, the SVS threshold tracks directly with the device minimum supply of 1.8 V, and there is no need to program SVS high-side levels as in the F4xx family (in which the SVS feature is available on selected devices only). Also, the SVSH block in the FR4xx is highly simplified. It is on by default at power-up and stays on. It can trigger BOR reset when the supply falls below the SVS level. It can be turned off in LPM3, LPM4, and LPMx.5 modes by setting SVSHE = 0, if required.

6.1.3 VREF

In F4xx, the voltage reference generators (VREF) are located in each module, such as the Comparator, ADC10, SD16, and so on. The VREF module in ADC10 can generate a 2.5-V or 1.5-V reference voltage, and the voltage can be buffered and output to a package pin.

Unlike in F4xx, the FR4xx includes a VREF generation block and a high-accuracy bandgap in the PMM module designed for low-power applications. Two voltage references are generated for internal use (1.5-V V_{REF}) and external use (1.2-V V_{REF}) (see Figure 2).

The 1.5-V V_{REF} is connected to the ADC module and can be used as a reference voltage for the ADC. It is also internally connected to the ADC channel 13. This makes a possible to monitor the DVCC voltage by using ADC sampling 1.5-V V_{REF} (set DVCC as ADC reference) without the support of any external components. For detailed information, see the sections *Power Management Module (PMM)* and *On-Chip Reference Voltages* in the device-specific data sheet.

The 1.2-V V_{REF} can be buffered and output to the pin P1.4/MCLK/TCK/A4 when ADC channel 4 is selected as the function. The 1.2-V V_{REF} has only 1-mA drive capability (see Figure 2). For more detailed information, see the PMM and ADC chapters in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

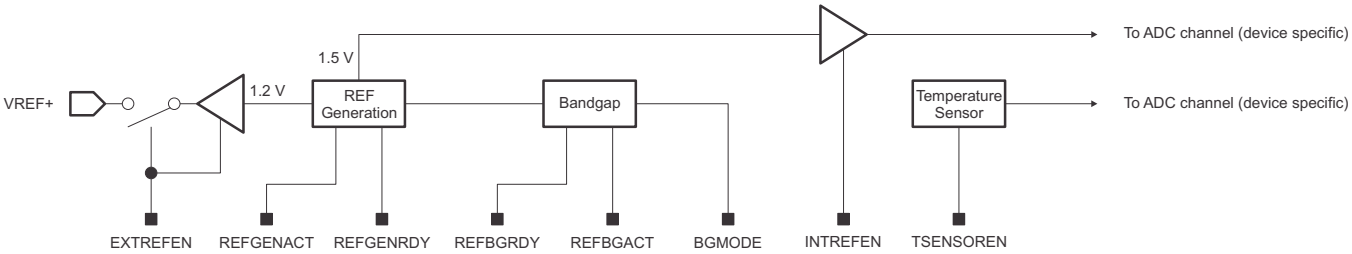

Figure 2. VREF Generation Block Diagram

6.1.4 Debug in Low-Power Mode

One of the main differences between the two families that can be observed while debugging can be attributed to the PMM module. In the FR4xx family, the VCORE regulator operates in two modes to conserve power: high-performance mode (used in active and LPM0 modes) and low-power mode (used in LPM3 and LPM4 modes). When the FR4xx device is plugged into the debugger, it automatically forces the LDO to the high-performance mode regardless of the operating mode (active or LPM) that is set by the application code. In an application, this affects current consumption and wake-up times, which may cause the device to behave differently between stand-alone and debugger modes. When debugging with any of the lower LPMs (LPM3 and LPM4), ensure that the debugger is disconnected to observe device performance accurately.

For LPMx.5, the debugger mode is not supported, because the core LDO is turned off. See Section 6.3.1 for more information about the LPMx.5 low-power mode.

6.2 Clock System

6.2.1 DCO Frequencies

Similar to the F4xx family, the FR4xx Clock System (CS) uses an internal digitally controlled oscillator (DCO) plus Frequency Locked Loop (FLL) to provide frequencies.

A significant difference in the FR4xx DCO+FLL is that it can be configured only to the factory-provided frequencies and does not provide all of the in-between frequency steps that the DCO+FLL based system in the F4xx family allowed.

The FR4xx also provides all of the same clock source options and system clocks as the F4xx family. However the clock distribution system is simplified. For example, the SMCLK is derived from MCLK. There is a SMCLK divider DIVS between MCLK and SMCLK. However, the MCLK divider DIVM also affects SMCLK. For more detailed information, see the Clock System chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

6.2.2 FLL, REFO, and DCO Tap

Another significant difference in the FR4xx CS module is that it has the internal trimmed low-frequency Reference Oscillator (REFO), which is not integrated in the F4xx FLL+ module.

The FLL stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency of FLLREFCLK/n. The FLL reference frequency can be XT1CLK (external crystal + internal XT1 oscillator), or internal 32-kHz reference oscillator REFOCLK. The value of n is defined by the FLLREFDIV bits (n = 1, 2, 4, 8, 12, or 16). The default is n = 1. In the devices on which XT1 supports only low frequency, FLLREFDIV is always read and written as 0 (n = 1).

For applications in which accurate frequency is needed, the FLL should be checked to determine if it is locked or not. The FLL lock status can be detected by reading the FLLUNLOCK bits. When changing clock frequency or changing FLL reference clock, FLL locks again if it is not disabled. For a detailed guide on how to check the FLL lock status, see the FLL Unlock Detection section in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

Nine of the integrator bits (CSCTL0 bits 8 to 0) set the DCO frequency tap. The nine DCOx bits divide the DCO range selected by the DCORSEL bits into 512 frequency steps, separated by approximately 0.1% (F4xx only has five DCOx bits to divide the DCO range selected by the FN_x bits into 29 frequency steps, separated by approximately 10%). One benefit from the nine DCOx bits is that the jitter performance for the DCOCLK is much better. See the device-specific data sheet for detailed specification.

The modulator mixes two adjacent DCO frequencies to produce fractional taps. When the FLL operation is enabled, the modulator settings and DCOx are controlled by the FLL hardware. When FLL operation is not desired, the modulator settings and DCOx control can be configured with software.

The DCO modulator is disabled when DISMOD is set (in F4xx, the SCFQ_M bit is used to disable the modulation). When the DCO modulator is disabled, the DCOCLK is adjusted to the DCO tap selected by the DCOx bits.

6.2.3 FRAM Access at 16 MHz, ADC Clock, and Clocks-on-Demand

While the FR4xx can source MCLK at 16 MHz, it should be noted that FRAM access is limited to 8 MHz by the FRAM controller and wait states are required for MCLK > 8 MHz. For configuring wait states, see Section 2.4. Code execution from RAM and accesses to peripherals can be carried out at 16 MHz.

The ADC module's internal oscillator ADC10OSC on the F4xx family has been renamed to MODOSC in the FR4xx family (similar to the F5xx family).

The FR4xx CS supports the 'clocks-on-demand' feature. In the F4xx family, the availability of a system clock is impacted by entry into a low-power mode. For example, SMCLK is turned off in LPM3 and, hence, any peripheral such as a timer that uses SMCLK is inactive in LPM3. The FR4xx, however, allows the LPM settings to be overridden by a clock request. As long as there is an active request for a clock from a peripheral, the clock remains on, regardless of the LPM setting. This is most easily seen when there is increased power consumption when porting code between families. It is left to the user to disable any modules requesting the clock source that prevents the device from entering the required LPM. As an option, this feature can be disabled using the Clock System Control 8 Register (CSCTL8) (bits MODOSCREQEN, SMCLKREQEN, MCLKREQEN, and ACLKREQEN).

Table 3 shows important differences between the clock systems.

Table 3. Comparison of FR4xx and F4xx Clock Systems

Parameter	FR4xx	F4xx
Maximum system frequency, f_{SYSTEM}	16 MHz	8 MHz to 16 MHz
XT1 oscillator	Supports only LF mode	Supports LF and HF modes
XT2 oscillator	Not available	Supports up to 16 MHz
DCO range	Factory-provided frequencies only	0.06 to 26 MHz
FLL	Available	Available
REFO	Available	Not available
LFMODCLK (MODOSC/128)	Not Available	Not available
VLO control	Available with VLOAUTOOFF	Available with OSCOFF in LPM4

Table 3. Comparison of FR4xx and F4xx Clock Systems (continued)

Parameter	FR4xx	F4xx
Clock sources for MCLK	DCOCLKDIV, XT1CLK, REFOCLK, VLOCLK	DCOCLK, VLOCLK, LFXT1CLK, or XT2CLK(1)
Clock sources for SMCLK	MCLK	DCOCLK, XT2CLK (selected F4xx devices)(1)
Clock sources for ACLK	XT1CLK, REFOCLK	LFXT1CLK, VLOCLK (selected F4xx devices)(1)
External crystal fail-safe operations	XT1, LF: defaults to REFOCLK, XT1, HF: defaults to DCOCLKDIV	For any crystal failure: OFIFG is set, MCLK sourced by crystal defaults to DCO. Other clock sources do not have a fail-safe option.
OFIE reset in fail-safe operation	Not reset automatically	Reset automatically
Registers	CSCTL0 to CSCTL8	SCFQCTL, SCFI0 and SCFI1, FLL_CTL0 to FLL_CTL2, IE1, IFG1
DCO bits	9	5
Internal load capacitors for XT1 oscillator	Not available	Available

(1) See the device-specific data sheet for the clock sources.

For more information about the clock system in the FR4xx devices, see *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

6.3 Operating Modes, Wakeup, and Reset

The operating modes that are available and the wakeup times from LPMs are compared in Table 4.

Table 4. Comparison of Operating Modes and Wakeup Times

Parameter or Feature	FR4xx(1)	F4xx(1)
LPM0, LPM1, LPM2, LPM3, LPM4	Available except LPM1 and LPM2	Available
LPM3.5, LPM4.5	Available	Not available
Wakeup time from LPM0	0.2 + 2.5 / f_{DCO} ≈ 2.7 µs (f_{DCO} = 1 MHz) (max)	2 µs
Wakeup time from LPM1 or LPM2	Not applicable	2 µs
Wakeup time from LPM3 or LPM4	10 µs	6 µs
Wakeup time from LPM3.5	350 µs	Not applicable
Wakeup time from LPM4.5	350 µs (SVSHE = 1) 1 ms (SVSHE = 0)	Not applicable
Wakeup time from BOR event	1 ms	2 ms (max)

(1) The values in this table are approximations; to find the values for a specific device, see the data sheet.

The code flow for entry into and exit out of low-power modes LPM0 to LPM4 remains the same in the FR4xx family as in the F4xx family. There are differences in functionality between the low-power modes on the F4xx compared to the FR4xx devices. These differences are described in the SYS chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

6.3.1 LPMx.5

Two new low-power modes introduced in the FR4xx family are LPM3.5 and LPM4.5. In both modes, the VCORE LDO is turned off, which powers down the digital core, RAM, and peripherals. To wake up from LPM3.5, RTC interrupts, LCD interrupts, oscillator fault, or port interrupts are required. All other system interrupts are not available. The RTC module and LCD module on the FR4xx device are powered from the LPM3.5 LDO rail and can, therefore, stay functional even when the core LDO is turned off. In LPM4.5, only port interrupts can be used to wake up the device.

It is important to understand that the LPMx.5 modes are inherently different from the typical LPMs (LPM0 through LPM4) in that a wake-up from these modes constitutes a device reset. Because RAM is not retained (except backup memory and LCD memory in LPM3), the state of the application (if stored in variables located in RAM) and register initialization is lost.

Note that LPM3.5 is different from LPM4.5 for entering low-power mode and RAM retention.

- The register setting is the same for entering LPM3.5 and LPM4.5. If the RTC or LCD is active, the FR4xx enters LPM3.5. If the RTC and LCD are off, the FR4xx enters LPM4.5. Power supply current can be checked to determine the current FR4xx power mode.
- In LPM3.5, backup memory (32 bytes) and LCD memory (40 bytes) are retained. If there is a requirement in application to retain some data after wakeup from LPM3.5, these 72 bytes can be used. In addition, FRAM can also be used for storing data, because FRAM is nonvolatile (see FRAM special features in Section 2).

These LPMx.5 modes are suited for applications that spend large amounts of time in 'deep sleep' and where wake-up time is not critical. To decide which power mode is appropriate for the application, the frequency of wake up needs to be considered because there is an energy penalty associated with the time spent during wake-up.

- For example, an F4xx application that wakes up every 1 ms from LPM3 to sample a signal can be more efficiently ported to LPM3 in FR4xx rather than LPM3.5. This is because LPM3.5 requires approximately 350 µs to wake up, and the application will spend 35% of its duty cycle during wake-up, which significantly impacts the power gains that were achieved in moving from LPM3 to LPM3.5.
- Consider a different application that wakes up once per minute to update a time stamp. In this case, LPM3.5 could be a better fit for maximizing power savings, because the average power during on time for LPM3.5 is 50% that of LPM3. Hence, selecting LPMs when migrating depends on the application and the on/off duty cycle that is required.

6.3.2 Reset

6.3.2.1 Behavior of POR and BOR

One important difference between the families is the behavior on reset. There are multiple levels of reset across all MSP430 families such as PUC, POR, and BOR. In the F4xx family, the program counter (PC) is reinitialized to the reset vector location on executing a PUC. In the case of a power cycle (POR), the PC is reinitialized after t_{DBOR} has elapsed [3]. In the FR4xx family, the behavior on executing a PUC is the same as the F4xx family as regards re-initialization of the PC and specific peripheral registers.

However, a deeper level of reset such as POR or BOR executes a boot code that is present in protected ROM. This boot code sets up the device and loads calibration settings that are essential to establish device functionality. Hence, the time to start up from a POR or BOR in the FR4xx family is different from the time in the F4xx family. For details, see the device-specific data sheet.

6.3.2.2 Reset Generation

There are also some differences on FR4xx from F4xx for which events generate BOR, POR, and PUC. For detailed information, see the System Reset and Initialization in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

The FR4xx can initiate all levels of reset in software (in the F4xx family, only a PUC can be initiated by software). The resets are initiated by setting the PMMSWBOR or PMMSWPOR bit in the PMMCTL0 control register.

6.3.2.3 Determining the Cause of Reset

In F4xx devices, a PUC can be triggered by multiple sources such as WDT timer expiration, WDT key violation, or flash key violation. To determine the cause of reset, it is necessary to investigate multiple registers, because each reset source is tracked by different interrupt flags and registers.

In the FR4xx devices, all sources of reset are combined into one System Reset Vector Register (SYSRSTIV), and it is no longer necessary to check multiple registers to determine the cause of reset. This register is very useful when debugging and lists all sources from all levels of reset (PUC, POR, and BOR). See the device-specific data sheet for a list of SYSRSTIV values for different reset sources.

6.4 Interrupt Vectors

The FR4xx devices use an interrupt vector (IV) structure for any interrupt service routine that is sourced by multiple flags.

For example, in the F4xx family, the USCI TX interrupt sources the RX and TX interrupt flags, and the USCI RX interrupt sources all the status flags. In the case of the FR4xx family, all of these interrupt flags are captured using a single interrupt vector UCBxIV. This allows interrupt servicing to be more efficient and ensures the same pre-defined latency for all interrupts.

6.5 FRAM and the FRAM Controller

6.5.1 Flash and FRAM Overview Comparison

The F4xx family flash controller is replaced by the FRAM controller in the FR4xx family.

The most significant differences between using FRAM and Flash pertain to (1) timing and (2) power requirements (see Table 5).

Table 5. Comparison of Flash and FRAM on MSP430 MCUs

Parameter	FRAM (FR4133)[1]	Flash (F2274)[1]
Program time for byte or word (maximum)	120 ns	116 µs (approximately)
Erase time for segment (maximum)	Not applicable (pre-erase not required)	18 ms
Supply current during program (maximum)	No extra current during write (included in active power specification)	5 mA
Supply current during erase (maximum)	Not applicable (pre-erase not required)	7 mA
Nonvolatile memory maximum read frequency	8 MHz	16 MHz

(1) The values in this table are approximations; to find the values for a specific device, see the data sheet.

Because every read from an FRAM location is also a write, there is no excess current penalty due to write or erase. Hence, the power consumption when writing to a block of FRAM is the same as when reading from it. This is different from flash, where the writing process consumes excess power due to the operation of a device-internal charge pump. Similarly, FRAM does not require a pre-erase before write and is not segmented like flash. Hence, there is no added erase current (or erase time) when writing to FRAM.

In terms of the write time, FRAM is written in four-word blocks, and the write time is built into each read cycle. Hence, there is no difference between the read time and write time for an FRAM byte, word, or 4-word block. With regards to the read frequency, FRAM accesses (both read and write) are capped at 8 MHz. However, flash reads can take place at the maximum speed allowed by the device (f_{SYSTEM}), which is 16 MHz in the F4xx devices.

Note that the speed of instruction execution in an FRAM-based system is affected by the architecture. The FR4xx uses a cache-based architecture that employs a combination of register and FRAM accesses when executing from nonvolatile memory. This allows the system throughput to be higher than the maximum allowable read frequency of 8 MHz.

6.5.2 Cache Architecture

The FRAM controller uses a 2-way associative cache that has a 64-bit line size. The cache stores prefetched instructions. The function of the FRAM controller is to prefetch four instruction words depending on the current PC location. The actual execution of these instructions is carried out in the cache. When the end of the cache buffer is reached, the FRAM controller preserves the four current words in the same cache line and fetches the next four words. If a code discontinuity is encountered at the end of a 2-way associative cache line, the cache is refreshed and the following four instruction words are retrieved from FRAM. However, if the application code loops back to a location already present in the cache when the last instruction in the cache is reached, the relevant instruction is executed directly from the cache instead of fetching code from FRAM again.

Note that only FRAM accesses are subject to the 8-MHz access limitation. When executing from cache, a system clock of up to 16 MHz can be used. Thus the cache is useful in (1) overcoming the 8-MHz limitation and increasing the average system throughput and (2) reducing overall active power by ensuring that most instructions are executed from it. Note that this is an instruction-only cache; all data is fetched directly from FRAM and is not cached.

The cached execution of instructions in the FR4xx family is different from the F4xx family, in which every instruction is directly executed from flash with no prefetches or caching, providing a 1:1 relationship between MCLK and instruction execution. For example, at MCLK = 16 MHz, eight two-cycle instructions can be executed in 16 clocks. For the FR4xx family, this relationship is application-dependent. The 1:1 relationship holds true only up to MCLK = 8 MHz. For MCLK > 8 MHz, the number of inserted wait states (directly proportional to how many times FRAM is accessed) determines the MCLK:instruction-execution ratio.

To provide another application example, with MCLK = 16 MHz, a JMP $ instruction (single cycle) is executed at the same rate in both devices. This is because the FR4xx fetches this instruction once and stores it in cache where it can be executed at the maximum MCLK speed. However, a loop that has more than eight instruction words would require accessing the FRAM every time a cache refresh is needed. These FRAM accesses take place at MCLK / 2 = 8 MHz, thereby reducing the overall throughput of the system when compared to an F4xx device.

7 Peripheral Considerations

Some of the peripherals in the FR4xx family have new features or existing features that are implemented differently. This section highlights the peripheral differences.

7.1 Watchdog Timer

The main difference between the two families lies in the fail-safe operation.

In the F4xx family, WDT is typically timed by ACLK, which is sourced by a crystal or the VLO. If ACLK or SMCLK failure occurs, WDT defaults to MCLK. If MCLK is also sourced by a crystal, and crystal has failed, the DCO is automatically activated.

In the FR4xx family, the WDT_A fail-safe defaults to VLOCLK if SMCLK or ACLK fails as the WDT_A clock source.

7.2 Ports

7.2.1 Digital Input/Output

The main differences in the FR4xx general-purpose I/O (GPIO) pins are:

- P1 and P2 ports are interruptible in the FR4xx devices, the same as F4xx devices. But P1 and P2 interrupts can be used to wake up FR4xx from LPMx.5 power modes.
- Peripheral function select in the F4xx devices uses one register for Port x Function Selection, PxSEL. FR4xx devices also use one register for Port x Function Selection but the register name is changed to PxSEL0. See device-specific data sheet for details.
- Only in some F4xx devices (MSP430F47x3, MSP430F47x4, and MSP430F471xx devices) all port pins have a programmable pullup or pulldown resistor. In all FR4xx devices, each I/O line is individually configurable for pullup or pulldown resistors.

- In F4xx, the high-impedance leakage current is ±50 nA. In FR4xx, this specification is ±20 nA.
- Configuration of digital I/Os after BOR reset.

  To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions are disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, refer to the Configuration After Reset section in the Digital I/O chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).
- Configuration for LPMx.5 power modes.

  During LPMx.5 the I/O pin states are held and locked based on the settings prior to LPMx.5 entry, regardless of the default I/O register settings. Note that only the pin conditions are retained. All other port configuration register settings such as PxDIR, PxREN, PxOUT, PxIES, and PxIE contents are lost and need to be reconfigured after exit from LPMx.5. After wake from LPMx.5, the LOCKLPM5 bit can be cleared to release I/O pin conditions and I/O interrupt configuration. For details, refer to the Configuration for LPMx.5 Low-Power Modes section in the Digital I/O chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).
- Configuration of unused port pins.

  To prevent a floating input and to reduce power consumption, unused I/O pins should be configured as I/O function, output direction, and left unconnected on the PCB. Alternatively, the integrated pullup or pulldown resistor can be enabled by setting the PxREN bit of the unused pin to prevent a floating input.
- Configuration of unbonded pins.

  In FR4xx, for some packages except PM64, there are some pins not bonded out to the package. For these pins, regard them as unused port pins to configure. See Table 6 for the unbonded out pins for different FR4xx packages.

Table 6. Pins Not Bonded Out on MSP430FR4xx Packages

Unbonded Pins for FR4xx Package G56(1)	Unbonded Pins for FR4xx Package G48(1)
P5.6/L38	P5.6/L38
P5.7/L39	P5.7/L39
P6.6/L22	P6.6/L22
P6.7/L23	P6.7/L23
P7.6/L6	P7.6/L6
P7.7/L7	P7.7/L7
P8.0/SMCLK/A8	P8.0/SMCLK/A8
P8.1/ACLK/A9	P8.1/ACLK/A9
	P8.2/TA1CLK
	P8.3/TA1.2
	P5.4/L36
	P5.5/L37
	P6.4/L20
	P6.5/L21
	P7.4/L4
	P7.5/L5

(1) See the device-specific data sheet for detailed information.

7.2.2 Capacitive Touch I/O

Another significant difference for the digital I/O in FR4xx is each I/O pin is Capacitive Touch I/O.

The Capacitive Touch IO module allows implementation of a simple capacitive touch sense application. When enabled pin oscillator, the integrated pullup and pulldown resistor and the external capacitance on the I/O pin form an oscillator by feeding back the inverted voltage to the pullup and pulldown control logic. Different external capacitance results in different frequency oscillator. The oscillator signal is internally routed to the input of Timer0_A3 in FR4xx. Then the capacitance change can be identified by using timer to measure the oscillator frequency change.

In the FR4xx devices, there is one register, CAPTIO0CTL, to select a port and a specific pin in that port to be used as capacitive touch I/O. For example, the CAPTIOPOSELx field in the Capacitive Touch IOx Control Register (CAPTIOxCTL) can select port 1. The CATPIOPISELx field in the same register can select pin 5. Hence, pin 1.5 is designated as a capacitive touch I/O. For more information, refer to the Capacitive Touch I/O section in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

7.3 Analog-to-Digital Converters

7.3.1 ADC10 to ADC

Compared to ADC10 in F4xx, the ADC module in the FR4xx has been redesigned for lower power and also includes some new features. Some of the significant differences are:

- The ADC10 internal reference is no longer a part of the ADC module in FR4xx. The VREF generation block is in the PMM module (see Section 6.1.3).
- If the reference buffer is used for the ADC reference voltage, and the conversion rate is below 50 kbps, setting ADCSR = 1 reduces the current consumption of the buffer approximately 50%.
- The data transfer controller (DTC), this is used for automatic storage of conversion results in the F4xx family. In FR4xx family, it is not supported.
- In FR4xx, there are up to 10 input channels available externally and 2 channels available internally. 1.2-V V_{REF} can be output to external channel A4. On-chip temperature sensor can be internally connected to channel A12. 1.5-V V_{REF} can be internally connected to channel A13. For detailed connection, see the section of 10-Bit Analog Digital Converter (ADC) in MSP430FR4xx/FR2xx family specific data sheet (SLAS865).
- In FR4xx, a new added window comparator block allows the ADC module to monitor analog signals without CPU interaction. It can generate interrupts when specific thresholds have been reached.
- An interrupt vector register ADCIVx has six interrupt flag sources including three from the window comparator function.
- Increased options for the ADC clock dividers and controlling the sampling rate in FR4xx.
- ADC10OSC is renamed to MODOSC in the FR4xx family.
- Because there is only one pair of power supply pins (DVCC and DVSS) in FR4xx devices, to achieve good ADC performance, board design should avoid system noise:
  - Place decoupling capacitors as close as possible to DVCC.
  - Select reference voltage carefully.
  - Do not layout high-frequency toggled digital signals close to power line and ADC input signals.
  - Do not toggle I/O pins while the ADC is working.
  - Find more design guidance for ADC in www.ti.com.

Some register names have been changed to include the added functionality. For more information when porting firmware, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

7.4 Communication Modules

7.4.1 USCI to eUSCI

The architecture and the internal state machine of the eUSCI in the FR4xx family are very similar to the USCI module in the F4xx family. However, there are many new features added in the eUSCI as well as changes made to the existing features. While most of the code is still compatible, it is recommended to review the register names. Table 7 shows most of the significant differences between the families. For more detailed information, see *Migrating from the USCI to the eUSCI Module* (SLAA522) [5].

Table 7. Comparison of USCI and eUSCI Modules

Parameter or Feature	USCI (F4xx)	eUSCI (FR4xx)
UART		
Enhanced baud rate generation	No	Yes
TXEPT interrupt (similar to USART)	No	Yes
Start edge interrupt	No	Yes
Selectable glitch filter	No	Yes
Interrupt vector generator	No	Yes
SPI		
Enhanced baud rate generation	No	Yes
Maximum baud rate	4 to 6 MHz	5 MHz(1)
Interrupt vector generator	No	Yes
I^2C		
Preload of transmit buffer	No	Yes
Clock low timeout	No	Yes
Byte counter	No	Yes
Multiple slave addressing	No	Yes
Address bit mask	No	Yes
Hardware clear of interrupt flags	Yes	No
Interrupt vector generator	No	Yes

(1) Calculated based on SPI timing with another MSP430FR4133 device in slave mode. For the formula to calculate the maximum baud rate, see device-specific data sheet.

The eUSCI_A module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, and IrDA. The eUSCI_B module provides support for SPI (3 pin or 4 pin) and I^2C.

Another significant difference for the eUSCI module in FR4xx is that there is no ACLK available for the clock source. That means UART, SPI, and I^2C cannot work in LPM3 mode.

In FR4xx, there is one eUSCI_A and one eUSCI_B. The pin configurations for the communication interfaces are shown in Table 8.

Table 8. FR4xx eUSCI Pin Configurations

	Pin	UART	SPI
eUSCI_A0	P1.0	TXD	SIMO
	P1.1	RXD	SOMI
	P1.2		SCLK
	P1.3		STE

Table 8. FR4xx eUSCI Pin Configurations (continued)

	Pin	I²C	SPI
eUSCI_B0	P5.0		STE
	P5.1		SCLK
	P5.2	SDA	SIMO
	P5.3	SCL	SOMI

7.5 Timer_A and IR Modulation Logic

There is no difference for the Timer_A module in F4xx and FR4xx. Note it is recommended to stop the timer before modifying its operation while it is running. A delay of at least 1.5 timer clocks is required to re-synchronize before restarting the timer if the timer clock source is asynchronous to MCLK.

There is a new IR modulation logic in the SYS module of FR4xx. This logic combines the two timer outputs to easily generate accurately modulated IR waveforms. Both ASK and FSK modulations can be implemented. Two other inputs to this logic are UCA0TXD/UCA0SIMO and the IRDATA bit in the SYSCFG1 register. This makes it possible to generate the modulation data by hardware using eUSCI_A or by software using IRDATA.

For more information, see the Infrared Modulation Function in *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445) and the application note *Infrared Remote Control Implementation With MSP430FR4xx* (SLAA644).

7.6 LCD or LCD_A to LCD_E

Migrating from LCD or LCD_A to LCD_E provides several new advanced features that simplify the design by optimizing the software or requiring fewer external components.

- LCD_E has a built-in charge pump, which means fewer external components are needed to drive a segmented LCD with adjustable contrast control.
- Each LCD_E pin is able to be software configured to Segment or COM functionality. This makes it possible to layout LCD circuit on a one-layer PCB.
- LCD_E can work in LPM3.5 low-power mode. This enables ultra-low power consumption for LCD applications.
- LCD_E supports individual segment blinking in static and 2-mux to 4-mux mode so that the software blinking is offloaded to hardware implementation. The blinking frequency is configurable and the built-in blinking memory can work with the LCD memory together to support the dual memory display. Note that the COM-related memory bits in blinking memory should be set to 0 when using individual segment blinking mode.
- LCD_E can support large LCD glass with equivalent capacitance up to 20 nF.

See Table 9 for a summary of the feature difference from LCD or LCD_A to LCD_E.:

Table 9. Comparison of LCD Modules

Parameter	LCD	LCD_A	LCD_E
Number of segments supported[(1)]	160/4-Mux (96 for MSP430F41x)	160/4-Mux (144 for MSP430F41x2IPM)	448/8-Mux (4x36, or 8x32 for MSP430FR413xIPM)
Mux mode supported	4, 3, 2, 1	4, 3, 2, 1	8, 7, 6, 5, 4, 3, 2, 1
Flexible configuration for COM and Segment pins	NO	NO	YES
Internal charge pump	NO	YES	YES
Contrast control	R03 voltage control with external resistor	Software controlled with internal charge pump	Software controlled with internal charge pump
Segment functionality against port pin selection	Minimum is group of 16	Selection done in groups of four segments	Individual selection can be done

(1) LCD pin count varies with package. See device-specific data sheet for detailed information

Table 9. Comparison of LCD Modules (continued)

Parameter	LCD	LCD_A	LCD_E
LCD clock selection	ACLK	ACLK	ACLK, XT1CLK, VLOCLK
LCD clock divider availability	NO	32 to 512 (8 settings with 32 counts apart)	8 to 2048 (depends on Mux mode)
Interrupt capabilities	NO	NO	YES (3 sources)
Individual segment blinking with separate memory	NO	NO	YES for Mux mode 4, 3, 2, 1 (COM related LCDBMx register should be set to 0)
Programmable blinking frequency	N/A	N/A	YES
Dual memory display	NO	NO	YES
LCD bias generation using resistive network	External	External or Internal	External or Internal
Device protection against no connected capacitance on LCDCAP when internal charge pump is enabled	No charge pump	NO (A 4.7-µF or larger capacitor must be connected from pin LCDCAP to ground)	NO need for protection (A 0.1-µF or larger capacitor must be connected from the LCDCAP0 to LCDCAP1 pins)
Charge pump voltage with external voltage reference	No charge pump	3 × Vref	Programmable (15 levels)
Low-power waveforms mode	NO	NO	YES
LPM3.5 Support	NO	NO	YES

For more information, see the LCD_E Controller chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445).

8 Conclusion

This application report describes many of the key feature changes and new modules in the MSP430FR4xx family compared to the MSP430F4xx family. While this document is intended to be comprehensive, there may be minor differences between the F4xx and the FR4xx families that have not been covered here. For details of a given device, the device-specific data sheet is always the best source of information. For module functionality and use, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445). For any bugs and workarounds in the FR4xx family devices, see the device-specific errata sheet.

9 References

1. *MSP430FR4xx and MSP430FR2xx Family User's Guide* (SLAU445)
2. *MSP430x4xx Family User's Guide* (SLAU056)
3. *MSP430F41x2 Mixed Signal Microcontroller* Data Sheet (SLAS648)
4. *MSP430FR413x Mixed-Signal Microcontrollers* Data Sheet (SLAS865)
5. *Migrating from the USCI Module to the eUSCI Module* (SLAA522)
6. *Maximizing FRAM Write Speed on the MSP430FR573x* (SLAA498)
7. *MSP430Fx41x Mixed Signal Microcontroller* Data Sheet (SLAS340)
8. *Migrating From the MSP430F4xx Family to the MSP430FR58xx/FR59xx/68xx/69xx Family* (SLAA646)
9. *Code Composer Studio™ User's Guide for MSP430™ User's Guide* (SLAU157)
10. *MSP430 Hardware Tools User's Guide* (SLAU278)
11. *MSP430 32-kHz Crystal Oscillators* (SLAA322)
12. *MSP430 FRAM Quality and Reliability* (SLAA526)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265