AM62Px Sitara™ プロセッサ

1 特長

プロセッサ コア:

- 最大 1.4GHz、クワッド 64 ビットまでの Arm® Cortex®-A53 マイクロプロセッサ サブシステム
  - SECDED ECC 付き 512KB L2 共有キャッシュ搭載、クワッド コア Cortex-A53 クラスタ
  - 各 A53 コアには、SECDED ECC を備えた 32KB L1 D キャッシュおよびパリティ保護を備えた 32KB L1 I キャッシュを搭載
- MCU チャネルの一部として統合され、最大 800MHz で動作するシングル コア Arm® Cortex®-R5F、FFI 付き
  - 32KB の I キャッシュと 32KB の L1 D キャッシュ、64KB TCM (全メモリに SECDED ECC 付き)
  - 512KB の SRAM (SECDED ECC 付き)
- デバイス管理をサポートするために集積化された、最大 800MHz、シングル コア Arm® Cortex®-R5F
  - 32KB の I キャッシュ、32KB の L1 D キャッシュ、および 64KB TCM (全メモリに SECDED ECC 付き)

マルチメディア:

- ディスプレイ サブシステム
  - OLDI (LVDS) (1x OLDI-DL、1x または 2x OLDI-SL)、DSI または DPI 経由でトリプル ディスプレイをサポート
    - OLDI-SL (シングル リンク):60fps で最大 1920 × 1080 (165MHz ピクセル クロック)
    - OLDI-DL (デュアル リンク):60fps で最大 3840 × 1080 (150MHz ピクセル クロック)
    - MIPI® DSI:4 レーン MIPI® D-PHY は 60fps で最大 3840 × 1080 (300MHz ピクセル クロック) をサポート
    - DPI (24 ビット RGB パラレル インターフェイス):60fps で最大 1920 × 1080 (165MHz ピクセル クロック)
  - ハードウェア オーバーレイを搭載した 4 つのディスプレイ パイプライン サポート。ディスプレイごとに最大 2 つのディスプレイ パイプラインを使用できます。
  - 凍結フレーム検出やデータ修正チェックなどの安全機能をサポート
- 3D グラフィックス処理ユニット
  - IMG BXS-4-64、256KB キャッシュ付き
  - 最大 50GFLOPS
  - シングル シェーダー コア
  - OpenGL ES3.2 および Vulkan 1.2 API サポート
- 1 つのカメラ シリアル インターフェイス (CSI-2) レシーバ、4 レーン搭載、D-PHY
  - MIPI® CSI-2 v1.3 準拠 + MIPI D-PHY 1.2
  - 最大 1.5Gbps の 1、2、3、4 データ レーン モードをサポート
  - CRC チェック + RAM 上の ECC による ECC 検証 / 訂正
  - 仮想チャネルのサポート (最大 16)
  - DMA 経由で DDR にストリーム データを直接書き込む機能
- ビデオ エンコーダ / デコーダ
  - HEVC (H.265) メイン プロファイルをレベル 5.1 上位層でサポート
  - H.264 ベースライン / メイン / ハイ プロファイルをレベル 5.2 でサポート
  - 最大 4K の UHD 解像度をサポート (3840 × 2160)
    - 最大 300M ピクセル / 秒の動作、パフォーマンス ニーズの低い低消費電力アプリケーション向けに低クロック オプションが利用可能

メモリ サブシステム:

- 最大 1.09MB のオンチップ RAM
  - SECDED ECC 付き 64KB オンチップ RAM (OCRAM) は、最大 2 つの独立したメモリ バンクについて、32KB 単位でより小さなバンクに分割可能
  - SMS サブシステムに SECDED ECC を搭載した 256KB のオンチップ RAM
  - テキサス・インスツルメンツのセキュリティ ファームウェア用の SMS サブシステムに SECDED ECC を搭載した 176KB のオンチップ RAM
  - Cortex-R5F MCU サブシステムに SECDED ECC を搭載した 512KB のオンチップ RAM
  - デバイス マネージャ サブシステムの SECDED ECC を搭載した 64KB のオンチップ RAM
- DDR サブシステム (DDRSS)
  - LPDDR4 メモリ タイプをサポート
  - インライン ECC 付きの 32 ビット データ バス
  - 最高 3200MT/s の速度をサポート
  - 最大サイズ:8GB

機能安全:

- 機能安全規格準拠を対象とする [産業用]
  - 機能安全アプリケーション向けに開発
  - IEC 61508 機能安全システム設計を支援するドキュメントを準備中
  - SIL 3 までの決定論的対応能力を対象とする

  - SIL 2 までを対象とするハードウェア インテグリティ
  - 安全関連認証
    - TÜV SÜD による IEC 61508 認定を計画中
- 機能安全規格準拠を対象とする [車載用]
  - 機能安全アプリケーション向けに開発
  - ISO 26262 機能安全システム設計を支援するドキュメントを準備中
  - ASIL D までの決定論的対応能力を対象とする
  - ASIL B までを対象とするハードウェア インテグリティ
  - 安全関連認証
    - TÜV SÜD による ISO 26262 認定を計画中
- AEC - Q100 認定済み [車載用]

セキュリティ:

- セキュア ブート対応
  - ハードウェアで強化された RoT (Root-of-Trust:信頼の基点)
  - バックアップ キーによる RoT の切り替えをサポート
  - テイクオーバー保護、IP 保護、ロールバック禁止保護のサポート
- 信頼できる実行環境 (TEE) に対応
  - Arm TrustZone® をベースとする TEE
  - 絶縁のための広範なファイアウォール サポート
  - セキュアなウォッチドッグ / タイマ / IPC
  - セキュアなストレージのサポート
  - リプレイ保護メモリ ブロック (RPMB) のサポート
- ユーザー プログラマブルな HSM コアと専用セキュリティ DMA および IPC サブシステムの搭載により絶縁処理を実現した専用セキュリティ コントローラ
- 暗号化アクセラレーションに対応
  - 受信データ ストリームに基づいてキーマテリアルを自動的に切り替えできるセッション認識暗号化エンジン
    - 暗号化コアをサポート
  - AES - 128/192/256 ビットのキー サイズ
  - SHA2 - 224/256/384/512 ビットのキー サイズ
  - DRBG と真性乱数発生器
  - セキュア ブート対応のため PKA (公開鍵アクセラレータ) により RSA/ECC 処理を支援
- デバッグのセキュリティ
  - ソフトウェア制御によるセキュアなデバッグ アクセス
  - セキュリティ対応のデバッグ

高速インターフェイス:

- 次の機能をサポートするイーサネット スイッチを内蔵 (合計 2 つの外部ポート)
  - RMII (10/100) または RGMII (10/100/1000)
  - IEEE1588 (Annex D、Annex E、Annex F と 802.1AS PTP)
  - Clause 45 MDIO PHY 管理
  - ALE エンジン (512 の分類子) に基づくパケット分類器
  - プライオリティ ベースのフロー制御
  - タイム センシティブ ネットワーキング (TSN) のサポート
  - 4 個の CPU ハードウェア割り込みペーシング
  - ハードウェアの IP/UDP/TCP チェックサム オフロード
- 2 つの USB2.0 ポート
  - USB ホスト、USB ペリフェラル、USB デュアルロール デバイス (DRD モード) として構成可能なポート
  - USB VBUS 検出機能を内蔵

一般的な接続機能:

- 9 個のユニバーサル非同期レシーバ トランスミッタ (UART)
- 5 個のシリアル ペリフェラル インターフェイス (SPI) コントローラ
- 6 個の内部集積回路 (I^2C) ポート
- 3 個のマルチチャネル オーディオ シリアル ポート (McASP)
  - 最高 50MHz の送信および受信クロック
  - 3 個の McASP で最大 16/10/6 本のシリアル データ ピンを使用でき、TX と RX の各クロックは独立しています
  - 時分割多重化 (TDM)、IC 間サウンド (I2S)、および類似のフォーマットをサポート
  - デジタル オーディオ インターフェイス送信 (SPDIF、IEC60958-1、AES-3 フォーマット) をサポート
  - 送受信用 FIFO バッファ (256 バイト)
  - オーディオ リファレンス出力クロックのサポート
- 3 つの拡張 PWM モジュール (ePWM)
- 3 個の拡張直交エンコーダ パルス モジュール (EQEP)
- 3 個の拡張キャプチャ モジュール (ECAP)
- 汎用 I/O (GPIO) では、すべての LVCMOS I/O を GPIO として構成可能
- 4 個のコントローラ エリア ネットワーク (CAN) モジュール、CAN-FD をサポート
  - CAN プロトコル 2.0A、B、ISO 11898-1 に準拠
  - 完全な CAN FD のサポート (最大 64 データ バイト)
  - メッセージ RAM のパリティ / ECC チェック
  - 最大速度:8Mbps

メディアおよびデータ ストレージ:

- 3 つのマルチメディア カード / セキュア デジタル® (MMC/SD®/SDIO) インターフェイス

  - 1 個の 8 ビット eMMC インターフェイス、最大速度 HS400
  - 2 個の 4 ビット SD/SDIO インターフェイス、最大 UHS-I
  - eMMC 5.1、SD 3.0、SDIO バージョン 3.0 に準拠
- 最大 133MHz の 1 つの汎用メモリ コントローラ (GPMC)
  - 柔軟な 8 および 16 ビットの非同期メモリ インターフェイスと、最大 4 つのチップ (22 ビット アドレス) セレクト (NAND、NOR、Muxed-NOR、SRAM)
  - BCH コードを使用して 4、8、または 16 ビット ECC をサポート
  - ハミング コードを使用して 1 ビット ECC をサポート
  - エラー特定モジュール (ELM)
    - GPMC と組み合わせて使用して、BCH アルゴリズムにより生成されたシンドローム多項式からデータ エラーのアドレスを特定
    - BCH アルゴリズムに基づいて、512 バイトのブロックごとに 4、8、16 ビットのエラーを特定可能
- DDR/SDR をサポートする OSPI/QSPI
  - シリアル NAND およびシリアル NOR フラッシュ デバイスをサポート
  - 4GByte のメモリ アドレスをサポート
  - オプションのオンザフライ暗号化を備えた XIP モード

パワー マネージメント:

- デバイス マネージャでサポートされている低消費電力モード:
  - CAN/GPIO/UART ウェイクアップに対する部分的 IO サポート
  - RAM へサスペンドするためセルフ リフレッシュで I/O のみ + DDR
  - ディープスリープ
  - MCU のみ
  - スタンバイ
  - ダイナミック周波数スケーリング

最適なパワー マネージメント ソリューション:

- 推奨されるテキサス・インスツルメンツ パワー マネージメント IC (PMIC)
  - AEC – Q100 認定済みの AM62P-Q1 デバイスへの電力供給時に、車載用の ASIL-B までの機能安全に対応
  - AM62P デバイスへの電力供給時に、SIL-2 までの機能安全産業用アプリケーションに対応
  - コンパニオン PMIC は電源要件を満たすように特別に設計
  - さまざまな使用事例をサポートするためのフレキシブルなマッピングと工場出荷時にプログラムされた構成

ブート オプション:

- UART
- I^2C EEPROM
- OSPI/QSPI フラッシュ
- GPMC NOR/NAND フラッシュ
- SD カード
- eMMC
- USB (ホスト) マス ストレージ
- 外部ホストからの USB (デバイス) ブート (DFU モード)
- イーサネット

テクノロジ / パッケージ:

- 16nm FinFET テクノロジ
- 17mm × 17mm、0.65/0.8mm ピッチ、VCA 付き、466 ピン FCBGA

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2 アプリケーション

- 産業用ヒューマン マシン インターフェイス (HMI)
- 家電製品向けユーザー インターフェイスとコネクティビティ
- 医療用機器
- 車載用計器盤
- 車載用ディスプレイ
- 拡張現実 (AR) HUD (ヘッド アップ ディスプレイ)

3 概要

AM62Px (P = Plus) は、高性能の組み込み 3D ディスプレイ アプリケーション向けに構築された、既存の Sitara™ AM62x 低コスト アプリケーション プロセッサ ファミリを拡張した製品です。スケーラブルな Arm ® Cortex ® -A53 の性能と組み込み機能 (マルチスクリーンの高解像度ディスプレイのサポート、3D グラフィックス アクセラレーション、4K ビデオ アクセラレーション、広範なペリフェラル) により、AM62Px は車載用デジタル計測機器、車載用ディスプレイ、産業用 HMI など、幅広い車載用および産業用アプリケーションに適しています。

主な機能と特長:

- Linux® および Android™ SDK と、リアルタイムの機能安全およびセキュリティ SDK の組み合わせにより、革新と迅速な開発に注力できます。
- 新世代の 3D GPU と 4K ビデオ アクセラレーションにより、、HMI の次世代設計に対応します。
- 次のような車載と高速の各 IO で構成された包括的なセットを活用して、設計のコネクティビティを強化しましょう。TSN サポート、および 2 個の USB2.0 ポートを搭載した 4 個の CAN-FD、3 ポートのギガビット イーサネット スイッチ (2 個の外部ポート)。
- 内蔵のハードウェア セキュリティ モジュール (HSM) により、最新のサイバーセキュリティ要件をサポートします。
- 複数の Arm® Cortex®-A53 CPU と、オープン ソースの AI ソフトウェアやツールを活用して、顔認識や非接触式 HMI などのインテリジェント機能を提供します。

AM62Px プロセッサは AEC-Q100 車載規格に準拠しており、産業用グレードをサポートしています。ASIL-B および SIL-2 の機能安全要件は、内蔵された Arm Cortex-R5F コアと専用ペリフェラルを使用して満たすことができます。これらはすべて、プロセッサの残り部分から分離できます。

AM62Px プロセッサ ファミリの製品:

AM62P-Q1 – スケーラブルな Arm Cortex-A53 の性能、マルチ HD ディスプレイのサポート、3D GPU および 4K ビデオ アクセラレーションを搭載した車載用デジタル計測 SoC。

主な設計リソース:

- ハードウェア評価基板 (EVM) - SK-AM62P-LP
- ソフトウェア開発キット (SDK) – PROCESSOR-SDK-AM62P
- Linux Academy

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
AM62P54 AM62P54-Q1	AMH (FCBGA、466) 0.65/0.8mm、VCA 付き	17mm × 17mm
AM62P52 AM62P52-Q1	AMH (FCBGA、466) 0.65/0.8mm、VCA 付き	17mm × 17mm
AM62P34 AM62P34-Q1	AMH (FCBGA、466) 0.65/0.8mm、VCA 付き	17mm × 17mm
AM62P32 AM62P32-Q1	AMH (FCBGA、466) 0.65/0.8mm、VCA 付き	17mm × 17mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。

(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

3.1 機能ブロック図

図 3-1 は、このデバイスの機能ブロック図です。

注

TI のソフトウェア開発キット (SDK) が現在サポートしているデバイス機能の詳細については、AM62Px ソフトウェア ビルドシートを参照してください。

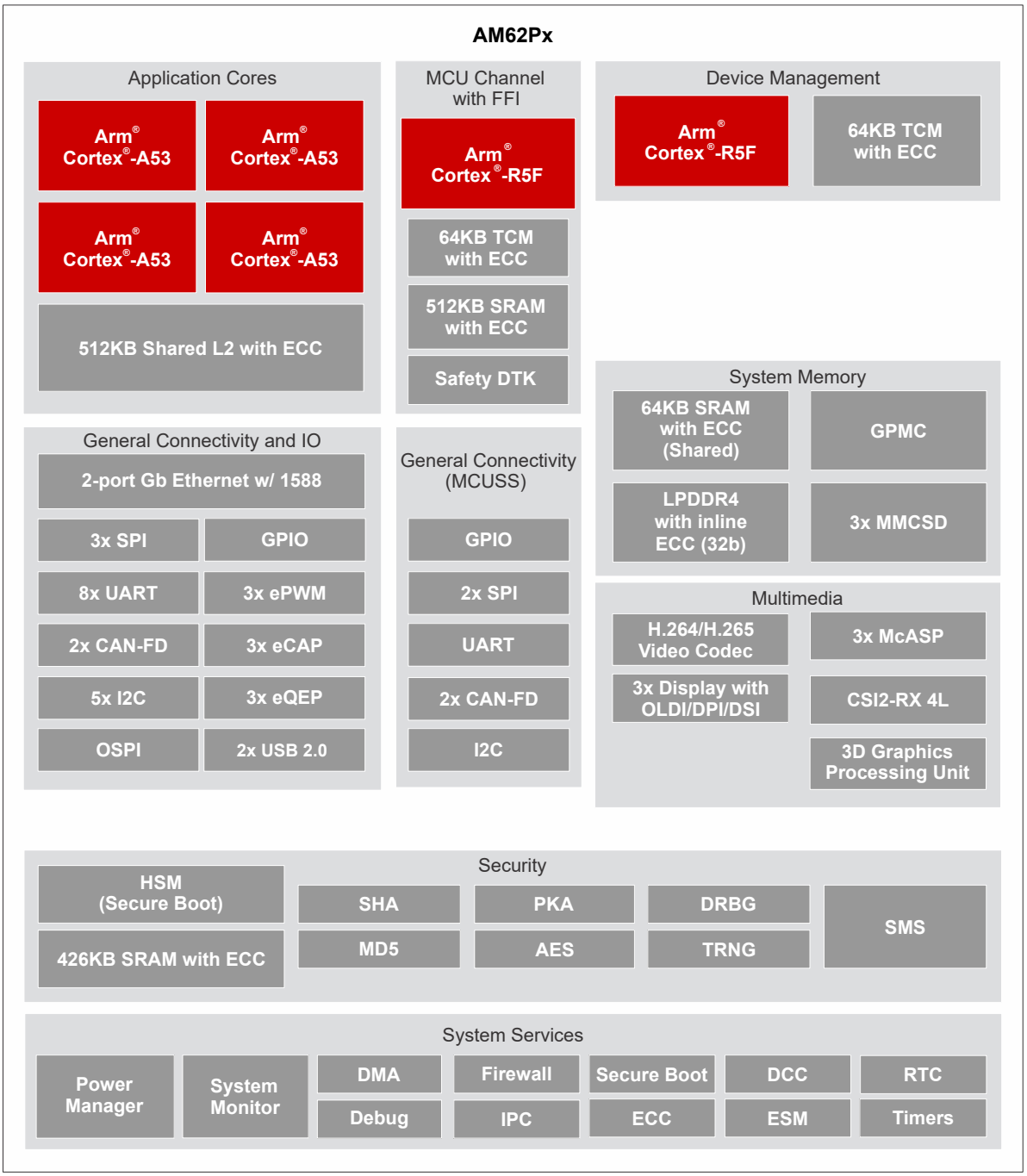

図 3-1. 機能ブロック図

ADVANCE INFORMATION

Table of Contents

1 特長 1
2 アプリケーション 4
3 概要 4
3.1 機能ブロック図 5
4 Device Comparison 7
4.1 Related Products 8
5 Terminal Configuration and Functions 10
5.1 Pin Diagrams 10
5.2 Pin Attributes 12
5.3 Signal Descriptions 48
5.4 Pin Connectivity Requirements 76
6 Specifications 81
6.1 Absolute Maximum Ratings 81
6.2 ESD Ratings for Devices which are not AEC - Q100 Qualified 83
6.3 ESD Ratings for AEC - Q100 Qualified Devices 83
6.4 Power-On Hours (POH) 83
6.5 Recommended Operating Conditions 84
6.6 Operating Performance Points 86
6.7 Power Consumption Summary 86
6.8 Electrical Characteristics 87
6.9 VPP Specifications for One-Time Programmable (OTP) eFuses 93
6.10 Thermal Resistance Characteristics 94
6.11 Timing and Switching Characteristics 95
7 Detailed Description 211
7.1 Overview 211
7.2 Processor Subsystems 212
7.3 Accelerators and Coprocessors 213
7.4 Other Subsystems 214
7.5 Peripherals 216
8 Applications, Implementation, and Layout 220
8.1 Device Connection and Layout Fundamentals 220
8.2 Peripheral- and Interface-Specific Design Information 221
8.3 Clock Routing Guidelines 228
9 Device and Documentation Support 229
9.1 Device Nomenclature 229
9.2 Tools and Software 232
9.3 Documentation Support 232
9.4 サポート・リソース 232
9.5 Trademarks 232
9.6 静電気放電に関する注意事項 233
9.7 用語集 233
10 Revision History 233
11 Mechanical, Packaging, and Orderable Information 234
11.1 Packaging Information 234

ADVANCE INFORMATION

4 Device Comparison

表 4-1 shows a comparison between devices, highlighting the differences.

注

Availability of features listed in this table are a function of shared IO pins, where IO signals associated with many of the features are multiplexed to a limited number of pins. The SysConfig tool should be used to assign signal functions to pins. This will provide a better understanding of limitations associated with pin multiplexing.

注

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the *AM62Px Software Build Sheet*.

表 4-1. Device Comparison

FEATURES	REFERENCE NAME	AM62P, AM62P-Q1			
		AM62P54	AM62P52	AM62P34	AM62P32
WKUP_CTRL_MMR_CFG0_JTAG_USER_ID[31:13] (1) Register bit values by device "Features" code (See Nomenclature Description table for more information on device features)					
G:		–	0x0D4A9F	–	0x0D469F
M:		0x0D4BB7	0x0D4AB7	0x0D47B6	0x0D46B7
PROCESSORS AND ACCELERATORS					
Speed Grades		See Device Speed Grades table			
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Quad Core	Dual Core	Quad Core	Dual Core
Arm Cortex-R5F in MCU domain	MCU_R5F	Single Core Functional Safety Optional(3)			
Graphics Processing Unit	GPU	Yes	Yes	No	No
Video Encoder / Decoder	VENC/VDEC	Yes			
Device Management Subsystem	WKUP_R5F	Single Core			
Hardware Security Module	HSM	Yes			
Crypto Accelerators	Security	Yes			
PROGRAM AND DATA STORAGE					
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	64KB			
On-Chip Shared Memory (RAM) in MCU Domain	MCU_MSRAM	512KB			
LPDDR4 DDR Subsystem	DDRSS	32-bit data with inline ECC up to 8GB			
General-Purpose Memory Controller	GPMC	Up to 128MB with ECC			
PERIPHERALS					
Display Subsystem	DSS	1x DPI			
		1x OLDI (LVDS)			
		1x DSI			
Modular Controller Area Network Interface	MCAN	4			
Full CAN-FD Support	CAN-FD	Yes			
General-Purpose I/O	GPIO	Up to 158			
Inter-Integrated Circuit Interface	I2C	6			
Multichannel Audio Serial Port	MCASP	3			
Multichannel Serial Peripheral Interface	MCSPI	5			
Multi-Media Card/Secure Digital Interface	MMC/SD	1x eMMC (8-bits)			
		2x SD/SDIO (4-bits)			
Flash Subsystem (FSS)(2)	OSPI0/QSPI0	Yes(2)			
Gigabit Ethernet Interface	CPSW3G	Yes			
General-Purpose Timers	TIMER	14 (4 in MCU and 2 in WKUP)			

ADVANCE INFORMATION

表 4-1. Device Comparison (続き)

FEATURES	REFERENCE NAME	AM62P, AM62P-Q1			
		AM62P54	AM62P52	AM62P34	AM62P32
Enhanced Pulse-Width Modulator Module	EPWM	3			
Enhanced Capture Module	ECAP	3			
Enhanced Quadrature Encoder Pulse Module	EQEP	3			
Universal Asynchronous Receiver and Transmitter	UART	9			
CSI2-RX Controller with DPHY	CSI-RX	1			
USB2.0 Controller with PHY	USB 2.0	2			

(1) For more details about the CTRLMMR_WKUP_JTAG_DEVICE_ID register and DEVICE_ID bit field, see the device TRM.
(2) One flash interface, configured as OSPI0 or QSPI0.
(3) Functional Safety is available when selecting an orderable part number that includes a feature code of F. Refer to Device Naming Convention for definition of feature codes.

ADVANCE INFORMATION

4.1 Related Products

Sitara™ processors are a broad family of scalable processors based on Arm® Cortex®-A cores with flexible accelerators, peripherals, connectivity, and unified software support – perfect for sensors to servers. Sitara processors have the reliability and functional safety support required for use in industrial and automotive applications.

Sitara™ microcontrollers are best-in-class Arm®-based 32-bit microcontrollers (MCUs) offering a scalable portfolio of high-performance and power-efficient devices to help meet your system needs. Bring capabilities such as functional safety, power efficiency, real-time control, advanced networking, analytics, and security to your designs.

AM64x Sitara™ processors target industrial applications such as Factory Automation and Control (FAC), and motor control that utilize Linux application processing cores (Cortex®-A53), real-time processing cores (Cortex®-R5F), and Industrial Communication Subsystems (PRU_ICSSGs) to support protocols such as EtherCAT, Profinet, or EtherNet/IP. AM64x implements one CPSW3G and two PRU_ICSSGs for supporting up to five gigabit Ethernet ports. The device also supports an extensive set of peripherals including a single lane of PCIe Gen2 or USB SuperSpeed Gen1, functional safety options, secure boot, and run-time security.

AM623 Sitara™ processors are an Internet of Things (IoT) and gateway SoC with Arm® Cortex®-A53-based object and gesture recognition. The low-cost AM623 Sitara™ MPU family of application processors are built for Linux® application development. With scalable Arm® Cortex®-A53 performance, embedded features such as dual-display support, and an extensive set of peripherals make the AM623 device well-suited for a broad range of industrial and automotive applications.

AM625 Sitara™ processors are a human-machine-interaction SoC with Arm® Cortex®-A53-and full-HD dual display. The low-cost AM625 Sitara™ MPU family of application processors are built for Linux® application development. With scalable Arm® Cortex®-A53 performance, embedded features such as dual-display support, 3D graphics acceleration, and an extensive set of peripherals make the AM625 device well-suited for a broad range of industrial and automotive applications.

AM62A3 Sitara™ and **AM62A7 Sitara™** processors are an embedded vision SoC that utilizes 1-4x Cortex A-53 ARM Cores and 1 or 2 TOPS analytics hardware accelerator. This scalable, high performance AM62Ax Sitara MPU family of application processors are built for Linux application development. AM62Ax is well suited for a broad range of industrial and automotive applications with embedded features such as h.264/h.265 encode/decode, secure boot, image signal processing and a deep learning accelerator.

Products to complete your design:

- Ethernet PHYs
- Power Management / PMICs
- Clocks and timing
- Power Switches

- CAN Transceivers
- ESD Protection

Please reference the AM62Ax EVM schematic for details of how these devices are implemented in a system design, and bill of materials for specific part number recommendations.

5 Terminal Configuration and Functions

5.1 Pin Diagrams

注

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

図 5-1 shows the ball locations for the 466-ball flip chip ball grid array (FCBGA) package, where the HTML version provides additional information when hovering your cursor over a ball. This figure is used in conjunction with セクション 5.2.1 through 表 5-74 (*Pin Attributes table and all Signal Descriptions tables, including the Connectivity Requirements table*).

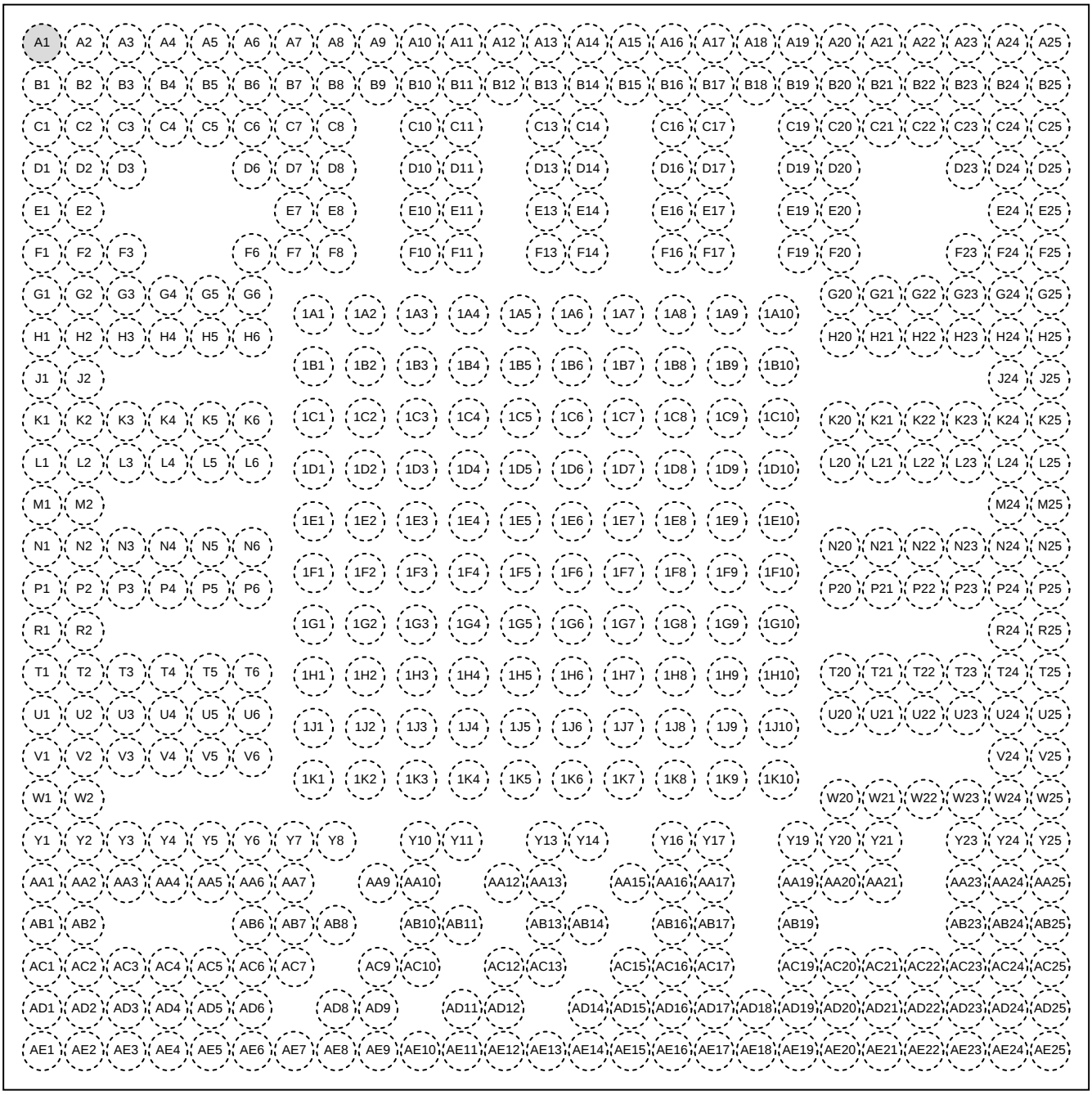

図 5-1. AMH FCBGA Package (Top View)

ADVANCE INFORMATION

5.2 Pin Attributes

The following list describes the contents of each column in the 表 5-1, *Pin Attributes (AMH Package)* table:

1. **BALL NUMBER:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **BALL NAME:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **SIGNAL NAME:** Signal name(s) of all dedicated and pin multiplexed signal functions associated with a ball.

注

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

The 表 5-1, *Pin Attributes (AMH Package)* table only defines signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see *Pad Configuration Registers* section in *Device Configuration* chapter of the device TRM. Refer to the respective peripheral chapter in the device TRM for information associated with peripheral signal multiplexing.

4. **MUX MODE:** The MUXMODE value associated with each pin multiplexed signal function:
   a. MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.

注

The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when MCU_PORz is deasserted.

   a. MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only valid values of MUXMODE should be used.
   b. Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz_OUT. These input signal functions are fixed to their respective pins and are not programable via MUXMODE.
   c. An empty box means Not Applicable.

注

The following configurations of MUXMODE must be avoided for proper device operation.

- Configuring multiple pins operating as inputs to the same pin multiplexed signal function is not supported as it can yield unexpected results.
- Configuring a pin to an undefined pin multiplexing mode will cause the pin behavior to be undefined.

5. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor.
6. **DSIS:** The deselected input state (DSIS) indicates the state driven to the subsystem input (logic "0", logic "1", or "pad" level) when the pin multiplexed signal function is not selected by MUXMODE.
   - 0: Logic 0 driven to the subsystem input.
   - 1: Logic 1 driven to the subsystem input.
   - pad: Logic state of the pad is driven to the subsystem input.
   - An empty box means Not Applicable.
7. **BALL STATE DURING RESET RX/TX/PULL:** State of the terminal while MCU_PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is disabled.
     - On: The input buffer is enabled.
   - TX (Output buffer)
     - Off: The output buffer is disabled.
     - Low: The output buffer is enabled and drives V_{OL}.
     - High: The output buffer is enabled and drives V_{OH}.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned off.
     - Up: Internal pull-up resistor is turned on.
     - Down: Internal pull-down resistor is turned on.
     - NA: Not Applicable.
   - An empty box means Not Applicable.
8. **BALL STATE AFTER RESET RX/TX/PULL:** State of the terminal after MCU_PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is disabled.
     - On: The input buffer is enabled.
   - TX (Output buffer)
     - Off: The output buffer is disabled.
     - SS: The subsystem selected with MUXMODE determines the output buffer state.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned off.
     - Up: Internal pull-up resistor is turned on.
     - Down: Internal pull-down resistor is turned on.
     - NA: Not Applicable.
   - An empty box means Not Applicable.

ADVANCE INFORMATION

9. **MUX MODE AFTER RESET:** The value found in this column defines the default pin multiplexed signal function after MCU_PORz is deasserted.

   An empty box means Not Applicable.

10. **I/O VOLTAGE VALUE**: This column describes I/O operating voltage options of the respective power supply, when applicable.

    An empty box means Not Applicable.

    For more information, see valid operating voltage range(s) defined for each power supply in セクション 6.5, *Recommended Operating Conditions*.

11. **POWER:** The power supply of the associated I/O, when applicable.

    An empty box means Not Applicable.

12. **HYS:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: With hysteresis
    - No: Without hysteresis
    - An empty box means Not Applicable.

    For more information, see the hysteresis values in セクション 6.8, *Electrical Characteristics*.

13. **BUFFER TYPE:** This column defines the buffer type associated with a terminal. This information can be used to determine which Electrical Characteristics table is applicable.

    An empty box means Not Applicable.

    For electrical characteristics, refer to the appropriate buffer type table in セクション 6.8, *Electrical Characteristics*.

14. **PULL UP/DOWN TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    - PU: Internal pull-up
    - PD: Internal pull-down
    - PU/PD: Internal pull-up and pull-down
    - An empty box means No internal pull.

15. **PADCONFIG Register:**Name of the IO pad configuration register associated with Ball.

16. **PADCONFIG Address:**Physical address of the IO pad configuration register associated with Ball.

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
1A8	CAP_VDDS0	CAP_VDDS0		CAP									
1C10	CAP_VDDS1	CAP_VDDS1		CAP									
1B6	CAP_VDDS2	CAP_VDDS2		CAP									
1F10	CAP_VDDS3	CAP_VDDS3		CAP									
1B9	CAP_VDDS5	CAP_VDDS5		CAP									
1C9	CAP_VDDS6	CAP_VDDS6		CAP									
1B2	CAP_VDDS_CANUART	CAP_VDDS_CANUART		CAP									
1B4	CAP_VDDS_MCU	CAP_VDDS_MCU		CAP									
AE12	CSI0_RXCLKN	CSI0_RXCLKN		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE11	CSI0_RXCLKP	CSI0_RXCLKP		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AA15	CSI0_RXRCALIB	CSI0_RXRCALIB		A					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AB11	CSI0_RXN0	CSI0_RXN0		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC10	CSI0_RXN1	CSI0_RXN1		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AA10	CSI0_RXN2	CSI0_RXN2		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD9	CSI0_RXN3	CSI0_RXN3		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AB10	CSI0_RXP0	CSI0_RXP0		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC9	CSI0_RXP1	CSI0_RXP1		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AA9	CSI0_RXP2	CSI0_RXP2		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD8	CSI0_RXP3	CSI0_RXP3		I					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
T6	DDR0_ACT_n	DDR0_ACT_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K3	DDR0_ALERT_n	DDR0_ALERT_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
T5	DDR0_CAS_n	DDR0_CAS_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
T1	DDR0_PAR	DDR0_PAR		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P6	DDR0_RAS_n	DDR0_RAS_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
T4	DDR0_WE_n	DDR0_WE_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K5	DDR0_A0	DDR0_A0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L2	DDR0_A1	DDR0_A1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L3	DDR0_A2	DDR0_A2		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M2	DDR0_A3	DDR0_A3		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
N2	DDR0_A4	DDR0_A4		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K2	DDR0_A5	DDR0_A5		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N3	DDR0_A6	DDR0_A6		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L1	DDR0_A7	DDR0_A7		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M1	DDR0_A8	DDR0_A8		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
T2	DDR0_A9	DDR0_A9		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R2	DDR0_A10	DDR0_A10		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N5	DDR0_A11	DDR0_A11		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P3	DDR0_A12	DDR0_A12		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P2	DDR0_A13	DDR0_A13		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N6	DDR0_BA0	DDR0_BA0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K4	DDR0_BA1	DDR0_BA1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
Y6	DDR0_BG0	DDR0_BG0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U6	DDR0_BG1	DDR0_BG1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
Y5	DDR0_CAL0	DDR0_CAL0		A					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
R1	DDR0_CK0	DDR0_CK0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P1	DDR0_CK0_n	DDR0_CK0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N4	DDR0_CKE0	DDR0_CKE0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
P5	DDR0_CKE1	DDR0_CKE1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L6	DDR0_CS0_n	DDR0_CS0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
T3	DDR0_CS1_n	DDR0_CS1_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
C3	DDR0_DM0	DDR0_DM0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
H3	DDR0_DM1	DDR0_DM1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
V4	DDR0_DM2	DDR0_DM2		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AD1	DDR0_DM3	DDR0_DM3		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B2	DDR0_DQ0	DDR0_DQ0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
A3	DDR0_DQ1	DDR0_DQ1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
A4	DDR0_DQ2	DDR0_DQ2		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
A5	DDR0_DQ3	DDR0_DQ3		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
A2	DDR0_DQ4	DDR0_DQ4		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B4	DDR0_DQ5	DDR0_DQ5		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D2	DDR0_DQ6	DDR0_DQ6		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
C4	DDR0_DQ7	DDR0_DQ7		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E2	DDR0_DQ8	DDR0_DQ8		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F1	DDR0_DQ9	DDR0_DQ9		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G5	DDR0_DQ10	DDR0_DQ10		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F2	DDR0_DQ11	DDR0_DQ11		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G3	DDR0_DQ12	DDR0_DQ12		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H4	DDR0_DQ13	DDR0_DQ13		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J2	DDR0_DQ14	DDR0_DQ14		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G2	DDR0_DQ15	DDR0_DQ15		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U2	DDR0_DQ16	DDR0_DQ16		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U3	DDR0_DQ17	DDR0_DQ17		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
U5	DDR0_DQ18	DDR0_DQ18		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
V5	DDR0_DQ19	DDR0_DQ19		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
V2	DDR0_DQ20	DDR0_DQ20		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
Y2	DDR0_DQ21	DDR0_DQ21		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
Y3	DDR0_DQ22	DDR0_DQ22		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AA4	DDR0_DQ23	DDR0_DQ23		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AC2	DDR0_DQ24	DDR0_DQ24		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AA2	DDR0_DQ25	DDR0_DQ25		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AC4	DDR0_DQ26	DDR0_DQ26		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AD2	DDR0_DQ27	DDR0_DQ27		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AD3	DDR0_DQ28	DDR0_DQ28		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AC3	DDR0_DQ29	DDR0_DQ29		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AE4	DDR0_DQ30	DDR0_DQ30		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AE3	DDR0_DQ31	DDR0_DQ31		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D1	DDR0_DQS0	DDR0_DQS0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
C1	DDR0_DQS0_n	DDR0_DQS0_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J1	DDR0_DQS1	DDR0_DQS1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H1	DDR0_DQS1_n	DDR0_DQS1_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
W1	DDR0_DQS2	DDR0_DQS2		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
V1	DDR0_DQS2_n	DDR0_DQS2_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AA1	DDR0_DQS3	DDR0_DQS3		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AB1	DDR0_DQS3_n	DDR0_DQS3_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L5	DDR0_ODT0	DDR0_ODT0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
V6	DDR0_ODT1	DDR0_ODT1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AA5	DDR0_RESET0_n	DDR0_RESET0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
AA12	DSI0_TXCLKN	DSI0_TXCLKN		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AA13	DSI0_TXCLKP	DSI0_TXCLKP		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
Y16	DSI0_TXRCALIB	DSI0_TXRCALIB		A					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD11	DSI0_TXN0	DSI0_TXN0		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AB13	DSI0_TXN1	DSI0_TXN1		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC12	DSI0_TXN2	DSI0_TXN2		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE14	DSI0_TXN3	DSI0_TXN3		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AD12	DSI0_TXP0	DSI0_TXP0		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AB14	DSI0_TXP1	DSI0_TXP1		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AC13	DSI0_TXP2	DSI0_TXP2		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
AE15	DSI0_TXP3	DSI0_TXP3		IO					1.8 V	VDDA_1P8_CSI_DSI		D-PHY	
B12	EMU0 PADCONFIG: MCU_PADCONFIG30 0x04084078	EMU0	0	IO	0	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
D13	EMU1 PADCONFIG: MCU_PADCONFIG31 0x0408407C	EMU1	0	IO	0	On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
C23	EXTINTn PADCONFIG: PADCONFIG125 0x000F41F4	EXTINTn	0	I	1	Off / Off / NA	Off / Off / NA	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS	
		GPIO1_31	7	IOD	pad								
C25	EXT_REFCLK1 PADCONFIG: PADCONFIG124 0x000F41F0	EXT_REFCLK1	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SYNC1_OUT	1	O									
		SPI2_CS3	2	IO	1								
		SYSCLKOUT0	3	O									
		TIMER_IO4	4	IO	0								
		CLKOUT0	5	O									
		CP_GEMAC_CPTS0_RFT_CLK	6	I	0								
		GPIO1_30	7	IO	pad								
		ECAP0_IN_APWM_OUT	8	IO	0								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
R25	GPMC0_ADVn_ALE PADCONFIG: PADCONFIG33 0x000F4084	GPMC0_ADVn_ALE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AXR2	2	IO	0								
		TRC_DATA7	6	O									
		GPIO0_32	7	IO	pad								
Y25	GPMC0_CLK PADCONFIG: PADCONFIG31 0x000F407C	GPMC0_CLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AXR3	2	IO	0								
		GPMC0_FCLK_MUX	3	O									
		TRC_DATA6	6	O									
		GPIO0_31	7	IO	pad								
P25	GPMC0_DIR PADCONFIG: PADCONFIG41 0x000F40A4	GPMC0_DIR	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR13	3	IO	0								
		MAIN_ERRORn	5	IO	1								
		TRC_DATA14	6	O									
		GPIO0_40	7	IO	pad								
		EQEP2_S	8	IO	0								
R24	GPMC0_OEn_REn PADCONFIG: PADCONFIG34 0x000F4088	GPMC0_OEn_REn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AXR1	2	IO	0								
		TRC_DATA8	6	O									
		GPIO0_33	7	IO	pad								
T25	GPMC0_WEn PADCONFIG: PADCONFIG35 0x000F408C	GPMC0_WEn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AXR0	2	IO	0								
		TRC_DATA9	6	O									
		GPIO0_34	7	IO	pad								
P24	GPMC0_WPn PADCONFIG: PADCONFIG40 0x000F40A0	GPMC0_WPn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK1	1	IO	0								
		GPMC0_A22	2	OZ									
		UART6_TXD	3	O									
		TRC_DATA13	6	O									
		GPIO0_39	7	IO	pad								
U22	GPMC0_AD0 PADCONFIG: PADCONFIG15 0x000F403C	GPMC0_AD0	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR4	3	IO	0								
		TRC_CLK	6	O									
		GPIO0_15	7	IO	pad								
		BOOTMODE00	Bootstrap	I									

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
U21	GPMC0_AD1 PADCONFIG: PADCONFIG16 0x000F4040	GPMC0_AD1	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR5	3	IO	0								
		TRC_CTL	6	O									
		GPIO0_16	7	IO	pad								
		BOOTMODE01	Bootstrap	I									
U20	GPMC0_AD2 PADCONFIG: PADCONFIG17 0x000F4044	GPMC0_AD2	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR6	3	IO	0								
		TRC_DATA0	6	O									
		GPIO0_17	7	IO	pad								
		BOOTMODE02	Bootstrap	I									
V25	GPMC0_AD3 PADCONFIG: PADCONFIG18 0x000F4048	GPMC0_AD3	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR7	3	IO	0								
		TRC_DATA1	6	O									
		GPIO0_18	7	IO	pad								
		BOOTMODE03	Bootstrap	I									
T20	GPMC0_AD4 PADCONFIG: PADCONFIG19 0x000F404C	GPMC0_AD4	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR8	3	IO	0								
		TRC_DATA2	6	O									
		GPIO0_19	7	IO	pad								
		BOOTMODE04	Bootstrap	I									
T21	GPMC0_AD5 PADCONFIG: PADCONFIG20 0x000F4050	GPMC0_AD5	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR9	3	IO	0								
		TRC_DATA3	6	O									
		GPIO0_20	7	IO	pad								
		BOOTMODE05	Bootstrap	I									
V24	GPMC0_AD6 PADCONFIG: PADCONFIG21 0x000F4054	GPMC0_AD6	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR10	3	IO	0								
		TRC_DATA4	6	O									
		GPIO0_21	7	IO	pad								
		BOOTMODE06	Bootstrap	I									
W25	GPMC0_AD7 PADCONFIG: PADCONFIG22 0x000F4058	GPMC0_AD7	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR11	3	IO	0								
		TRC_DATA5	6	O									
		GPIO0_22	7	IO	pad								
		BOOTMODE07	Bootstrap	I									

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AC25	GPMC0_AD8 PADCONFIG: PADCONFIG23 0x000F405C	GPMC0_AD8	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA16	1	O									
		UART2_RXD	2	I	1								
		MCASP2_AXR0	3	IO	0								
		GPIO0_23	7	IO	pad								
		BOOTMODE08	Bootstrap	I									
AB25	GPMC0_AD9 PADCONFIG: PADCONFIG24 0x000F4060	GPMC0_AD9	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA17	1	O									
		UART2_TXD	2	O									
		MCASP2_AXR1	3	IO	0								
		GPIO0_24	7	IO	pad								
		BOOTMODE09	Bootstrap	I									
AA25	GPMC0_AD10 PADCONFIG: PADCONFIG25 0x000F4064	GPMC0_AD10	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA18	1	O									
		UART3_RXD	2	I	1								
		MCASP2_AXR2	3	IO	0								
		GPIO0_25	7	IO	pad								
		OBSCLK0	8	O									
		BOOTMODE10	Bootstrap	I									
W24	GPMC0_AD11 PADCONFIG: PADCONFIG26 0x000F4068	GPMC0_AD11	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA19	1	O									
		UART3_TXD	2	O									
		MCASP2_AXR3	3	IO	0								
		TRC_DATA23	6	O									
		GPIO0_26	7	IO	pad								
		BOOTMODE11	Bootstrap	I									
Y24	GPMC0_AD12 PADCONFIG: PADCONFIG27 0x000F406C	GPMC0_AD12	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA20	1	O									
		UART4_RXD	2	I	1								
		MCASP2_AFSX	3	IO	0								
		TRC_DATA22	6	O									
		GPIO0_27	7	IO	pad								
		BOOTMODE12	Bootstrap	I									

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AD25	GPMC0_AD13 PADCONFIG: PADCONFIG28 0x000F4070	GPMC0_AD13	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA21	1	O									
		UART4_TXD	2	O									
		MCASP2_ACLKX	3	IO	0								
		TRC_DATA21	6	O									
		GPIO0_28	7	IO	pad								
		BOOTMODE13	Bootstrap	I									
AB24	GPMC0_AD14 PADCONFIG: PADCONFIG29 0x000F4074	GPMC0_AD14	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA22	1	O									
		UART5_RXD	2	I	1								
		MCASP2_AFSR	3	IO	0								
		MCASP2_AXR4	4	IO	0								
		TRC_DATA20	6	O									
		GPIO0_29	7	IO	pad								
		UART2_CTSn	8	I	1								
		BOOTMODE14	Bootstrap	I									
AC24	GPMC0_AD15 PADCONFIG: PADCONFIG30 0x000F4078	GPMC0_AD15	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_DATA23	1	O									
		UART5_TXD	2	O									
		MCASP2_ACLKR	3	IO	0								
		MCASP2_AXR5	4	IO	0								
		TRC_DATA19	6	O									
		GPIO0_30	7	IO	pad								
		UART2_RTSn	8	O									
		BOOTMODE15	Bootstrap	I									
U24	GPMC0_BE0n_CLE PADCONFIG: PADCONFIG36 0x000F4090	GPMC0_BE0n_CLE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_ACLKX	2	IO	0								
		TRC_DATA10	6	O									
		GPIO0_35	7	IO	pad								
T24	GPMC0_BE1n PADCONFIG: PADCONFIG37 0x000F4094	GPMC0_BE1n	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR12	3	IO	0								
		TRC_DATA11	6	O									
		GPIO0_36	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
T23	GPMC0_CSn0 PADCONFIG: PADCONFIG42 0x000F40A8	GPMC0_CSn0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR14	3	IO	0								
		TRC_DATA15	6	O									
		GPIO0_41	7	IO	pad								
U23	GPMC0_CSn1 PADCONFIG: PADCONFIG43 0x000F40AC	GPMC0_CSn1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP2_AXR15	3	IO	0								
		TRC_DATA16	6	O									
		GPIO0_42	7	IO	pad								
T22	GPMC0_CSn2 PADCONFIG: PADCONFIG44 0x000F40B0	GPMC0_CSn2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C2_SCL	1	IOD	1								
		MCASP1_AXR4	2	IO	0								
		UART4_RXD	3	I	1								
		MCAN1_TX	5	O									
		TRC_DATA17	6	O									
		GPIO0_43	7	IO	pad								
		MCASP1_AFSR	8	IO	0								
U25	GPMC0_CSn3 PADCONFIG: PADCONFIG45 0x000F40B4	GPMC0_CSn3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C2_SDA	1	IOD	1								
		GPMC0_A20	2	OZ									
		UART4_TXD	3	O									
		MCASP1_AXR5	4	IO	0								
		MCAN1_RX	5	I	1								
		TRC_DATA18	6	O									
		GPIO0_44	7	IO	pad								
		MCASP1_ACLKR	8	IO	0								
AA24	GPMC0_WAIT0 PADCONFIG: PADCONFIG38 0x000F4098	GPMC0_WAIT0	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		MCASP1_AFSX	2	IO	0								
		TRC_DATA12	6	O									
		GPIO0_37	7	IO	pad								
AD24	GPMC0_WAIT1 PADCONFIG: PADCONFIG39 0x000F409C	GPMC0_WAIT1	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		VOUT0_EXTPCLKIN	1	I	0								
		GPMC0_A21	2	OZ									
		UART6_RXD	3	I	1								
		GPIO0_38	7	IO	pad								
		EQEP2_I	8	IO	0								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
B25	I2C0_SCL PADCONFIG: PADCONFIG120 0x000F41E0	I2C0_SCL	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SYNC0_OUT	2	O									
		OBSCLK1	3	O									
		UART1_DCDn	4	I	1								
		EQEP2_A	5	I	0								
		EHRPWM_SOCA	6	O									
		GPIO1_26	7	IO	pad								
		ECAP1_IN_APWM_OUT	8	IO	0								
		SPI2_CS0	9	IO	1								
A24	I2C0_SDA PADCONFIG: PADCONFIG121 0x000F41E4	I2C0_SDA	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS2	2	IO	1								
		TIMER_IO5	3	IO	0								
		UART1_DSRn	4	I	1								
		EQEP2_B	5	I	0								
		EHRPWM_SOCB	6	O									
		GPIO1_27	7	IO	pad								
		ECAP2_IN_APWM_OUT	8	IO	0								
C24	I2C1_SCL PADCONFIG: PADCONFIG122 0x000F41E8	I2C1_SCL	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_RXD	1	I	1								
		TIMER_IO0	2	IO	0								
		SPI2_CS1	3	IO	1								
		EHRPWM0_SYNCI	4	I	0								
		GPIO1_28	7	IO	pad								
		EHRPWM2_A	8	IO	0								
		MMC2_SDCD	9	I	0								
B24	I2C1_SDA PADCONFIG: PADCONFIG123 0x000F41EC	I2C1_SDA	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART1_TXD	1	O									
		TIMER_IO1	2	IO	0								
		SPI2_CLK	3	IO	0								
		EHRPWM0_SYNCO	4	O									
		GPIO1_29	7	IO	pad								
		EHRPWM2_B	8	IO	0								
		MMC2_SDWP	9	I	0								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
F20	MCAN0_RX PADCONFIG: PADCONFIG119 0x000F41DC	MCAN0_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART5_TXD	1	O									
		TIMER_IO3	2	IO	0								
		SYNC3_OUT	3	O									
		UART1_RIn	4	I	1								
		EQEP2_S	5	IO	0								
		GPIO1_25	7	IO	pad								
		MCASP2_AXR1	8	IO	0								
		EHRPWM_TZn_IN4	9	I	0								
B23	MCAN0_TX PADCONFIG: PADCONFIG118 0x000F41D8	MCAN0_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART5_RXD	1	I	1								
		TIMER_IO2	2	IO	0								
		SYNC2_OUT	3	O									
		UART1_DTRn	4	O									
		EQEP2_I	5	IO	0								
		GPIO1_24	7	IO	pad								
		MCASP2_AXR0	8	IO	0								
		EHRPWM_TZn_IN3	9	I	0								
G20	MCASP0_ACLKR PADCONFIG: PADCONFIG108 0x000F41B0	MCASP0_ACLKR	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CLK	1	IO	0								
		UART1_TXD	2	O									
		EHRPWM0_B	6	IO	0								
		GPIO1_14	7	IO	pad								
		EQEP1_I	8	IO	0								
F24	MCASP0_ACLKX PADCONFIG: PADCONFIG105 0x000F41A4	MCASP0_ACLKX	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS1	1	IO	1								
		ECAP2_IN_APWM_OUT	2	IO	0								
		GPIO1_11	7	IO	pad								
		EQEP1_A	8	I	0								
G23	MCASP0_AFSR PADCONFIG: PADCONFIG107 0x000F41AC	MCASP0_AFSR	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS0	1	IO	1								
		UART1_RXD	2	I	1								
		EHRPWM0_A	6	IO	0								
		GPIO1_13	7	IO	pad								
		EQEP1_S	8	IO	0								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
F25	MCASP0_AFSX PADCONFIG: PADCONFIG106 0x000F41A8	MCASP0_AFSX	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS3	1	IO	1								
		AUDIO_EXT_REFCLK1	2	IO	0								
		GPIO1_12	7	IO	pad								
		EQEP1_B	8	I	0								
F23	MCASP0_AXR0 PADCONFIG: PADCONFIG104 0x000F41A0	MCASP0_AXR0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK0	2	IO	0								
		EHRPWM1_B	6	IO	0								
		GPIO1_10	7	IO	pad								
		EQEP0_I	8	IO	0								
E24	MCASP0_AXR1 PADCONFIG: PADCONFIG103 0x000F419C	MCASP0_AXR1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS2	1	IO	1								
		ECAP1_IN_APWM_OUT	2	IO	0								
		MAIN_ERRORn	5	IO	1								
		EHRPWM1_A	6	IO	0								
		GPIO1_9	7	IO	pad								
		EQEP0_S	8	IO	0								
E25	MCASP0_AXR2 PADCONFIG: PADCONFIG102 0x000F4198	MCASP0_AXR2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_D1	1	IO	0								
		UART1_RTSn	2	O									
		UART6_TXD	3	O									
		ECAP2_IN_APWM_OUT	5	IO	0								
		GPIO1_8	7	IO	pad								
		EQEP0_B	8	I	0								
D25	MCASP0_AXR3 PADCONFIG: PADCONFIG101 0x000F4194	MCASP0_AXR3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_D0	1	IO	0								
		UART1_CTSn	2	I	1								
		UART6_RXD	3	I	1								
		ECAP1_IN_APWM_OUT	5	IO	0								
		GPIO1_7	7	IO	pad								
		EQEP0_A	8	I	0								
G6	MCU_ERRORn PADCONFIG: MCU_PADCONFIG24 0x04084060	MCU_ERRORn	0	IO		Off / Off / Down	On / SS / Down	0	1.8 V	VDDS_OSC0	Yes	LVCMOS	PU/PD

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
E11	MCU_I2C0_SCL PADCONFIG: MCU_PADCONFIG17 0x04084044	MCU_I2C0_SCL	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
		MCU_GPIO0_17	7	IOD	pad								
D11	MCU_I2C0_SDA PADCONFIG: MCU_PADCONFIG18 0x04084048	MCU_I2C0_SDA	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
		MCU_GPIO0_18	7	IOD	pad								
D6	MCU_MCAN0_RX PADCONFIG: MCU_PADCONFIG14 0x04084038	MCU_MCAN0_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO0	1	IO	0								
		MCU_SPI1_CS3	2	IO	1								
		MCU_GPIO0_14	7	IO	pad								
E8	MCU_MCAN0_TX PADCONFIG: MCU_PADCONFIG13 0x04084034	MCU_MCAN0_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		WKUP_TIMER_IO0	1	IO	0								
		MCU_SPI0_CS3	2	IO	1								
		MCU_GPIO0_13	7	IO	pad								
E7	MCU_MCAN1_RX PADCONFIG: MCU_PADCONFIG16 0x04084040	MCU_MCAN1_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO3	1	IO	0								
		MCU_SPI0_CS2	2	IO	1								
		MCU_SPI1_CS2	3	IO	1								
		MCU_SPI1_CLK	4	IO	0								
		MCU_GPIO0_16	7	IO	pad								
F8	MCU_MCAN1_TX PADCONFIG: MCU_PADCONFIG15 0x0408403C	MCU_MCAN1_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO2	1	IO	0								
		MCU_SPI1_CS1	3	IO	1								
		MCU_EXT_REFCLK0	4	I	0								
		MCU_GPIO0_15	7	IO	pad								
A10	MCU_OSC0_XI	MCU_OSC0_XI		I					1.8 V	VDDS_OSC0		HFOSC	
A11	MCU_OSC0_XO	MCU_OSC0_XO		O					1.8 V	VDDS_OSC0		HFOSC	
H6	MCU_PORz PADCONFIG: MCU_PADCONFIG22 0x04084058	MCU_PORz	0	I				0	1.8 V	VDDS_OSC0	Yes	FS RESET	
F14	MCU_RESETSTATz PADCONFIG: MCU_PADCONFIG23 0x0408405C	MCU_RESETSTATz	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_21	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
F11	MCU_RESETz PADCONFIG: MCU_PADCONFIG21 0x04084054	MCU_RESETz	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
C10	MCU_SPI0_CLK PADCONFIG: MCU_PADCONFIG2 0x04084008	MCU_SPI0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_2	7	IO	pad								
B10	MCU_SPI0_CS0 PADCONFIG: MCU_PADCONFIG0 0x04084000	MCU_SPI0_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		WKUP_TIMER_IO1	4	IO	0								
		MCU_GPIO0_0	7	IO	pad								
E10	MCU_SPI0_CS1 PADCONFIG: MCU_PADCONFIG1 0x04084004	MCU_SPI0_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_OBSCLK0	1	O									
		MCU_SYSCLKOUT0	2	O									
		MCU_EXT_REFCLK0	3	I	0								
		MCU_TIMER_IO1	4	IO	0								
		MCU_GPIO0_1	7	IO	pad								
B11	MCU_SPI0_D0 PADCONFIG: MCU_PADCONFIG3 0x0408400C	MCU_SPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_3	7	IO	pad								
D10	MCU_SPI0_D1 PADCONFIG: MCU_PADCONFIG4 0x04084010	MCU_SPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_4	7	IO	pad								
B8	MCU_UART0_CTSn PADCONFIG: MCU_PADCONFIG7 0x0408401C	MCU_UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO0	1	IO	0								
		MCU_SPI1_D0	3	IO	0								
		MCU_GPIO0_7	7	IO	pad								
B7	MCU_UART0_RTSn PADCONFIG: MCU_PADCONFIG8 0x04084020	MCU_UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO1	1	IO	0								
		MCU_SPI1_D1	3	IO	0								
		MCU_GPIO0_8	7	IO	pad								
B6	MCU_UART0_RXD PADCONFIG: MCU_PADCONFIG5 0x04084014	MCU_UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_GPIO0_5	7	IO	pad								
C8	MCU_UART0_TXD PADCONFIG: MCU_PADCONFIG6 0x04084018	MCU_UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_GPIO0_6	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
F17	MDIO0_MDC PADCONFIG: PADCONFIG88 0x000F4160	MDIO0_MDC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_86	7	IO	pad								
F16	MDIO0_MDIO PADCONFIG: PADCONFIG87 0x000F415C	MDIO0_MDIO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_85	7	IO	pad								
AC5	MMC0_CALPAD	MMC0_CALPAD		A					1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	
AA6	MMC0_CLK	MMC0_CLK		O		On / Low / Off	On / SS / Off		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD
AB8	MMC0_CMD	MMC0_CMD		IO		On / High / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD
AD5	MMC0_DS	MMC0_DS		I		On / Off / Down	On / Off / Down		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD
J24	MMC1_CLK PADCONFIG: PADCONFIG141 0x000F4234	MMC1_CLK	0	O	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		TIMER_IO4	2	IO	0								
		UART3_RXD	3	I	1								
		SPI1_CS0	5	IO	1								
		SPI2_CS2	6	IO	1								
		GPIO1_46	7	IO	pad								
H20	MMC1_CMD PADCONFIG: PADCONFIG143 0x000F423C	MMC1_CMD	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		TIMER_IO5	2	IO	0								
		UART3_TXD	3	O									
		SPI1_CLK	5	IO	0								
		SPI2_CS0	6	IO	1								
		GPIO1_47	7	IO	pad								
D23	MMC1_SDCD PADCONFIG: PADCONFIG144 0x000F4240	MMC1_SDCD	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART6_RXD	1	I	1								
		TIMER_IO6	2	IO	0								
		UART3_RTSn	3	O									
		MCAN1_TX	4	O									
		SPI1_CS3	5	IO	1								
		SPI2_CLK	6	IO	0								
		GPIO1_48	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
D24	MMC1_SDWP PADCONFIG: PADCONFIG145 0x000F4244	MMC1_SDWP	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART6_TXD	1	O									
		TIMER_IO7	2	IO	0								
		UART3_CTSn	3	I	1								
		MCAN1_RX	4	I	1								
		SPI1_CS1	5	IO	1								
		GPIO1_49	7	IO	pad								
K21	MMC2_CLK PADCONFIG: PADCONFIG70 0x000F4118	MMC2_CLK	0	O	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_ACLKR	1	IO	0								
		MCASP1_AXR5	2	IO	0								
		UART6_RXD	3	I	1								
		EHRPWM0_SYNCI	4	I	0								
		I2C3_SCL	6	IOD	1								
		GPIO0_69	7	IO	pad								
K24	MMC2_CMD PADCONFIG: PADCONFIG72 0x000F4120	MMC2_CMD	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_AFSR	1	IO	0								
		MCASP1_AXR4	2	IO	0								
		UART6_TXD	3	O									
		EHRPWM0_SYNCO	4	O									
		EHRPWM_TZn_IN0	5	I	0								
		I2C3_SDA	6	IOD	1								
		GPIO0_70	7	IO	pad								
J25	MMC2_SDCD PADCONFIG: PADCONFIG73 0x000F4124	MMC2_SDCD	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	LVCMOS	PU/PD
		MCASP1_ACLKX	1	IO	0								
		UART4_RXD	3	I	1								
		EHRPWM2_A	4	IO	0								
		EHRPWM_TZn_IN1	5	I	0								
		GPIO0_71	7	IO	pad								
K25	MMC2_SDWP PADCONFIG: PADCONFIG74 0x000F4128	MMC2_SDWP	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	LVCMOS	PU/PD
		MCASP1_AFSX	1	IO	0								
		UART4_TXD	3	O									
		EHRPWM2_B	4	IO	0								
		EHRPWM_TZn_IN2	5	I	0								
		GPIO0_72	7	IO	pad								
AC7	MMC0_DAT0	MMC0_DAT0		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AB7	MMC0_DAT1	MMC0_DAT1		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD
AD6	MMC0_DAT2	MMC0_DAT2		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD
AE5	MMC0_DAT3	MMC0_DAT3		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD
AE6	MMC0_DAT4	MMC0_DAT4		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD
AC6	MMC0_DAT5	MMC0_DAT5		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD
AA7	MMC0_DAT6	MMC0_DAT6		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD
AB6	MMC0_DAT7	MMC0_DAT7		IO		On / Off / Up	On / SS / Up		1.8 V	VDDS_MMC0, VDDA_0P85_DLL_MMC0	No	eMMCPHY	PU/PD
H21	MMC1_DAT0 PADCONFIG: PADCONFIG140 0x000F4230	MMC1_DAT0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_HW2TSPUSH	1	I	0								
		TIMER_IO3	2	IO	0								
		UART2_CTSn	3	I	1								
		ECAP2_IN_APWM_OUT	4	IO	0								
		SPI2_D1	6	IO	0								
		GPIO1_45	7	IO	pad								
H23	MMC1_DAT1 PADCONFIG: PADCONFIG139 0x000F422C	MMC1_DAT1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_HW1TSPUSH	1	I	0								
		TIMER_IO2	2	IO	0								
		UART2_RTSn	3	O									
		ECAP1_IN_APWM_OUT	4	IO	0								
		SPI1_CS2	5	IO	1								
		SPI2_D0	6	IO	0								
		GPIO1_44	7	IO	pad								

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
H22	MMC1_DAT2 PADCONFIG: PADCONFIG138 0x000F4228	MMC1_DAT2	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_TS_SYNC	1	O									
		TIMER_IO1	2	IO	0								
		UART2_TXD	3	O									
		MCAN1_RX	4	I	1								
		SPI1_D1	5	IO	0								
		SPI2_CS3	6	IO	1								
		GPIO1_43	7	IO	pad								
H25	MMC1_DAT3 PADCONFIG: PADCONFIG137 0x000F4224	MMC1_DAT3	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_TS_COMP	1	O									
		TIMER_IO0	2	IO	0								
		UART2_RXD	3	I	1								
		MCAN1_TX	4	O									
		SPI1_D0	5	IO	0								
		SPI2_CS1	6	IO	1								
		GPIO1_42	7	IO	pad								
K23	MMC2_DAT0 PADCONFIG: PADCONFIG69 0x000F4114	MMC2_DAT0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_AXR0	1	IO	0								
		EHRPWM1_B	4	IO	0								
		I2C2_SCL	5	IOD	1								
		GPIO0_68	7	IO	pad								
K22	MMC2_DAT1 PADCONFIG: PADCONFIG68 0x000F4110	MMC2_DAT1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_AXR1	1	IO	0								
		EHRPWM1_A	4	IO	0								
		I2C2_SDA	5	IOD	1								
		GPIO0_67	7	IO	pad								
L20	MMC2_DAT2 PADCONFIG: PADCONFIG67 0x000F410C	MMC2_DAT2	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_AXR2	1	IO	0								
		UART5_TXD	3	O									
		EHRPWM0_B	4	IO	0								
		I2C2_SDA	5	IOD	1								
		GPIO0_66	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
L21	MMC2_DAT3 PADCONFIG: PADCONFIG66 0x000F4108	MMC2_DAT3	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD
		MCASP1_AXR3	1	IO	0								
		UART5_RXD	3	I	1								
		EHRPWM0_A	4	IO	0								
		GPIO0_65	7	IO	pad								
AE20	OLDI0_A0N	OLDI0_A0N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD20	OLDI0_A0P	OLDI0_A0P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AC19	OLDI0_A1N	OLDI0_A1N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD19	OLDI0_A1P	OLDI0_A1P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AA19	OLDI0_A2N	OLDI0_A2N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AB19	OLDI0_A2P	OLDI0_A2P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD18	OLDI0_A3N	OLDI0_A3N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AE19	OLDI0_A3P	OLDI0_A3P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD17	OLDI0_A4N	OLDI0_A4N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD16	OLDI0_A4P	OLDI0_A4P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AB17	OLDI0_A5N	OLDI0_A5N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AC17	OLDI0_A5P	OLDI0_A5P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AC16	OLDI0_A6N	OLDI0_A6N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AC15	OLDI0_A6P	OLDI0_A6P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AB16	OLDI0_A7N	OLDI0_A7N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AA16	OLDI0_A7P	OLDI0_A7P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AE18	OLDI0_CLK0N	OLDI0_CLK0N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AE17	OLDI0_CLK0P	OLDI0_CLK0P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD15	OLDI0_CLK1N	OLDI0_CLK1N		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
AD14	OLDI0_CLK1P	OLDI0_CLK1P		IO					1.8 V	VDDA_1P8_OLDI		OLDI	
P23	OSPI0_CLK PADCONFIG: PADCONFIG0 0x000F4000	OSPI0_CLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO0_0	7	IO	pad								
P22	OSPI0_DQS PADCONFIG: PADCONFIG2 0x000F4008	OSPI0_DQS	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART5_CTSn	5	I	1								
		GPIO0_2	7	IO	pad								
N23	OSPI0_LBCLKO PADCONFIG: PADCONFIG1 0x000F4004	OSPI0_LBCLKO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		UART5_RTSn	5	O									
		GPIO0_1	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
M25	OSPI0_CSn0	OSPI0_CSn0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG: PADCONFIG11 0x000F402C	GPIO0_11	7	IO	pad								
L24	OSPI0_CSn1	OSPI0_CSn1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG: PADCONFIG12 0x000F4030	GPIO0_12	7	IO	pad								
L22	OSPI0_CSn2 PADCONFIG: PADCONFIG13 0x000F4034	OSPI0_CSn2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_CS1	1	IO	1								
		OSPI0_RESET_OUT1	2	O									
		MCASP1_AFSR	3	IO	0								
		MCASP1_AXR2	4	IO	0								
		UART5_RXD	5	I	1								
		GPIO0_13	7	IO	pad								
L23	OSPI0_CSn3 PADCONFIG: PADCONFIG14 0x000F4038	OSPI0_CSn3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		OSPI0_RESET_OUT0	1	O									
		OSPI0_ECC_FAIL	2	I	1								
		MCASP1_ACLKR	3	IO	0								
		MCASP1_AXR3	4	IO	0								
		UART5_TXD	5	O									
		GPIO0_14	7	IO	pad								
L25	OSPI0_D0	OSPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG: PADCONFIG3 0x000F400C	GPIO0_3	7	IO	pad								
N24	OSPI0_D1	OSPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG: PADCONFIG4 0x000F4010	GPIO0_4	7	IO	pad								
N25	OSPI0_D2	OSPI0_D2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG: PADCONFIG5 0x000F4014	GPIO0_5	7	IO	pad								
M24	OSPI0_D3	OSPI0_D3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
	PADCONFIG: PADCONFIG6 0x000F4018	GPIO0_6	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
N21	OSPI0_D4 PADCONFIG: PADCONFIG7 0x000F401C	OSPI0_D4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_CS0	1	IO	1								
		MCASP1_AXR1	2	IO	0								
		UART6_RXD	3	I	1								
		GPIO0_7	7	IO	pad								
N22	OSPI0_D5 PADCONFIG: PADCONFIG8 0x000F4020	OSPI0_D5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_CLK	1	IO	0								
		MCASP1_AXR0	2	IO	0								
		UART6_TXD	3	O									
		GPIO0_8	7	IO	pad								
P21	OSPI0_D6 PADCONFIG: PADCONFIG9 0x000F4024	OSPI0_D6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_D0	1	IO	0								
		MCASP1_ACLKX	2	IO	0								
		UART6_RTSn	3	O									
		GPIO0_9	7	IO	pad								
N20	OSPI0_D7 PADCONFIG: PADCONFIG10 0x000F4028	OSPI0_D7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		SPI1_D1	1	IO	0								
		MCASP1_AFSX	2	IO	0								
		UART6_CTSn	3	I	1								
		GPIO0_10	7	IO	pad								
B9	PMIC_LPM_EN0 PADCONFIG: MCU_PADCONFIG32 0x04084080	PMIC_LPM_EN0	0	O		Off / Off / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_GPIO0_22	7	IO	pad								
H24	PORz_OUT PADCONFIG: PADCONFIG148 0x000F4250	PORz_OUT	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
G25	RESETSTATz PADCONFIG: PADCONFIG147 0x000F424C	RESETSTATz	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
G24	RESET_REQz PADCONFIG: PADCONFIG146 0x000F4248	RESET_REQz	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
A16	RGMII1_RXC PADCONFIG: PADCONFIG82 0x000F4148	RGMII1_RXC	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_REF_CLK	1	I	0								
		GPIO0_80	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A15	RGMII1_RX_CTL PADCONFIG: PADCONFIG81 0x000F4144	RGMII1_RX_CTL	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_RX_ER	1	I	0								
		GPIO0_79	7	IO	pad								
B17	RGMII1_TXC PADCONFIG: PADCONFIG76 0x000F4130	RGMII1_TXC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_CRS_DV	1	I	0								
		GPIO0_74	7	IO	pad								
B18	RGMII1_TX_CTL PADCONFIG: PADCONFIG75 0x000F412C	RGMII1_TX_CTL	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_TX_EN	1	O									
		GPIO0_73	7	IO	pad								
D19	RGMII2_RXC PADCONFIG: PADCONFIG96 0x000F4180	RGMII2_RXC	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_REF_CLK	1	I	0								
		MCASP2_AXR1	2	IO	0								
		GPIO1_2	7	IO	pad								
F19	RGMII2_RX_CTL PADCONFIG: PADCONFIG95 0x000F417C	RGMII2_RX_CTL	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_RX_ER	1	I	0								
		MCASP2_AXR3	2	IO	0								
		GPIO1_1	7	IO	pad								
D16	RGMII2_TXC PADCONFIG: PADCONFIG90 0x000F4168	RGMII2_TXC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_CRS_DV	1	I	0								
		MCASP2_AXR5	2	IO	0								
		GPIO0_88	7	IO	pad								
A20	RGMII2_TX_CTL PADCONFIG: PADCONFIG89 0x000F4164	RGMII2_TX_CTL	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_TX_EN	1	O									
		MCASP2_AXR4	2	IO	0								
		GPIO0_87	7	IO	pad								
B15	RGMII1_RD0 PADCONFIG: PADCONFIG83 0x000F414C	RGMII1_RD0	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_RXD0	1	I	0								
		GPIO0_81	7	IO	pad								
B16	RGMII1_RD1 PADCONFIG: PADCONFIG84 0x000F4150	RGMII1_RD1	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_RXD1	1	I	0								
		GPIO0_82	7	IO	pad								
A14	RGMII1_RD2 PADCONFIG: PADCONFIG85 0x000F4154	RGMII1_RD2	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_83	7	IO	pad								

ADVANCE INFORMATION

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
B14	RGMII1_RD3 PADCONFIG: PADCONFIG86 0x000F4158	RGMII1_RD3	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_84	7	IO	pad								
A18	RGMII1_TD0 PADCONFIG: PADCONFIG77 0x000F4134	RGMII1_TD0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_TXD0	1	O									
		GPIO0_75	7	IO	pad								
C17	RGMII1_TD1 PADCONFIG: PADCONFIG78 0x000F4138	RGMII1_TD1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII1_TXD1	1	O									
		GPIO0_76	7	IO	pad								
A17	RGMII1_TD2 PADCONFIG: PADCONFIG79 0x000F413C	RGMII1_TD2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		GPIO0_77	7	IO	pad								
C16	RGMII1_TD3 PADCONFIG: PADCONFIG80 0x000F4140	RGMII1_TD3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		CLKOUT0	1	O									
		GPIO0_78	7	IO	pad								
E19	RGMII2_RD0 PADCONFIG: PADCONFIG97 0x000F4184	RGMII2_RD0	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_RXD0	1	I	0								
		MCASP2_AXR2	2	IO	0								
		GPIO1_3	7	IO	pad								
E16	RGMII2_RD1 PADCONFIG: PADCONFIG98 0x000F4188	RGMII2_RD1	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_RXD1	1	I	0								
		MCASP2_AFSR	2	IO	0								
		MCASP2_AXR7	5	IO	0								
		GPIO1_4	7	IO	pad								
E17	RGMII2_RD2 PADCONFIG: PADCONFIG99 0x000F418C	RGMII2_RD2	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP2_AXR0	2	IO	0								
		GPIO1_5	7	IO	pad								
		EQEP2_A	8	I	0								
C19	RGMII2_RD3 PADCONFIG: PADCONFIG100 0x000F4190	RGMII2_RD3	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		AUDIO_EXT_REFCLK0	2	IO	0								
		GPIO1_6	7	IO	pad								
		EQEP2_B	8	I	0								

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
B19	RGMII2_TD0 PADCONFIG: PADCONFIG91 0x000F416C	RGMII2_TD0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_TXD0	1	O									
		MCASP2_AXR6	2	IO	0								
		GPIO0_89	7	IO	pad								
A21	RGMII2_TD1 PADCONFIG: PADCONFIG92 0x000F4170	RGMII2_TD1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		RMII2_TXD1	1	O									
		MCASP2_ACLKR	2	IO	0								
		MCASP2_AXR8	5	IO	0								
		GPIO0_90	7	IO	pad								
D17	RGMII2_TD2 PADCONFIG: PADCONFIG93 0x000F4174	RGMII2_TD2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MCASP2_AFSX	2	IO	0								
		GPIO0_91	7	IO	pad								
		EQEP2_I	8	IO	0								
A19	RGMII2_TD3 PADCONFIG: PADCONFIG94 0x000F4178	RGMII2_TD3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		CLKOUT0	1	O									
		MCASP2_ACLKX	2	IO	0								
		GPIO1_0	7	IO	pad								
		EQEP2_S	8	IO	0								
Y13	RSVD0	RSVD0		N/A									
Y14	RSVD1	RSVD1		N/A									
Y17	RSVD2	RSVD2		N/A									
Y19	RSVD3	RSVD3		N/A									
AA17	RSVD4	RSVD4		N/A									
B5	RSVD5	RSVD5		N/A									
C5	RSVD6	RSVD6		N/A									
F6	RSVD7	RSVD7		N/A									
F10	RSVD8	RSVD8		N/A									
H5	RSVD9	RSVD9		N/A									
K6	RSVD10	RSVD10		N/A									
B21	SPI0_CLK PADCONFIG: PADCONFIG111 0x000F41BC	SPI0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_TS_SYNC	1	O									
		EHRPWM1_A	2	IO	0								
		GPIO1_17	7	IO	pad								
D20	SPI0_CS0 PADCONFIG: PADCONFIG109 0x000F41B4	SPI0_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		EHRPWM0_A	2	IO	0								
		GPIO1_15	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
E20	SPI0_CS1 PADCONFIG: PADCONFIG110 0x000F41B8	SPI0_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_TS_COMP	1	O									
		EHRPWM0_B	2	IO	0								
		ECAP0_IN_APWM_OUT	3	IO	0								
		MAIN_ERRORn	5	IO	1								
		GPIO1_16	7	IO	pad								
		EHRPWM_TZn_IN5	9	I	0								
B20	SPI0_D0 PADCONFIG: PADCONFIG112 0x000F41C0	SPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_HW1TSPUSH	1	I	0								
		EHRPWM1_B	2	IO	0								
		GPIO1_18	7	IO	pad								
C21	SPI0_D1 PADCONFIG: PADCONFIG113 0x000F41C4	SPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CP_GEMAC_CPTS0_HW2TSPUSH	1	I	0								
		EHRPWM_TZn_IN0	2	I	0								
		GPIO1_19	7	IO	pad								
C13	TCK PADCONFIG: MCU_PADCONFIG25 0x04084064	TCK	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
E13	TDI PADCONFIG: MCU_PADCONFIG27 0x0408406C	TDI	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
C14	TDO PADCONFIG: MCU_PADCONFIG28 0x04084070	TDO	0	OZ		Off / Off / Up	Off / SS / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
E14	TMS PADCONFIG: MCU_PADCONFIG29 0x04084074	TMS	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
B13	TRSTn PADCONFIG: MCU_PADCONFIG26 0x04084068	TRSTn	0	I		On / Off / Down	On / Off / Down	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
A23	UART0_CTSn PADCONFIG: PADCONFIG116 0x000F41D0	UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI0_CS2	1	IO	1								
		I2C3_SCL	2	IOD	1								
		UART2_RXD	3	I	1								
		TIMER_IO6	4	IO	0								
		AUDIO_EXT_REFCLK0	5	IO	0								
		GPIO1_22	7	IO	pad								
		MCASP2_AFSX	8	IO	0								
		MMC2_SDCD	9	I	0								
C22	UART0_RTSn PADCONFIG: PADCONFIG117 0x000F41D4	UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI0_CS3	1	IO	1								
		I2C3_SDA	2	IOD	1								
		UART2_TXD	3	O									
		TIMER_IO7	4	IO	0								
		AUDIO_EXT_REFCLK1	5	IO	0								
		GPIO1_23	7	IO	pad								
		MCASP2_ACLKX	8	IO	0								
		MMC2_SDWP	9	I	0								
A22	UART0_RXD PADCONFIG: PADCONFIG114 0x000F41C8	UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP1_IN_APWM_OUT	1	IO	0								
		SPI2_D0	2	IO	0								
		EHRPWM2_A	3	IO	0								
		GPIO1_20	7	IO	pad								
B22	UART0_TXD PADCONFIG: PADCONFIG115 0x000F41CC	UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		ECAP2_IN_APWM_OUT	1	IO	0								
		SPI2_D1	2	IO	0								
		EHRPWM2_B	3	IO	0								
		GPIO1_21	7	IO	pad								
AE8	USB0_DM	USB0_DM		IO					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
AE7	USB0_DP	USB0_DP		IO					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
G22	USB0_DRVVBUS PADCONFIG: PADCONFIG149 0x000F4254	USB0_DRVVBUS	0	O		Off / Off / Down	Off / Off / Down	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		GPIO1_50	7	IO	pad								
Y8	USB0_RCALIB	USB0_RCALIB		A					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y7	USB0_VBUS	USB0_VBUS		A					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
AE10	USB1_DM	USB1_DM		IO					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
AE9	USB1_DP	USB1_DP		IO					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
G21	USB1_DRVVBUS	USB1_DRVVBUS	0	O		Off / Off / Down	Off / Off / Down	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
	PADCONFIG: PADCONFIG150 0x000F4258	GPIO1_51	7	IO	pad								
1K4	USB1_RCALIB	USB1_RCALIB		A					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
Y10	USB1_VBUS	USB1_VBUS		A					1.8 V/3.3 V	VDDA_1P8_USB, VDDA_3P3_USB		USB2PHY	
1J1	VDDA_0P85_DLL_MMC0	VDDA_0P85_DLL_MMC0		PWR									
1K7	VDDA_1P8_CSI_DSI	VDDA_1P8_CSI_DSI		PWR									
1K5	VDDA_1P8_USB	VDDA_1P8_USB		PWR									
1K10	VDDA_1P8_OLDI0	VDDA_1P8_OLDI0		PWR									
Y11	VDDA_3P3_USB	VDDA_3P3_USB		PWR									
1K6	VDDA_CORE_CSI_DSI	VDDA_CORE_CSI_DSI		PWR									
1K8	VDDA_CORE_DSI_CLK	VDDA_CORE_DSI_CLK		PWR									
1J4	VDDA_CORE_USB	VDDA_CORE_USB		PWR									
1F2	VDDA_DDR_PLL0	VDDA_DDR_PLL0		PWR									
1C3	VDDA_MCU	VDDA_MCU		PWR									
1D4	VDDA_PLL0	VDDA_PLL0		PWR									
1H7	VDDA_PLL1	VDDA_PLL1		PWR									
1F6	VDDA_PLL2	VDDA_PLL2		PWR									
1F4	VDDA_PLL3	VDDA_PLL3		PWR									
1D7	VDDA_PLL4	VDDA_PLL4		PWR									
1F5	VDDA_TEMP0	VDDA_TEMP0		PWR									
K20	VDDA_TEMP1	VDDA_TEMP1		PWR									
1D3	VDDA_TEMP2	VDDA_TEMP2		PWR									
1C8, 1E5, 1H3	VDDR_CORE	VDDR_CORE		PWR									
1B7	VDDSHV0	VDDSHV0		PWR									
1D10	VDDSHV1	VDDSHV1		PWR									
1B5	VDDSHV2	VDDSHV2		PWR									
1E10, 1G10	VDDSHV3	VDDSHV3		PWR									
1A9	VDDSHV5	VDDSHV5		PWR									

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
1B10	VDDSHV6	VDDSHV6		PWR									
1A2	VDDSHV_CANUART	VDDSHV_CANUART		PWR									
1B3	VDDSHV_MCU	VDDSHV_MCU		PWR									
1C1, 1D2, 1E1, 1F1, 1G2, 1H1, AE2, B1	VDDS_DDR	VDDS_DDR		PWR									
1E2	VDDS_DDR_C	VDDS_DDR_C		PWR									
1K2	VDDS_MMC0	VDDS_MMC0		PWR									
1C2	VDDS_OSC0	VDDS_OSC0		PWR									
1A1	VDD_CANUART	VDD_CANUART		PWR									
1C5, 1C7, 1D6, 1D8, 1E3, 1E7, 1E9, 1F8, 1G3, 1G5, 1G7, 1G9, 1H10, 1H4, 1H6, 1H8, 1J2, 1J5, 1J7, 1J9	VDD_CORE	VDD_CORE		PWR									
1K3	VDD_MMC0	VDD_MMC0		PWR									
1A10	VMON_1P8_SOC	VMON_1P8_SOC		A									
1A4	VMON_3P3_SOC	VMON_3P3_SOC		A									
1A6	VMON_VSYS	VMON_VSYS		A									
W21	VOUT0_DE PADCONFIG: PADCONFIG63 0x000F40FC	VOUT0_DE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A17	1	OZ									
		UART3_CTSn	4	I	1								
		GPIO0_62	7	IO	pad								
AC20	VOUT0_HSYNC PADCONFIG: PADCONFIG62 0x000F40F8	VOUT0_HSYNC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A16	1	OZ									
		UART3_RTSn	4	O									
		GPIO0_61	7	IO	pad								
Y21	VOUT0_PCLK PADCONFIG: PADCONFIG65 0x000F4104	VOUT0_PCLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A19	1	OZ									
		UART2_CTSn	4	I	1								
		GPIO0_64	7	IO	pad								
W20	VOUT0_VSYNC PADCONFIG: PADCONFIG64 0x000F4100	VOUT0_VSYNC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A18	1	OZ									
		UART2_RTSn	4	O									
		GPIO0_63	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AE24	VOUT0_DATA0 PADCONFIG: PADCONFIG46 0x000F40B8	VOUT0_DATA0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A0	1	OZ									
		UART2_RXD	4	I	1								
		GPIO0_45	7	IO	pad								
W23	VOUT0_DATA1 PADCONFIG: PADCONFIG47 0x000F40BC	VOUT0_DATA1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A1	1	OZ									
		UART2_TXD	4	O									
		GPIO0_46	7	IO	pad								
AA23	VOUT0_DATA2 PADCONFIG: PADCONFIG48 0x000F40C0	VOUT0_DATA2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A2	1	OZ									
		UART3_RXD	4	I	1								
		GPIO0_47	7	IO	pad								
Y23	VOUT0_DATA3 PADCONFIG: PADCONFIG49 0x000F40C4	VOUT0_DATA3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A3	1	OZ									
		UART3_TXD	4	O									
		AUDIO_EXT_REFCLK0	5	IO	0								
		GPIO0_48	7	IO	pad								
AB23	VOUT0_DATA4 PADCONFIG: PADCONFIG50 0x000F40C8	VOUT0_DATA4	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A4	1	OZ									
		UART4_RXD	4	I	1								
		EQEP2_I	5	IO	0								
		GPIO0_49	7	IO	pad								
AD23	VOUT0_DATA5 PADCONFIG: PADCONFIG51 0x000F40CC	VOUT0_DATA5	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A5	1	OZ									
		UART4_TXD	4	O									
		EQEP2_S	5	IO	0								
		GPIO0_50	7	IO	pad								
AC23	VOUT0_DATA6 PADCONFIG: PADCONFIG52 0x000F40D0	VOUT0_DATA6	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A6	1	OZ									
		UART5_RXD	4	I	1								
		EQEP2_A	5	I	0								
		GPIO0_51	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
AE23	VOUT0_DATA7 PADCONFIG: PADCONFIG53 0x000F40D4	VOUT0_DATA7	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A7	1	OZ									
		UART5_TXD	4	O									
		EQEP2_B	5	I	0								
		GPIO0_52	7	IO	pad								
AE22	VOUT0_DATA8 PADCONFIG: PADCONFIG54 0x000F40D8	VOUT0_DATA8	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A8	1	OZ									
		UART6_RXD	4	I	1								
		GPIO0_53	7	IO	pad								
AC22	VOUT0_DATA9 PADCONFIG: PADCONFIG55 0x000F40DC	VOUT0_DATA9	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A9	1	OZ									
		UART6_TXD	4	O									
		GPIO0_54	7	IO	pad								
W22	VOUT0_DATA10 PADCONFIG: PADCONFIG56 0x000F40E0	VOUT0_DATA10	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A10	1	OZ									
		UART6_RTSn	4	O									
		GPIO0_55	7	IO	pad								
AE21	VOUT0_DATA11 PADCONFIG: PADCONFIG57 0x000F40E4	VOUT0_DATA11	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A11	1	OZ									
		UART6_CTSn	4	I	1								
		GPIO0_56	7	IO	pad								
AD21	VOUT0_DATA12 PADCONFIG: PADCONFIG58 0x000F40E8	VOUT0_DATA12	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A12	1	OZ									
		UART5_RTSn	4	O									
		GPIO0_57	7	IO	pad								
AC21	VOUT0_DATA13 PADCONFIG: PADCONFIG59 0x000F40EC	VOUT0_DATA13	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A13	1	OZ									
		UART5_CTSn	4	I	1								
		GPIO0_58	7	IO	pad								
AA20	VOUT0_DATA14 PADCONFIG: PADCONFIG60 0x000F40F0	VOUT0_DATA14	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A14	1	OZ									
		UART4_RTSn	4	O									
		GPIO0_59	7	IO	pad								

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
Y20	VOUT0_DATA15 PADCONFIG: PADCONFIG61 0x000F40F4	VOUT0_DATA15	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		GPMC0_A15	1	OZ									
		UART4_CTSn	4	I	1								
		GPIO0_60	7	IO	pad								
F7	VPP	VPP		PWR									
1A3, 1A5, 1A7, 1B1, 1B8, 1C4, 1C6, 1D1, 1D5, 1D9, 1E4, 1E6, 1E8, 1F3, 1F7, 1F9, 1G1, 1G4, 1G6, 1G8, 1H2, 1H5, 1H9, 1J10, 1J3, 1J6, 1J8, 1K1, 1K9, A1, A12, A25, A6, A9, AA21, AA3, AB2, AC1, AD22, AD4, AE1, AE13, AE16, AE25, B3, C2, C20, D14, D3, E1, F3, G1, G4, H2, K1, L4, N1, P20, P4, U1, U4, V3, W2, Y1, Y4	VSS	VSS		PWR									
F13	WKUP_CLKOUT0 PADCONFIG: MCU_PADCONFIG33 0x04084084	WKUP_CLKOUT0	0	O		Off / Off / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_23	7	IO	pad								
A13	WKUP_I2C0_SCL PADCONFIG: MCU_PADCONFIG19 0x0408404C	WKUP_I2C0_SCL	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
		MCU_GPIO0_19	7	IOD	pad								
C11	WKUP_I2C0_SDA PADCONFIG: MCU_PADCONFIG20 0x04084050	WKUP_I2C0_SDA	0	IOD	1	Off / Off / NA	On / SS / NA	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
		MCU_GPIO0_20	7	IOD	pad								
A7	WKUP_LFOSC0_XI	WKUP_LFOSC0_XI		I					1.8 V	VDDS_OSC0		LFXOSC	
A8	WKUP_LFOSC0_XO	WKUP_LFOSC0_XO		O					1.8 V	VDDS_OSC0		LFXOSC	

ADVANCE INFORMATION

表 5-1. Pin Attributes (AMH Package) (続き)

BALL NUMBER [1]	BALL NAME [2] PADCONFIG Register [15] PADCONFIG Address [16]	SIGNAL NAME [3]	MUX MODE [4]	TYPE [5]	DSIS [6]	BALL STATE DURING RESET (RX/TX/PULL) [7]	BALL STATE AFTER RESET (RX/TX/PULL) [8]	MUX MODE AFTER RESET [9]	I/O OPERATING VOLTAGE [10]	POWER [11]	HYS [12]	BUFFER TYPE [13]	PULL UP/DOWN TYPE [14]
C7	WKUP_UART0_CTSn PADCONFIG: MCU_PADCONFIG11 0x0408402C	WKUP_UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		WKUP_TIMER_IO0	1	IO	0								
		MCU_SPI1_CS0	3	IO	1								
		MCU_GPIO0_11	7	IO	pad								
C6	WKUP_UART0_RTSn PADCONFIG: MCU_PADCONFIG12 0x04084030	WKUP_UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		WKUP_TIMER_IO1	1	IO	0								
		MCU_SPI1_CLK	3	IO	0								
		MCU_GPIO0_12	7	IO	pad								
D8	WKUP_UART0_RXD PADCONFIG: MCU_PADCONFIG9 0x04084024	WKUP_UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_SPI0_CS2	2	IO	1								
		MCU_GPIO0_9	7	IO	pad								
D7	WKUP_UART0_TXD PADCONFIG: MCU_PADCONFIG10 0x04084028	WKUP_UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_CANUART	Yes	LVCMOS	PU/PD
		MCU_SPI1_CS2	2	IO	1								
		MCU_GPIO0_10	7	IO	pad								

ADVANCE INFORMATION

5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

> 注
>
> Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via PADCONFIG registers. Device subsystems may provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Ball number(s) associated with signal

5.3.1 CPSW3G

5.3.1.1 MAIN Domain

表 5-2. CPSW3G0 RGMII1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
RGMII1_RXC	I	RGMII Receive Clock	A16
RGMII1_RX_CTL	I	RGMII Receive Control	A15
RGMII1_TXC	O	RGMII Transmit Clock	B17
RGMII1_TX_CTL	O	RGMII Transmit Control	B18
RGMII1_RD0	I	RGMII Receive Data 0	B15
RGMII1_RD1	I	RGMII Receive Data 1	B16
RGMII1_RD2	I	RGMII Receive Data 2	A14
RGMII1_RD3	I	RGMII Receive Data 3	B14
RGMII1_TD0	O	RGMII Transmit Data 0	A18
RGMII1_TD1	O	RGMII Transmit Data 1	C17
RGMII1_TD2	O	RGMII Transmit Data 2	A17
RGMII1_TD3	O	RGMII Transmit Data 3	C16

表 5-3. CPSW3G0 RGMII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
RGMII2_RXC	I	RGMII Receive Clock	D19
RGMII2_RX_CTL	I	RGMII Receive Control	F19
RGMII2_TXC	O	RGMII Transmit Clock	D16
RGMII2_TX_CTL	O	RGMII Transmit Control	A20
RGMII2_RD0	I	RGMII Receive Data 0	E19
RGMII2_RD1	I	RGMII Receive Data 1	E16
RGMII2_RD2	I	RGMII Receive Data 2	E17
RGMII2_RD3	I	RGMII Receive Data 3	C19
RGMII2_TD0	O	RGMII Transmit Data 0	B19
RGMII2_TD1	O	RGMII Transmit Data 1	A21
RGMII2_TD2	O	RGMII Transmit Data 2	D17
RGMII2_TD3	O	RGMII Transmit Data 3	A19

表 5-4. CPSW3G0 RMII1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
RMII1_CRS_DV	I	RMII Carrier Sense / Data Valid	B17
RMII1_REF_CLK	I	RMII Reference Clock	A16
RMII1_RX_ER	I	RMII Receive Data Error	A15
RMII1_TX_EN	O	RMII Transmit Enable	B18
RMII1_RXD0	I	RMII Receive Data 0	B15
RMII1_RXD1	I	RMII Receive Data 1	B16
RMII1_TXD0	O	RMII Transmit Data 0	A18
RMII1_TXD1	O	RMII Transmit Data 1	C17

表 5-5. CPSW3G0 RMII2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
RMII2_CRS_DV	I	RMII Carrier Sense / Data Valid	D16
RMII2_REF_CLK	I	RMII Reference Clock	D19
RMII2_RX_ER	I	RMII Receive Data Error	F19
RMII2_TX_EN	O	RMII Transmit Enable	A20
RMII2_RXD0	I	RMII Receive Data 0	E19
RMII2_RXD1	I	RMII Receive Data 1	E16
RMII2_TXD0	O	RMII Transmit Data 0	B19
RMII2_TXD1	O	RMII Transmit Data 1	A21

5.3.2 CPTS

注

Some CPTS signals are connected directly to CPTS modules within the device. Other CPTS signals are connected to the Time Sync Router and fanned out to peripherals linked to the router. Input signals are sent to the peripherals while output signals are sourced from the peripherals. For more information, see the Time Sync and Compare Events section in the Time Sync chapter in the device TRM.

ADVANCE INFORMATION

5.3.2.1 MAIN Domain

表 5-6. CPTS Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
CP_GEMAC_CPTS0_RFT_CLK	I	CPTS Reference Clock Input	C25
CP_GEMAC_CPTS0_TS_COMP	O	CPTS Time Stamp Counter Compare Output from CPSW3G0 CPTS	E20, H25
CP_GEMAC_CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit Output from CPSW3G0 CPTS	B21, H22
CP_GEMAC_CPTS0_HW1TSPUSH	I	CPTS Hardware Time Stamp Push Input to Time Sync Router	B20, H23
CP_GEMAC_CPTS0_HW2TSPUSH	I	CPTS Hardware Time Stamp Push Input to Time Sync Router	C21, H21
SYNC0_OUT	O	CPTS Time Stamp Generator Bit 0 Output from Time Sync Router	B25
SYNC1_OUT	O	CPTS Time Stamp Generator Bit 1 Output from Time Sync Router	C25
SYNC2_OUT	O	CPTS Time Stamp Generator Bit 2 Output from Time Sync Router	B23
SYNC3_OUT	O	CPTS Time Stamp Generator Bit 3 Output from Time Sync Router	F20

5.3.3 CSI-2

5.3.3.1 MAIN Domain

表 5-7. CSIRX0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
CSI0_RXCLKN	I	CSI Differential Receive Clock Input (negative)	AE12
CSI0_RXCLKP	I	CSI Differential Receive Clock Input (positive)	AE11
CSI0_RXRCALIB (1)	A	CSI pin connected to external resistor for on-chip resistor calibration	AA15
CSI0_RXN0	I	CSI Differential Receive Input (negative)	AB11
CSI0_RXN1	I	CSI Differential Receive Input (negative)	AC10
CSI0_RXN2	I	CSI Differential Receive Input (negative)	AA10
CSI0_RXN3	I	CSI Differential Receive Input (negative)	AD9
CSI0_RXP0	I	CSI Differential Receive Input (positive)	AB10
CSI0_RXP1	I	CSI Differential Receive Input (positive)	AC9
CSI0_RXP2	I	CSI Differential Receive Input (positive)	AA9
CSI0_RXP3	I	CSI Differential Receive Input (positive)	AD8

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.

5.3.4 DDRSS

5.3.4.1 MAIN Domain

表 5-8. DDRSS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
DDR0_ACT_n	O	DDRSS Activation Command	T6
DDR0_ALERT_n	IO	DDRSS Alert	K3
DDR0_CAS_n (1)	O	DDRSS Column Address Strobe / LPDDR4 Chip Select 1B	T5
DDR0_PAR	O	DDRSS Command and Address Parity	T1

ADVANCE INFORMATION

表 5-8. DDRSS0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
DDR0_RAS_n (1)	O	DDRSS Row Address Strobe / LPDDR4 Chip Select 0B	P6
DDR0_WE_n	O	DDRSS Write Enable	T4
DDR0_A0	O	DDRSS Address Bus	K5
DDR0_A1	O	DDRSS Address Bus	L2
DDR0_A2	O	DDRSS Address Bus	L3
DDR0_A3	O	DDRSS Address Bus	M2
DDR0_A4	O	DDRSS Address Bus	N2
DDR0_A5	O	DDRSS Address Bus	K2
DDR0_A6	O	DDRSS Address Bus	N3
DDR0_A7	O	DDRSS Address Bus	L1
DDR0_A8	O	DDRSS Address Bus	M1
DDR0_A9	O	DDRSS Address Bus	T2
DDR0_A10	O	DDRSS Address Bus	R2
DDR0_A11	O	DDRSS Address Bus	N5
DDR0_A12	O	DDRSS Address Bus	P3
DDR0_A13	O	DDRSS Address Bus	P2
DDR0_BA0	O	DDRSS Bank Address	N6
DDR0_BA1	O	DDRSS Bank Address	K4
DDR0_BG0	O	DDRSS Bank Group	Y6
DDR0_BG1	O	DDRSS Bank Group	U6
DDR0_CAL0 (2)	A	IO Pad Calibration Resistor	Y5
DDR0_CK0	O	DDRSS Clock	R1
DDR0_CK0_n	O	DDRSS Negative Clock	P1
DDR0_CKE0	O	DDRSS Clock Enable	N4
DDR0_CKE1	O	DDRSS Clock Enable	P5
DDR0_CS0_n (1)	O	DDRSS Chip Select 0 / LPDDR4 Chip Select 0A	L6
DDR0_CS1_n (1)	O	DDRSS Chip Select 1 / LPDDR4 Chip Select 1A	T3
DDR0_DM0	IO	DDRSS Data Mask	C3
DDR0_DM1	IO	DDRSS Data Mask	H3
DDR0_DM2	IO	DDRSS Data Mask	V4
DDR0_DM3	IO	DDRSS Data Mask	AD1
DDR0_DQ0	IO	DDRSS Data	B2
DDR0_DQ1	IO	DDRSS Data	A3
DDR0_DQ2	IO	DDRSS Data	A4
DDR0_DQ3	IO	DDRSS Data	A5
DDR0_DQ4	IO	DDRSS Data	A2
DDR0_DQ5	IO	DDRSS Data	B4
DDR0_DQ6	IO	DDRSS Data	D2
DDR0_DQ7	IO	DDRSS Data	C4
DDR0_DQ8	IO	DDRSS Data	E2
DDR0_DQ9	IO	DDRSS Data	F1
DDR0_DQ10	IO	DDRSS Data	G5
DDR0_DQ11	IO	DDRSS Data	F2
DDR0_DQ12	IO	DDRSS Data	G3

ADVANCE INFORMATION

表 5-8. DDRSS0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
DDR0_DQ13	IO	DDRSS Data	H4
DDR0_DQ14	IO	DDRSS Data	J2
DDR0_DQ15	IO	DDRSS Data	G2
DDR0_DQ16	IO	DDRSS Data	U2
DDR0_DQ17	IO	DDRSS Data	U3
DDR0_DQ18	IO	DDRSS Data	U5
DDR0_DQ19	IO	DDRSS Data	V5
DDR0_DQ20	IO	DDRSS Data	V2
DDR0_DQ21	IO	DDRSS Data	Y2
DDR0_DQ22	IO	DDRSS Data	Y3
DDR0_DQ23	IO	DDRSS Data	AA4
DDR0_DQ24	IO	DDRSS Data	AC2
DDR0_DQ25	IO	DDRSS Data	AA2
DDR0_DQ26	IO	DDRSS Data	AC4
DDR0_DQ27	IO	DDRSS Data	AD2
DDR0_DQ28	IO	DDRSS Data	AD3
DDR0_DQ29	IO	DDRSS Data	AC3
DDR0_DQ30	IO	DDRSS Data	AE4
DDR0_DQ31	IO	DDRSS Data	AE3
DDR0_DQS0	IO	DDRSS Data Strobe	D1
DDR0_DQS0_n	IO	DDRSS Complimentary Data Strobe	C1
DDR0_DQS1	IO	DDRSS Data Strobe	J1
DDR0_DQS1_n	IO	DDRSS Complimentary Data Strobe	H1
DDR0_DQS2	IO	DDRSS Data Strobe	W1
DDR0_DQS2_n	IO	DDRSS Complimentary Data Strobe	V1
DDR0_DQS3	IO	DDRSS Data Strobe	AA1
DDR0_DQS3_n	IO	DDRSS Complimentary Data Strobe	AB1
DDR0_ODT0	O	DDRSS On-Die Termination for Chip Select 0	L5
DDR0_ODT1	O	DDRSS On-Die Termination for Chip Select 1	V6
DDR0_RESET0_n	O	DDRSS Reset	AA5

(1) DDRSS implements different signal functions on Column Address Strobe, Row Address Strobe, Chip Select 0, and Chip Select 1 when configured to operate with LPDDR4 memory devices. These signals function as Chip Select 1B, Chip Select 0B, Chip Select 0A, and Chip Select 1A respectively when DDRSS is configured to operate with LPDDR4 memory devices. For more information, refer to セクション 8.2.1, *DDR Board Design and Layout Guidelines*.
(2) An external 240 Ω ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

5.3.5 DSI

5.3.5.1 MAIN Domain

表 5-9. DSITX0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
DSI0_TXCLKN	IO	DSI Differential Transmit Clock Output (negative)	AA12
DSI0_TXCLKP	IO	DSI Differential Transmit Clock Output (positive)	AA13
DSI0_TXRCALIB (1)	A	DSI pin connected to external resistor for on-chip resistor calibration	Y16
DSI0_TXN0	IO	DSI Differential Transmit Output (negative)	AD11
DSI0_TXN1	IO	DSI Differential Transmit Output (negative)	AB13

表 5-9. DSITX0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
DSI0_TXN2	IO	DSI Differential Transmit Output (negative)	AC12
DSI0_TXN3	IO	DSI Differential Transmit Output (negative)	AE14
DSI0_TXP0	IO	DSI Differential Transmit Output (positive)	AD12
DSI0_TXP1	IO	DSI Differential Transmit Output (positive)	AB14
DSI0_TXP2	IO	DSI Differential Transmit Output (positive)	AC13
DSI0_TXP3	IO	DSI Differential Transmit Output (positive)	AE15

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.

5.3.6 DSS

5.3.6.1 MAIN Domain

表 5-10. DSS0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
VOUT0_DE	O	Video Output Data Enable	W21
VOUT0_EXTPCLKIN	I	Video Output External Pixel Clock Input	AD24
VOUT0_HSYNC	O	Video Output Horizontal Sync	AC20
VOUT0_PCLK	O	Video Output Pixel Clock Output	Y21
VOUT0_VSYNC	O	Video Output Vertical Sync	W20
VOUT0_DATA0	O	Video Output Data 0	AE24
VOUT0_DATA1	O	Video Output Data 1	W23
VOUT0_DATA2	O	Video Output Data 2	AA23
VOUT0_DATA3	O	Video Output Data 3	Y23
VOUT0_DATA4	O	Video Output Data 4	AB23
VOUT0_DATA5	O	Video Output Data 5	AD23
VOUT0_DATA6	O	Video Output Data 6	AC23
VOUT0_DATA7	O	Video Output Data 7	AE23
VOUT0_DATA8	O	Video Output Data 8	AE22
VOUT0_DATA9	O	Video Output Data 9	AC22
VOUT0_DATA10	O	Video Output Data 10	W22
VOUT0_DATA11	O	Video Output Data 11	AE21
VOUT0_DATA12	O	Video Output Data 12	AD21
VOUT0_DATA13	O	Video Output Data 13	AC21
VOUT0_DATA14	O	Video Output Data 14	AA20
VOUT0_DATA15	O	Video Output Data 15	Y20
VOUT0_DATA16	O	Video Output Data 16	AC25
VOUT0_DATA17	O	Video Output Data 17	AB25
VOUT0_DATA18	O	Video Output Data 18	AA25
VOUT0_DATA19	O	Video Output Data 19	W24
VOUT0_DATA20	O	Video Output Data 20	Y24
VOUT0_DATA21	O	Video Output Data 21	AD25
VOUT0_DATA22	O	Video Output Data 22	AB24
VOUT0_DATA23	O	Video Output Data 23	AC24

ADVANCE INFORMATION

5.3.7 ECAP

5.3.7.1 MAIN Domain

表 5-11. ECAP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
ECAP0_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	C25, E20

表 5-12. ECAP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
ECAP1_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	A22, B25, D25, E24, H23

表 5-13. ECAP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
ECAP2_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	A24, B22, E25, F24, H21

5.3.8 Emulation and Debug

5.3.8.1 MAIN Domain

表 5-14. Trace Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
TRC_CLK	O	Trace Clock	U22
TRC_CTL	O	Trace Control	U21
TRC_DATA0	O	Trace Data 0	U20
TRC_DATA1	O	Trace Data 1	V25
TRC_DATA2	O	Trace Data 2	T20
TRC_DATA3	O	Trace Data 3	T21
TRC_DATA4	O	Trace Data 4	V24
TRC_DATA5	O	Trace Data 5	W25
TRC_DATA6	O	Trace Data 6	Y25
TRC_DATA7	O	Trace Data 7	R25
TRC_DATA8	O	Trace Data 8	R24
TRC_DATA9	O	Trace Data 9	T25
TRC_DATA10	O	Trace Data 10	U24
TRC_DATA11	O	Trace Data 11	T24
TRC_DATA12	O	Trace Data 12	AA24
TRC_DATA13	O	Trace Data 13	P24
TRC_DATA14	O	Trace Data 14	P25
TRC_DATA15	O	Trace Data 15	T23
TRC_DATA16	O	Trace Data 16	U23
TRC_DATA17	O	Trace Data 17	T22
TRC_DATA18	O	Trace Data 18	U25
TRC_DATA19	O	Trace Data 19	AC24
TRC_DATA20	O	Trace Data 20	AB24
TRC_DATA21	O	Trace Data 21	AD25
TRC_DATA22	O	Trace Data 22	Y24

表 5-14. Trace Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
TRC_DATA23	O	Trace Data 23	W24

5.3.8.2 MCU Domain

表 5-15. JTAG Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
EMU0	IO	Emulation Control 0	B12
EMU1	IO	Emulation Control 1	D13
TCK	I	JTAG Test Clock Input	C13
TDI	I	JTAG Test Data Input	E13
TDO	OZ	JTAG Test Data Output	C14
TMS	I	JTAG Test Mode Select Input	E14
TRSTn	I	JTAG Reset	B13

5.3.9 EPWM

5.3.9.1 MAIN Domain

表 5-16. EPWM Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
EHRPWM_SOCA	O	EHRPWM Start of Conversion A	B25
EHRPWM_SOCB	O	EHRPWM Start of Conversion B	A24
EHRPWM_TZn_IN0	I	EHRPWM Trip Zone Input 0 (active low)	C21, K24
EHRPWM_TZn_IN1	I	EHRPWM Trip Zone Input 1 (active low)	J25
EHRPWM_TZn_IN2	I	EHRPWM Trip Zone Input 2 (active low)	K25
EHRPWM_TZn_IN3	I	EHRPWM Trip Zone Input 3 (active low)	B23
EHRPWM_TZn_IN4	I	EHRPWM Trip Zone Input 4 (active low)	F20
EHRPWM_TZn_IN5	I	EHRPWM Trip Zone Input 5 (active low)	E20

表 5-17. EPWM0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
EHRPWM0_A	IO	EHRPWM Output A	D20, G23, L21
EHRPWM0_B	IO	EHRPWM Output B	E20, G20, L20
EHRPWM0_SYNCI	I	Sync Input to EHRPWM module from an external pin	C24, K21
EHRPWM0_SYNCO	O	Sync Input to EHRPWM module from an external pin	B24, K24

表 5-18. EPWM1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
EHRPWM1_A	IO	EHRPWM Output A	B21, E24, K22
EHRPWM1_B	IO	EHRPWM Output B	B20, F23, K23

表 5-19. EPWM2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
EHRPWM2_A	IO	EHRPWM Output A	A22, C24, J25
EHRPWM2_B	IO	EHRPWM Output B	B22, B24, K25

ADVANCE INFORMATION

5.3.10 EQEP

5.3.10.1 MAIN Domain

表 5-20. EQEP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
EQEP0_A (1)	I	EQEP Quadrature Input A	D25
EQEP0_B (1)	I	EQEP Quadrature Input B	E25
EQEP0_I (1)	IO	EQEP Index	F23
EQEP0_S (1)	IO	EQEP Strobe	E24

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

表 5-21. EQEP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
EQEP1_A (1)	I	EQEP Quadrature Input A	F24
EQEP1_B (1)	I	EQEP Quadrature Input B	F25
EQEP1_I (1)	IO	EQEP Index	G20
EQEP1_S (1)	IO	EQEP Strobe	G23

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

表 5-22. EQEP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
EQEP2_A (1)	I	EQEP Quadrature Input A	AC23, B25, E17
EQEP2_B (1)	I	EQEP Quadrature Input B	A24, AE23, C19
EQEP2_I (1)	IO	EQEP Index	AB23, AD24, B23, D17
EQEP2_S (1)	IO	EQEP Strobe	A19, AD23, F20, P25

(1) This EQEP input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

5.3.11 GPIO

5.3.11.1 MAIN Domain

表 5-23. GPIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
GPIO0_0	IO	General Purpose Input/Output	P23
GPIO0_1	IO	General Purpose Input/Output	N23
GPIO0_2	IO	General Purpose Input/Output	P22
GPIO0_3	IO	General Purpose Input/Output	L25
GPIO0_4	IO	General Purpose Input/Output	N24
GPIO0_5	IO	General Purpose Input/Output	N25
GPIO0_6	IO	General Purpose Input/Output	M24
GPIO0_7	IO	General Purpose Input/Output	N21
GPIO0_8	IO	General Purpose Input/Output	N22
GPIO0_9	IO	General Purpose Input/Output	P21
GPIO0_10	IO	General Purpose Input/Output	N20
GPIO0_11	IO	General Purpose Input/Output	M25
GPIO0_12	IO	General Purpose Input/Output	L24

表 5-23. GPIO0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
GPIO0_13 (1)	IO	General Purpose Input/Output	L22
GPIO0_14 (1)	IO	General Purpose Input/Output	L23
GPIO0_15	IO	General Purpose Input/Output	U22
GPIO0_16	IO	General Purpose Input/Output	U21
GPIO0_17	IO	General Purpose Input/Output	U20
GPIO0_18	IO	General Purpose Input/Output	V25
GPIO0_19	IO	General Purpose Input/Output	T20
GPIO0_20	IO	General Purpose Input/Output	T21
GPIO0_21	IO	General Purpose Input/Output	V24
GPIO0_22	IO	General Purpose Input/Output	W25
GPIO0_23	IO	General Purpose Input/Output	AC25
GPIO0_24	IO	General Purpose Input/Output	AB25
GPIO0_25	IO	General Purpose Input/Output	AA25
GPIO0_26	IO	General Purpose Input/Output	W24
GPIO0_27	IO	General Purpose Input/Output	Y24
GPIO0_28	IO	General Purpose Input/Output	AD25
GPIO0_29	IO	General Purpose Input/Output	AB24
GPIO0_30	IO	General Purpose Input/Output	AC24
GPIO0_31	IO	General Purpose Input/Output	Y25
GPIO0_32	IO	General Purpose Input/Output	R25
GPIO0_33	IO	General Purpose Input/Output	R24
GPIO0_34	IO	General Purpose Input/Output	T25
GPIO0_35	IO	General Purpose Input/Output	U24
GPIO0_36	IO	General Purpose Input/Output	T24
GPIO0_37	IO	General Purpose Input/Output	AA24
GPIO0_38	IO	General Purpose Input/Output	AD24
GPIO0_39	IO	General Purpose Input/Output	P24
GPIO0_40	IO	General Purpose Input/Output	P25
GPIO0_41	IO	General Purpose Input/Output	T23
GPIO0_42	IO	General Purpose Input/Output	U23
GPIO0_43 (1)	IO	General Purpose Input/Output	T22
GPIO0_44 (1)	IO	General Purpose Input/Output	U25
GPIO0_45	IO	General Purpose Input/Output	AE24
GPIO0_46	IO	General Purpose Input/Output	W23
GPIO0_47	IO	General Purpose Input/Output	AA23
GPIO0_48	IO	General Purpose Input/Output	Y23
GPIO0_49	IO	General Purpose Input/Output	AB23
GPIO0_50	IO	General Purpose Input/Output	AD23
GPIO0_51	IO	General Purpose Input/Output	AC23
GPIO0_52	IO	General Purpose Input/Output	AE23
GPIO0_53	IO	General Purpose Input/Output	AE22
GPIO0_54	IO	General Purpose Input/Output	AC22
GPIO0_55	IO	General Purpose Input/Output	W22
GPIO0_56	IO	General Purpose Input/Output	AE21
GPIO0_57	IO	General Purpose Input/Output	AD21

ADVANCE INFORMATION

表 5-23. GPIO0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
GPIO0_58	IO	General Purpose Input/Output	AC21
GPIO0_59	IO	General Purpose Input/Output	AA20
GPIO0_60	IO	General Purpose Input/Output	Y20
GPIO0_61	IO	General Purpose Input/Output	AC20
GPIO0_62	IO	General Purpose Input/Output	W21
GPIO0_63	IO	General Purpose Input/Output	W20
GPIO0_64	IO	General Purpose Input/Output	Y21
GPIO0_65 (1)	IO	General Purpose Input/Output	L21
GPIO0_66 (1)	IO	General Purpose Input/Output	L20
GPIO0_67 (1)	IO	General Purpose Input/Output	K22
GPIO0_68 (1)	IO	General Purpose Input/Output	K23
GPIO0_69 (1)	IO	General Purpose Input/Output	K21
GPIO0_70 (1)	IO	General Purpose Input/Output	K24
GPIO0_71 (1)	IO	General Purpose Input/Output	J25
GPIO0_72 (1)	IO	General Purpose Input/Output	K25
GPIO0_73	IO	General Purpose Input/Output	B18
GPIO0_74	IO	General Purpose Input/Output	B17
GPIO0_75	IO	General Purpose Input/Output	A18
GPIO0_76	IO	General Purpose Input/Output	C17
GPIO0_77	IO	General Purpose Input/Output	A17
GPIO0_78	IO	General Purpose Input/Output	C16
GPIO0_79	IO	General Purpose Input/Output	A15
GPIO0_80	IO	General Purpose Input/Output	A16
GPIO0_81	IO	General Purpose Input/Output	B15
GPIO0_82	IO	General Purpose Input/Output	B16
GPIO0_83	IO	General Purpose Input/Output	A14
GPIO0_84	IO	General Purpose Input/Output	B14
GPIO0_85	IO	General Purpose Input/Output	F16
GPIO0_86	IO	General Purpose Input/Output	F17
GPIO0_87	IO	General Purpose Input/Output	A20
GPIO0_88	IO	General Purpose Input/Output	D16
GPIO0_89	IO	General Purpose Input/Output	B19
GPIO0_90	IO	General Purpose Input/Output	A21
GPIO0_91	IO	General Purpose Input/Output	D17

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

表 5-24. GPIO1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
GPIO1_0	IO	General Purpose Input/Output	A19
GPIO1_1	IO	General Purpose Input/Output	F19
GPIO1_2	IO	General Purpose Input/Output	D19
GPIO1_3	IO	General Purpose Input/Output	E19
GPIO1_4	IO	General Purpose Input/Output	E16
GPIO1_5	IO	General Purpose Input/Output	E17

表 5-24. GPIO1 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
GPIO1_6	IO	General Purpose Input/Output	C19
GPIO1_7	IO	General Purpose Input/Output	D25
GPIO1_8	IO	General Purpose Input/Output	E25
GPIO1_9	IO	General Purpose Input/Output	E24
GPIO1_10	IO	General Purpose Input/Output	F23
GPIO1_11	IO	General Purpose Input/Output	F24
GPIO1_12	IO	General Purpose Input/Output	F25
GPIO1_13	IO	General Purpose Input/Output	G23
GPIO1_14	IO	General Purpose Input/Output	G20
GPIO1_15	IO	General Purpose Input/Output	D20
GPIO1_16 (1)	IO	General Purpose Input/Output	E20
GPIO1_17	IO	General Purpose Input/Output	B21
GPIO1_18	IO	General Purpose Input/Output	B20
GPIO1_19	IO	General Purpose Input/Output	C21
GPIO1_20	IO	General Purpose Input/Output	A22
GPIO1_21	IO	General Purpose Input/Output	B22
GPIO1_22	IO	General Purpose Input/Output	A23
GPIO1_23	IO	General Purpose Input/Output	C22
GPIO1_24	IO	General Purpose Input/Output	B23
GPIO1_25	IO	General Purpose Input/Output	F20
GPIO1_26	IO	General Purpose Input/Output	B25
GPIO1_27	IO	General Purpose Input/Output	A24
GPIO1_28	IO	General Purpose Input/Output	C24
GPIO1_29	IO	General Purpose Input/Output	B24
GPIO1_30	IO	General Purpose Input/Output	C25
GPIO1_31 (1)	IOD	General Purpose Input/Output	C23
GPIO1_42 (1)	IO	General Purpose Input/Output	H25
GPIO1_43 (1)	IO	General Purpose Input/Output	H22
GPIO1_44 (1)	IO	General Purpose Input/Output	H23
GPIO1_45 (1)	IO	General Purpose Input/Output	H21
GPIO1_46 (1)	IO	General Purpose Input/Output	J24
GPIO1_47 (1)	IO	General Purpose Input/Output	H20
GPIO1_48 (1)	IO	General Purpose Input/Output	D23
GPIO1_49 (1)	IO	General Purpose Input/Output	D24
GPIO1_50	IO	General Purpose Input/Output	G22
GPIO1_51	IO	General Purpose Input/Output	G21

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

5.3.11.2 MCU Domain

表 5-25. MCU_GPIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_GPIO0_0 (1)	IO	General Purpose Input/Output	B10
MCU_GPIO0_1 (1)	IO	General Purpose Input/Output	E10
MCU_GPIO0_2	IO	General Purpose Input/Output	C10

ADVANCE INFORMATION

表 5-25. MCU_GPIO0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_GPIO0_3	IO	General Purpose Input/Output	B11
MCU_GPIO0_4	IO	General Purpose Input/Output	D10
MCU_GPIO0_5	IO	General Purpose Input/Output	B6
MCU_GPIO0_6	IO	General Purpose Input/Output	C8
MCU_GPIO0_7 (1)	IO	General Purpose Input/Output	B8
MCU_GPIO0_8 (1)	IO	General Purpose Input/Output	B7
MCU_GPIO0_9	IO	General Purpose Input/Output	D8
MCU_GPIO0_10	IO	General Purpose Input/Output	D7
MCU_GPIO0_11 (1)	IO	General Purpose Input/Output	C7
MCU_GPIO0_12 (1)	IO	General Purpose Input/Output	C6
MCU_GPIO0_13	IO	General Purpose Input/Output	E8
MCU_GPIO0_14	IO	General Purpose Input/Output	D6
MCU_GPIO0_15 (1)	IO	General Purpose Input/Output	F8
MCU_GPIO0_16 (1)	IO	General Purpose Input/Output	E7
MCU_GPIO0_17	IOD	General Purpose Input/Output	E11
MCU_GPIO0_18	IOD	General Purpose Input/Output	D11
MCU_GPIO0_19	IOD	General Purpose Input/Output	A13
MCU_GPIO0_20	IOD	General Purpose Input/Output	C11
MCU_GPIO0_21	IO	General Purpose Input/Output	F14
MCU_GPIO0_22	IO	General Purpose Input/Output	B9
MCU_GPIO0_23	IO	General Purpose Input/Output	F13

(1) This GPIO input signal has a debounce function. For more information on I/O Debounce configuration, see the TRM *Device Configuration* chapter.

5.3.12 GPMC

5.3.12.1 MAIN Domain

表 5-26. GPMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
GPMC0_ADVn_ALE	O	GPMC Address Valid (active low) or Address Latch Enable	R25
GPMC0_CLK	O	GPMC clock	Y25
GPMC0_DIR	O	GPMC Data Bus Signal Direction Control	P25
GPMC0_FCLK_MUX	O	GPMC functional clock output	Y25
GPMC0_OEn_REn	O	GPMC Output Enable (active low) or Read Enable (active low)	R24
GPMC0_WEn	O	GPMC Write Enable (active low)	T25
GPMC0_WPn	O	GPMC Flash Write Protect (active low)	P24
GPMC0_A0	OZ	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories	AE24
GPMC0_A1	OZ	GPMC address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode	W23
GPMC0_A2	OZ	GPMC address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode	AA23
GPMC0_A3	OZ	GPMC address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode	Y23
GPMC0_A4	OZ	GPMC address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode	AB23

表 5-26. GPMC0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
GPMC0_A5	OZ	GPMC address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode	AD23
GPMC0_A6	OZ	GPMC address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode	AC23
GPMC0_A7	OZ	GPMC address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode	AE23
GPMC0_A8	OZ	GPMC address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode	AE22
GPMC0_A9	OZ	GPMC address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode	AC22
GPMC0_A10	OZ	GPMC address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode	W22
GPMC0_A11	OZ	GPMC address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AE21
GPMC0_A12	OZ	GPMC address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AD21
GPMC0_A13	OZ	GPMC address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AC21
GPMC0_A14	OZ	GPMC address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA20
GPMC0_A15	OZ	GPMC address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	Y20
GPMC0_A16	OZ	GPMC address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AC20
GPMC0_A17	OZ	GPMC address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	W21
GPMC0_A18	OZ	GPMC address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	W20
GPMC0_A19	OZ	GPMC address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	Y21
GPMC0_A20	OZ	GPMC address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	U25
GPMC0_A21	OZ	GPMC address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AD24
GPMC0_A22	OZ	GPMC address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	P24
GPMC0_AD0	IO	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode	U22
GPMC0_AD1	IO	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode	U21
GPMC0_AD2	IO	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	U20
GPMC0_AD3	IO	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	V25
GPMC0_AD4	IO	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	T20
GPMC0_AD5	IO	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	T21

ADVANCE INFORMATION

表 5-26. GPMC0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
GPMC0_AD6	IO	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	V24
GPMC0_AD7	IO	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	W25
GPMC0_AD8	IO	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	AC25
GPMC0_AD9	IO	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	AB25
GPMC0_AD10	IO	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode	AA25
GPMC0_AD11	IO	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode	W24
GPMC0_AD12	IO	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode	Y24
GPMC0_AD13	IO	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode	AD25
GPMC0_AD14	IO	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode	AB24
GPMC0_AD15	IO	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode	AC24
GPMC0_BE0n_CLE	O	GPMC Lower-Byte Enable (active low) or Command Latch Enable	U24
GPMC0_BE1n	O	GPMC Upper-Byte Enable (active low)	T24
GPMC0_CSn0	O	GPMC Chip Select 0 (active low)	T23
GPMC0_CSn1	O	GPMC Chip Select 1 (active low)	U23
GPMC0_CSn2	O	GPMC Chip Select 2 (active low)	T22
GPMC0_CSn3	O	GPMC Chip Select 3 (active low)	U25
GPMC0_WAIT0	I	GPMC External Indication of Wait	AA24
GPMC0_WAIT1	I	GPMC External Indication of Wait	AD24

5.3.13 I2C

5.3.13.1 MAIN Domain

表 5-27. I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
I2C0_SCL	IOD	I2C Clock	B25
I2C0_SDA	IOD	I2C Data	A24

表 5-28. I2C1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
I2C1_SCL	IOD	I2C Clock	C24

表 5-28. I2C1 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
I2C1_SDA	IOD	I2C Data	B24

表 5-29. I2C2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
I2C2_SCL	IOD	I2C Clock	K23, T22
I2C2_SDA	IOD	I2C Data	K22, L20, U25

表 5-30. I2C3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
I2C3_SCL	IOD	I2C Clock	A23, K21
I2C3_SDA	IOD	I2C Data	C22, K24

5.3.13.2 MCU Domain

表 5-31. MCU_I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_I2C0_SCL	IOD	I2C Clock	E11
MCU_I2C0_SDA	IOD	I2C Data	D11

5.3.13.3 WKUP Domain

表 5-32. WKUP_I2C0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
WKUP_I2C0_SCL	IOD	I2C Clock	A13
WKUP_I2C0_SDA	IOD	I2C Data	C11

5.3.14 MCAN

5.3.14.1 MAIN Domain

表 5-33. MCAN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCAN0_RX	I	MCAN Receive Data	F20
MCAN0_TX	O	MCAN Transmit Data	B23

表 5-34. MCAN1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCAN1_RX	I	MCAN Receive Data	D24, H22, U25
MCAN1_TX	O	MCAN Transmit Data	D23, H25, T22

5.3.14.2 MCU Domain

表 5-35. MCU_MCAN0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_MCAN0_RX	I	MCAN Receive Data	D6
MCU_MCAN0_TX	O	MCAN Transmit Data	E8

ADVANCE INFORMATION

表 5-36. MCU_MCAN1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_MCAN1_RX	I	MCAN Receive Data	E7
MCU_MCAN1_TX	O	MCAN Transmit Data	F8

5.3.15 MCASP

5.3.15.1 MAIN Domain

表 5-37. MCASP0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCASP0_ACLKR	IO	MCASP Receive Bit Clock	G20
MCASP0_ACLKX	IO	MCASP Transmit Bit Clock	F24
MCASP0_AFSR	IO	MCASP Receive Frame Sync	G23
MCASP0_AFSX	IO	MCASP Transmit Frame Sync	F25
MCASP0_AXR0	IO	MCASP Serial Data (Input/Output)	F23
MCASP0_AXR1	IO	MCASP Serial Data (Input/Output)	E24
MCASP0_AXR2	IO	MCASP Serial Data (Input/Output)	E25
MCASP0_AXR3	IO	MCASP Serial Data (Input/Output)	D25

表 5-38. MCASP1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCASP1_ACLKR	IO	MCASP Receive Bit Clock	K21, L23, U25
MCASP1_ACLKX	IO	MCASP Transmit Bit Clock	J25, P21, U24
MCASP1_AFSR	IO	MCASP Receive Frame Sync	K24, L22, T22
MCASP1_AFSX	IO	MCASP Transmit Frame Sync	AA24, K25, N20
MCASP1_AXR0	IO	MCASP Serial Data (Input/Output)	K23, N22, T25
MCASP1_AXR1	IO	MCASP Serial Data (Input/Output)	K22, N21, R24
MCASP1_AXR2	IO	MCASP Serial Data (Input/Output)	L20, L22, R25
MCASP1_AXR3	IO	MCASP Serial Data (Input/Output)	L21, L23, Y25
MCASP1_AXR4	IO	MCASP Serial Data (Input/Output)	K24, T22
MCASP1_AXR5	IO	MCASP Serial Data (Input/Output)	K21, U25

表 5-39. MCASP2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCASP2_ACLKR	IO	MCASP Receive Bit Clock	A21, AC24
MCASP2_ACLKX	IO	MCASP Transmit Bit Clock	A19, AD25, C22
MCASP2_AFSR	IO	MCASP Receive Frame Sync	AB24, E16
MCASP2_AFSX	IO	MCASP Transmit Frame Sync	A23, D17, Y24
MCASP2_AXR0	IO	MCASP Serial Data (Input/Output)	AC25, B23, E17
MCASP2_AXR1	IO	MCASP Serial Data (Input/Output)	AB25, D19, F20
MCASP2_AXR2	IO	MCASP Serial Data (Input/Output)	AA25, E19
MCASP2_AXR3	IO	MCASP Serial Data (Input/Output)	F19, W24
MCASP2_AXR4	IO	MCASP Serial Data (Input/Output)	A20, AB24, U22
MCASP2_AXR5	IO	MCASP Serial Data (Input/Output)	AC24, D16, U21
MCASP2_AXR6	IO	MCASP Serial Data (Input/Output)	B19, U20
MCASP2_AXR7	IO	MCASP Serial Data (Input/Output)	E16, V25
MCASP2_AXR8	IO	MCASP Serial Data (Input/Output)	A21, T20

表 5-39. MCASP2 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCASP2_AXR9	IO	MCASP Serial Data (Input/Output)	T21
MCASP2_AXR10	IO	MCASP Serial Data (Input/Output)	V24
MCASP2_AXR11	IO	MCASP Serial Data (Input/Output)	W25
MCASP2_AXR12	IO	MCASP Serial Data (Input/Output)	T24
MCASP2_AXR13	IO	MCASP Serial Data (Input/Output)	P25
MCASP2_AXR14	IO	MCASP Serial Data (Input/Output)	T23
MCASP2_AXR15	IO	MCASP Serial Data (Input/Output)	U23

5.3.16 MCSPI

5.3.16.1 MAIN Domain

表 5-40. MCSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
SPI0_CLK	IO	SPI Clock	B21
SPI0_CS0	IO	SPI Chip Select 0	D20
SPI0_CS1	IO	SPI Chip Select 1	E20
SPI0_CS2	IO	SPI Chip Select 2	A23
SPI0_CS3	IO	SPI Chip Select 3	C22
SPI0_D0	IO	SPI Data 0	B20
SPI0_D1	IO	SPI Data 1	C21

表 5-41. MCSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
SPI1_CLK	IO	SPI Clock	H20, N22
SPI1_CS0	IO	SPI Chip Select 0	J24, N21
SPI1_CS1	IO	SPI Chip Select 1	D24, L22
SPI1_CS2	IO	SPI Chip Select 2	H23
SPI1_CS3	IO	SPI Chip Select 3	D23
SPI1_D0	IO	SPI Data 0	H25, P21
SPI1_D1	IO	SPI Data 1	H22, N20

表 5-42. MCSPI2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
SPI2_CLK	IO	SPI Clock	B24, D23, G20
SPI2_CS0	IO	SPI Chip Select 0	B25, G23, H20
SPI2_CS1	IO	SPI Chip Select 1	C24, F24, H25
SPI2_CS2	IO	SPI Chip Select 2	A24, E24, J24
SPI2_CS3	IO	SPI Chip Select 3	C25, F25, H22
SPI2_D0	IO	SPI Data 0	A22, D25, H23
SPI2_D1	IO	SPI Data 1	B22, E25, H21

5.3.16.2 MCU Domain

表 5-43. MCU_MCSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_SPI0_CLK	IO	SPI Clock	C10

ADVANCE INFORMATION

表 5-43. MCU_MCSPI0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_SPI0_CS0	IO	SPI Chip Select 0	B10
MCU_SPI0_CS1	IO	SPI Chip Select 1	E10
MCU_SPI0_CS2	IO	SPI Chip Select 2	D8, E7
MCU_SPI0_CS3	IO	SPI Chip Select 3	E8
MCU_SPI0_D0	IO	SPI Data 0	B11
MCU_SPI0_D1	IO	SPI Data 1	D10

表 5-44. MCU_MCSPI1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_SPI1_CLK	IO	SPI Clock	C6, E7
MCU_SPI1_CS0	IO	SPI Chip Select 0	C7
MCU_SPI1_CS1	IO	SPI Chip Select 2	F8
MCU_SPI1_CS2	IO	SPI Chip Select 2	D7, E7
MCU_SPI1_CS3	IO	SPI Chip Select 3	D6
MCU_SPI1_D0	IO	SPI Data 0	B8
MCU_SPI1_D1	IO	SPI Data 1	B7

5.3.17 MDIO

5.3.17.1 MAIN Domain

表 5-45. MDIO0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MDIO0_MDC	O	MDIO Clock	F17
MDIO0_MDIO	IO	MDIO Data	F16

5.3.18 MMC

5.3.18.1 MAIN Domain

表 5-46. MMC0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MMC0_CALPAD (1)	A	MMC/SD/SDIO Calibration Resistor	AC5
MMC0_CLK	O	MMC/SD/SDIO Clock	AA6
MMC0_CMD	IO	MMC/SD/SDIO Command	AB8
MMC0_DS	I	MMC Data Strobe	AD5
MMC0_DAT0	IO	MMC/SD/SDIO Data	AC7
MMC0_DAT1	IO	MMC/SD/SDIO Data	AB7
MMC0_DAT2	IO	MMC/SD/SDIO Data	AD6
MMC0_DAT3	IO	MMC/SD/SDIO Data	AE5
MMC0_DAT4	IO	MMC/SD/SDIO Data	AE6
MMC0_DAT5	IO	MMC/SD/SDIO Data	AC6
MMC0_DAT6	IO	MMC/SD/SDIO Data	AA7
MMC0_DAT7	IO	MMC/SD/SDIO Data	AB6

(1) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

表 5-47. MMC1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MMC1_CLK	O	MMC/SD/SDIO Clock	J24

ADVANCE INFORMATION

表 5-47. MMC1 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MMC1_CMD	IO	MMC/SD/SDIO Command	H20
MMC1_SDCD	I	SD Card Detect	D23
MMC1_SDWP	I	SD Write Protect	D24
MMC1_DAT0	IO	MMC/SD/SDIO Data	H21
MMC1_DAT1	IO	MMC/SD/SDIO Data	H23
MMC1_DAT2	IO	MMC/SD/SDIO Data	H22
MMC1_DAT3	IO	MMC/SD/SDIO Data	H25

表 5-48. MMC2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MMC2_CLK (1)	O	MMC/SD/SDIO Clock	K21
MMC2_CMD	IO	MMC/SD/SDIO Command	K24
MMC2_SDCD	I	SD Card Detect	A23, C24, J25
MMC2_SDWP	I	SD Write Protect	B24, C22, K25
MMC2_DAT0	IO	MMC/SD/SDIO Data	K23
MMC2_DAT1	IO	MMC/SD/SDIO Data	K22
MMC2_DAT2	IO	MMC/SD/SDIO Data	L20
MMC2_DAT3	IO	MMC/SD/SDIO Data	L21

(1) For MMC2 to work properly, the CTRLMMR_PADCONFIG71 register must be configured to set (1) the RXACTIVE bit and reset (0) the TX_DIS bit.

5.3.19 OLDI

5.3.19.1 MAIN Domain

表 5-49. OLDI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
OLDI0_A0N	IO	OLDI Differential Data (negative)	AE20
OLDI0_A0P	IO	OLDI Differential Data (positive)	AD20
OLDI0_A1N	IO	OLDI Differential Data (negative)	AC19
OLDI0_A1P	IO	OLDI Differential Data (positive)	AD19
OLDI0_A2N	IO	OLDI Differential Data (negative)	AA19
OLDI0_A2P	IO	OLDI Differential Data (positive)	AB19
OLDI0_A3N	IO	OLDI Differential Data (negative)	AD18
OLDI0_A3P	IO	OLDI Differential Data (positive)	AE19
OLDI0_A4N	IO	OLDI Differential Data (negative)	AD17
OLDI0_A4P	IO	OLDI Differential Data (positive)	AD16
OLDI0_A5N	IO	OLDI Differential Data (negative)	AB17
OLDI0_A5P	IO	OLDI Differential Data (positive)	AC17
OLDI0_A6N	IO	OLDI Differential Data (negative)	AC16
OLDI0_A6P	IO	OLDI Differential Data (positive)	AC15
OLDI0_A7N	IO	OLDI Differential Data (negative)	AB16
OLDI0_A7P	IO	OLDI Differential Data (positive)	AA16
OLDI0_CLK0N	IO	OLDI Differential Clock (negative)	AE18
OLDI0_CLK0P	IO	OLDI Differential Clock (positive)	AE17
OLDI0_CLK1N	IO	OLDI Differential Clock (negative)	AD15

ADVANCE INFORMATION

表 5-49. OLDI0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
OLDI0_CLK1P	IO	OLDI Differential Clock (positive)	AD14

5.3.20 OSPI

5.3.20.1 MAIN Domain

表 5-50. OSPI0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
OSPI0_CLK	O	OSPI Clock	P23
OSPI0_DQS	I	OSPI Data Strobe (DQS) or Loopback Clock Input	P22
OSPI0_ECC_FAIL	I	OSPI ECC Status	L23
OSPI0_LBCLKO	IO	OSPI Loopback Clock Output	N23
OSPI0_CSn0	O	OSPI Chip Select 0 (active low)	M25
OSPI0_CSn1	O	OSPI Chip Select 1 (active low)	L24
OSPI0_CSn2	O	OSPI Chip Select 2 (active low)	L22
OSPI0_CSn3	O	OSPI Chip Select 3 (active low)	L23
OSPI0_D0	IO	OSPI Data 0	L25
OSPI0_D1	IO	OSPI Data 1	N24
OSPI0_D2	IO	OSPI Data 2	N25
OSPI0_D3	IO	OSPI Data 3	M24
OSPI0_D4	IO	OSPI Data 4	N21
OSPI0_D5	IO	OSPI Data 5	N22
OSPI0_D6	IO	OSPI Data 6	P21
OSPI0_D7	IO	OSPI Data 7	N20
OSPI0_RESET_OUT0	O	OSPI Reset	L23
OSPI0_RESET_OUT1	O	OSPI Reset	L22

5.3.21 Power Supply

表 5-51. Power Supply Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
CAP_VDDS0 (1)	CAP	External capacitor connection for IO group 0	1A8
CAP_VDDS1 (1)	CAP	External capacitor connection for IO group 1	1C10
CAP_VDDS2 (1)	CAP	External capacitor connection for IO group 2	1B6
CAP_VDDS3 (1)	CAP	External capacitor connection for IO group 3	1F10
CAP_VDDS5 (1)	CAP	External capacitor connection for IO group 5	1B9
CAP_VDDS6 (1)	CAP	External capacitor connection for IO group 6	1C9
CAP_VDDS_CANUART (1)	CAP	External capacitor connection for IO group CANUART	1B2
CAP_VDDS_MCU (1)	CAP	External capacitor connection for IO group MCU	1B4
VDDA_0P85_DLL_MMC0	PWR	MMC0 DLL analog supply	1J1
VDDA_1P8_CSI_DSI	PWR	CSIRX0 and DSITX0 1.8 V analog supply	1K7
VDDA_1P8_USB	PWR	USB0 and USB1 1.8 V analog supply	1K5
VDDA_1P8_OLDI0	PWR	OLDI0 analog supply	1K10
VDDA_3P3_USB	PWR	USB0 and USB1 3.3 V analog supply	Y11
VDDA_CORE_CSI_DSI	PWR	CSIRX0 and DSITX0 core supply	1K6
VDDA_CORE_DSI_CLK	PWR	DSITX0 clock core supply	1K8
VDDA_CORE_USB	PWR	USB0 and USB1 core supply	1J4

表 5-51. Power Supply Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
VDDA_DDR_PLL0	PWR	DDR deskew PLL supply	1F2
VDDA_MCU	PWR	RCOSC, POR, POK, and MCU PLL analog supply	1C3
VDDA_PLL0	PWR	MAIN PLL, PER0 PLL, and PER1 PLL analog supply	1D4
VDDA_PLL1	PWR	DSS PLL0, DSS PLL1, and DSS PLL2 analog supply	1H7
VDDA_PLL2	PWR	VIDEO PLL analog supply	1F6
VDDA_PLL3	PWR	DDR PLL and GPU PLL analog supply	1F4
VDDA_PLL4	PWR	ARM0 PLL and SMS PLL analog supply	1D7
VDDA_TEMP0	PWR	TEMP0 analog supply	1F5
VDDA_TEMP1	PWR	TEMP1 analog supply	K20
VDDA_TEMP2	PWR	TEMP2 analog supply	1D3
VDDR_CORE	PWR	RAM core supply	1C8, 1E5, 1H3
VDDSHV0	PWR	IO supply for IO group 0	1B7
VDDSHV1	PWR	IO supply for IO group 1	1D10
VDDSHV2	PWR	IO supply for IO group 2	1B5
VDDSHV3	PWR	IO supply for IO group 3	1E10, 1G10
VDDSHV5	PWR	IO supply for IO group 5	1A9
VDDSHV6	PWR	IO supply for IO group 6	1B10
VDDSHV_CANUART	PWR	IO supply for IO group CANUART	1A2
VDDSHV_MCU	PWR	IO supply for IO group MCU	1B3
VDDS_DDR	PWR	DDR PHY IO supply	1C1, 1D2, 1E1, 1F1, 1G2, 1H1, AE2, B1
VDDS_DDR_C	PWR	DDR clock IO supply	1E2
VDDS_MMC0	PWR	MMC0 PHY IO supply	1K2
VDDS_OSC0	PWR	MCU_OSC0 and WKUP_LFOSC0 supply	1C2
VDD_CANUART	PWR	CANUART core supply	1A1
VDD_CORE	PWR	Core supply	1C5, 1C7, 1D6, 1D8, 1E3, 1E7, 1E9, 1F8, 1G3, 1G5, 1G7, 1G9, 1H10, 1H4, 1H6, 1H8, 1J2, 1J5, 1J7, 1J9
VDD_MMC0	PWR	MMC0 PHY core supply	1K3
VPP	PWR	eFuse ROM programming supply	F7

ADVANCE INFORMATION

表 5-51. Power Supply Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
VSS	PWR	Ground	1A3, 1A5, 1A7, 1B1, 1B8, 1C4, 1C6, 1D1, 1D5, 1D9, 1E4, 1E6, 1E8, 1F3, 1F7, 1F9, 1G1, 1G4, 1G6, 1G8, 1H2, 1H5, 1H9, 1J10, 1J3, 1J6, 1J8, 1K1, 1K9, A1, A12, A25, A6, A9, AA21, AA3, AB2, AC1, AD22, AD4, AE1, AE13, AE16, AE25, B3, C2, C20, D14, D3, E1, F3, G1, G4, H2, K1, L4, N1, P20, P4, U1, U4, V3, W2, Y1, Y4

(1) This pin must always be connected via a 6.3V, 1µF capacitor to VSS.

5.3.22 Reserved

表 5-52. Reserved Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
RSVD0	N/A	Reserved, must be left unconnected	Y13
RSVD1	N/A	Reserved, must be left unconnected	Y14
RSVD2	N/A	Reserved, must be left unconnected	Y17
RSVD3	N/A	Reserved, must be left unconnected	Y19
RSVD4	N/A	Reserved, must be left unconnected	AA17
RSVD5	N/A	Reserved, must be left unconnected	B5
RSVD6	N/A	Reserved, must be left unconnected	C5
RSVD7	N/A	Reserved, must be left unconnected	F6
RSVD8	N/A	Reserved, must be left unconnected	F10
RSVD9	N/A	Reserved, must be left unconnected	H5
RSVD10	N/A	Reserved, must be left unconnected	K6

5.3.23 System and Miscellaneous

5.3.23.1 Boot Mode Configuration

5.3.23.1.1 MAIN Domain

表 5-53. Sysboot Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
BOOTMODE00	I	Bootmode pin 0	U22
BOOTMODE01	I	Bootmode pin 1	U21
BOOTMODE02	I	Bootmode pin 2	U20
BOOTMODE03	I	Bootmode pin 3	V25
BOOTMODE04	I	Bootmode pin 4	T20
BOOTMODE05	I	Bootmode pin 5	T21
BOOTMODE06	I	Bootmode pin 6	V24
BOOTMODE07	I	Bootmode pin 7	W25

ADVANCE INFORMATION

表 5-53. Sysboot Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
BOOTMODE08	I	Bootmode pin 8	AC25
BOOTMODE09	I	Bootmode pin 9	AB25
BOOTMODE10	I	Bootmode pin 10	AA25
BOOTMODE11	I	Bootmode pin 11	W24
BOOTMODE12	I	Bootmode pin 12	Y24
BOOTMODE13	I	Bootmode pin 13	AD25
BOOTMODE14	I	Bootmode pin 14	AB24
BOOTMODE15	I	Bootmode pin 15	AC24

5.3.23.2 Clock

5.3.23.2.1 MCU Domain

表 5-54. MCU Clock Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_OSC0_XI	I	High frequency oscillator input	A10
MCU_OSC0_XO	O	High frequency oscillator output	A11

5.3.23.2.2 WKUP Domain

表 5-55. WKUP Clock Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
WKUP_LFOSC0_XI	I	Low frequency (32.768 KHz) oscillator input	A7
WKUP_LFOSC0_XO	O	Low frequency (32.768 KHz) oscillator output	A8

5.3.23.3 System

5.3.23.3.1 MAIN Domain

表 5-56. System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
AUDIO_EXT_REFCLK0	IO	External clock input to McASP or output from McASP	A23, C19, F23, Y23
AUDIO_EXT_REFCLK1	IO	External clock input to McASP or output from McASP	C22, F25, P24
CLKOUT0	O	RMII Clock Output (50 MHz). This pin is used for clock source to the external RMII PHY and must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.	A19, C16, C25
EXTINTn	I	External Interrupt	C23
EXT_REFCLK1	I	External clock input to Main Domain	C25
MAIN_ERRORn	IO	Error signal output from MAIN Domain ESM	E20, E24, P25
OBSCLK0	O	Main Domain Observation clock output for test and debug purposes only	AA25
OBSCLK1	O	Main Domain Observation clock output for test and debug purposes only	B25
PORz_OUT	O	Main Domain POR status output	H24
RESETSTATz	O	Main Domain warm reset status output	G25
RESET_REQz	I	Main Domain external warm reset request input	G24
SYSCLKOUT0	O	Main Domain system clock output (divided by 4) for test and debug purposes only	C25

ADVANCE INFORMATION

5.3.23.3.2 MCU Domain

表 5-57. MCU System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_ERRORn	IO	Error signal output from MCU Domain ESM	G6
MCU_EXT_REFCLK0	I	External input to MCU Domain	E10, F8
MCU_OBSCLK0	O	MCU Domain Observation clock output for test and debug purposes only	E10
MCU_PORz	I	MCU and Main Domain cold reset	H6
MCU_RESETSTATz	O	MCU Domain warm reset status output	F14
MCU_RESETz	I	MCU and Main Domain warm reset	F11
MCU_SYSCLKOUT0	O	MCU Domain system clock output (divided by 4) for test and debug purposes only	E10

5.3.23.3.3 WKUP Domain

表 5-58. WKUP System Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
PMIC_LPM_EN0	O	Dual-function PMIC control output, Low Power Mode (active low) or PMIC Enable (active high)	B9
WKUP_CLKOUT0	O	WKUP Domain CLKOUT0 output	F13

5.3.23.4 VMON

表 5-59. VMON Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
VMON_1P8_SOC	A	Voltage monitor input for 1.8 V SoC power supply	1A10
VMON_3P3_SOC	A	Voltage monitor input for 3.3 V SoC power supply	1A4
VMON_VSYS	A	Voltage monitor input, fixed 0.45 V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply.	1A6

5.3.24 TIMER

5.3.24.1 MAIN Domain

表 5-60. TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	C24, H25
TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	B24, H22
TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	B23, H23
TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	F20, H21
TIMER_IO4	IO	Timer Inputs and Outputs (not tied to single timer instance)	C25, J24
TIMER_IO5	IO	Timer Inputs and Outputs (not tied to single timer instance)	A24, H20
TIMER_IO6	IO	Timer Inputs and Outputs (not tied to single timer instance)	A23, D23
TIMER_IO7	IO	Timer Inputs and Outputs (not tied to single timer instance)	C22, D24

5.3.24.2 MCU Domain

表 5-61. MCU_TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	B8, D6
MCU_TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	B7, E10
MCU_TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	F8
MCU_TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	E7

5.3.24.3 WKUP Domain

表 5-62. WKUP_TIMER Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
WKUP_TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	C7, E8
WKUP_TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	B10, C6

5.3.25 UART

5.3.25.1 MAIN Domain

表 5-63. UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
UART0_CTSn	I	UART Clear to Send (active low)	A23
UART0_RTSn	O	UART Request to Send (active low)	C22
UART0_RXD	I	UART Receive Data	A22
UART0_TXD	O	UART Transmit Data	B22

表 5-64. UART1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
UART1_CTSn	I	UART Clear to Send (active low)	D25
UART1_DCDn	I	UART Clear to Send (active low)	B25
UART1_DSRn	I	UART Data Set Ready (active low)	A24
UART1_DTRn	O	UART Data Terminal Ready (active low)	B23
UART1_RIn	I	UART Ring Indicator	F20
UART1_RTSn	O	UART Request to Send (active low)	E25
UART1_RXD	I	UART Receive Data	C24, G23
UART1_TXD	O	UART Transmit Data	B24, G20

表 5-65. UART2 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
UART2_CTSn	I	UART Clear to Send (active low)	AB24, H21, Y21
UART2_RTSn	O	UART Request to Send (active low)	AC24, H23, W20
UART2_RXD	I	UART Receive Data	A23, AC25, AE24, H25
UART2_TXD	O	UART Transmit Data	AB25, C22, H22, W23

ADVANCE INFORMATION

表 5-66. UART3 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
UART3_CTSn	I	UART Clear to Send (active low)	D24, W21
UART3_RTSn	O	UART Request to Send (active low)	AC20, D23
UART3_RXD	I	UART Receive Data	AA23, AA25, J24
UART3_TXD	O	UART Transmit Data	H20, W24, Y23

表 5-67. UART4 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
UART4_CTSn	I	UART Clear to Send (active low)	Y20
UART4_RTSn	O	UART Request to Send (active low)	AA20
UART4_RXD	I	UART Receive Data	AB23, J25, T22, Y24
UART4_TXD	O	UART Transmit Data	AD23, AD25, K25, U25

表 5-68. UART5 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
UART5_CTSn	I	UART Clear to Send (active low)	AC21, P22
UART5_RTSn	O	UART Request to Send (active low)	AD21, N23
UART5_RXD	I	UART Receive Data	AB24, AC23, B23, L21, L22
UART5_TXD	O	UART Transmit Data	AC24, AE23, F20, L20, L23

表 5-69. UART6 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
UART6_CTSn	I	UART Clear to Send (active low)	AE21, N20
UART6_RTSn	O	UART Request to Send (active low)	P21, W22
UART6_RXD	I	UART Receive Data	AD24, AE22, D23, D25, K21, N21
UART6_TXD	O	UART Transmit Data	AC22, D24, E25, K24, N22, P24

5.3.25.2 MCU Domain

表 5-70. MCU_UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
MCU_UART0_CTSn	I	UART Clear to Send (active low)	B8
MCU_UART0_RTSn	O	UART Request to Send (active low)	B7
MCU_UART0_RXD	I	UART Receive Data	B6
MCU_UART0_TXD	O	UART Transmit Data	C8

5.3.25.3 WKUP Domain

表 5-71. WKUP_UART0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
WKUP_UART0_CTSn	I	UART Clear to Send (active low)	C7
WKUP_UART0_RTSn	O	UART Request to Send (active low)	C6
WKUP_UART0_RXD	I	UART Receive Data	D8

表 5-71. WKUP_UART0 Signal Descriptions (続き)

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
WKUP_UART0_TXD	O	UART Transmit Data	D7

5.3.26 USB

5.3.26.1 MAIN Domain

表 5-72. USB0 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
USB0_DM	IO	USB 2.0 Differential Data (negative)	AE8
USB0_DP	IO	USB 2.0 Differential Data (positive)	AE7
USB0_DRVVBUS	O	USB VBUS control output (active high)	G22
USB0_RCALIB (1)	A	Pin to connect to calibration resistor	Y8
USB0_VBUS (2)	A	USB Level-shifted VBUS Input	Y7

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.
(2) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see セクション 8.2.3, *USB VBUS Design Guidelines*.

表 5-73. USB1 Signal Descriptions

SIGNAL NAME [1]	PIN TYPE [2]	DESCRIPTION [3]	AMH PIN [4]
USB1_DM	IO	USB 2.0 Differential Data (negative)	AE10
USB1_DP	IO	USB 2.0 Differential Data (positive)	AE9
USB1_DRVVBUS	O	USB VBUS control output (active high)	G21
USB1_RCALIB (1)	A	Pin to connect to calibration resistor	1K4
USB1_VBUS (2)	A	USB Level-shifted VBUS Input	Y10

(1) An external 499 Ω ±1% resistor must be connected between this pin and VSS and the maximum power dissipation for the resistor is 7.2mW. No external voltage should be applied to this pin.
(2) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see セクション 8.2.3, *USB VBUS Design Guidelines*.

ADVANCE INFORMATION

5.4 Pin Connectivity Requirements

This section describes connectivity requirements for package balls that have specific connectivity requirements and unused package balls.

注

All power pins must be supplied with the voltages specified in セクション 6.5, *Recommended Operating Conditions*, unless otherwise specified.

注

For additional clarification, "leave unconnected" or "no connect" (NC) means **no** signal traces can be connected to these device ball numbers.

表 5-74. Connectivity Requirements

AMH BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
G6 B13	MCU_ERRORn TRSTn	Each of these balls must be connected to VSS through separate external pull resistors to ensure these balls are held to a valid logic low level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-down can be used to hold a valid logic low level if no PCB signal trace is connected to the ball.
B12 D13 F11 G24 C13 E13 E14	EMU0 EMU1 MCU_RESETz RESET_REQz TCK TDI TMS	Each of these balls must be connected to the corresponding power supply(1) through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull-up can be used to hold a valid logic high level if no PCB signal trace is connected to the ball.
E11 D11 A13 C11	MCU_I2C0_SCL MCU_I2C0_SDA WKUP_I2C0_SCL WKUP_I2C0_SDA	Each of these balls must be connected to the corresponding power supply(1) through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high level.
U22 U21 U20 V25 T20 T21 V24 W25 AC25 AB25 AA25 W24 Y24 AD25 AB24 AC24	GPMC0_AD0 GPMC0_AD1 GPMC0_AD2 GPMC0_AD3 GPMC0_AD4 GPMC0_AD5 GPMC0_AD6 GPMC0_AD7 GPMC0_AD8 GPMC0_AD9 GPMC0_AD10 GPMC0_AD11 GPMC0_AD12 GPMC0_AD13 GPMC0_AD14 GPMC0_AD15	Each of these balls must be connected to the corresponding power supply(1) or VSS through separate external pull resistors to ensure the inputs associated with these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.
1G2 1H1 AE2 B1 1C1 1D2 1E1 1F1 1E2	VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR_C	If DDRSS is not used, each of these balls must be connected directly to VSS.

ADVANCE INFORMATION

表 5-74. Connectivity Requirements (続き)

AMH BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
T6	DDR0_ACT_n	If DDRSS is not used, leave unconnected. Note: The DDR0 pins in this list can only be left unconnected when VDDS_DDR and VDDS_DDR_C are connected to VSS. The DDR0 pins must be connected as defined in the DDR Board Design and Layout Guidelines, when VDDS_DDR and VDDS_DDR_C are connected to a power source.
K3	DDR0_ALERT_n	
T5	DDR0_CAS_n	
T1	DDR0_PAR	
P6	DDR0_RAS_n	
T4	DDR0_WE_n	
K5	DDR0_A0	
L2	DDR0_A1	
L3	DDR0_A2	
M2	DDR0_A3	
N2	DDR0_A4	
K2	DDR0_A5	
N3	DDR0_A6	
L1	DDR0_A7	
M1	DDR0_A8	
T2	DDR0_A9	
R2	DDR0_A10	
N5	DDR0_A11	
P3	DDR0_A12	
P2	DDR0_A13	
N6	DDR0_BA0	
K4	DDR0_BA1	
Y6	DDR0_BG0	
U6	DDR0_BG1	
Y5	DDR0_CAL0	
R1	DDR0_CK0	
P1	DDR0_CK0_n	
N4	DDR0_CKE0	
P5	DDR0_CKE1	
L6	DDR0_CS0_n	
T3	DDR0_CS1_n	
C3	DDR0_DM0	
H3	DDR0_DM1	
V4	DDR0_DM2	
AD1	DDR0_DM3	
B2	DDR0_DQ0	
A3	DDR0_DQ1	
A4	DDR0_DQ2	
A5	DDR0_DQ3	
A2	DDR0_DQ4	
B4	DDR0_DQ5	
D2	DDR0_DQ6	
C4	DDR0_DQ7	
E2	DDR0_DQ8	
F1	DDR0_DQ9	
G5	DDR0_DQ10	
F2	DDR0_DQ11	
G3	DDR0_DQ12	
H4	DDR0_DQ13	
J2	DDR0_DQ14	
G2	DDR0_DQ15	
U2	DDR0_DQ16	
U3	DDR0_DQ17	
U5	DDR0_DQ18	
V5	DDR0_DQ19	
V2	DDR0_DQ20	
Y2	DDR0_DQ21	
Y3	DDR0_DQ22	
AA4	DDR0_DQ23	
AC2	DDR0_DQ24	
AA2	DDR0_DQ25	
AC4	DDR0_DQ26	
AD2	DDR0_DQ27	

ADVANCE INFORMATION

表 5-74. Connectivity Requirements (続き)

AMH BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
AD3 AC3 AE4 AE3 D1 C1 J1 H1 W1 V1 AA1 AB1 L5 V6 AA5	DDR0_DQ28 DDR0_DQ29 DDR0_DQ30 DDR0_DQ31 DDR0_DQS0 DDR0_DQS0_n DDR0_DQS1 DDR0_DQS1_n DDR0_DQS2 DDR0_DQS2_n DDR0_DQS2 DDR0_DQS2_n DDR0_ODT0 DDR0_ODT1 DDR0_RESET0_n	
1K3 1J1	VDD_MMC0 VDDA_0P85_DLL_MMC0	If MMC0 is not used, each of these balls must be connected to the same power source as VDD_CORE.
1K2	VDDS_MMC0	If MMC0 is not used, each of these balls must be connected to any 1.8-V power source that does not violate device power supply sequencing requirements.
AC5 AA6 AB8 AD5 AC7 AB7 AD6 AE5 AE6 AC6 AA7 AB6	MMC0_CALPAD MMC0_CLK MMC0_CMD MMC0_DS MMC0_DAT0 MMC0_DAT1 MMC0_DAT2 MMC0_DAT3 MMC0_DAT4 MMC0_DAT5 MMC0_DAT6 MMC0_DAT7	If MMC0 is not used, each of these balls must be left unconnected.
1J4 1K5 Y11	VDDA_CORE_USB VDDA_1P8_USB VDDA_3P3_USB	USB0 and USB1 share these power rails, so each of these balls must be connected to valid power sources when either USB0 or USB1 is used. If USB0 and USB1 are not used, each of these balls must be connected directly to VSS.
AE8 AE7 Y8 Y7 AE10 AE9 1K4 Y10	USB0_DM USB0_DP USB0_RCALIB USB0_VBUS USB1_DM USB1_DP USB1_RCALIB USB1_VBUS	If USB0 or USB1 is not used, leave the respective DM, DP, and VBUS balls unconnected. Note: The USB0_RCALIB and USB1_RCALIB pins can only be left unconnected when VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB are connected to VSS. The USB0_RCALIB and USB1_RCALIB pins must be connected to VSS through separate appropriate external resistors when VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB are connected to power sources.
1K6 IK8 IK7	VDDA_CORE_CSI_DSI VDDA_CORE_DSI_CLK VDDA_1P8_CSI_DSI	If CSIRX0 and DSITX0 are not used and the device boundary scan function is required, each of these balls must be connected to valid power sources. If CSIRX0 and DSITX0 are not used and the device boundary scan function is not required, each of these balls can alternatively be connected directly to VSS.

ADVANCE INFORMATION

表 5-74. Connectivity Requirements (続き)

AMH BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
AE12 AE11 AB11 AB10 AC10 AC9 AA10 AA9 AD9 AD8 AA15	CSI0_RXCLKN CSI0_RXCLKP CSI0_RXN0 CSI0_RXP0 CSI0_RXN1 CSI0_RXP1 CSI0_RXN2 CSI0_RXP2 CSI0_RXN3 CSI0_RXP3 CSI0_RXRCALIB	If CSIRX0 is not used, leave unconnected.
AA12 AA13 AD11 AD12 AB13 AB14 AC12 AC13 AE14 AE15 Y16	DSI0_TXCLKN DSI0_TXCLKP DSI0_TXN0 DSI0_TXP0 DSI0_TXN1 DSI0_TXP1 DSI0_TXN2 DSI0_TXP2 DSI0_TXN3 DSI0_TXP3 DSI0_TXRCALIB	If DSITX0 is not used, leave unconnected.
AE20 AD20 AC19 AD19 AA19 AB19 AD18 AE19 AD17 AD16 AB17 AC17 AC16 AC15 AB16 AA16 AE18 AE17 AD15 AD14	OLDI0_A0N OLDI0_A0P OLDI0_A1N OLDI0_A1P OLDI0_A2N OLDI0_A2P OLDI0_A3N OLDI0_A3P OLDI0_A4N OLDI0_A4P OLDI0_A5N OLDI0_A5P OLDI0_A6N OLDI0_A6P OLDI0_A7N OLDI0_A7P OLDI0_CLK0N OLDI0_CLK0P OLDI0_CLK1N OLDI0_CLK1P	If OLDI0 is not used, leave unconnected.
1A6	VMON_VSYS	If VMON_VSYS is not used, this ball must be connected directly to VSS.
1A10 1A4	VMON_1P8_SOC VMON_3P3_SOC	If VMON_1P8_SOC and VMON_3P3_SOC are not used to monitor the SOC power rails, these balls must remain connected to their respective 1.8-V and 3.3-V power rails or connected directly to VSS.

(1) To determine which power supply is associated with any IO, see the POWER column of the *Pin Attributes* table.

ADVANCE INFORMATION

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Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This can be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors are recommended to hold a valid logic level on balls with external connections.

Many of the device IOs are turned off by default and external pull resistors may be required to hold inputs of any attached device in a valid logic state until software initializes the respective IOs. The state of configurable device IOs are defined in the BALL STATE DURING RESET RX/TX/PULL and BALL STATE AFTER RESET RX/TX/PULL columns of the *Pin Attributes* table. Any IO with its input buffer (RX) turned off is allowed to float without damaging the device. However, any IO with its input buffer (RX) turned on shall never be allowed to float to any potential between V_{ILSS} and V_{IHSS}. The input buffer can enter a high-current state which could damage the IO cell if allowed to float between these levels.

6 Specifications

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All specifications listed are preliminary and may change during device characterization.

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1) (2)

PARAMETER		MIN	MAX	UNIT
VDD_CORE	Core supply	-0.3	1.05	V
VDDR_CORE	RAM core supply	-0.3	1.05	V
VDD_CANUART	CANUART core supply	-0.3	1.05	V
VDDA_CORE_CSI_DSI	CSIRX0 and DSITX0 core supply	-0.3	1.05	V
VDDA_CORE_DSI_CLK	DSITX0 clock core supply	-0.3	1.05	V
VDDA_CORE_USB	USB0 and USB1 core supply	-0.3	1.05	V
VDDA_DDR_PLL0	DDR deskew PLL supply	-0.3	1.05	V
VDD_MMC0	MMC0 PHY core supply	-0.3	1.05	V
VDDA_0P85_DLL_MMC0	MMC0 DLL analog supply	-0.3	1.05	V
VDDS_DDR	DDR PHY IO supply	-0.3	1.57	V
VDDS_DDR_C	DDR clock IO supply	-0.3	1.57	V
VDDS_MMC0	MMC0 PHY IO supply	-0.3	1.98	V
VDDS_OSC0	MCU_OSC0 and WKUP_LFOSC0 supply	-0.3	1.98	V
VDDA_MCU	RCOSC, POR, POK, and MCU PLL analog supply	-0.3	1.98	V
VDDA_PLL0	MAIN PLL, PER0 PLL, and PER1 PLL analog supply	-0.3	1.98	V
VDDA_PLL1	DSS PLL0, DSS PLL1, and DSS PLL2 analog supply	-0.3	1.98	V
VDDA_PLL2	GPU PLL analog supply	-0.3	1.98	V
VDDA_PLL3	DDR PLL analog supply	-0.3	1.98	V
VDDA_PLL4	ARM0 PLL and SMS PLL analog supply	-0.3	1.98	V
VDDA_1P8_CSI_DSI	CSIRX0 and DSITX0 1.8 V analog supply	-0.3	1.98	V
VDDA_1P8_OLDI0	OLDI0 1.8 V analog supply	-0.3	1.98	V
VDDA_1P8_USB	USB0 and USB1 1.8 V analog supply	-0.3	1.98	V
VDDA_TEMP0	TEMP0 analog supply	-0.3	1.98	V
VDDA_TEMP1	TEMP1 analog supply	-0.3	1.98	V
VDDA_TEMP2	TEMP2 analog supply	-0.3	1.98	V
VPP	eFuse ROM programming supply	-0.3	1.98	V
VDDSHV_MCU	IO supply for IO group MCU	-0.3	3.63	V
VDDSHV_CANUART	IO supply for IO group CANUART	-0.3	3.63	V
VDDSHV0	IO supply for IO group 0	-0.3	3.63	V
VDDSHV1	IO supply for IO group 1	-0.3	3.63	V
VDDSHV2	IO supply for IO group 2	-0.3	3.63	V
VDDSHV3	IO supply for IO group 3	-0.3	3.63	V
VDDSHV5	IO supply for IO group 5	-0.3	3.63	V
VDDSHV6	IO supply for IO group 6	-0.3	3.63	V
VDDA_3P3_USB	USB0 and USB1 3.3 V analog supply	-0.3	3.63	V

ADVANCE INFORMATION

over operating junction temperature range (unless otherwise noted)(1) (2)

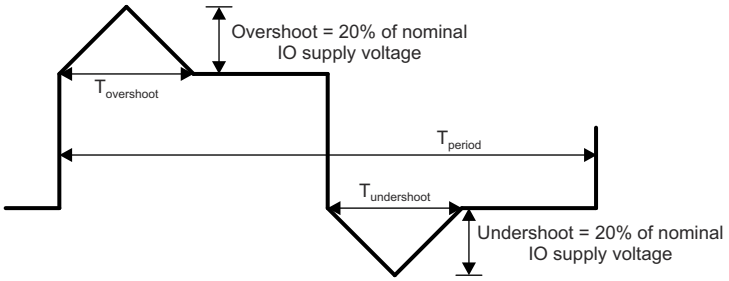
PARAMETER		MIN	MAX	UNIT
Steady-state max voltage at all fail-safe IO pins	MCU_PORz	-0.3	3.63	V
	MCU_I2C0_SCL, MCU_I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, EXTINTn When operating at 1.8V	-0.3	1.98(3)	V
	MCU_I2C0_SCL, MCU_I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, EXTINTn When operating at 3.3V	-0.3	3.63(3)	
	VMON_1P8_SOC	-0.3	1.98	V
	VMON_3P3_SOC	-0.3	3.63	V
	VMON_VSYS(4)	-0.3	1.98	V
Steady-state max voltage at all other IO pins(5)	USB0_VBUS, USB1_VBUS(6)	-0.3	3.6	V
	All other IO pins	-0.3	IO supply voltage + 0.3	V
Transient overshoot and undershoot at IO pin	20% of IO supply voltage for up to 20% of the signal period (see 図 6-1, *IO Transient Voltage Ranges*)		0.2 × VDD(7)	V
Latch-up performance(8)	I-Test	-100	100	mA
	Over-Voltage (OV) Test		1.5 x VDD(7)	V
T_{STG}	Storage temperature	-55	+150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the セクション 6.5, *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) The absolute maximum ratings for these fail-safe pins depends on their IO supply operating voltage. Therefore, this value is also defined by the maximum V_{IH} value found in the *I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics* section, where the electrical characteristics table has separate parameter values for 1.8-V mode and 3.3-V mode.
(4) The VMON_VSYS pin provides a way to monitor the system power supply. For more information, see セクション 8.2.4, *System Power Supply Monitor Design Guidelines*.
(5) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
(6) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see セクション 8.2.3, *USB Design Guidelines*.
(7) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
(8) For current pulse injection (I-Test):
- Pins stressed per JEDEC JESD78 (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

For over-voltage performance (Over-Voltage (OV) Test):
- Supplies stressed per JEDEC JESD78 (Class II) and passed specified voltage injection.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The MCU_I2C0_SCL, MCU_I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, EXTINTn, VMON_1P8_SOC, VMON_3P3_SOC, and MCU_PORz are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in セクション 6.1.

ADVANCE INFORMATION



A. $T_{overshoot} + T_{undershoot} < 20\%$ of T_{period}

図 6-1. IO Transient Voltage Ranges

6.2 ESD Ratings for Devices which are not AEC - Q100 Qualified

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings for AEC - Q100 Qualified Devices

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC - Q100-002(1)		±1000	V
		Charged-device model (CDM), per AEC - Q100-011	Corner pins (A1,A25, AE1, and AE25)	±750	
			All other pins	±250	

(1) AEC - Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Power-On Hours (POH)

POWER ON HOURS (POH)(1) (2) (3)		
JUNCTION TEMPERATURE RANGE (T_J)		LIFETIME (POH)
125°C Industrial and Automotive(4)	–40°C to 105°C	100000
	–40°C to 125°C	20000(5)

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
(3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.
(4) Either -40 to 105C or -40 to 125C profile should be chosen and applied through the lifetime of the application. Mixing of these profiles for the purposes of extending temperature and/or POH may result in increased reliability failure risk and is not recommended.
(5) The -40 to 125C profile is defined as 20000 power on hours with a junction temperature as follows: 5%@-40°C, 65%@70°C, 20%@110°C, and 10%@125°C.

ADVANCE INFORMATION

6.5 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
VDD_CORE(2) VDDA_CORE_CSI_DSI(2) VDDA_CORE_DSI_CLK(2) VDDA_CORE_USB(2) VDDA_DDR_PLL0(2)	Core supply CSIRX0 and DSITX0 core supply DSITX0 clock core supply USB0 and USB1 core supply DDR deskew PLL supply	0.75-V operation	0.715	0.75	0.79	V
		0.85-V operation	0.81	0.85	0.895	V
VDD_CANUART(3)	CANUART core supply	0.75-V operation	0.715	0.75	0.79	V
		0.85-V operation	0.81	0.85	0.895	V
VDDR_CORE	RAM core supply		0.81	0.85	0.895	V
VDD_MMC0(4) VDDA_0P85_DLL_MMC0(4)	MMC0 PHY core supply MMC0 DLL analog supply		0.81	0.85	0.895	V
VDDS_DDR(5) VDDS_DDR_C(5)	DDR PHY IO supply DDR clock IO supply	1.1-V operation	1.06	1.1	1.17	V
VDDS_MMC0	MMC0 PHY IO supply		1.71	1.8	1.89	V
VDDS_OSC0	MCU_OSC0 and WKUP_LFOSC0 supply		1.71	1.8	1.89	V
VDDA_MCU	RCOSC, POR, POK, and MCU PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL0	MAIN PLL, PER0 PLL, and PER1 PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL1	DSS PLL0, DSS PLL1, and DSS PLL2 analog supply		1.71	1.8	1.89	V
VDDA_PLL2	GPU PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL3	DDR PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL4	ARM0 PLL and SMS PLL analog supply		1.71	1.8	1.89	V
VDDA_1P8_CSI_DSI	CSIRX0 and DSITX0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_1P8_OLDI0	OLDI0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_1P8_USB	USB0 and USB1 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_TEMP0	TEMP0 analog supply		1.71	1.8	1.89	V
VDDA_TEMP1	TEMP1 analog supply		1.71	1.8	1.89	V
VDDA_TEMP2	TEMP2 analog supply		1.71	1.8	1.89	V
VPP	eFuse ROM programming supply		see(6)	see(6)	see(6)	V
VMON_1P8_SOC	Voltage monitor for 1.8 V SoC power supply		1.71	1.8	1.89	V
VDDA_3P3_USB	USB0 and USB1 3.3 V analog supply		3.135	3.3	3.465	V
VMON_3P3_SOC	Voltage monitor for 3.3 V SoC power supply		3.135	3.3	3.465	V
VMON_VSYS	Voltage monitor for system power supply		0	see(7)	1	V
USB0_VBUS	USB0 Level-shifted VBUS Input		0	see(8)	3.465	V
USB1_VBUS	USB1 Level-shifted VBUS Input		0	see(8)	3.465	V
VDDSHV_CANUART(9)	Dual-voltage IO supply for IO group CANUART	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV_MCU	Dual-voltage IO supply for IO group MCU	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV0	Dual-voltage IO supply for IO group 0	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV1	Dual-voltage IO supply for IO group 1	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV2	Dual-voltage IO supply for IO group 2	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V

ADVANCE INFORMATION

over operating junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
VDDSHV3	Dual-voltage IO supply for IO group 3	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV5	Dual-voltage IO supply for IO group 5	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
VDDSHV6	Dual-voltage IO supply for IO group 6	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.135	3.3	3.465	V
T_J	Operating junction temperature range	125°C Industrial and Automotive	-40		125	°C

(1) The voltage at the device ball must never drop below the MIN voltage or rise above the MAX voltage for any amount of time during normal device operation.
(2) VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 shall be sourced from the same power source. Care should be taken to ensure that voltage differential between VDD_CORE and VDDA_CORE_USB is within +/- 1%.
(3) VDD_CANUART shall be connected to an always on power source when using Partial IO or IO Only + DDR Self-refresh low power modes. VDD_CANUART shall be connected to the same power source as VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_USB, and VDDA_DDR_PLL0 when not using Partial IO or IO Only + DDR Self-refresh low power modes.
(4) VDD_MMC0 and VDDA_0P85_DLL_MMC0 must be connected to the same power source as VDD_CORE when MMC0 is not used. In this case, VDD_MMC0 and VDDA_0P85_DLL_MMC0 may be operated at a nominal voltage of 0.75 or 0.85.
(5) VDDS_DDR and VDDS_DDR_C shall be sourced from the same power source.
(6) Refer to the Recommended Operating Conditions for OTP eFuse Programming table for VPP supply voltages based on eFuse usage.
(7) The VMON_VSYS pin provides a way to monitor the system power supply. For more information, see セクション 8.2.4, *System Power Supply Monitor Design Guidelines*.
(8) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see セクション 8.2.3, *USB Design Guidelines*.
(9) VDDSHV_CANUART shall be connected to an always on power source when using Partial IO or IO Only + DDR Self-refresh low power modes. VDDSHV_CANUART shall be connected to any valid IO power source when not using Partial IO or IO Only + DDR Self-refresh low power modes.

ADVANCE INFORMATION

6.6 Operating Performance Points

表 6-1defines the maximum operating frequency of the clocks for each device speed grade and 表 6-2 defines the only valid Operating Performance Points (OPPs) for the device subsystem and core clocks..

表 6-1. Device Speed Grades

Speed Grade	VDD_CORE (V)(1)	MAXIMUM OPERATING FREQUNCY (MHz)									MAXIMUM TRANSITION RATE (MT/s) (2)
		A53SS (Cortex-A53x)	MAIN DOMAIN SYSCLK	MCU R5F	MCU DOMAIN SYSCLK	DEVICE MANAGER R5F	DEVICE MANAGER DOMAIN CLK	HSM	GPU	VPU	LPDDR4
O	0.75/0.85	1000	500	800	400	800	400	400	560	500	3200
S	0.75	1250	500	800	400	800	400	400	560	500	3200
	0.85	1400									
U	0.75	1250	500	800	400	800	400	400	720	500	3200
	0.85	1400							800		

(1) Nominal operating voltage, see *Recommended Operating Conditions*.
(2) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to DDR Board Design and Layout Guidelines for the proper PCB implementation to achieve maximum DDR frequency.

表 6-2. Device Operating Performance Points

OPP	A53SS(1)	FIXED OPERATING FREQUENCY OPTIONS (MHz)(2)								MT/s(3)
		MAIN DOMAIN SYSCLK	MCU R5F	MCU DOMAIN SYSCLK	DEVICE MANAGER R5F	DEVICE MANAGER DOMAIN CLK	HSM	GPU	VPU	LPDDR4
High	From ARM0 PLL Bypass to Speed Grade Maximum	500	800	400	800	400	400	Up to Speed Grade Maximum	500, 400, 200, or 100	From DDR PLL Bypass(4) to Speed Grade Maximum
Low		250	400	200	400	133	133			

(1) Default operating frequency, set by software at boot. Supports Dynamic Frequency Scaling after boot.
(2) Fixed operating frequency, set by software at boot.
(3) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to DDR Board Design and Layout Guidelines for the proper PCB implementation to achieve maximum DDR frequency.
(4) The DDR PLL output, which sources DDR0_CK0 and DDR0_CK0_n, is typically defined in units of frequency. So the "DDR PLL Bypass" transaction rate is equal to 2x the DDR PLL output frequency when operating in bypass mode.

6.7 Power Consumption Summary

For information on the device power consumption contact your TI Representative.

6.8 Electrical Characteristics

注

The interfaces or signals described in セクション 6.8 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Signal Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

6.8.1 I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8 V MODE						
V_{IL}	Input Low Voltage				0.3 × VDD[1]	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD[1]	V
V_{IH}	Input High Voltage		0.7 × VDD[1]		1.98[2]	V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDD[1]			V
V_{HYS}	Input Hysteresis Voltage		0.1 × VDD[1]			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0 V			±10	µA
V_{OL}	Output Low Voltage				0.2 × VDD[1]	V
I_{OL} [3]	Low Level Output Current	$V_{OL(MAX)}$	10			mA
SR_I [5]	Input Slew Rate		18f[4] or 1.8E+6			V/s
3.3 V MODE [6]						
V_{IL}	Input Low Voltage				0.3 × VDD[1]	V
V_{ILSS}	Input Low Voltage Steady State				0.25 × VDD[1]	V
V_{IH}	Input High Voltage		0.7 × VDD[1]		3.63[2]	V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDD[1]			V
V_{HYS}	Input Hysteresis Voltage		0.05 × VDD[1]			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or V_I = 0 V			±10	µA
V_{OL}	Output Low Voltage				0.4	V
I_{OL} [3]	Low Level Output Current	$V_{OL(MAX)}$	10			mA
SR_I [5]	Input Slew Rate		33f[4] or 3.3E+6		8E+7	V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
(2) This value also defines the Absolute Maximum Ratings value the IO.
(3) The I_{OL} parameter defines the minimum Low Level Output Current for which the device is able to maintain the specified V_{OL} value. The value defined by this parameter should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} value for attached components.
(4) f = toggle frequency of the input signal in Hz.
(5) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.
(6) I2C Hs-mode is not supported when operating the IO in 3.3 V mode.

ADVANCE INFORMATION

6.8.2 Fail-Safe Reset (FS RESET) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.3 × VDDS_OSC0	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.7 × VDDS_OSC0			V
V_{IHSS}	Input High Voltage Steady State		0.7 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage		200			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0 V			±10	µA
SR_I (2)	Input Slew Rate		18f(1) or 1.8E+6			V/s

(1) f = toggle frequency of the input signal in Hz.
(2) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

6.8.3 High-Frequency Oscillator (HFOSC) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.35 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.65 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage			49		mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0.0 V			±10	µA

6.8.4 Low-Frequency Oscillator (LFXOSC) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.30 × VDDS_OSC0	V
V_{IH}	Input High Voltage		0.70 × VDDS_OSC0			V
V_{HYS}	Input Hysteresis Voltage	Active Mode		85		mV
		Bypass Mode		324		mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0.0 V			±10	µA

6.8.5 eMMCPHY Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage				0.35 × VDDS_MMC0	V
V_{ILSS}	Input Low Voltage Steady State				0.20	V

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		0.65 × VDDS_MMC0			V
V_{IHSS}	Input High Voltage Steady State		1.4			V
I_{IN}	Input Leakage Current.	V_I = 1.8 V or 0 V			±10	µA
R_{PU}	Pull-up Resistor		15	20	25	kΩ
R_{PD}	Pull-down Resistor		15	20	25	kΩ
V_{OL}	Output Low Voltage	I_{OL} = 2 mA			0.30	V
V_{OH}	Output High Voltage	I_{OH} = -2 mA	VDDS_MMC0 - 0.30			V
SR_I	Input Slew Rate		5E+8			V/s

ADVANCE INFORMATION

6.8.6 SDIO Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8 V MODE						
V_{IL}	Input Low Voltage				0.58	V
V_{ILSS}	Input Low Voltage Steady State				0.58	V
V_{IH}	Input High Voltage		1.27			V
V_{IHSS}	Input High Voltage Steady State		1.7			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0 V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDDSHV5 - 0.45			V
I_{OL} (1)	Low Level Output Current	$V_{OL(MAX)}$	4			mA
I_{OH} (1)	High Level Output Current	$V_{OH(MIN)}$	4			mA
SR_I (3)	Input Slew Rate		18f(2) or 1.8E+6			V/s
3.3 V MODE						
V_{IL}	Input Low Voltage				0.25 × VDDSHV5	V
V_{ILSS}	Input Low Voltage Steady State				0.15 × VDDSHV5	V
V_{IH}	Input High Voltage		0.625 × VDDSHV5			V
V_{IHSS}	Input High Voltage Steady State		0.625 × VDDSHV5			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or V_I = 0 V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output Low Voltage				0.125 × VDDSHV5	V
V_{OH}	Output High Voltage		0.75 × VDDSHV5			V
I_{OL} (1)	Low Level Output Current	$V_{OL(MAX)}$	6			mA
I_{OH} (1)	High Level Output Current	$V_{OH(MIN)}$	10			mA
SR_I (3)	Input Slew Rate		33f(2) or 3.3E+6			V/s

(1) The I_{OL} and I_{OH} parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.
(2) f = toggle frequency of the input signal in Hz.
(3) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

6.8.7 LVCMOS Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8-V MODE						
V_{IL}	Input Low Voltage				0.35 × VDD(1)	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD(1)	V
V_{IH}	Input High Voltage		0.65 × VDD(1)			V
V_{IHSS}	Input High Voltage Steady State		0.85 × VDD(1)			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or V_I = 0.0 V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDD(1) - 0.45			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	3			mA
I_{OH} (2)	High Level Output Current	$V_{OH(MIN)}$	3			mA
SR_I (4)	Input Slew Rate		18f(3) or 1.8E+6			V/s
3.3-V MODE						
V_{IL}	Input Low Voltage				0.8	V
V_{ILSS}	Input Low Voltage Steady State				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{IHSS}	Input High Voltage Steady State		2.0			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or V_I = 0.0 V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{OL} (2)	Low Level Output Current	$V_{OL(MAX)}$	5			mA
I_{OH} (2)	High Level Output Current	$V_{OH(MIN)}$	9			mA
SR_I (4)	Input Slew Rate		33f(3) or 3.3E+6			V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.
(2) The I_{OL} and I_{OH} parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.
(3) f = toggle frequency of the input signal in Hz.
(4) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

ADVANCE INFORMATION

6.8.8 OLDI LVDS (OLDI) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Voltage, Output High	Differential Load = 100Ω			1.5	V
V_{OL}	Voltage, Output Low		0.925			V
V_{OCM}	Voltage, Output Common Mode		1.125		1.375	V
ΔV_{OCM}	Delta Voltage, Output Common Mode (Difference between high and low steady-states)				30	mV
V_{OD}	Voltage, Output Differential		250		400	mV
ΔV_{OD}	Delta Voltage, Output Differential (Difference between high and low steady-states)				50	mV
I_{OS}	Current, Output Short-Circuit	V = VSS Differential Load = 100Ω			-5	mA
I_{OZ}	Current, Output High-Z	V = VDD(1) or V = VSS	-10	4	40	µA

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

6.8.9 CSI-2 (D-PHY) Electrical Characteristics

注

CSIRX0 is compliant with MIPI DPHY v1.2 dated August 1, 2014, including ECNs and Errata as applicable.

6.8.10 DSI (D-PHY) Electrical Characteristics

注

DSITX0 is compliant with MIPI DPHY v1.2 dated August 1, 2014, including ECNs and Errata as applicable.

6.8.11 USB2PHY Electrical Characteristics

注

The USB0 and USB1 interfaces are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

6.8.12 DDR Electrical Characteristics

注

The DDR interface is compatible with LPDDR4 devices that are **JESD209-4B standard-compliant**

ADVANCE INFORMATION

6.9 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses .

6.9.1 Recommended Operating Conditions for OTP eFuse Programming

over operating junction temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD_CORE	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)		See セクション 6.5		V
VPP	Supply voltage range for the eFuse ROM domain during normal operation without hardware support to program eFuse ROM		NC(1)		V
	Supply voltage range for the eFuse ROM domain during normal operation with hardware support to program eFuse ROM		0		V
	Supply voltage range for the eFuse ROM domain during OTP programming(2)	1.71	1.8	1.89	V
$I_{(VPP)}$	VPP current			400	mA
$SR_{(VPP)}$	VPP Slew Rate			6E + 4	V/s
Tj	Operating junction temperature range while programming eFuse ROM.	0	25	85	°C

(1) NC indicates No Connect.
(2) Supply voltage range includes DC errors and peak-to-peak noise.

6.9.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-up sequence (for more details, see セクション 6.11.2.2, *Power Supply Sequencing*).

6.9.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP terminal according to the specification in セクション 6.9.1.
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP terminal.

6.9.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

ADVANCE INFORMATION

6.10 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in セクション 6.5, *Recommended Operating Conditions*.

6.10.1 Thermal Resistance Characteristics for AMH Package

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

NO.	PARAMETER	DESCRIPTION	AMH PACKAGE	
			°C/W(1) (3)	AIR FLOW (m/s)(2)
T1	$R\Theta_{JC}$	Junction-to-case	0.86	N/A
T2	$R\Theta_{JB}$	Junction-to-board	3.3	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	13.8	0
T4		Junction-to-moving air	8.8	1
T5			7.7	2
T6			7.2	3
T7	Ψ_{JT}	Junction-to-package top	0.50	0
T8			0.52	1
T9			0.53	2
T10			0.54	3
T11	Ψ_{JB}	Junction-to-board	3.2	0
T12			2.8	1
T13			2.7	2
T14			2.6	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [RΘJC] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.
(3) °C/W = degrees Celsius per watt.

ADVANCE INFORMATION

6.11 Timing and Switching Characteristics

注

The Timing Requirements and Switching Characteristics values may change following the silicon characterization result.

注

The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

6.11.1 Timing Parameters and Information

The timing parameter symbols used in セクション 6.11, *Timing and Switching Characteristics* are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in 表 6-3:

表 6-3. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

ADVANCE INFORMATION

6.11.2 Power Supply Requirements

This section describes the power supply requirements to ensure proper device operation.

注

All power balls must be supplied with the voltages specified in the *Recommended Operating Conditions* section, unless otherwise specified in *Signal Descriptions* and *Pin Connectivity Requirements*.

6.11.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 18 mV/µs. For instance, as shown in 図 6-2, TI recommends having the supply ramp slew for a 1.8-V supply of more than 100 µs.

図 6-2 describes the Power Supply Slew Rate Requirement in the device.

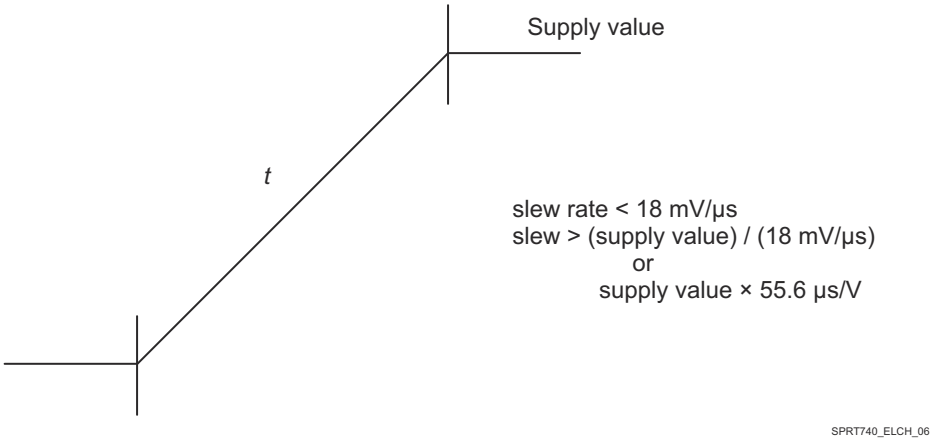


図 6-2. Power Supply Slew and Slew Rate

ADVANCE INFORMATION

6.11.2.2 Power Supply Sequencing

This section describes power sequence requirements using power sequence diagrams and associated notes. Each power sequence diagram demonstrates the sequential order expected for each device power rail. This is done by assigning each device power rail to one or more waveform. A dual-voltage power rail may be associated with more than one waveform and the associated note will describe which waveform is applicable. Each waveform defines a transition region for the associated power rails and shows its sequential relationship to the transition regions of other power rails. The notes associated with the power sequence diagram provides further detail of these requirements. See the *Power-up Sequence* section for details on power-up requirements, and the *Power-down Sequence* section for details on power-down requirements.

Two types of power supply transition regions are used to simplify the power supply sequencing diagrams. The legends shown in 図 6-3 and 図 6-4 along with their descriptions are provided to clarify what each transition regions represents.

図 6-3 defines a transition region with multiple power rails which may be sourced from multiple power supplies or a single power supply. Transitions shown within the transition region represent a use case where multiple power supplies are used to source power rails associated with this waveform, and these power supplies are allowed to ramp at different times within the region since they do not have any specific sequence requirement relative to each other.

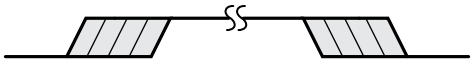


図 6-3. Multiple Power Supply Transition Legend

図 6-4 defines a transition region with one or more power rails which must be sourced from a single common power supply. No transitions are shown within the region to represent a single ramp within the transition region.

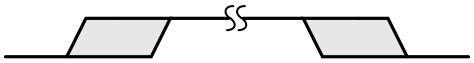


図 6-4. Single Common Power Supply Transition Legend

ADVANCE INFORMATION

6.11.2.2.1 Power-Up Sequencing

表 6-4 and 図 6-5 describes the device power-up sequencing.

注

The power supply sequencing requirements defined in this section does not include entry or exit from low power modes. See セクション 6.11.2.2.3, *Partial IO Power Sequencing* for more information on the requirements for entering or exiting from Partial IO low power mode.

表 6-4. Power-Up Sequencing – Supply / Signal Assignments

See: 図 6-5

WAVEFORM	SUPPLY / SIGNAL NAME
A	VSYS(1), VMON_VSYS(2)
B	VDDSHV_CANUART(3), VDDSHV_MCU(3), VDDSHV0(3), VDDSHV1(3), VDDSHV2(3), VDDSHV3(3), VDDA_3P3_USB, VMON_3P3_SOC(4)
C	VDDSHV_CANUART(5), VDDSHV_MCU(5), VDDSHV0(5), VDDSHV1(5), VDDSHV2(5), VDDSHV3(5), VDDS_MMC0, VDDA_MCU, VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_CSI_DSI, VDDA_1P8_OLDI0, VDDA_1P8_USB, VDDA_TEMP0, VDDA_TEMP1, VMON_1P8_SOC(6)
D	VDDSHV5(7), VDDSHV6(7)
E	VDDS_DDR(8), VDDS_DDR_C(8)
F	VDD_CANUART(9)
G	VDD_CANUART(10), VDD_CORE(10) (12), VDDA_CORE_CSI_DSI(10), VDDA_CORE_DSI_CLK(10), VDDA_CORE_USB0(10), VDDA_DDR_PLL0(10)
H	VDD_CANUART(11), VDD_CORE(11) (12), VDDA_CORE_CSI_DSI(11), VDDA_CORE_DSI_CLK(11), VDDA_CORE_USB0(11), VDDA_DDR_PLL0(11), VDDR_CORE(12), VDD_MMC0, VDDA_0P85_DLL_MMC0
I	VPP(13)
J	MCU_PORz
K	MCU_OSC0_XI, MCU_OSC0_XI

(1) VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.

(2) VMON_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see the セクション 8.2.4, *System Power Supply Monitor Design Guidelines*.

(3) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode, or connected to any valid IO power source when not using Partial IO low power mode. When VDDSHV_CANUART is not connected to an always-on power source and is operating at 3.3V, it shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.

When any of the VDDSHV_MCU and VDDSHVx [x=0-3] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.

(4) The VMON_3P3_SOC input is used to monitor supply voltage and shall be connected to the respective 3.3V supply source.

(5) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements.

VDDSHV_CANUART shall be connected to an always-on power source when using Partial IO low power mode, or connected to any valid IO power source when not using Partial IO low power mode. When VDDSHV_CANUART is not connected to an always-on power source and is operating at 1.8V, it shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.

When any of the VDDSHV_MCU and VDDSHVx [x=0-3] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.

(6) The VMON_1P8_SOC input is used to monitor supply voltage and shall be connected to the respective 1.8V supply source.

(7) VDDSHV5, and VDDSHV6 were designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

(8) VDDS_DDR and VDDS_DDR_C are expected to be powered by the same source such that they ramp together.

(9) VDD_CANUART shall be connected to an always-on power source when using Partial IO low power mode.

ADVANCE INFORMATION

When VDD_CANUART is connected to an always-on power source, the potential applied to VDD_CORE must never be greater than the potential applied to VDD_CANUART + 0.18V during power-up or power-down. This requires VDD_CANUART to ramp up before and ramp down after VDD_CORE. VDD_CANUART does not have any ramp requirements beyond the one defined for VDD_CORE.

(10) VDD_CANUART shall be connected to the same power source as VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 when not using Partial IO low power mode.

VDD_CANUART, VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 can be operated at 0.75V or 0.85V. When these supplies are operating at 0.75V, they shall be ramped up prior to VDDR_CORE as defined by this waveform.

(11) VDD_CANUART shall be connected to the same power source as VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 when not using Partial IO low power mode.

VDD_CANUART, VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 can be operated at 0.75V or 0.85V. When these supplies are operating at 0.85V, they shall be powered from the same source as VDDR_CORE and ramped during the 0.85V ramp period defined by this waveform.

(12) The potential applied to VDDR_CORE must never be greater than the potential applied to VDD_CORE + 0.18V during power-up or power-down. This requires VDD_CORE to ramp up before and ramp down after VDDR_CORE when VDD_CORE is operating at 0.75V. VDD_CORE does not have any ramp requirements beyond the one defined for VDDR_CORE.

VDD_CORE and VDDR_CORE are expected to be powered by the same source so they ramp together when VDD_CORE is operating at 0.85V.

(13) VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.

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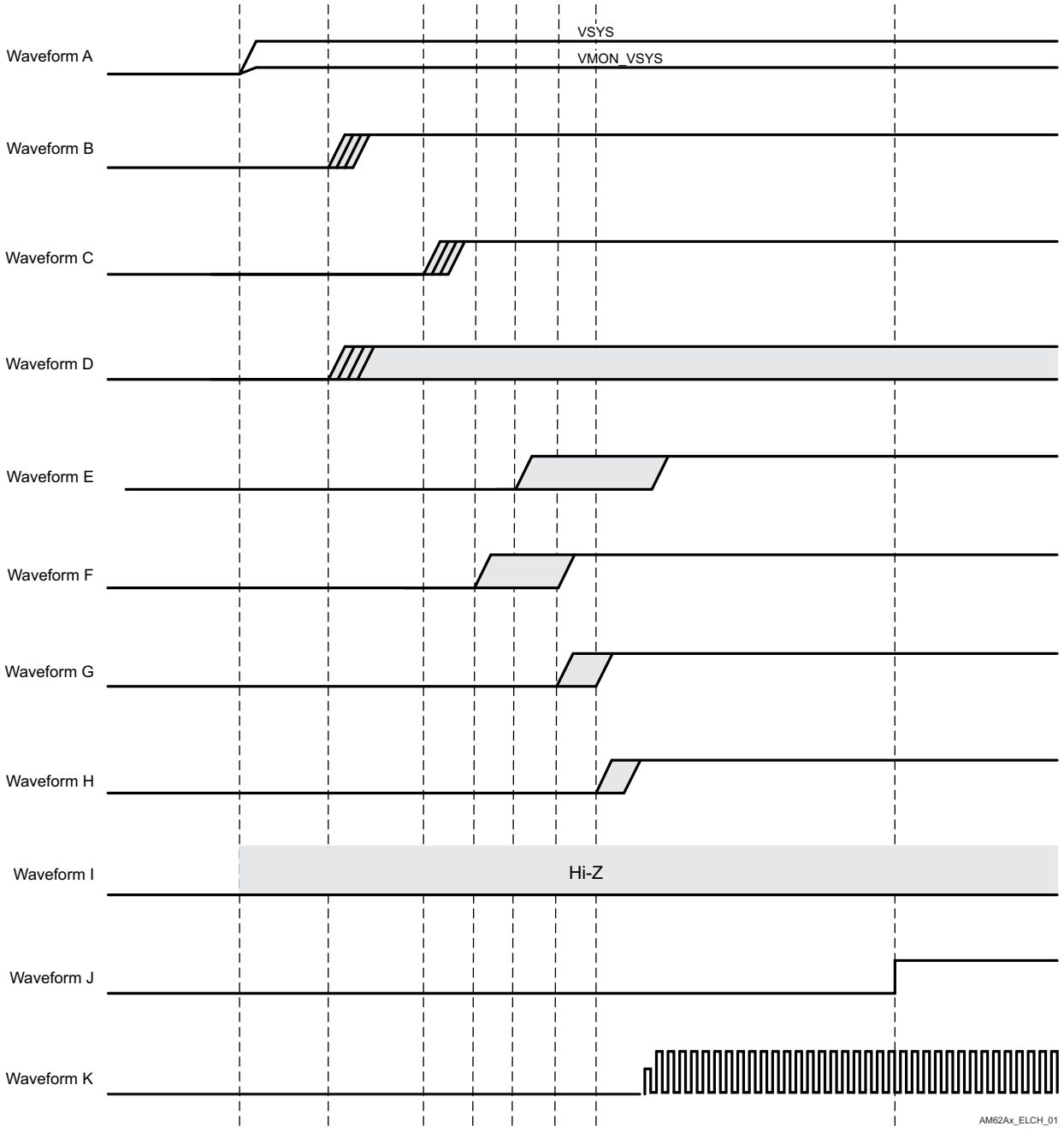

図 6-5. Power-Up Sequencing

6.11.2.2.2 Power-Down Sequencing

表 6-5 and 図 6-6 describes the device power-down sequencing.

注

The power supply sequencing requirements defined in this section does not include entry or exit from low power modes. See セクション 6.11.2.2.3, *Partial IO Power Sequencing* for more information on the requirements for entering or exiting from Partial IO low power mode.

表 6-5. Power-Down Sequencing – Supply / Signal Assignments

See: 図 6-6

WAVEFORM	SUPPLY / SIGNAL NAME
A	VSYS, VMON_VSYS
B	VDDSHV_CANUART(1), VDDSHV_MCU(1), VDDSHV0(1), VDDSHV1(1), VDDSHV2(1), VDDSHV3(1), VDDA_3P3_USB, VMON_3P3_SOC
C	VDDSHV_CANUART(2), VDDSHV_MCU(2), VDDSHV0(2), VDDSHV1(2), VDDSHV2(2), VDDSHV3(2), VDDS_MMC0, VDDA_MCU, VDDS_OSC0, VDDA_PLL0, VDDA_PLL1, VDDA_PLL2, VDDA_1P8_CSI_DSI, VDDA_1P8_OLDI0, VDDA_1P8_USB, VDDA_TEMP0, VDDA_TEMP1, VMON_1P8_SOC
D	VDDSHV5(3), VDDSHV6(3)
E	VDDS_DDR, VDDS_DDR_C
F	VDD_CANUART(4)
G	VDD_CANUART(5), VDD_CORE(5), VDDA_CORE_CSI_DSI(5), , VDDA_CORE_DSI_CLK(5), VDDA_CORE_USB0(5), VDDA_DDR_PLL0(5)
H	VDD_CANUART(6), VDD_CORE(6), VDDA_CORE_CSI_DSI(6), , VDDA_CORE_DSI_CLK(6), VDDA_CORE_USB0(6), VDDA_DDR_PLL0(6), VDDR_CORE, VDD_MMC0, VDDA_0P85_DLL_MMC0
I	VPP
J	MCU_PORz
K	MCU_OSC0_XI, MCU_OSC0_XI

(1) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] when operating at 3.3V.

(2) VDDSHV_CANUART, VDDSHV_MCU, and VDDSHVx [x=0-3] when operating at 1.8V.

(3) VDDSHV5, and VDDSHV6 were designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

(4) VDD_CANUART when connected to an always-on power source for Partial IO low power mode.

(5) VDD_CANUART, VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB0, and VDDA_DDR_PLL0 when operating at 0.75V

(6) VDD_CANUART, VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB0, and VDDA_DDR_PLL0 when operating at 0.85V

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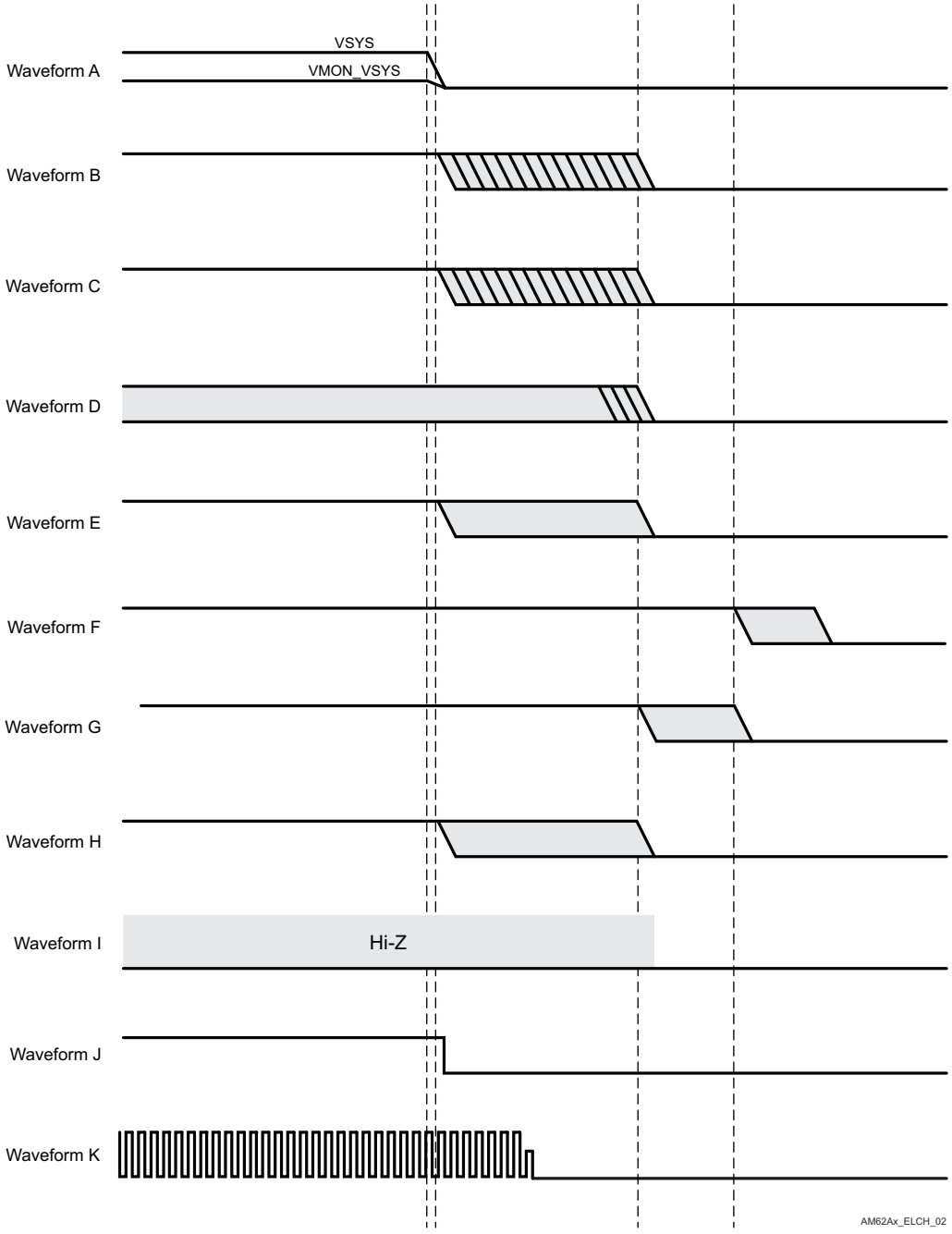


図 6-6. Power-Down Sequencing

6.11.2.2.3 Partial IO Power Sequencing

This section describes power supply sequence requirements when entering or exiting low power modes.

For more information on low power modes supported by this device and the names assigned to each low power mode, see the Power Modes section in the Device Configuration chapter of the Technical Reference Manual.

Partial IO is the only low power mode that requires power supply changes to the device power rails. All power supply rails except VDD_CANUART and VDDSHV_CANUART are turned off when operating in Partial IO mode. The power sequence required to enter Partial IO is the same sequence defined in セクション 6.11.2.2.2, *Power-Down Sequencing* with the exception of VDD_CANUART and VDDSHV_CANUART, which remain powered. The power sequence required to exit Partial IO is the same sequence defined in セクション 6.11.2.2.1, *Power-Up Sequencing* with the exception of VDD_CANUART and VDDSHV_CANUART, which are already powered.

6.11.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.11.3.1 Reset Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for reset related signals.

表 6-6. Reset Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8V	0.0018		V/ns
		VDD(1) = 3.3V	0.0033		V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance			30	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

表 6-7. MCU_PORz Timing Requirements

see 図 6-7

NO.	PARAMETER		MIN	MAX	UNIT
RST1	$t_{h(SUPPLIES\_VALID - MCU\_PORz)}$	Hold time, MCU_PORz active (low) at Power-up after supplies valid (using external crystal circuit)	9500000		ns
RST2		Hold time, MCU_PORz active (low) at Power-up after supplies valid and external clock stable (using external LVCMOS clock source)	1200		ns
RST3	$t_{w(MCU\_PORzL)}$	Pulse Width, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)	1200		ns

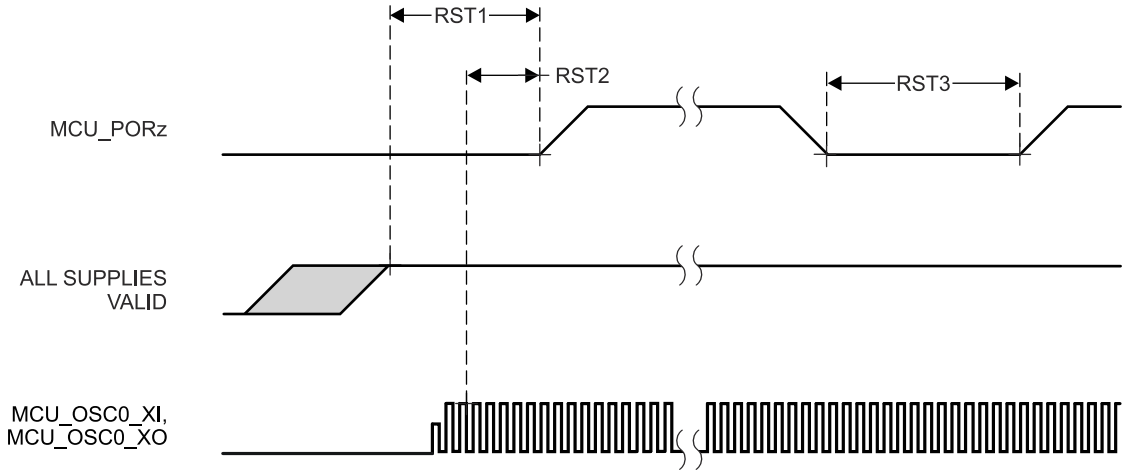


図 6-7. MCU_PORz Timing Requirements

ADVANCE INFORMATION

表 6-8. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see 図 6-8

NO.	PARAMETER		MIN	MAX	UNIT
RST4	$t_{d(MCU\_PORzL-MCU\_RESETSTATzL)}$	Delay time, MCU_PORz active (low) to MCU_RESETSTATz active (low)	0		ns
RST5	$t_{d(MCU\_PORzH-MCU\_RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to MCU_RESETSTATz inactive (high)	6120*S(1)		ns
RST6	$t_{d(MCU\_PORzL-RESETSTATzL)}$	Delay time, MCU_PORz active (low) to RESETSTATz active (low)	0		ns
RST7	$t_{d(MCU\_PORzH-RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)	9195*S(1)		ns
RST8	$t_{w(MCU\_RESETSTATzL)}$	Pulse Width, MCU_RESETSTATz low (SW_MCU_WARMRST)	966*S(1)		ns
RST9	$t_{w(RESETSTATzL)}$	Pulse Width, RESETSTATz low (SW_MCU_WARMRST, SW_MAIN_PORz, or SW_MAIN_WARMRST)	4040*S		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

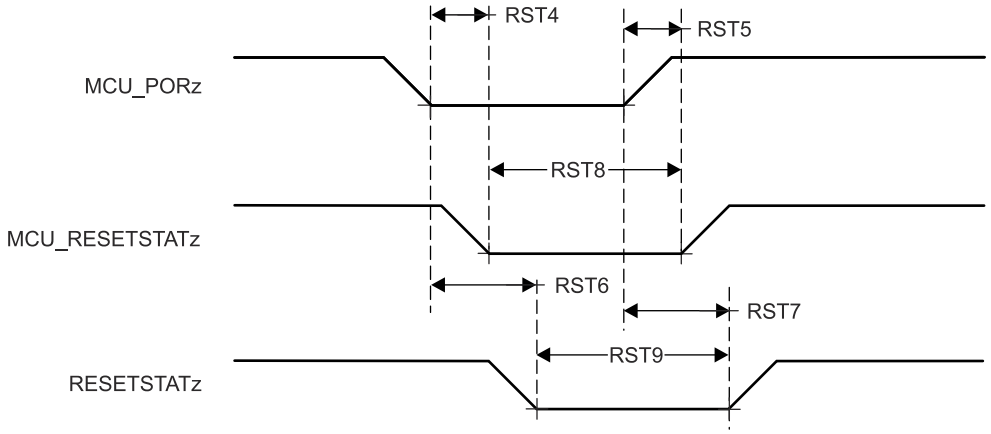


図 6-8. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

ADVANCE INFORMATION

表 6-9. MCU_RESETz Timing Requirements

see 図 6-9

NO.	PARAMETER		MIN	MAX	UNIT
RST10	$t_{w(MCU\_RESETzL)}$ (1)	Pulse Width, MCU_RESETz active (low)	1200		ns

(1) This timing parameter is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

表 6-10. MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see 図 6-9

NO.	PARAMETER		MIN	MAX	UNIT
RST11	$t_{d(MCU\_RESETzL-MCU\_RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)	0		ns
RST12	$t_{d(MCU\_RESETzH-MCU\_RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high)	966*S(1)		ns
RST13	$t_{d(MCU\_RESETzL-RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to RESETSTATz active (low)	960		ns
RST14	$t_{d(MCU\_RESETzH-RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)	4040*S(1)		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

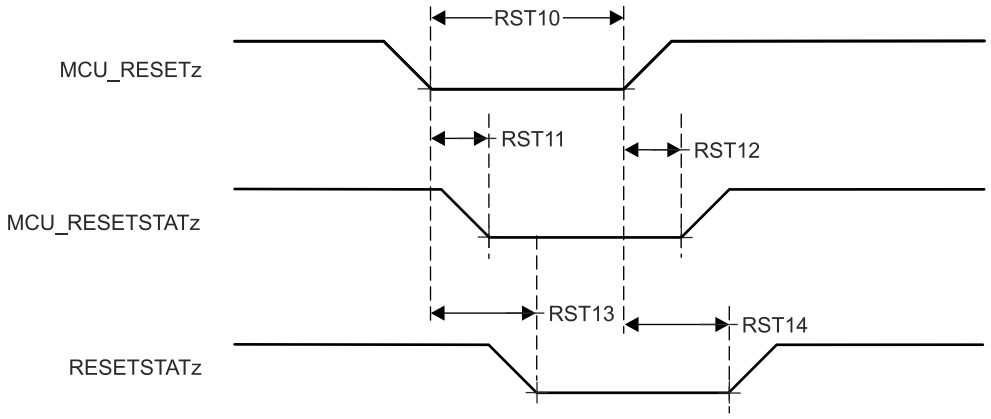


図 6-9. MCU_RESETz, MCU_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics

表 6-11. RESET_REQz Timing Requirements

see 図 6-10

NO.	PARAMETER		MIN	MAX	UNIT
RST15	$t_{w(RESET\_REQzL)}$ (1)	Pulse Width, RESET_REQz active (low)	1200		ns

(1) This timing parameter is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

表 6-12. RESETSTATz Switching Characteristics

see 図 6-10

NO.	PARAMETER		MIN	MAX	UNIT
RST16	$t_{d(RESET\_REQzL-RESETSTATzL)}$	Delay time, RESET_REQz active (low) to RESETSTATz active (low)	900*T(1)		ns
RST17	$t_{d(RESET\_REQzH-RESETSTATzH)}$	Delay time, RESET_REQz inactive (high) to RESETSTATz inactive (high)	4040*S(2)		ns

(1) T = Reset Isolation Time (Software Dependent)
(2) S = MCU_OSC0_XI/XO clock period in ns.

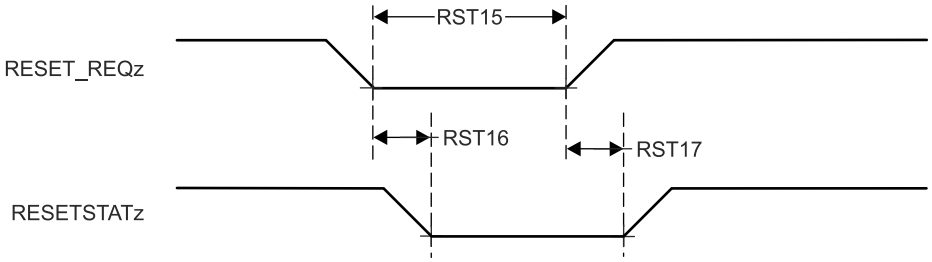


図 6-10. RESET_REQz and RESETSTATz Timing Requirements and Switching Characteristics

表 6-13. EMUx Timing Requirements

see 図 6-11

NO.	PARAMETER		MIN	MAX	UNIT
RST18	$t_{su(EMUx-MCU\_PORz)}$	Setup time, EMU[1:0] before MCU_PORz inactive (high)	3*S(1)		ns
RST19	$t_{h(MCU\_PORz - EMUx)}$	Hold time, EMU[1:0] after MCU_PORz inactive (high)	10		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

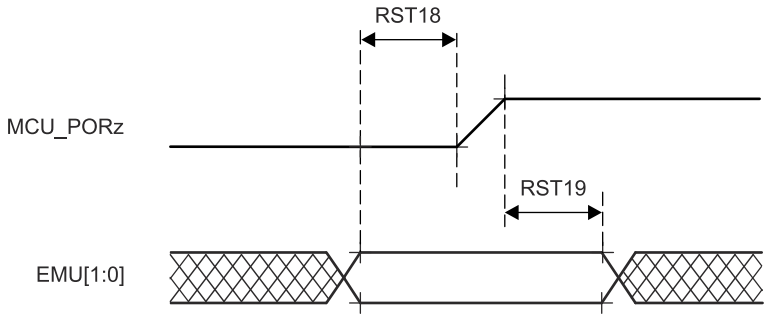


図 6-11. EMUx Timing Requirements

ADVANCE INFORMATION

表 6-14. BOOTMODE Timing Requirements

see 図 6-12

NO.	PARAMETER		MIN	MAX	UNIT
RST23	$t_{su(BOOTMODE-PORz\_OUT)}$	Setup time, BOOTMODE[15:00] before PORz_OUT high (External MCU PORz event or Software SW_MAIN_PORz)	3*S(1)		ns
RST24	$t_{h(PORz\_OUT - BOOTMODE)}$	Hold time, BOOTMODE[15:00] after PORz_OUT high (External MCU PORz event, or Software SW_MAIN_PORz)	0		ns

(1) S = MCU_OSC0_XI/XO clock period in ns.

表 6-15. PORz_OUT Switching Characteristics

see 図 6-12

NO.	PARAMETER		MIN	MAX	UNIT
RST25	$t_{d(MCU\_PORzL-PORz\_OUT)}$	Delay time, MCU_PORz active (low) to PORz_OUT active (low)	0		ns
RST26	$t_{d(MCU\_PORzH-PORz\_OUT)}$	Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high)	1840		ns
RST27	$t_{w(PORz\_OUTL)}$	Pulse Width, PORz_OUT low (MCU_PORz or SW_MAIN_PORz)	1200		ns

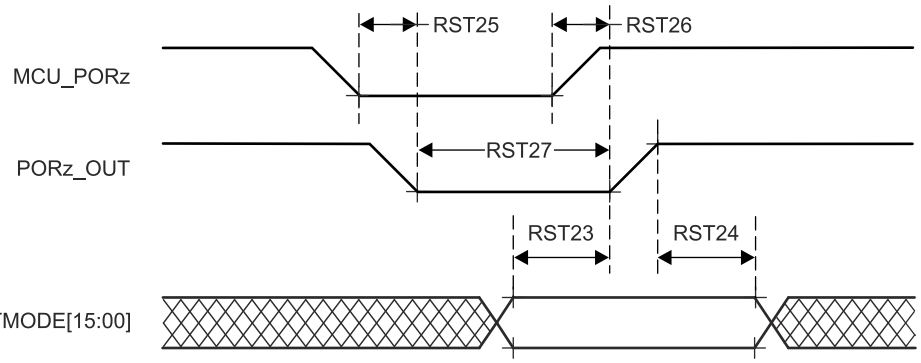


図 6-12. BOOTMODE Timing Requirements and PORz_OUT Switching Characteristics

6.11.3.2 Error Signal Timing

Tables and figures provided in this section define timing conditions and switching characteristics for MCU_ERRORn.

表 6-16. Error Signal Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance		30	pF

表 6-17. MCU_ERRORn Switching Characteristics

see 図 6-13

NO.	PARAMETER		MIN	MAX	UNIT
ERR1	$t_{c(MCU\_ERRORn)}$	Cycle time minimum, MCU_ERRORn (PWM mode enabled)	(P*H)+(P*L)(1) (3) (4)		ns
ERR2	$t_{w(MCU\_ERRORn)}$	Pulse width minimum, MCU_ERRORn active (PWM mode disabled)(5)	P*R(1) (2)		ns
ERR3	$t_{d\ (ERROR\_CONDITION-MCU\_ERRORnL)}$	Delay time, ERROR CONDITION to MCU_ERRORn active(5)	50*P(1)		ns

(1) P = ESM functional clock period in ns.
(2) R = Error Pin Counter Pre-Load Register count value.
(3) H = Error Pin PWM High Pre-Load Register count value.
(4) L = Error Pin PWM Low Pre-Load Register count value.
(5) When PWM mode is enabled, MCU_ERRORn stops toggling after ERR3 and will maintain its value (either high or low) until the error is cleared. When PWM mode is disabled, MCU_ERRORn is active low.

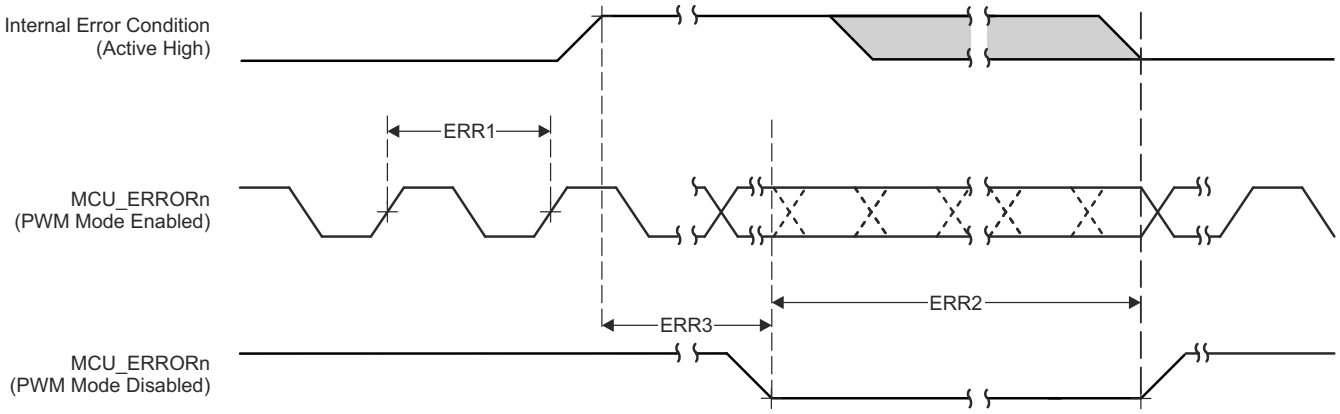


図 6-13. MCU_ERRORn Timing Requirements and Switching Characteristics

ADVANCE INFORMATION

6.11.3.3 Clock Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for clock signals.

表 6-18. Clock Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		0.5		V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	5 ns ≤ t_c < 8 ns		5	pF
		8 ns ≤ t_c < 20 ns		10	pF
		20 ns ≤ t_c		30	pF

表 6-19. Clock Timing Requirements

see 図 6-14

NO.			MIN	MAX	UNIT
CLK1	$t_{c(EXT\_REFCLK1)}$	Cycle time minimum, EXT_REFCLK1	10		ns
CLK2	$t_{w(EXT\_REFCLK1H)}$	Pulse Duration, EXT_REFCLK1 high	E*0.45(1)	E*0.55(1)	ns
CLK3	$t_{w(EXT\_REFCLK1L)}$	Pulse Duration, EXT_REFCLK1 low	E*0.45(1)	E*0.55(1)	ns
CLK1	$t_{c(MCU\_EXT\_REFCLK0)}$	Cycle time minimum, MCU_EXT_REFCLK0	10		ns
CLK2	$t_{w(MCU\_EXT\_REFCLK0H)}$	Pulse Duration, MCU_EXT_REFCLK0 high	F*0.45(2)	F*0.55(2)	ns
CLK3	$t_{w(MCU\_EXT\_REFCLK0L)}$	Pulse Duration, MCU_EXT_REFCLK0 low	F*0.45(2)	F*0.55(2)	ns
CLK1	$t_{c(AUDIO\_EXT\_REFCLK0)}$	Cycle time minimum, AUDIO_EXT_REFCLK0	20		ns
CLK2	$t_{w(AUDIO\_EXT\_REFCLK0H)}$	Pulse Duration, AUDIO_EXT_REFCLK0 high	G*0.45(3)	G*0.55(3)	ns
CLK3	$t_{w(AUDIO\_EXT\_REFCLK0L)}$	Pulse Duration, AUDIO_EXT_REFCLK0 low	G*0.45(3)	G*0.55(3)	ns
CLK1	$t_{c(AUDIO\_EXT\_REFCLK1)}$	Cycle time minimum, AUDIO_EXT_REFCLK1	20		ns
CLK2	$t_{w(AUDIO\_EXT\_REFCLK1H)}$	Pulse Duration, AUDIO_EXT_REFCLK1 high	H*0.45(4)	H*0.55(4)	ns
CLK3	$t_{w(AUDIO\_EXT\_REFCLK1L)}$	Pulse Duration, AUDIO_EXT_REFCLK1 low	H*0.45(4)	H*0.55(4)	ns

(1) E = EXT_REFCLK1 cycle time in ns.
(2) F = MCU_EXT_REFCLK0 cycle time in ns.
(3) G = AUDIO_EXT_REFCLK0 cycle time in ns.
(4) H = AUDIO_EXT_REFCLK1 cycle time in ns.

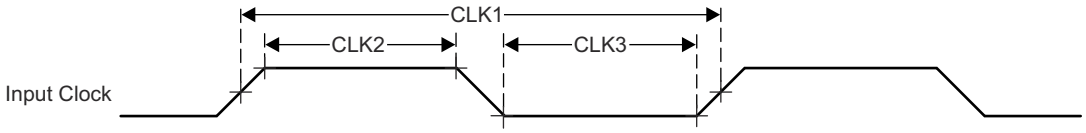


図 6-14. Clock Timing Requirements

ADVANCE INFORMATION

表 6-20. Clock Switching Characteristics

see 図 6-15

NO.	PARAMETER		MIN	MAX	UNIT
CLK4	$t_{c(SYSCLKOUT0)}$	Cycle time minimum,SYSCLKOUT0	8		ns
CLK5	$t_{w(SYSCLKOUT0H)}$	Pulse Duration, SYSCLKOUT0 high	A*0.4(1)	A*0.6(1)	ns
CLK6	$t_{w(SYSCLKOUT0L)}$	Pulse Duration, SYSCLKOUT0 low	A*0.4(1)	A*0.6(1)	ns
CLK4	$t_{c(OBSCLK0)}$	Cycle time minimum, OBSCLK0	5		ns
CLK5	$t_{w(OBSCLK0H)}$	Pulse Duration, OBSCLK0 high	B*0.45(2)	B*0.55(2)	ns
CLK6	$t_{w(OBSCLK0L)}$	Pulse Duration, OBSCLK0 low	B*0.45(2)	B*0.55(2)	ns
CLK4	$t_{c(OBSCLK1)}$	Cycle time minimum, OBSCLK1	5		ns
CLK5	$t_{w(OBSCLK1H)}$	Pulse Duration, OBSCLK1 high	F*0.45(3)	F*0.55(3)	ns
CLK6	$t_{w(OBSCLK1L)}$	Pulse Duration, OBSCLK1 low	F*0.45(3)	F*0.55(3)	ns
CLK4	$t_{c(CLKOUT0)}$	Cycle time minimum, CLKOUT0	20		ns
CLK5	$t_{w(CLKOUT0H)}$	Pulse Duration, CLKOUT0 high	C*0.4(4)	C*0.6(4)	ns
CLK6	$t_{w(CLKOUT0L)}$	Pulse Duration, CLKOUT0 low	C*0.4(4)	C*0.6(4)	ns
CLK4	$t_{c(MCU\_SYSCLKOUT0)}$	Cycle time minimum, MCU_SYSCLKOUT0	10		ns
CLK5	$t_{w(MCU\_SYSCLKOUT0H)}$	Pulse Duration, MCU_SYSCLKOUT0 high	E*0.4(5)	E*0.6(5)	ns
CLK6	$t_{w(MCU\_SYSCLKOUT0L)}$	Pulse Duration, MCU_SYSCLKOUT0 low	E*0.4(5)	E*0.6(5)	ns
CLK4	$t_{c(MCU\_OBSCLK0)}$	Cycle time minimum, MCU_OBSCLK0	5		ns
CLK5	$t_{w(MCU\_OBSCLK0H)}$	Pulse Duration, MCU_OBSCLK0 high	D*0.45(6)	D*0.55(6)	ns
CLK6	$t_{w(MCU\_OBSCLK0L)}$	Pulse Duration, MCU_OBSCLK0 low	D*0.45(6)	D*0.55(6)	ns
CLK4	$t_{c(WKUP\_CLKOUT0)}$	Cycle time minimum, WKUP_CLKOUT0	5		ns
CLK5	$t_{w(WKUP\_CLKOUT0H)}$	Pulse Duration, WKUP_CLKOUT0 high	W*0.4(7)	W*0.6(7)	ns
CLK6	$t_{w(WKUP\_CLKOUT0L)}$	Pulse Duration, WKUP_CLKOUT0 low	W*0.4(7)	W*0.6(7)	ns
CLK4	$t_{c(AUDIO\_EXT\_REFCLK0)}$	Cycle time minimum, AUDIO_EXT_REFCLK0 (McASP Clock Source)	20		ns
		Cycle time minimum, AUDIO_EXT_REFCLK0 (PLL Clock Source)	10		ns
CLK5	$t_{w(AUDIO\_EXT\_REFCLK0\ H)}$	Pulse Duration, AUDIO_EXT_REFCLK0 high	G*0.4(8)	G*0.6(8)	ns
CLK6	$t_{w(AUDIO\_EXT\_REFCLK0\ L)}$	Pulse Duration, AUDIO_EXT_REFCLK0 low	G*0.4(8)	G*0.6(8)	ns
CLK4	$t_{c(AUDIO\_EXT\_REFCLK1)}$	Cycle time minimum, AUDIO_EXT_REFCLK1 (McASP Clock Source)	20		ns
		Cycle time minimum, AUDIO_EXT_REFCLK1 (PLL Clock Source)	10		ns
CLK5	$t_{w(AUDIO\_EXT\_REFCLK1\ H)}$	Pulse Duration, AUDIO_EXT_REFCLK1 high	J*0.4(9)	J*0.6(9)	ns
CLK6	$t_{w(AUDIO\_EXT\_REFCLK1\ L)}$	Pulse Duration, AUDIO_EXT_REFCLK1 low	J*0.4(9)	J*0.6(9)	ns

(1) A = SYSCLKOUT0 cycle time in ns.
(2) B = OBSCLK0 cycle time in ns.
(3) F = OBSCLK1 cycle time in ns.
(4) C = CLKOUT0 cycle time in ns.
(5) E = MCU_SYSCLKOUT0 cycle time in ns.
(6) D = MCU_OBSCLK0 cycle time in ns.
(7) W = WKUP_CLKOUT0 cycle time in ns.
(8) G = AUDIO_EXT_REFCLK0 cycle time in ns.
(9) J = AUDIO_EXT_REFCLK1 cycle time in ns.

ADVANCE INFORMATION

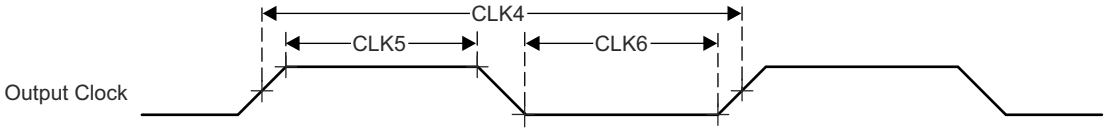


図 6-15. Clock Switching Characteristics

6.11.4 Clock Specifications

6.11.4.1 Input Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- MCU_OSC0_XO/MCU_OSC0_XI — external main crystal interface pins connected to the internal high-frequency oscillator (MCU_HFOSC0), which is the default clock source for internal reference clock HFOSC0_CLKOUT.
- WKUP_LFOSC0_XO/WKUP_LFOSC0_XI — external crystal interface pins connected to internal low-frequency oscillator (WKUP_LFOSC0), which sources optional 32768 Hz reference clock.
- General purpose clock inputs
  - MCU_EXT_REFCLK0 — optional external system clock.
  - EXT_REFCLK1 — optional external system clock.
- External CPTS reference clock input
  - CP_GEMAC_CPTS0_RFT_CLK — optional reference clock input for CPTS_RFT_CLK.
- External audio reference clock inputs/outputs
  - AUDIO_EXT_REFCLK[1:0] — optional McASP high-frequency input clocks when configured to operate as an input.

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

ADVANCE INFORMATION

6.11.4.1.1 MCU_OSC0 Internal Oscillator Clock Source

図 6-16 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit must be placed as close as possible to the MCU_OSC0_XI and MCU_OSC0_XO pins.

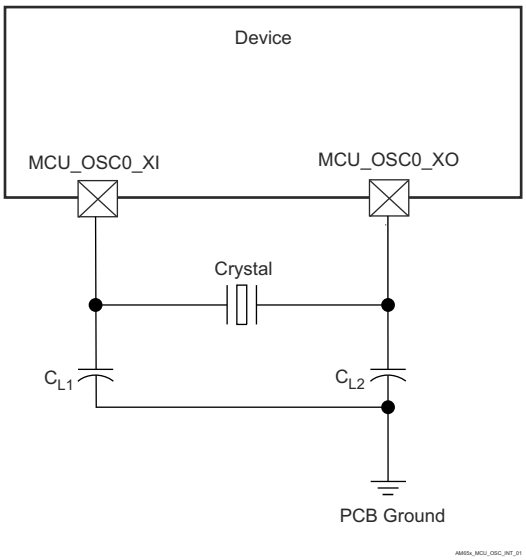


図 6-16. MCU_OSC0 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. 表 6-21 summarizes the required electrical constraints.

表 6-21. MCU_OSC0 Crystal Circuit Requirements

PARAMETER				MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency				25		MHz
F_{xtal}	Crystal Frequency Stability and Tolerance		Ethernet RGMII and RMII not used			±100	ppm
			Ethernet RGMII and RMII using derived clock			±50	
$C_{L1+PCBXI}$	Capacitance of C_{L1} + C_{PCBXI}			12		24	pF
$C_{L2+PCBXO}$	Capacitance of C_{L2} + C_{PCBXO}			12		24	pF
C_L	Crystal Load Capacitance			6		12	pF
C_{shunt}	Crystal Circuit Shunt Capacitance	ESR_{xtal} = 30 Ω	25 MHz			7	pF
		ESR_{xtal} = 40 Ω	25 MHz			5	pF
		ESR_{xtal} = 50 Ω	25 MHz			5	pF
ESR_{xtal}	Crystal Effective Series Resistance					(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

When selecting a crystal, the system design must consider temperature and aging characteristics of the crystal based on worst case environment and expected life expectancy of the system.

表 6-22 details the switching characteristics of the oscillator.

表 6-22. MCU_OSC0 Switching Characteristics - Crystal Mode

PARAMETER		MIN	TYP	MAX	UNIT
C_{XI}	XI Capacitance			1.58	pF
C_{XO}	XO Capacitance			1.49	pF
C_{XIXO}	XI to XO Mutual Capacitance			0.01	pF

ADVANCE INFORMATION

表 6-22. MCU_OSC0 Switching Characteristics - Crystal Mode (続き)

PARAMETER		MIN	TYP	MAX	UNIT
t_s	Start-up Time		4		ms

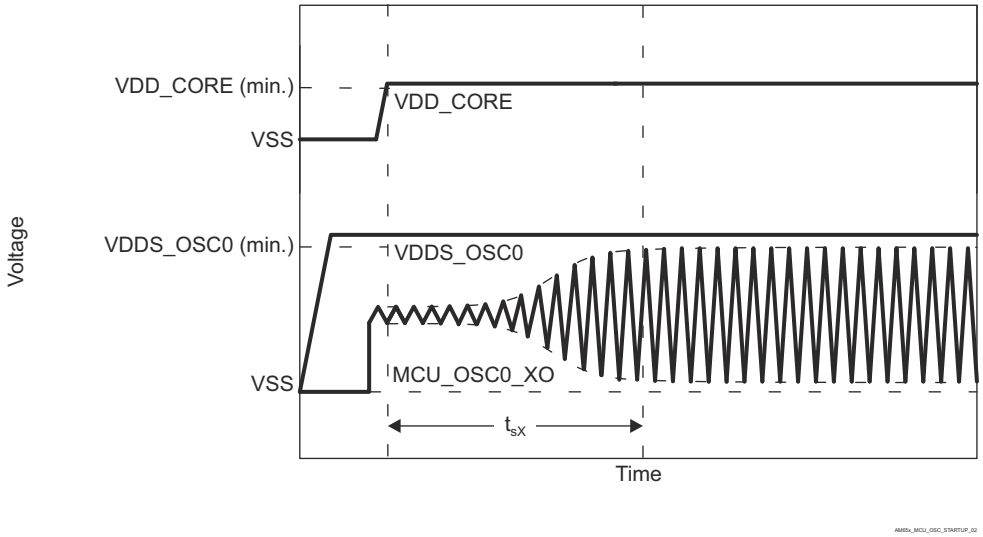


図 6-17. MCU_OSC0 Start-up Time

6.11.4.1.1.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C_L, of this circuit is a combination of discrete capacitors C_{L1}, C_{L2}, and several parasitic contributions. PCB signal traces which connect crystal circuit components to MCU_OSC0_XI and MCU_OSC0_XO have parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where the PCB designer should be able to extract parasitic capacitance for each signal trace. The MCU_OSC0 circuits and device package have combined parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where these parasitic capacitance values are defined in 表 6-22.

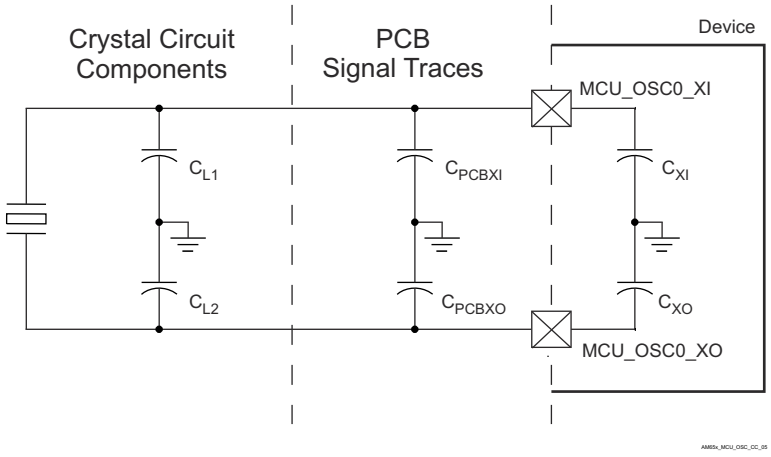


図 6-18. Load Capacitance

Load capacitors, C_{L1} and C_{L2} in 図 6-16, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of C_{L1} and C_{L2}, multiply the capacitive load value C_L by 2. Using this result, subtract the combined values of C_{PCBXI} + C_{XI} to determine the value of C_{L1} and the combined values of C_{PCBXO} + C_{XO} to determine the value of C_{L2}. For example, if C_L = 10 pF, C_{PCBXI} = 2.9 pF, C_{XI} = 0.5 pF, C_{PCBXO} = 3.7 pF, C_{XO} = 0.5 pF, the value of C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 × 10 pF) - 2.9 pF - 0.5 pF)] = 16.6 pF and C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 × 10 pF) - 3.7 pF - 0.5 pF)] = 15.8 pF

6.11.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for MCU_OSC0 operating conditions defined in 表 6-21. Shunt capacitance, C_{shunt}, of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to MCU_OSC0 have mutual parasitic capacitance to each other, $C_{PCBXIXO}$, where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance, C_{XIXO}, where this mutual parasitic capacitance value is defined in 表 6-22.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

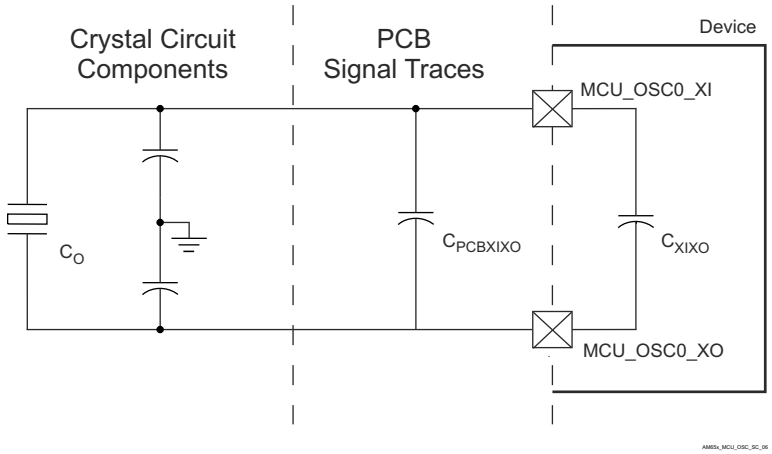


図 6-19. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied. C_O in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30 Ω, $C_{PCBXIXO}$ = 0.04 pF, C_{XIXO} = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

ADVANCE INFORMATION

6.11.4.1.2 MCU_OSC0 LVCMOS Digital Clock Source

図 6-20 shows the recommended oscillator connections when MCU_OSC0_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

注

A DC steady-state condition is not allowed on MCU_OSC0_XI when the oscillator is powered up. This is not allowed because MCU_OSC0_XI is internally AC coupled to a comparator that can enter an unknown state when DC is applied to the input. Therefore, application software must power down MCU_OSC0 any time MCU_OSC0_XI is not toggling between logic states.

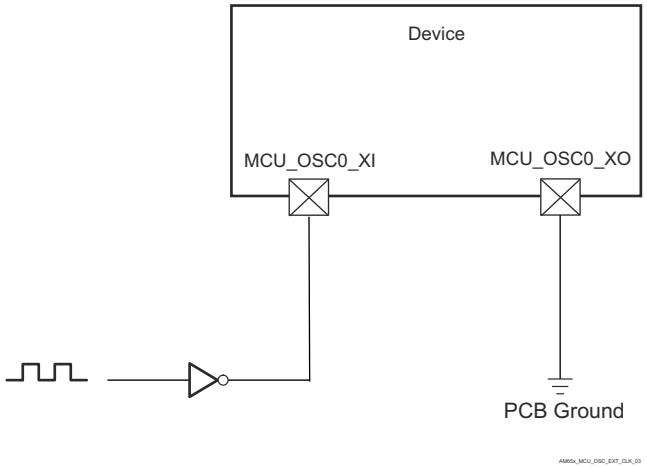


図 6-20. 1.8-V LVCMOS-Compatible Clock Input

6.11.4.1.3 WKUP_LFOSC0 Internal Oscillator Clock Source

図 6-21 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors R_{bias} and R_d in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, R_{bias} is not required and R_d is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

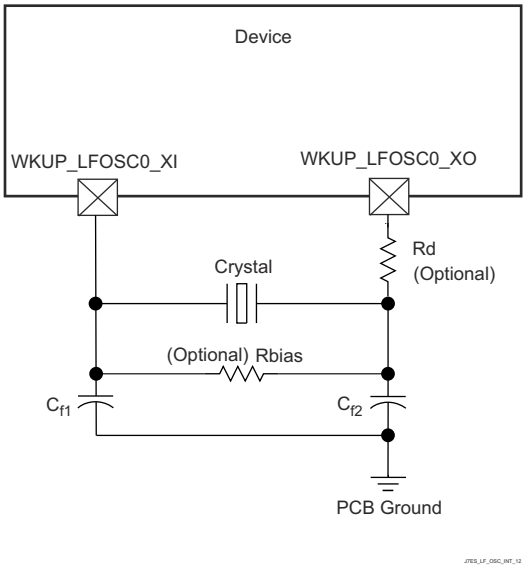


図 6-21. WKUP_LFOSC0 Crystal Implementation

表 6-23 presents LFXOSC modes of operation.

表 6-23. LFXOSC Modes of Operation

MODE	BP_C	PD_C	XI	XO	CLK_OUT	DESCRIPTION
ACTIVE	0	0	XTAL	XTAL	CLK_OUT	Active oscillator mode providing 32kHz
PWRDN	0	1	X	PD	LOW	Output will be pulled down to LOW. PAD to be tri-stated. Active mode disabled
BYPASS	1	0	CLK	PD	CLK	XI is driven by external clock source. XO is pulled down to LOW. Due to ESD diode to supply, XI should not be driven unless oscillator supply is present.

注

User should set CTRLMMR_WKUP_LFXOSC_TRIM[18:16] i_mult = 3b’001 for CL in the range 6pf to 9.5pf. CTRLMMR_WKUP_LFXOSC_TRIM [18:16] i_mult = 3b’010 for CL in the range 8.5pf to 12pf. Default setting is 3b’010.

注

The load capacitors, C_{f1} and C_{f2} in 図 6-22, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator WKUP_LFOSC0_XI, WKUP_LFOSC0_XO, and VSS pins.

ADVANCE INFORMATION

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

JTES_CL_MATH_03

図 6-22. Load Capacitance Equation

The crystal must be in the fundamental mode of operation and parallel resonant. 表 6-24 summarizes the required electrical constraints.

表 6-24. WKUP_LFOSC0 Crystal Electrical Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency			32768		Hz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{shunt}	Shunt capacitance	ESRxtal – 40 kΩ			4	pF
		ESRxtal – 60 kΩ			3	pF
		ESRxtal – 80 kΩ			2	pF
		ESRxtal – 100 kΩ			1	pF
ESR	Crystal effective series resistance				(1)	Ω

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C_{shunt} parameter.

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

表 6-25 details the switching characteristics of the oscillator and the requirements of the input clock.

表 6-25. WKUP_LFOSC0 Switching Characteristics – Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_{xtal}	Oscillation frequency		32768		Hz
t_{sX}	Start-up time			96.5	ms

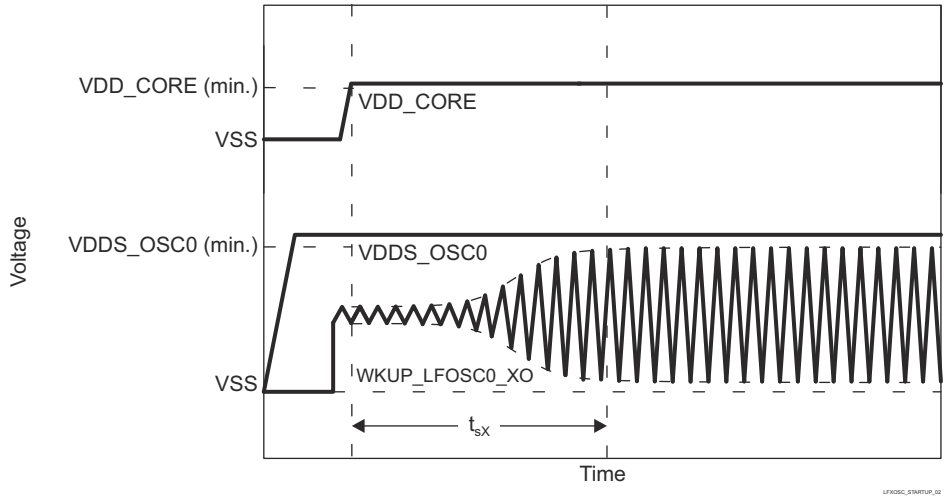


図 6-23. WKUP_LFOSC0 Start-up Time

6.11.4.1.4 WKUP_LFOSC0 LVCMOS Digital Clock Source

図 6-24 shows the recommended oscillator connections when WKUP_LFOSC0_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

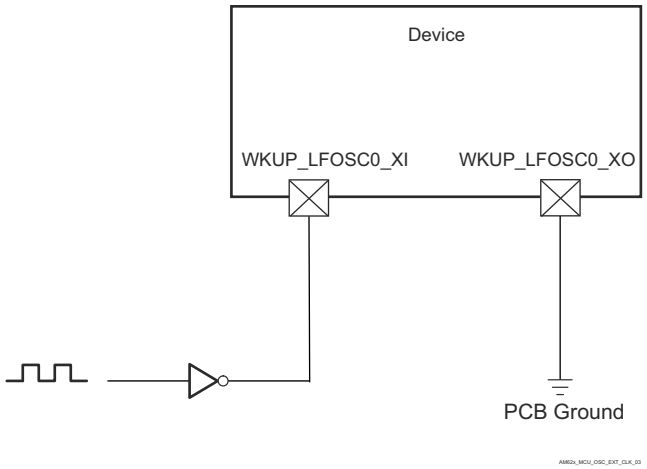


図 6-24. 1.8-V LVCMOS-Compatible Clock Input

6.11.4.1.5 WKUP_LFOSC0 Not Used

図 6-25 shows the recommended oscillator connections when WKUP_LFOSC0 is not used.

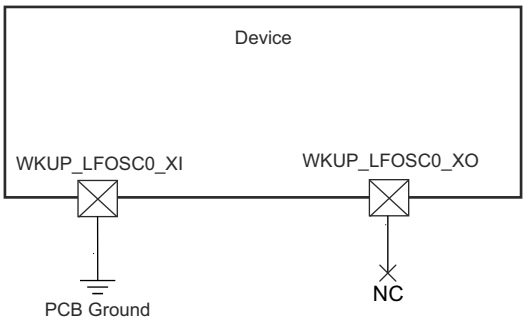


図 6-25. WKUP_LFOSC0 Not Used

ADVANCE INFORMATION

6.11.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU_SYSCLKOUT0**
  - MCU_PLL0_HSDIV0_CLKOUT (MCU_SYSCLKOUT0) divided by 4 and sent out of the device as MCU_SYSCLKOUT0. This clock output is provided for test and debug purposes only.
- **MCU_OBSCLK0**
  - Observation clock output for test and debug purposes only.
- **WKUP_CLKOUT0**
  - WKUP domain CLKOUT0 output.
- **SYSCLKOUT0**
  - MAIN_PLL0_HSDIV0_CLKOUT (SYSCLKOUT0) divided by 4 and then sent out of the device as SYSCLKOUT0. This clock output is provided for test and debug purposes only.
- **CLKOUT0**
  - CLKOUT0 is the Ethernet subsystem clock (MAIN_PLL2_HSDIV1_CLKOUT) divided-by-5 or divided-by-10. This clock output was provided as an optional source to the external PHY. When configured to operate as the RMII Clock source (50 MHz) the signal must also be routed back to the respective RMII[x]_REF_CLK pin for proper device operation.
- **OBSCLK[1:0]**
  - Observation clock outputs for test and debug purposes only.
- **AUDIO_EXT_REFCLK[1:0]**
  - Option of sourcing one of six McASP high-frequency audio reference clocks, MAIN_PLL1_HSDIV6_CLKOUT, or MAIN_PLL2_HSDIV8_CLKOUT when configured to operate as an output.

6.11.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuits (PLLs) by internal regulators that derive their power from off-chip power-sources.

There is one PLL in the MCU domain:

- MCU PLL

There are nine PLLs in the MAIN domain:

- MAIN PLL
- PER0 PLL
- PER1 PLL
- GPU PLL
- ARM0 PLL
- DDR PLL
- SMS PLL
- DSS PLL0
- DSS PLL1
- DSS PLL2

The system designer should consider the reference clock source start-up time and the PLL lock requirements before configuring and using any of the PLL outputs as clock sources. The device reference clock input requirements are defined in セクション 6.11.4.1, *Input Clocks / Oscillators*. PLL configuration details are described in the device TRM.

For more information on PLLs, see the *PLL* subsection in the *Clocking* subsection of the *Device Configuration* section in the device TRM.

6.11.4.4 Recommended System Precautions for Clock and Control Signal Transitions

All clock and strobe signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Monotonic transitions are more likely to occur with fast signal transitions. It is easy for noise to create non-monotonic events on a signal with slow transitions. Therefore, avoid slow signal transitions on all clock and control signals since they are more likely to generate glitches inside the device.

6.11.5 Peripherals

6.11.5.1 CPSW3G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.11.5.1.1 CPSW3G MDIO Timing

表 6-26, 表 6-27, 表 6-28, and 図 6-26 present timing conditions, requirements, and switching characteristics for CPSW3G MDIO.

表 6-26. CPSW3G MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	10	470	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	0	5	ns
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		1	ns

表 6-27. CPSW3G MDIO Timing Requirements

see 図 6-26

NO.	PARAMETER		MIN	MAX	UNIT
MDIO1	$t_{su(MDIO\_MDC)}$	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	45		ns
MDIO2	$t_{h(MDC\_MDIO)}$	Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high	0		ns

表 6-28. CPSW3G MDIO Switching Characteristics

see 図 6-26

NO.	PARAMETER		MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse Duration, MDIO[x]_MDC high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse Duration, MDIO[x]_MDC low	160		ns
MDIO7	$t_{d(MDC\_MDIO)}$	Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid	-10	10	ns

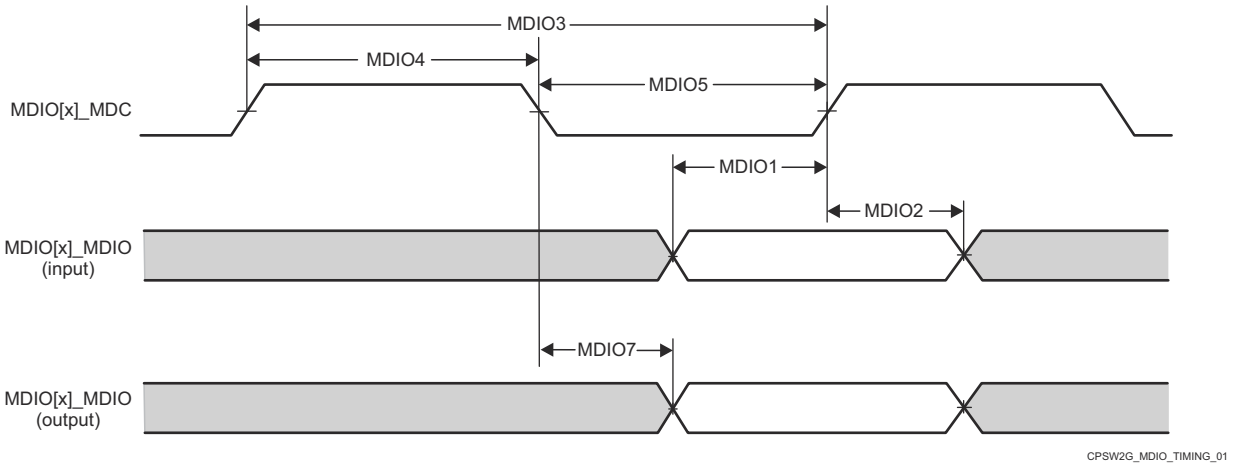


図 6-26. CPSW3G MDIO Timing Requirements and Switching Characteristics

6.11.5.1.2 CPSW3G RMII Timing

表 6-29, 表 6-30, 図 6-27, 表 6-31, 図 6-28, 表 6-32, and 図 6-29 present timing conditions, requirements, and switching characteristics for CPSW3G RMII.

表 6-29. CPSW3G RMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDD(1) = 1.8V	0.18	0.54	V/ns
		VDD(1) = 3.3V	0.4	1.2	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	25	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

表 6-30. RMII[x]_REF_CLK Timing Requirements – RMII Mode

see 図 6-27

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF\_CLK)}$	Cycle time, RMII[x]_REF_CLK	19.999	20.001	ns
RMII2	$t_{w(REF\_CLKH)}$	Pulse Duration, RMII[x]_REF_CLK High	7	13	ns
RMII3	$t_{w(REF\_CLKL)}$	Pulse Duration, RMII[x]_REF_CLK Low	7	13	ns

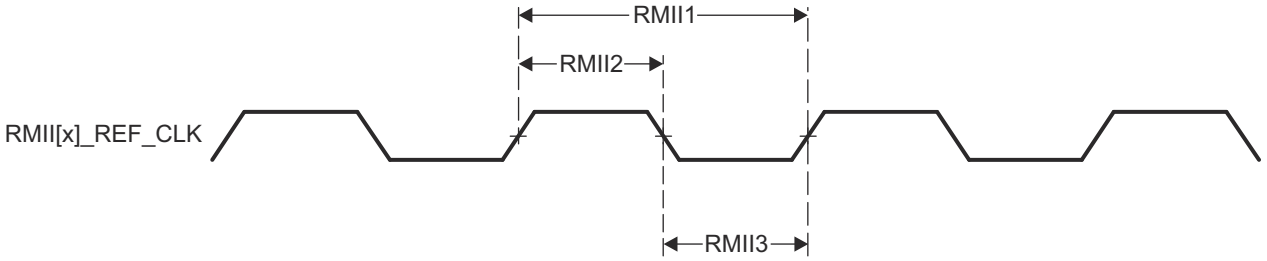


図 6-27. CPSW3G RMII[x]_REF_CLK Timing Requirements – RMII Mode

表 6-31. RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RX_ER Timing Requirements – RMII Mode

see 図 6-28

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII4	$t_{su(RXD-REF\_CLK)}$	Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK	4		ns
	$t_{su(CRS\_DV-REF\_CLK)}$	Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK	4		ns
	$t_{su(RX\_ER-REF\_CLK)}$	Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK	4		ns
RMII5	$t_{h(REF\_CLK-RXD)}$	Hold time RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK	2		ns
	$t_{h(REF\_CLK-CRS\_DV)}$	Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK	2		ns
	$t_{h(REF\_CLK-RX\_ER)}$	Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK	2		ns

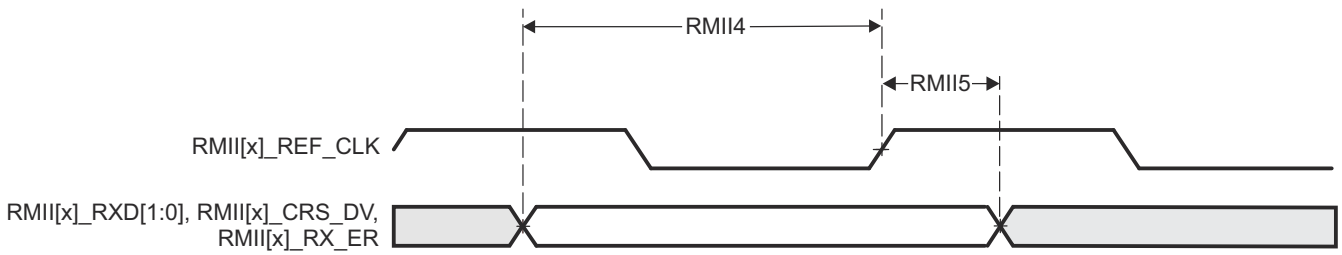


図 6-28. CPSW3G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RX_ER Timing Requirements – RMII Mode

ADVANCE INFORMATION

表 6-32. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

see 図 6-29

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII6	$t_{d(REF\_CLK-TXD)}$	Delay time, RMII[x]_REF_CLK High to RMII[x]_TXD[1:0] valid	2	10	ns
	$t_{d(REF\_CLK-TX\_EN)}$	Delay time, RMII[x]_REF_CLK to RMII[x]_TX_EN valid	2	10	ns

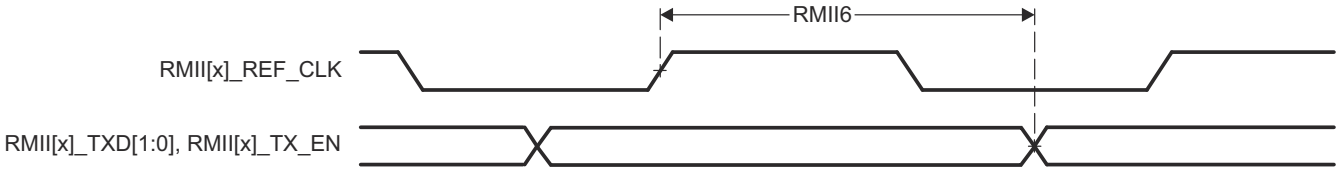


図 6-29. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

ADVANCE INFORMATION

6.11.5.1.3 CPSW3G RGMII Timing

表 6-33, 表 6-34, 表 6-35, 図 6-30, 表 6-36, 表 6-37, and 図 6-31 present timing conditions, requirements, and switching characteristics for CPSW3G RGMII.

表 6-33. CPSW3G RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2.64	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL		50	ps

ADVANCE INFORMATION

表 6-34. RGMII[x]_RXC Timing Requirements – RGMII Mode

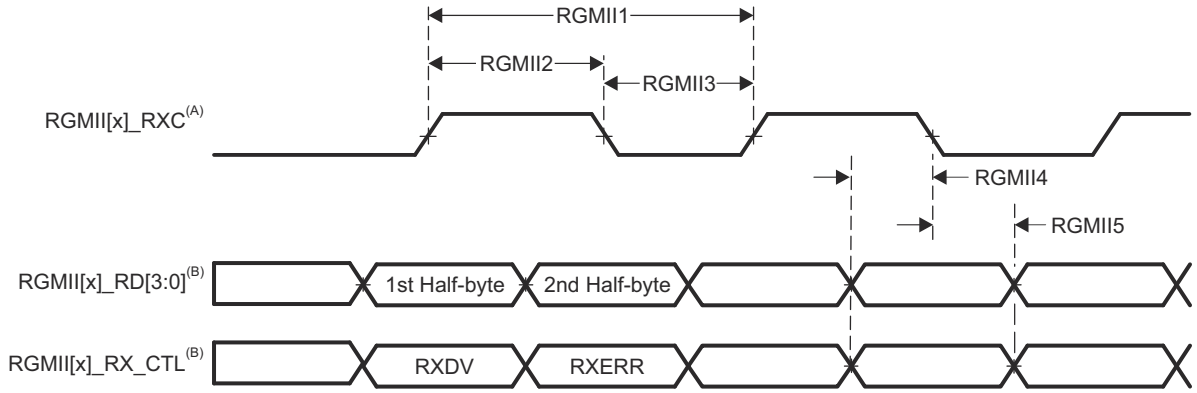
see 図 6-30

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RGMII[x]_RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	$t_{w(RXCH)}$	Pulse duration, RGMII[x]_RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	$t_{w(RXCL)}$	Pulse duration, RGMII[x]_RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

表 6-35. RGMII[x]_RD[3:0], and RGMII[x]_RX_CTL Timing Requirements – RGMII Mode

see 図 6-30

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII4	$t_{su(RD-RXC)}$	Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su(RX\_CTL-RXC)}$	Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_{h(RXC-RD)}$	Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{h(RXC-RX\_CTL)}$	Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns



A. RGMII[x]_RXC must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RXC and data bits 7-4 on the falling edge of RGMII[x]_RXC. Similarly, RGMII[x]_RX_CTL carries RXDV on rising edge of RGMII[x]_RXC and RXERR on falling edge of RGMII[x]_RXC.

図 6-30. CPSW3G RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL Timing Requirements - RGMII Mode

表 6-36. RGMII[x]_TXC Switching Characteristics – RGMII Mode

see 図 6-31

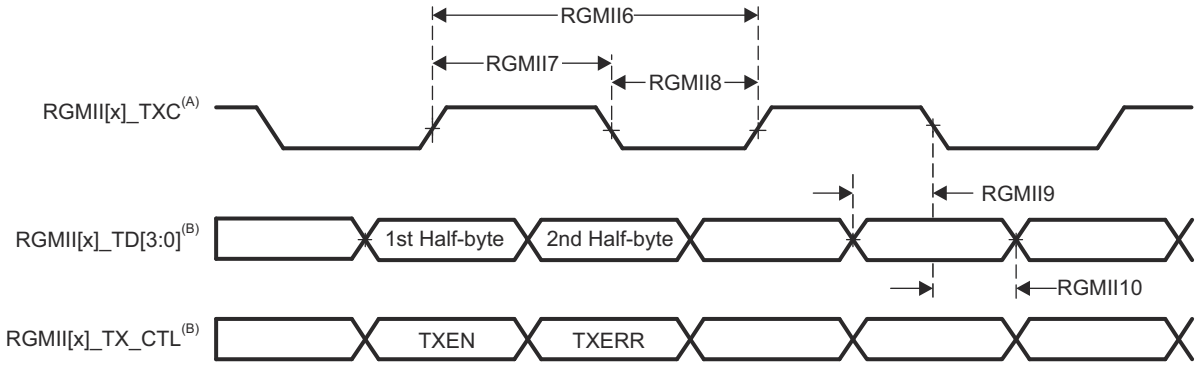
NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII6	$t_{c(TXC)}$	Cycle time, RGMII[x]_TXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII7	$t_{w(TXCH)}$	Pulse duration, RGMII[x]_TXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII8	$t_{w(TXCL)}$	Pulse duration, RGMII[x]_TXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

表 6-37. RGMII[x]_TD[3:0] and RGMII[x]_TX_CTL Switching Characteristics – RGMII Mode

see 図 6-31

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(TD-TXC)}$	Output setup time(1), RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{osu(TX\_CTL-TXC)}$	Output setup time(1), RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
RGMII10	$t_{oh(TXC-TD)}$	Output hold time(1), RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{oh(TXC-TX\_CTL)}$	Output hold time(1), RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns

(1) Output setup/hold times are defining a delay relationship of the transmit data and control outputs relative to the transmit clock output, but this output relationship is being presented as the minimum setup/hold times provided to the attached receiver. This approach matches how the output timing relationships are defined in the RGMII specification.



A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is always enabled.

B. Data and control information is received using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TXC and data bits 7-4 on the falling edge of RGMII[x]_TXC. Similarly, RGMII[x]_TX_CTL carries TXEN on rising edge of RGMII[x]_TXC and TXERR on falling edge of RGMII[x]_TXC.

図 6-31. CPSW3G RGMII[x]_TXC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode

ADVANCE INFORMATION

6.11.5.2 CPTS

表 6-38, 表 6-39, 図 6-32, 表 6-40, and 図 6-33 present timing conditions, requirements, and switching characteristics for CPTS.

表 6-38. CPTS Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	10	pF

表 6-39. CPTS Timing Requirements

see 図 6-32

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T1	$t_{w(HWTSPUSHH)}$	Pulse duration, HWnTSPUSH high	12P(1) + 2		ns
T2	$t_{w(HWTSPUSHL)}$	Pulse duration, HWnTSPUSH low	12P(1) + 2		ns
T3	$t_{c(RFT\_CLK)}$	Cycle time, RFT_CLK	5	8	ns
T4	$t_{w(RFT\_CLKH)}$	Pulse duration, RFT_CLK high	0.45T(2)		ns
T5	$t_{w(RFT\_CLKL)}$	Pulse duration, RFT_CLK low	0.45T(2)		ns

(1) P = functional clock period in ns.
(2) T = RFT_CLK cycle time in ns.

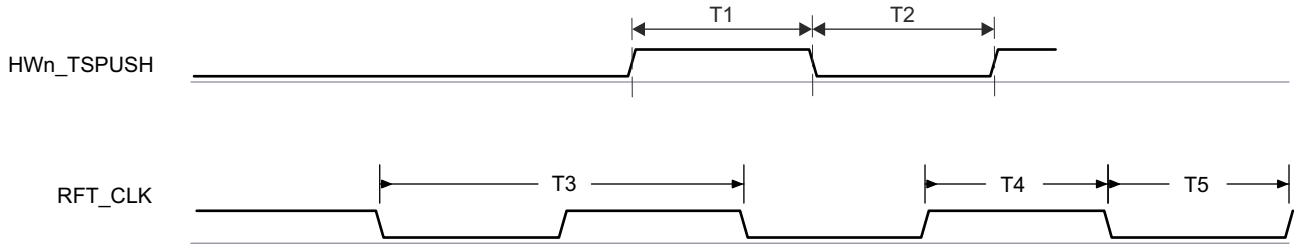


図 6-32. CPTS Timing Requirements

ADVANCE INFORMATION

表 6-40. CPTS Switching Characteristics

see 図 6-33

NO.	PARAMETER	DESCRIPTION	SOURCE	MIN	MAX	UNIT
T6	$t_{w(TS\_COMPH)}$	Pulse duration, TS_COMP high		36P(1) - 2		ns
T7	$t_{w(TS\_COMPL)}$	Pulse duration, TS_COMP low		36P(1) - 2		ns
T8	$t_{w(TS\_SYNCH)}$	Pulse duration, TS_SYNC high		36P(1) - 2		ns
T9	$t_{w(TS\_SYNCL)}$	Pulse duration, TS_SYNC low		36P(1) - 2		ns
T10	$t_{w(SYNC\_OUTH)}$	Pulse duration, SYNCn_OUT high	TS_SYNC	36P(1) - 2		ns
			GENF	5P(1) - 2		ns
T11	$t_{w(SYNC\_OUTL)}$	Pulse duration, SYNCn_OUT low	TS_SYNC	36P(1) - 2		ns
			GENF	5P(1) - 2		ns

(1) P = functional clock period in ns.

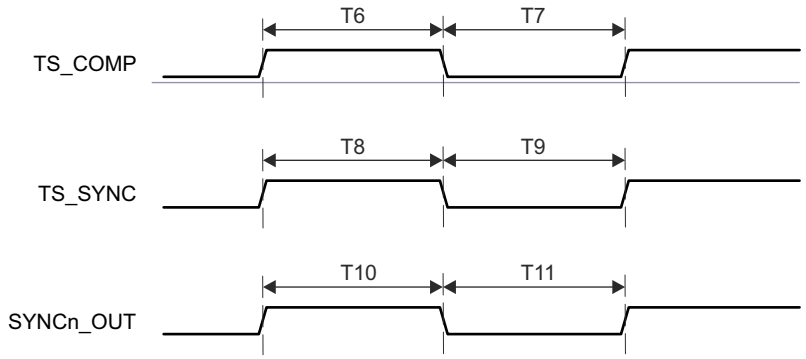


図 6-33. CPTS Switching Characteristics

For more information, see *Data Movement Architecture (DMA)* chapter in the device TRM.

6.11.5.3 CSI-2

注

For more information, see the *Camera Serial Interface Receiver (CSI_RX_IF)* section in the device TRM. The CSI_RX_IF is connected to device port instances named CSIRXn, where n is the instance number.

The CSI_RX_IF and associated D-PHY implements a CSI-2 port (CSIRX0) compliant with the MIPI D-PHY specification v1.2 and the MIPI CSI-2 specification v1.3, with 4 differential data lanes plus 1 differential clock lane operating in synchronous double data rate mode. For CSI-2 timing details, see the respective MIPI specifications mentioned above.

- Support for 1-, 2-, 3- or 4-lane data transfer modes up to 1.5 Gbps

ADVANCE INFORMATION

6.11.5.4 DDRSS

For more details about features and additional description information on the device LPDDR4 Memory Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 6-41 and 図 6-34 present switching characteristics for DDRSS.

表 6-41. DDRSS Switching Characteristics

see 図 6-34

NO.	PARAMETER		DDR TYPE	MIN	MAX	UNIT
1	$t_{c(DDR\_CKP/DDR\_CKN)}$	Cycle time, DDR_CKP and DDR_CKN	LPDDR4	0.6250(1)	20	ns

(1) Minimum DDR clock Cycle time will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Refer to *AM62Px DDR Board Design and Layout Guidelines* for the proper PCB implementation to achieve maximum DDR frequency.

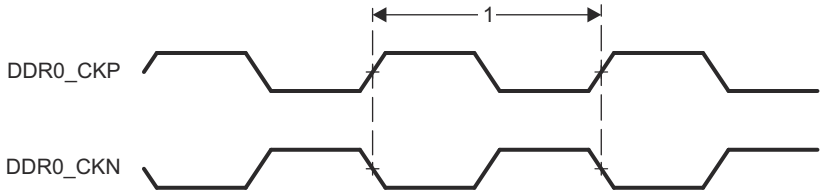


図 6-34. DDRSS Switching Characteristics

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

6.11.5.5 DSI

注

For more information, see the *MIPI Display Serial Interface (DSI) Controller* section in the device TRM. The DSI transmitter controller is connected to device port instances named DSITXn, where n is the instance number.

The DSI transmitter controller and associated D-PHY implements a DSI port (DSITX0) compliant with the MIPI D-PHY specification v1.2 and the MIPI DSI specification v1.3, with 4 differential data lanes plus 1 differential clock lane operating in synchronous double data rate mode. For DSI timing details, see the respective MIPI specifications mentioned above.

- Support for 1-, 2-, 3- or 4-lane data transfer modes up to 1.8 Gbps

ADVANCE INFORMATION

6.11.5.6 DSS

表 6-42, 表 6-43, 図 6-35, 表 6-44 and 図 6-36 present timing conditions, requirements, and switching characteristics for DSS.

表 6-42. DSS Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1.44	26.4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1.5	5	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

表 6-43. DSS External Pixel Clock Timing Requirements

see 図 6-35

NO.			MIN	MAX	UNIT
D6	$t_{c(extpclkin)}$	Cycle time, VOUT(x)_EXTPCLKIN(2)	6.06		ns
D7	$t_{w(extpclkinL)}$	Pulse duration, VOUT(x)_EXTPCLKIN(2) low	0.475P(1)		ns
D8	$t_{w(extpclkinH)}$	Pulse duration, VOUT(x)_EXTPCLKIN(2) high	0.475P(1)		ns

(1) P = VOUT(x)_EXTPCLKIN cycle time in ns
(2) x in VOUT(x) = 0

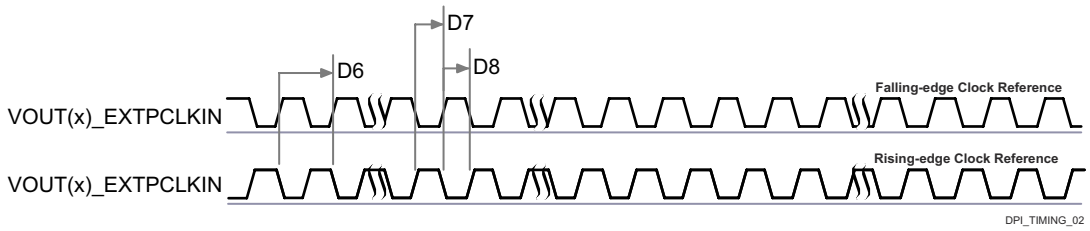


図 6-35. DSS External Pixel Clock Timing Requirements

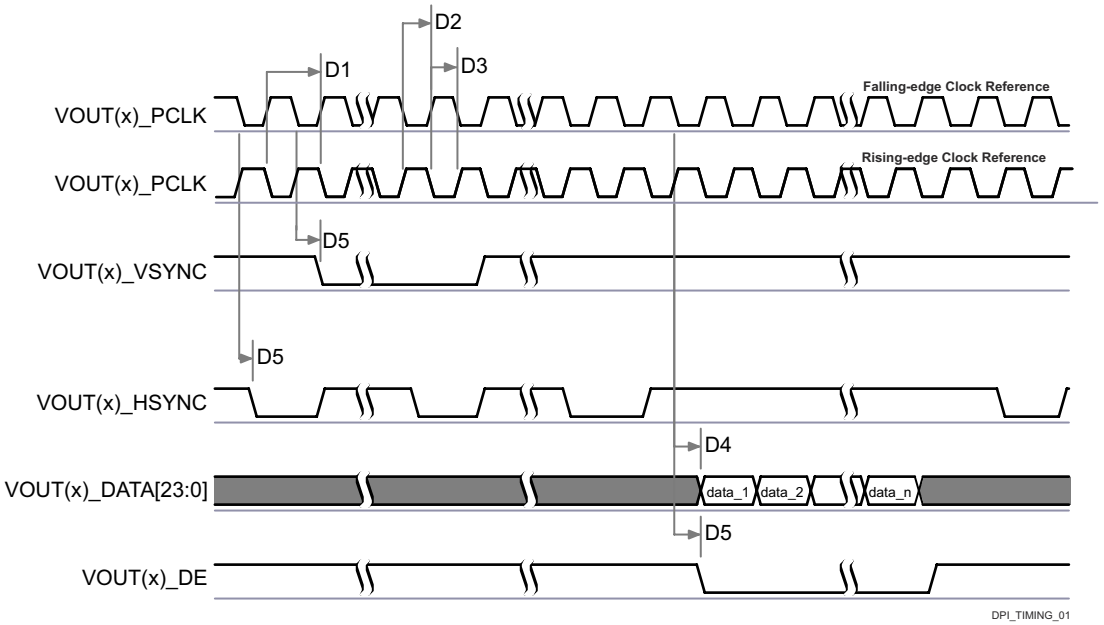
ADVANCE INFORMATION

表 6-44. DSS Switching Characteristics

see 図 6-36

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D1	$t_{c(pclk)}$	Cycle time, VOUT(x)_PCLK(2)		6.06		ns
D2	$t_{w(pclkL)}$	Pulse duration, VOUT(x)_PCLK(2) low	Internal PLL	0.475P(1) - 0.3		ns
			EXTPCLKIN	Y(3) - 0.45		ns
D3	$t_{w(pclkH)}$	Pulse duration, VOUT(x)_PCLK(2) high	Internal PLL	0.475P(1) -0.3		ns
			EXTPCLKIN	Z(4) - 0.45		ns
D4	$t_{d(pclkV-dataV)}$	Delay time, VOUT(x)_PCLK(2) transition to VOUT(x)_DATA[23:0](2) transition	Internal PLL	-0.68	1.78	ns
			EXTPCLKIN	-0.68	1.78	ns
D5	$t_{d(pclkV-ctrlL)}$	Delay time, VOUT(x)_PCLK(2) transition to control signals VOUT(x)_VSYNC(2), VOUT(x)_HSYNC(2), VOUT(x)_DE(2) falling edge	Internal PLL	-0.68	1.78	ns
			EXTPCLKIN	-0.68	1.78	ns

(1) P = VOUT(x)_PCLK cycle time in ns
(2) x in VOUT(x) = 0
(3) Y = $t_{w(extpclkinL)}$, parameter D7 from 表 6-43, *DSS External Pixel Clock Timing Requirements*
(4) Z = $t_{w(extpclkinH)}$, parameter D8 from 表 6-43, *DSS External Pixel Clock Timing Requirements*



A. The assertion of data can be programmed to occur on the falling or rising edge of the pixel clock. Refer to *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.
B. The polarity and pulse width of VOUT(x)_HSYNC and VOUT(x)_VSYNC are programmable, refer to *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.
C. The VOUT(x)_PCLK frequency is configurable, refer to *Display Subsystem* section in *Peripherals* chapter in the device TRM.

図 6-36. DSS Switching Characteristics

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter of the device TRM.

6.11.5.7 ECAP

表 6-45, 表 6-46, 図 6-37, 表 6-47, and 図 6-38 present timing conditions, requirements, and switching characteristics for ECAP.

表 6-45. ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

表 6-46. ECAP Timing Requirements

see 図 6-37

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP1	$t_{w(CAP)}$	Pulse duration, CAP (asynchronous)	2P(1) + 2		ns

(1) P = sysclk period in ns.

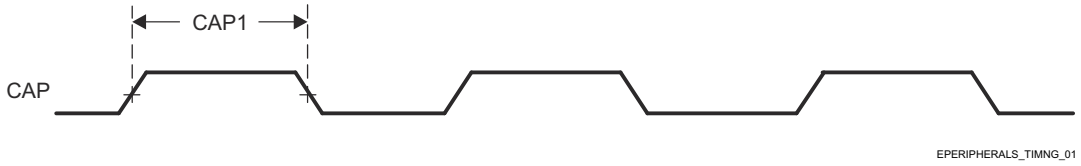


図 6-37. ECAP Timings Requirements

表 6-47. ECAP Switching Characteristics

see 図 6-38

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP2	$t_{w(APWM)}$	Pulse duration, APWMx high/low	2P(1) - 2		ns

(1) P = sysclk period in ns.

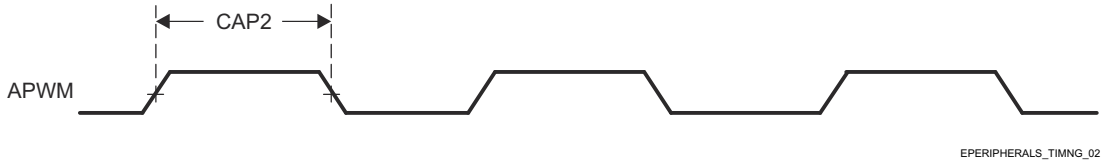


図 6-38. ECAP Switching Characteristics

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

ADVANCE INFORMATION

6.11.5.8 Emulation and Debug

For more details about features and additional description information on the device Trace and JTAG interfaces, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.11.5.8.1 Trace

表 6-48. Trace Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	5	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch)}$	Propagation delay mismatch across all traces		200	ps

表 6-49. Trace Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1.8V Mode					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	6.83		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	2.66		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	2.66		ns
DBTR4	$t_{osu(TRC\_DATAV\text{-}TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	0.85		ns
DBTR5	$t_{oh(TRC\_CLK\text{-}TRC\_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	0.85		ns
DBTR6	$t_{osu(TRC\_CTLV\text{-}TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	0.85		ns
DBTR7	$t_{oh(TRC\_CLK\text{-}TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	0.85		ns
3.3V Mode					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	8.78		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	3.64		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	3.64		ns
DBTR4	$t_{osu(TRC\_DATAV\text{-}TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.10		ns
DBTR5	$t_{oh(TRC\_CLK\text{-}TRC\_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.10		ns
DBTR6	$t_{osu(TRC\_CTLV\text{-}TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.10		ns
DBTR7	$t_{oh(TRC\_CLK\text{-}TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.10		ns

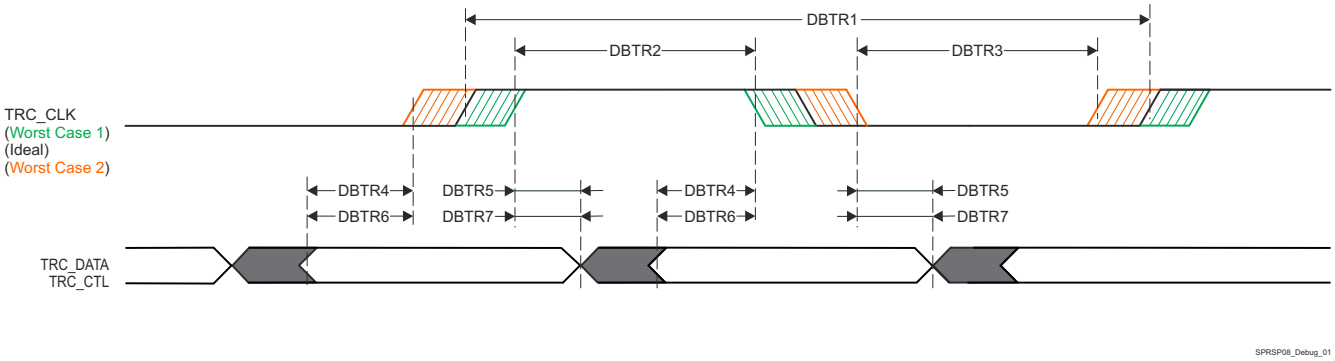


図 6-39. Trace Switching Characteristics

6.11.5.8.2 JTAG

表 6-50. JTAG Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	2.0	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	5	15	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	83.5	1000(1)	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

(1) Maximum propagation delay associated with the JTAG signal traces has a significant impact on maximum TCK operating frequency. It may be possible to increase the trace delay beyond this value, but the operating frequency of TCK must be reduced to account for the additional trace delay.

表 6-51. JTAG Timing Requirements

see 図 6-40

NO.			MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time minimum, TCK	40(1)		ns
J2	$t_{w(TCKH)}$	Pulse width minimum, TCK high	0.4P(2)		ns
J3	$t_{w(TCKL)}$	Pulse width minimum, TCK low	0.4P(2)		ns
J4	$t_{su(TDI-TCK)}$	Input setup time minimum, TDI valid to TCK high	2		ns
	$t_{su(TMS-TCK)}$	Input setup time minimum, TMS valid to TCK high	2		ns
J5	$t_{h(TCK-TDI)}$	Input hold time minimum, TDI valid from TCK high	3		ns
	$t_{h(TCK-TMS)}$	Input hold time minimum, TMS valid from TCK high	3		ns

(1) The maximum TCK operating frequency assumes the following timing requirements and switching characteristis for the attached debugger. The operating frequency of TCK must be reduced to provide appropriate timing margin if the debugger exceeds any of these assumptions.
- Minimum TDO setup time of 2 ns relative to the rising edge of TCK
- TDI and TMS output delay in the range of -12.9 ns to 13.9 ns relative to the falling edge of TCK

(2) P = TCK cycle time in ns

表 6-52. JTAG Switching Characteristics

see 図 6-40

NO.	PARAMETER		MIN	MAX	UNIT
J6	$t_{d(TCKL-TDOI)}$	Delay time minimum, TCK low to TDO invalid	0		ns
J7	$t_{d(TCKL-TDOV)}$	Delay time maximum, TCK low to TDO valid		12	ns

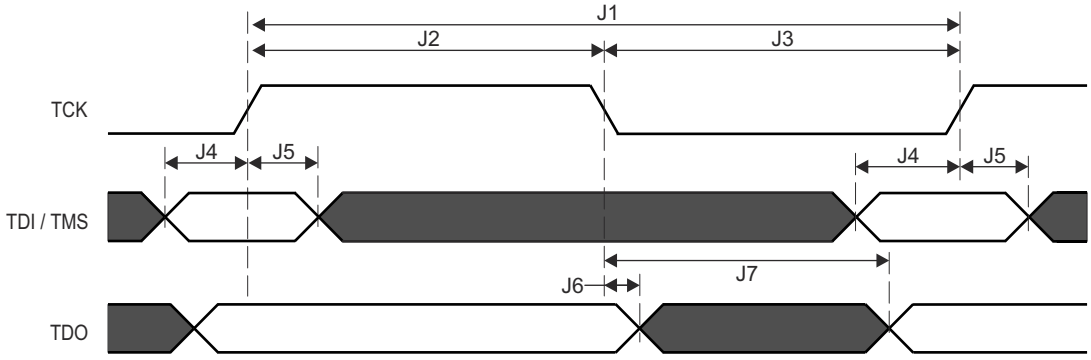


図 6-40. JTAG Timing Requirements and Switching Characteristics

ADVANCE INFORMATION

6.11.5.9 EPWM

表 6-53, 表 6-54, 図 6-41, 表 6-55, 図 6-42, 図 6-43, and 図 6-44 present timing conditions, requirements, and switching characteristics for EPWM.

表 6-53. EPWM Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

表 6-54. EPWM Timing Requirements

see 図 6-41

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	$t_{w(SYNCIN)}$	Pulse duration, EHRPWM_SYNCI	2P(1) + 2		ns
PWM7	$t_{w(TZ)}$	Pulse duration, EHRPWM_TZn_IN low	3P(1) + 2		ns

(1) P = sysclk period in ns.

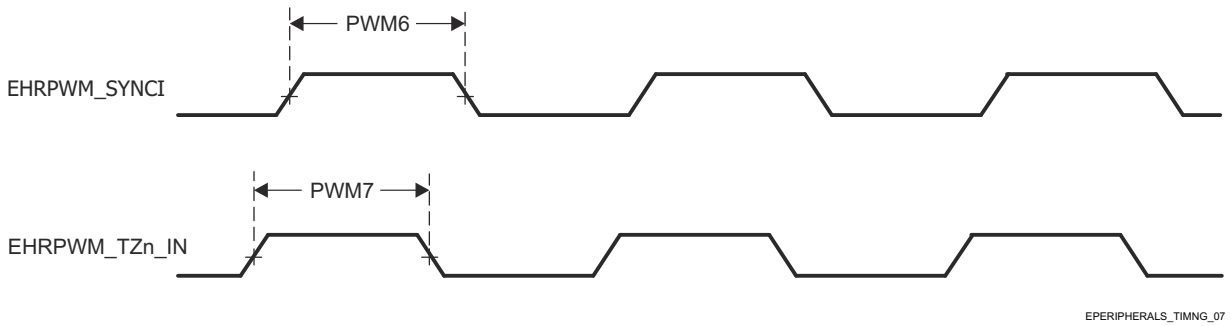


図 6-41. EPWM Timing Requirements

ADVANCE INFORMATION

表 6-55. EPWM Switching Characteristics

see 図 6-42, 図 6-43, and 図 6-44

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	$t_{w(PWM)}$	Pulse duration, EHRPWM_A/B high/low	P(1) - 3		ns
PWM2	$t_{w(SYNCOUT)}$	Pulse duration, EHRPWM_SYNCO	P(1) - 3		ns
PWM3	$t_{d(TZ-PWM)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low		11	ns
PWM4	$t_{d(TZ-PWMZ)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z		11	ns
PWM5	$t_{w(SOC)}$	Pulse duration, EHRPWM_SOCA/B output	P(1) - 3		ns

(1) P = sysclk period in ns.

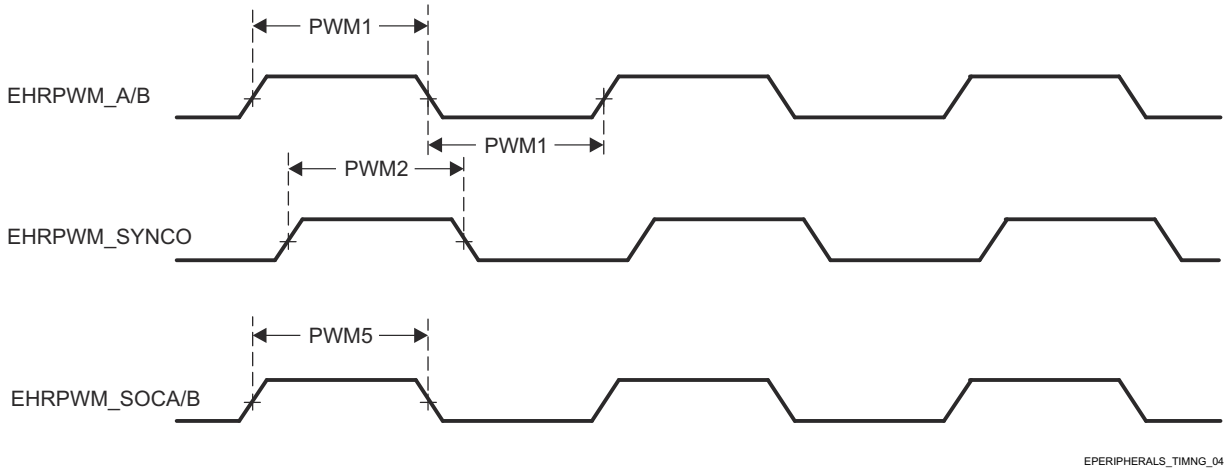


図 6-42. EHRPWM Switching Characteristics

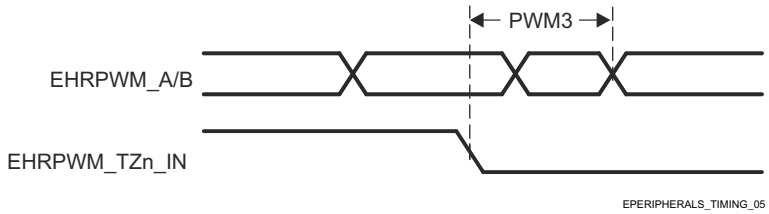


図 6-43. EHRPWM_TZn_IN to EHRPWM_A/B Forced Switching Characteristics

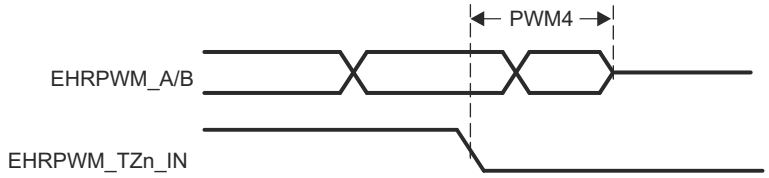


図 6-44. EHRPWM_TZn_IN to EHRPWM_A/B Hi-Z Switching Characteristics

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

ADVANCE INFORMATION

6.11.5.10 EQEP

表 6-56, 表 6-57, 図 6-45, and 表 6-58 present timing conditions, requirements, and switching characteristics for EQEP.

表 6-56. EQEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

表 6-57. EQEP Timing Requirements

see 図 6-45

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP1	$t_{w(QEP)}$	Pulse duration, QEP_A/B	2P(1) + 2		ns
QEP2	$t_{w(QEPIH)}$	Pulse duration, QEP_I high	2P(1) + 2		ns
QEP3	$t_{w(QEPIL)}$	Pulse duration, QEP_I low	2P(1) + 2		ns
QEP4	$t_{w(QEPSH)}$	Pulse duration, QEP_S high	2P(1) + 2		ns
QEP5	$t_{w(QEPSL)}$	Pulse duration, QEP_S low	2P(1) + 2		ns

(1) P = sysclk period in ns

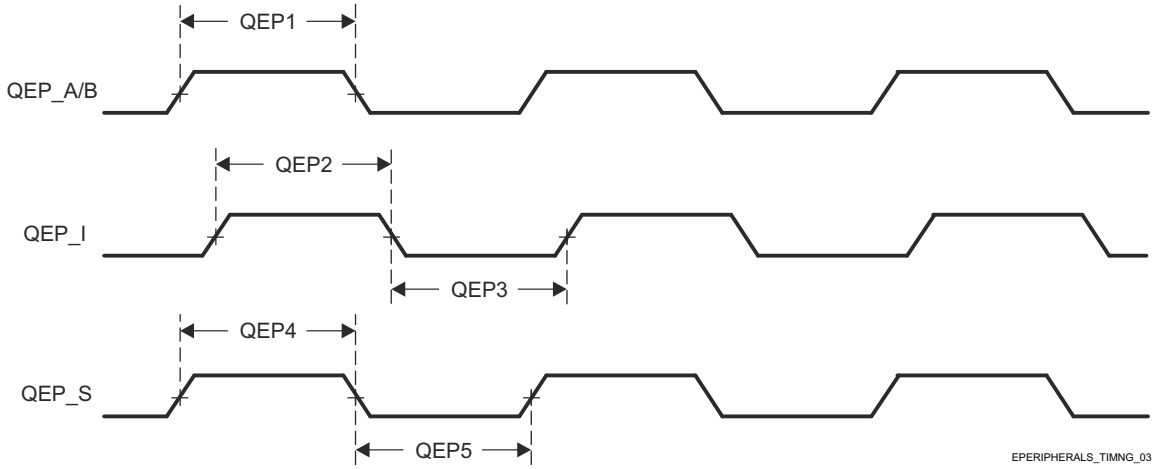


図 6-45. EQEP Timing Requirements

表 6-58. EQEP Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP6	$t_{d(QEP-CNTR)}$	Delay time, external clock to counter increment		24	ns

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

6.11.5.11 GPIO

表 6-59, 表 6-60, and 表 6-61 present timing conditions, requirements, and switching characteristics for GPIO.

The device has three instances of the GPIO module.

- MCU_GPIO0
- GPIO0
- GPIO1

注

GPIOn_x is generic name used to describe a GPIO signal, where n represents the specific GPIO module and x represents one of the input/output signals associated with the module.

For additional description information on the device GPIO, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 6-59. GPIO Timing Conditions

PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	LVCMOS (VDD(1) = 1.8 V)	0.0018	6.6	V/ns
		LVCMOS (VDD(1) = 3.3V)	0.0033	6.6	V/ns
		I2C OD FS (VDD(1) = 1.8 V)	0.0018	6.6	V/ns
		I2C OD FS (VDD(1) = 3.3V)	0.0033	0.08	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	LVCMOS	3	10	pF
		I2C OD FS	3	100	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

表 6-60. GPIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GPIO1	$t_{w(GPIO\_IN)}$	Pulse width, GPIOn_x	2P(1) + 30		ns

(1) P = functional clock period in ns.

表 6-61. GPIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
GPIO2	$t_{w(GPIO\_OUT)}$	Pulse width, GPIOn_x	LVCMOS	0.975P(1) - 3.6		ns
			I2C OD FS	160		ns

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

ADVANCE INFORMATION

6.11.5.12 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 6-62 presents timing conditions for GPMC.

表 6-62. GPMC Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1.65	4	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	133 MHz Synchronous Mode	140	360	ps
		All other modes	140	720	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces			200	ps

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

6.11.5.12.1 GPMC and NOR Flash — Synchronous Mode

表 6-63 and 表 6-64 present timing requirements and switching characteristics for GPMC and NOR Flash - Synchronous Mode.

表 6-63. GPMC and NOR Flash Timing Requirements — Synchronous Mode

see 図 6-46, 図 6-47, and 図 6-50

NO.	PARAMETER	DESCRIPTION	MODE[4]	MIN MAX GPMC_FCLK = 100 MHz[1]	MIN MAX GPMC_FCLK = 133 MHz[1]	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.61	0.92	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.86	3.41	ns
F13	$t_{h(clkH-dV)}$	Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns
F21	$t_{su(waitV-clkH)}$	Setup time, input wait GPMC_WAIT[j][2] [3] valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.61	0.92	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.86	3.41	ns

表 6-63. GPMC and NOR Flash Timing Requirements — Synchronous Mode (続き)

see 図 6-46, 図 6-47, and 図 6-50

NO.	PARAMETER	DESCRIPTION	MODE[4]	MIN MAX GPMC_FCLK = 100 MHz[1]	MIN MAX GPMC_FCLK = 133 MHz[1]	UNIT
F22	$t_{h(clkH-waitV)}$	Hold time, input wait GPMC_WAIT[j][2] [3] valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.09	2.09	ns

(1) GPMC_FCLK select
- gpmc_fclk_sel[1:0] = 2b01 to select the 100MHz GPMC_FCLK
- gpmc_fclk_sel[1:0] = 2b00 to select the 133MHz GPMC_FCLK

(2) In GPMC_WAIT[j], j is equal to 0 or 1.

(3) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.

(4) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For not_div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC_CLK frequency = GPMC_FCLK frequency / (2 to 4)

For GPMC_FCLK_MUX:
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY_X1:
- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

表 6-64. GPMC and NOR Flash Switching Characteristics – Synchronous Mode

see 図 6-46, 図 6-47, 図 6-48, 図 6-49, and 図 6-50

NO. (2)	PARAMETER	DESCRIPTION	MODE[16]	MIN MAX 100 MHz		MIN MAX 133 MHz		UNIT
F0	1 / tc(clk)	Period, output clock GPMC_CLK[15]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	10.00		7.52		ns
F1	$t_{w(clkH)}$	Typical pulse duration, output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475P - 0.3[14]		0.475P - 0.3[14]		ns
F1	$t_{w(clkL)}$	Typical pulse duration, output clock GPMC_CLK low	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475P - 0.3[14]		0.475P - 0.3[14]		ns
F2	$t_{d(clkH-csnV)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] transition[13]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	F - 2.2 [5]	F + 3.75	F - 2.2 [5]	F + 3.75	ns
F3	$t_{d(clkH-CSn[i]V)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] invalid[13]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	E - 2.2 [4]	E + 3.18	E - 2.2 [4]	E + 4.5	ns

ADVANCE INFORMATION

表 6-64. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (続き)

see 図 6-46, 図 6-47, 図 6-48, 図 6-49, and 図 6-50

NO. (2)	PARAMETER	DESCRIPTION	MODE(16)	MIN MAX 100 MHz	MIN MAX 133 MHz	UNIT
F4	$t_{d(aV-clk)}$	Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2.3 (2) B + 4.5	B - 2.3 (2) B + 4.5	ns
F5	$t_{d(clkH-aIV)}$	Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	-2.3 4.5	-2.3 4.5	ns
F6	$t_{d(be[x]nV-clk)}$	Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2.3 (2) B + 1.9	B - 2.3 (2) B + 1.9	ns
F7	$t_{d(clkH-be[x]nIV)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid(10)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3(3) D + 1.9	D - 2.3 (3) D + 1.9	ns
F7	$t_{d(clkL-be[x]nIV)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 (3) D + 1.9	D - 2.3 (3) D + 1.9	ns
F7	$t_{d(clkL-be[x]nIV).}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 (3) D + 1.9	D - 2.3 (3) D + 1.9	ns
F8	$t_{d(clkH-advn)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	G - 2.3(6) G + 4.5	G - 2.3 (6) G + 4.5	ns
F9	$t_{d(clkH-advnIV)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	D - 2.3 (3) D + 4.5	D - 2.3 (3) D + 4.5	ns
F10	$t_{d(clkH-oen)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	H - 2.3 (7) H + 3.5	H - 2.3 (7) H + 3.5	ns
F11	$t_{d(clkH-oenIV)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	H - 2.3 (7) H + 3.5	H - 2.3 (7) H + 3.5	ns
F14	$t_{d(clkH-wen)}$	Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	I - 2.3 (8) I + 4.5	I - 2.3 (8) I + 4.5	ns
F15	$t_{d(clkH-do)}$	Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition(10)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 2.7	J - 2.3 (9) J + 2.7	ns
F15	$t_{d(clkL-do)}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 2.7	J - 2.3 (9) J + 2.7	ns
F15	$t_{d(clkL-do).}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 2.7	J - 2.3 (9) J + 2.7	ns
F17	$t_{d(clkH-be[x]n)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition(10)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 1.9	J - 2.3 (9) J + 1.9	ns

表 6-64. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (続き)

see 図 6-46, 図 6-47, 図 6-48, 図 6-49, and 図 6-50

NO. (2)	PARAMETER	DESCRIPTION	MODE(16)	MIN MAX 100 MHz	MIN MAX 133 MHz	UNIT
F17	$t_{d(clkL-be[x]n)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition(11)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 1.9	J - 2.3 (9) J + 1.9	ns
F17	$t_{d(clkL-be[x]n)}$.	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition(12)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9) J + 1.9	J - 2.3 (9) J + 1.9	ns
F18	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i](13) low	Read	A	A	ns
			Write	A	A	ns
F19	$t_{w(be[x]nV)}$	Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low	Read	C	C	ns
			Write	C	C	ns
F20	$t_{w(advnV)}$	Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low	Read	K	K	ns
			Write	K	K	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
With n being the page burst access number.

(2) B = ClkActivationTime × GPMC_FCLK(14)

(3) For single read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: D = (WrCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(4) For single read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: E = (CSWrOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(5) For csn falling edge (CS activated):
- Case GPMCFCLKDIVIDER = 0:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK(14) if ((CSOnTime - ClkActivationTime) is a multiple of 3)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(14) if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
  - F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK(14) if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(6) For ADV falling edge (ADV activated):
- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:
- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14)

ADVANCE INFORMATION

- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK(14) if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(14) if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(7) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK(14) if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(14) if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For WE falling edge (WE activated):

- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14)
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK (14)
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK(14) if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(14) if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) J = GPMC_FCLK(14)
(10) First transfer only for CLK DIV 1 mode.
(11) Half cycle; for all data after initial transfer for CLK DIV 1 mode.
(12) Half cycle of GPMC_CLKOUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLKOUT divide down from GPMC_FCLK.
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
(14) P = GPMC_CLK period in ns
(15) Related to the GPMC_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_i configuration register bit field GPMCFCLKDIVIDER.
(16) For div_by_1_mode:

- GPMC_CONFIG1_i register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = PER1_PLL_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

For no extra_delay:

- GPMC_CONFIG2_i Register: CSEXTRADELAY = 0h = CSn Timing control signal is not delayed
- GPMC_CONFIG4_i Register: WEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC_CONFIG4_i Register: OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC_CONFIG3_i Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed

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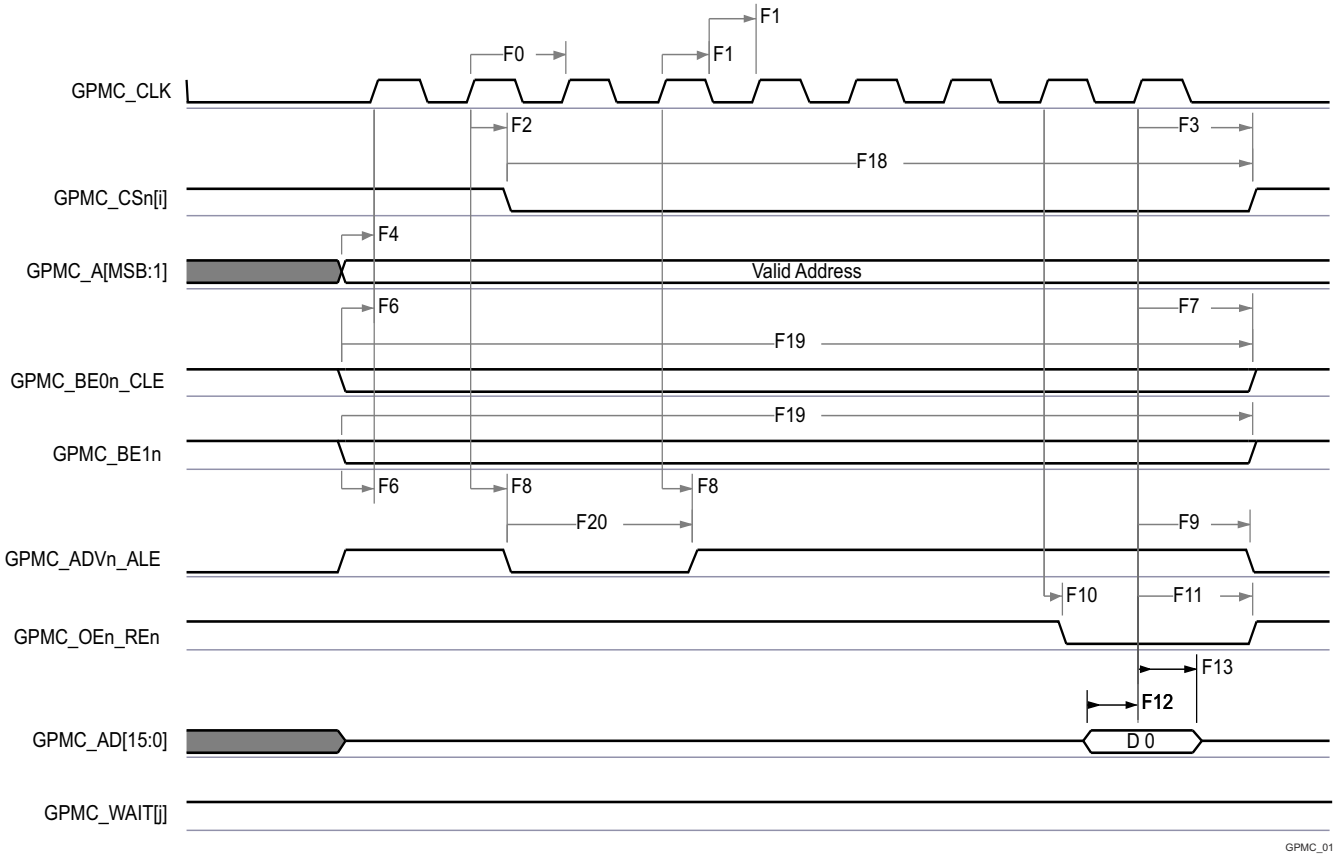
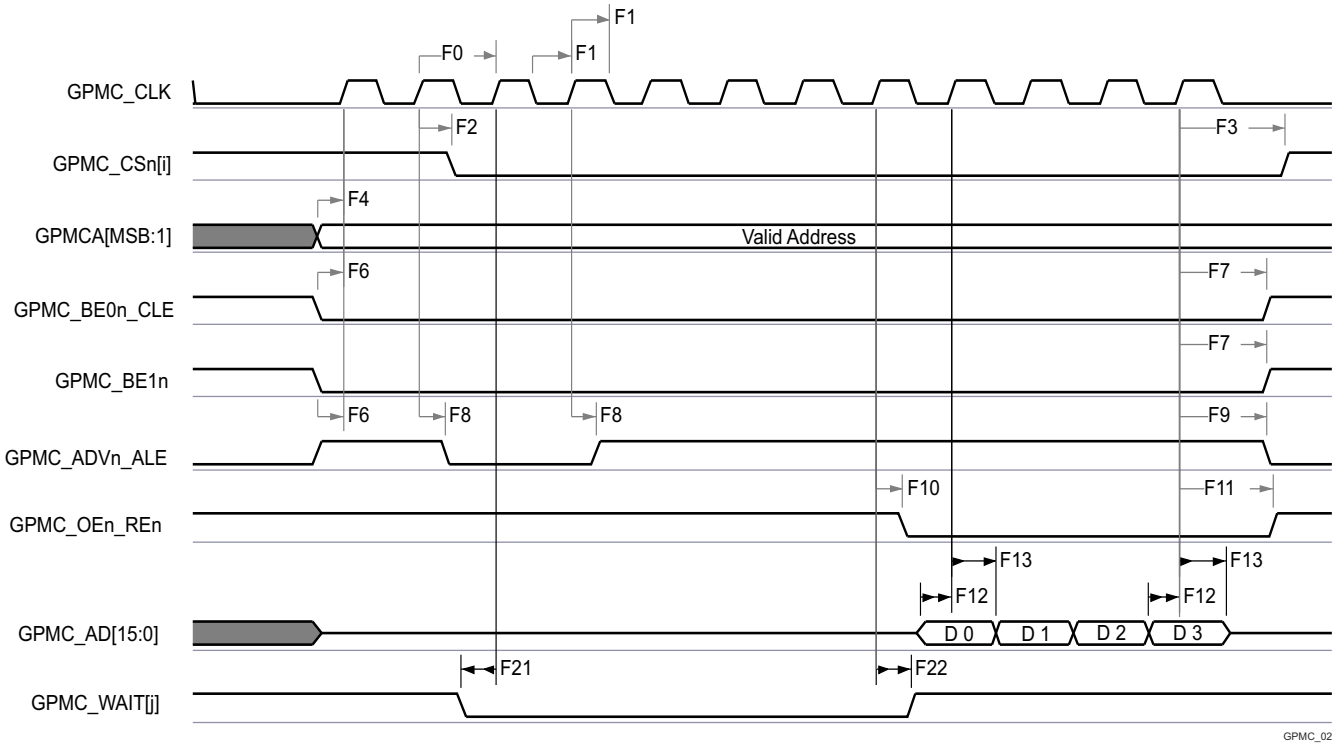


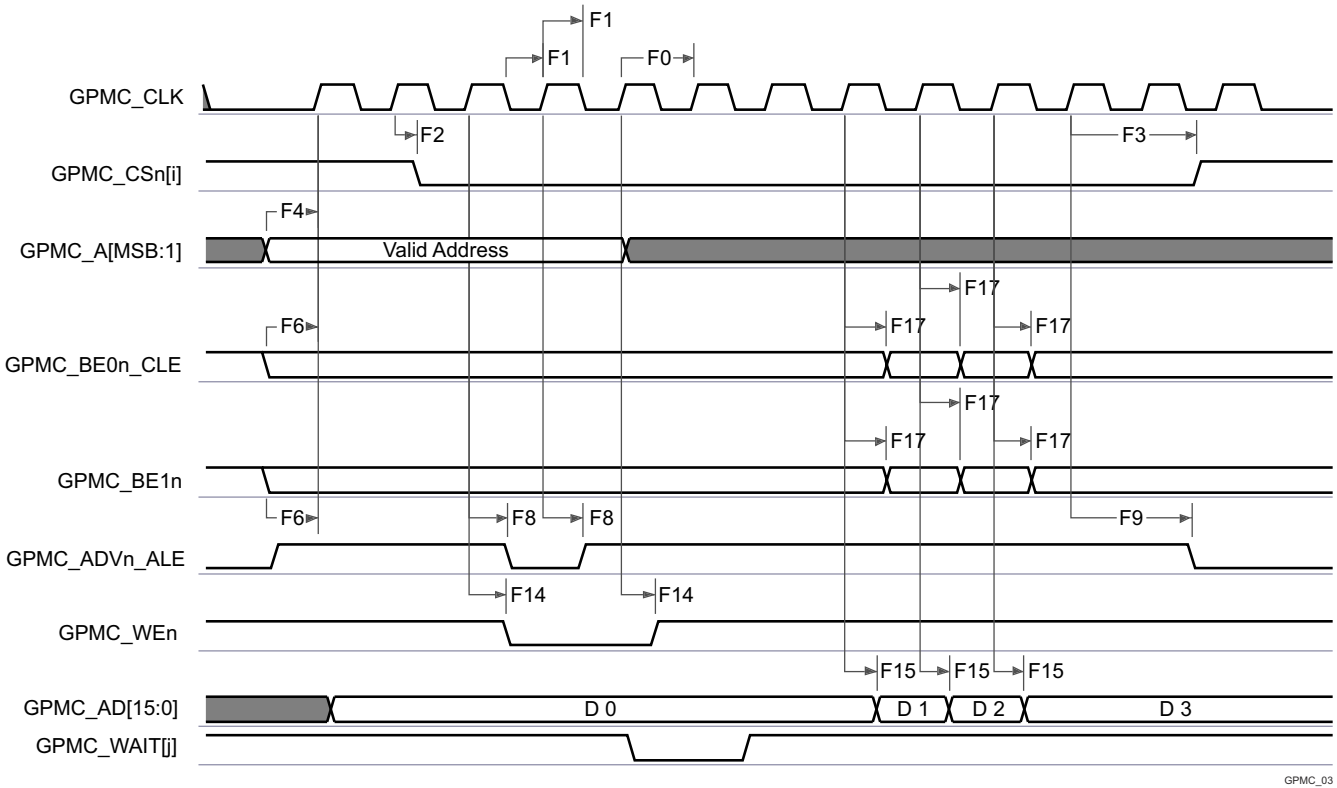
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

図 6-46. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

図 6-47. GPMC and NOR Flash — Synchronous Burst Read — 4x16–bit (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

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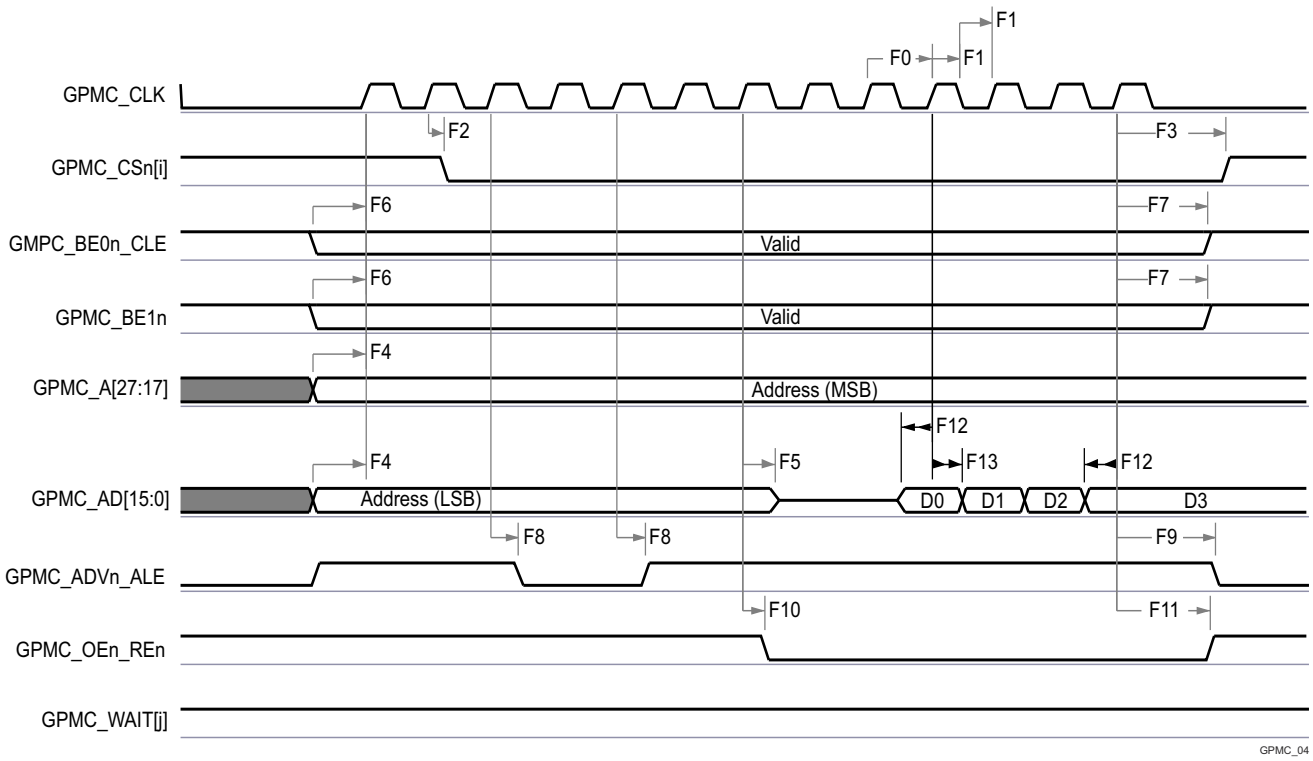
B. In GPMC_WAIT[j], j is equal to 0 or 1.

図 6-48. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

図 6-49. GPMC and Multiplexed NOR Flash — Synchronous Burst Read

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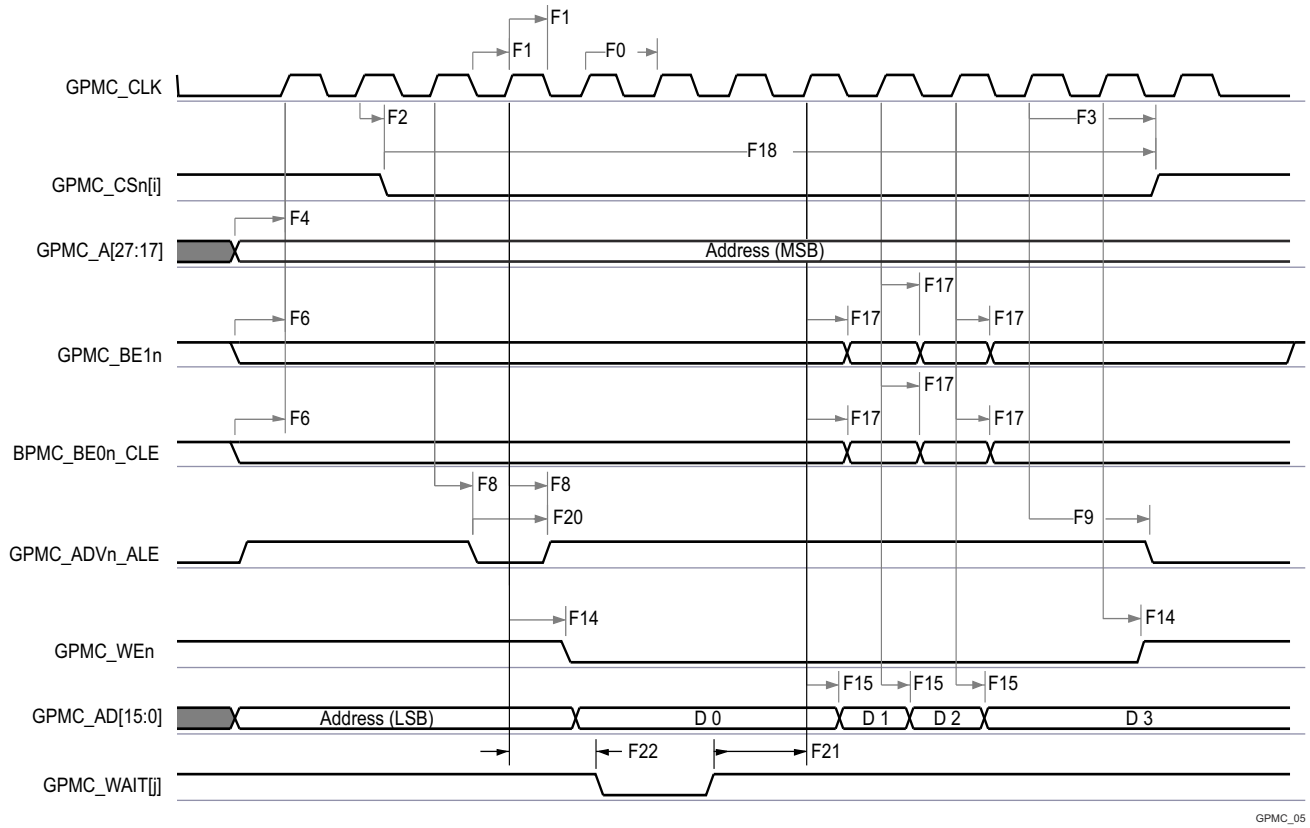

A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

図 6-50. GPMC and Multiplexed NOR Flash — Synchronous Burst Write

ADVANCE INFORMATION

6.11.5.12.2 GPMC and NOR Flash — Asynchronous Mode

表 6-65 and 表 6-66 present timing requirements and switching characteristics for GPMC and NOR Flash — Asynchronous Mode.

表 6-65. GPMC and NOR Flash Timing Requirements – Asynchronous Mode

see 図 6-51, 図 6-52, 図 6-53, and 図 6-55

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
FA5[1]	$t_{acc(d)}$	Data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H[4]	ns
FA20[2]	$t_{acc1-pgmode(d)}$	Page mode successive data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		P[3]	ns
FA21[1]	$t_{acc2-pgmode(d)}$	Page mode first data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H[4]	ns

(1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
(2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
(3) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[5]
(4) H = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[5]
(5) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

表 6-66. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode

see 図 6-51, 図 6-52, 図 6-53, 図 6-54, 図 6-55, and 図 6-56

NO.	PARAMETER	DESCRIPTION	MODE[15]	MIN	MAX	UNIT
				133 MHz		
FA0	$t_{w(be[x]nV)}$	Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time	Read		N [12]	ns
			Write		N [12]	
FA1	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i][13] low	Read		A [1]	ns
			Write		A [1]	
FA3	$t_{d(csnV-advnIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output address valid and address latch enable GPMC_ADVn_ALE invalid	Read	B - 2 [2]	B + 2[2]	ns
			Write	B - 2[2]	B + 2[2]	
FA4	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn invalid (Single read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2[3]	C + 2[3]	ns
FA9	$t_{d(aV-csnV)}$	Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2[9]	J + 2[9]	ns
FA10	$t_{d(be[x]nV-csnV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2[9]	J + 2[9]	ns
FA12	$t_{d(csnV-advnV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output address valid and address latch enable GPMC_ADVn_ALE valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	K - 2[10]	K + 2[10]	ns
FA13	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L - 2[11]	L + 2[11]	ns
FA16	$t_{w(aIV)}$	Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G [7]		ns

表 6-66. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode (続き)

see 図 6-51, 図 6-52, 図 6-53, 図 6-54, 図 6-55, and 図 6-56

NO.	PARAMETER	DESCRIPTION	MODE[15]	MIN	MAX	UNIT
				133 MHz		
FA18	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn invalid (Burst read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I - 2[8]	I + 2[8]	ns
FA20	$t_{w(aV)}$	Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D [4]		ns
FA25	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E - 2[5]	E + 2[5]	ns
FA27	$t_{d(csnV-wenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2[6]	F + 2[6]	ns
FA28	$t_{d(wenV-dV)}$	Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2	ns
FA29	$t_{d(dV-csnV)}$	Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2[9]	J + 2[9]	ns
FA37	$t_{d(oenV-aIV)}$	Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For single write: A = (CSWrOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
with n being the page burst access number
(2) For reading: B = ((ADVRdOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
For writing: B = ((ADVWrOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(3) C = ((OEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(4) D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(5) E = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(6) F = ((WEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(7) G = Cycle2CycleDelay × GPMC_FCLK[14]
(8) I = ((OEOffTime + (n - 1) × PageBurstAccessTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(9) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK[14]
(10) K = ((ADVOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(11) L = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(12) For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst read: N = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst write: N = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(15) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME,

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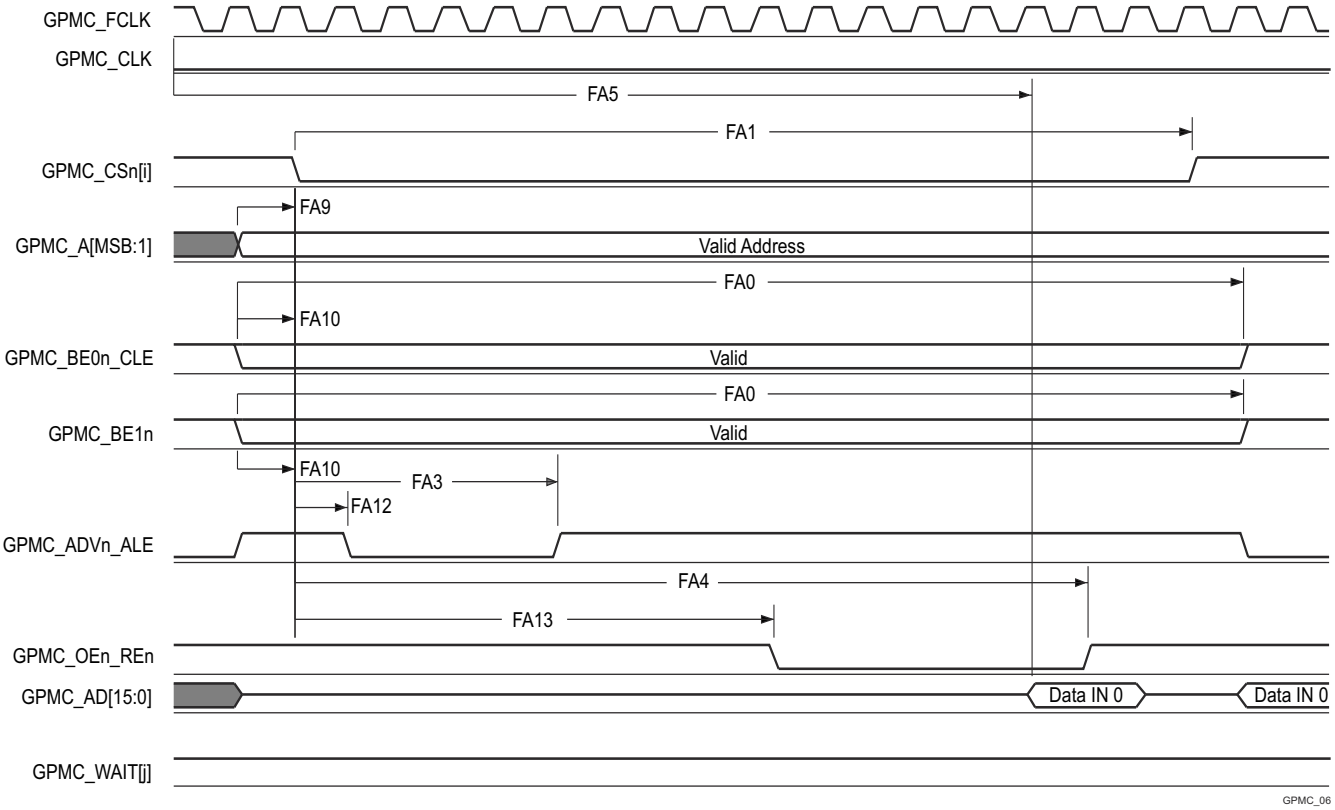
OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], jis equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

図 6-51. GPMC and NOR Flash — Asynchronous Read — Single Word

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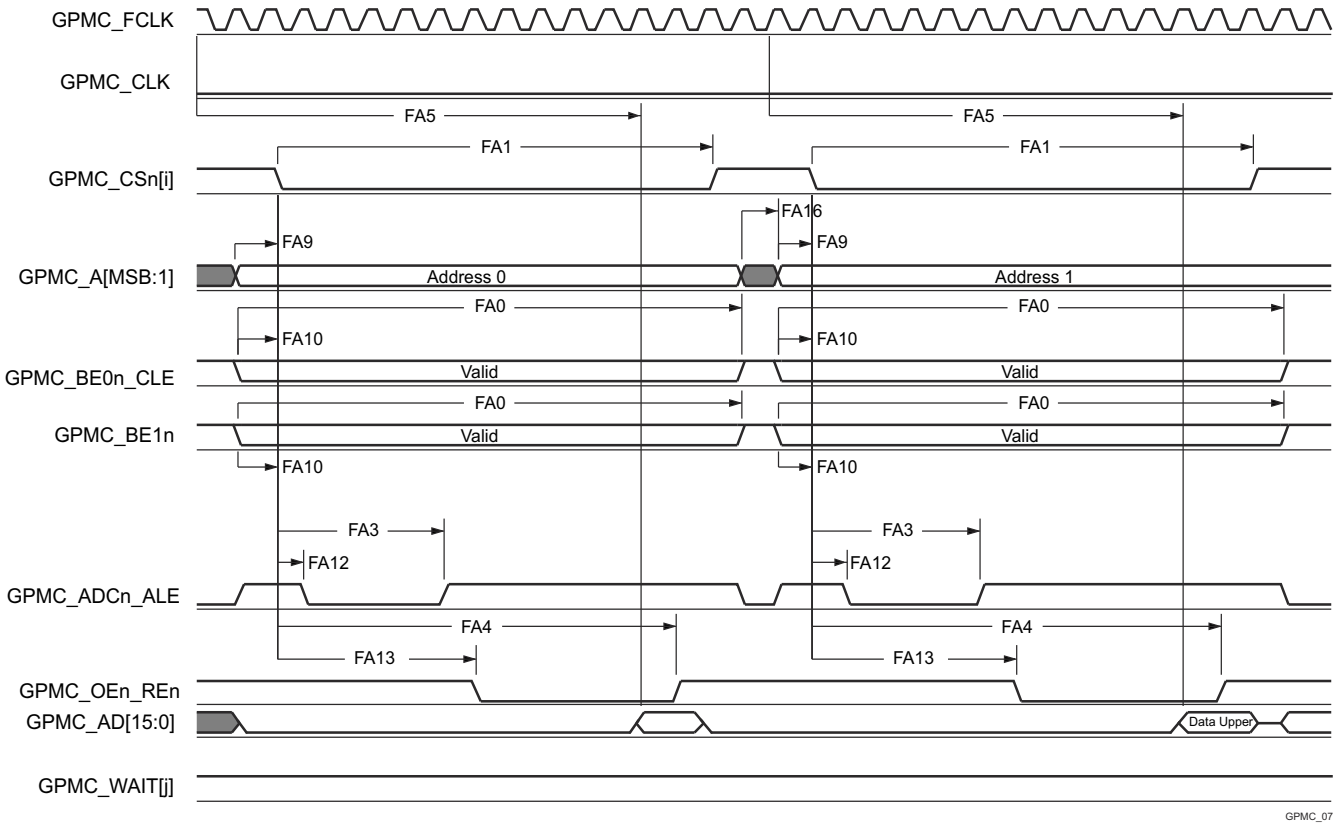
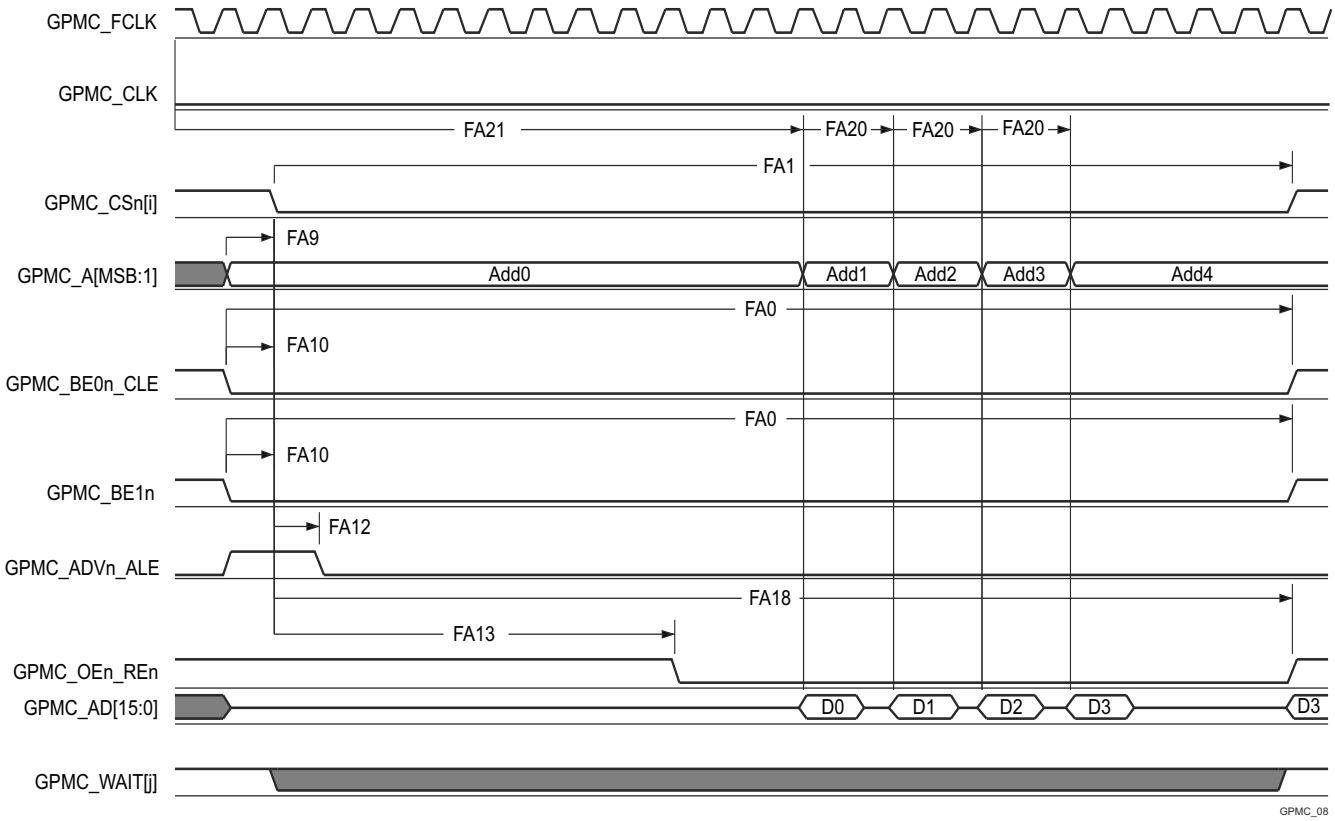


A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

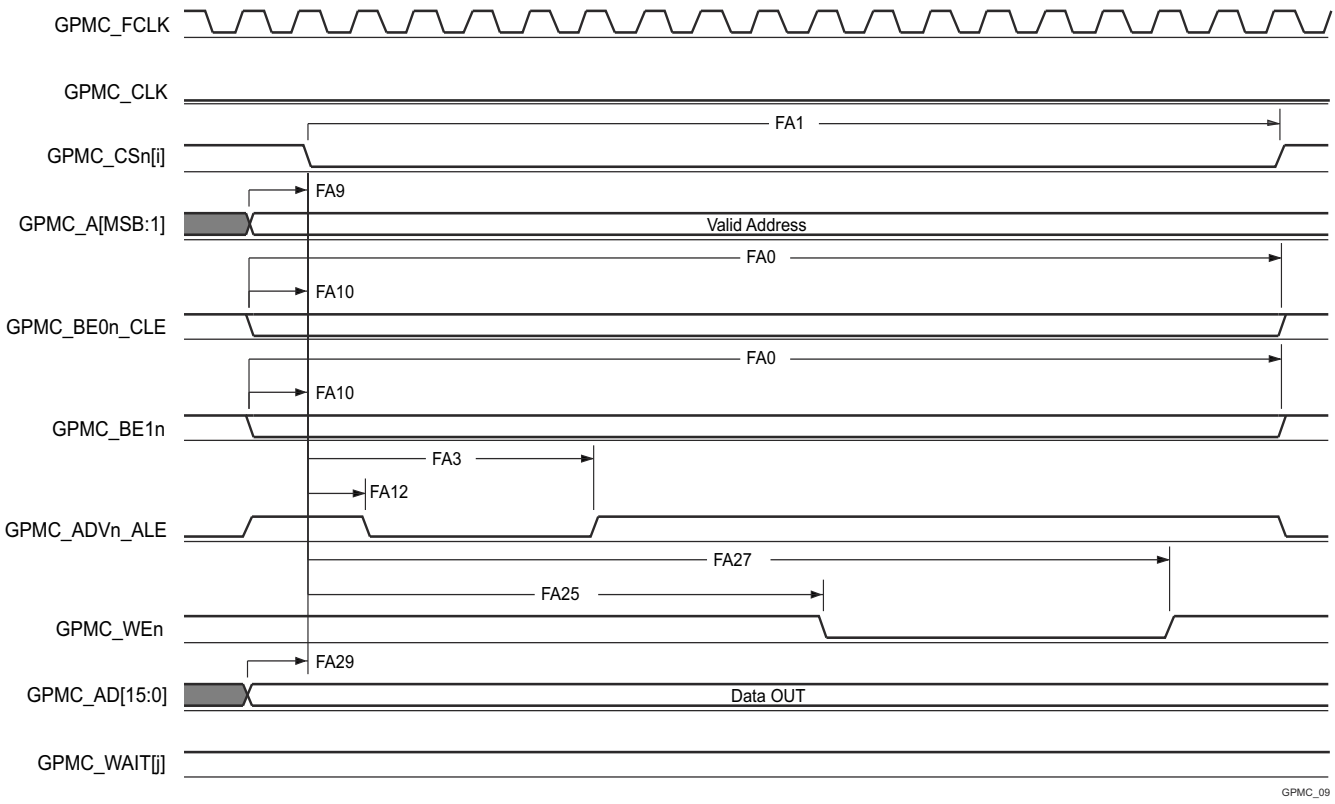
図 6-52. GPMC and NOR Flash — Asynchronous Read — 32–Bit

ADVANCE INFORMATION



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
D. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

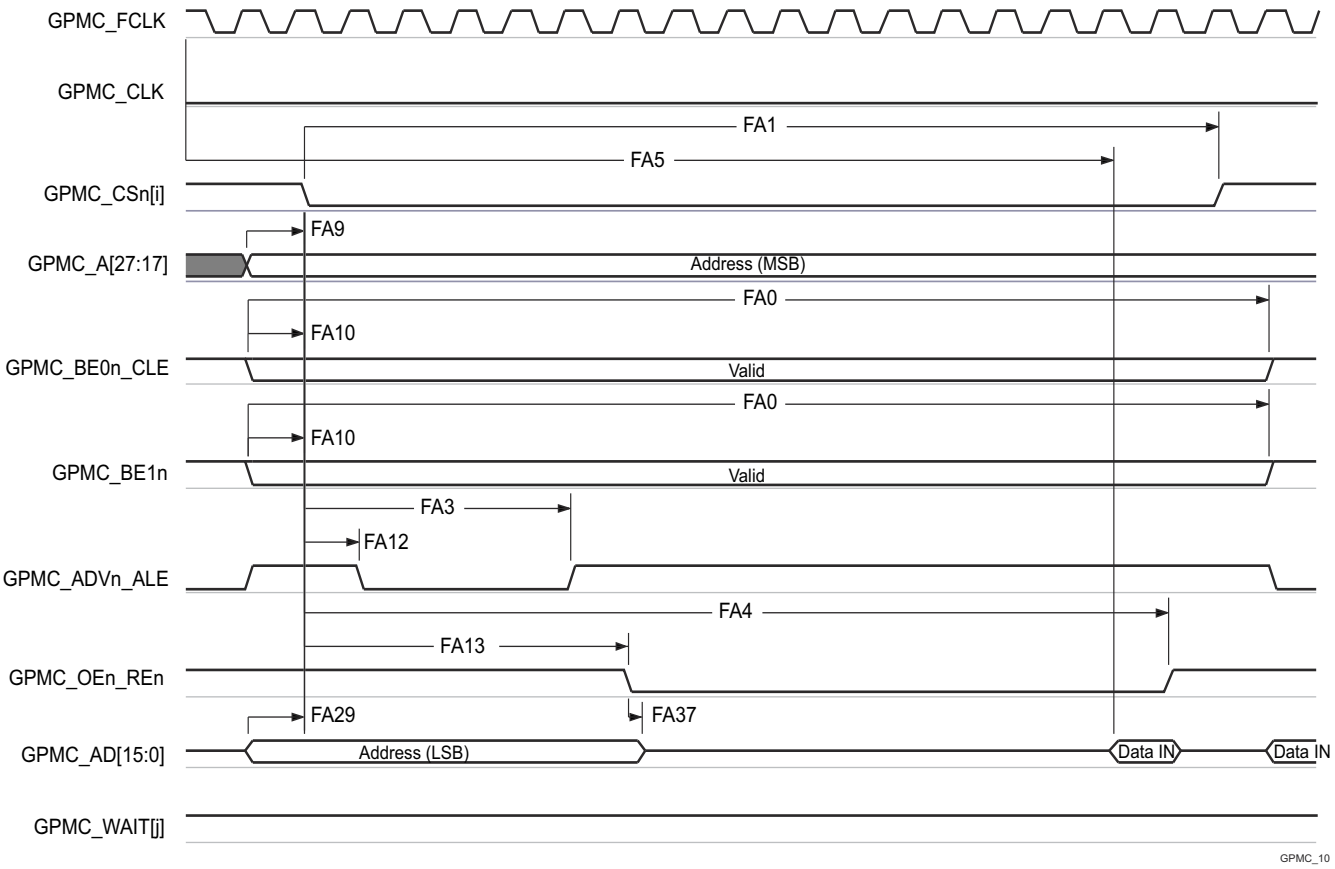
図 6-53. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16–Bit



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

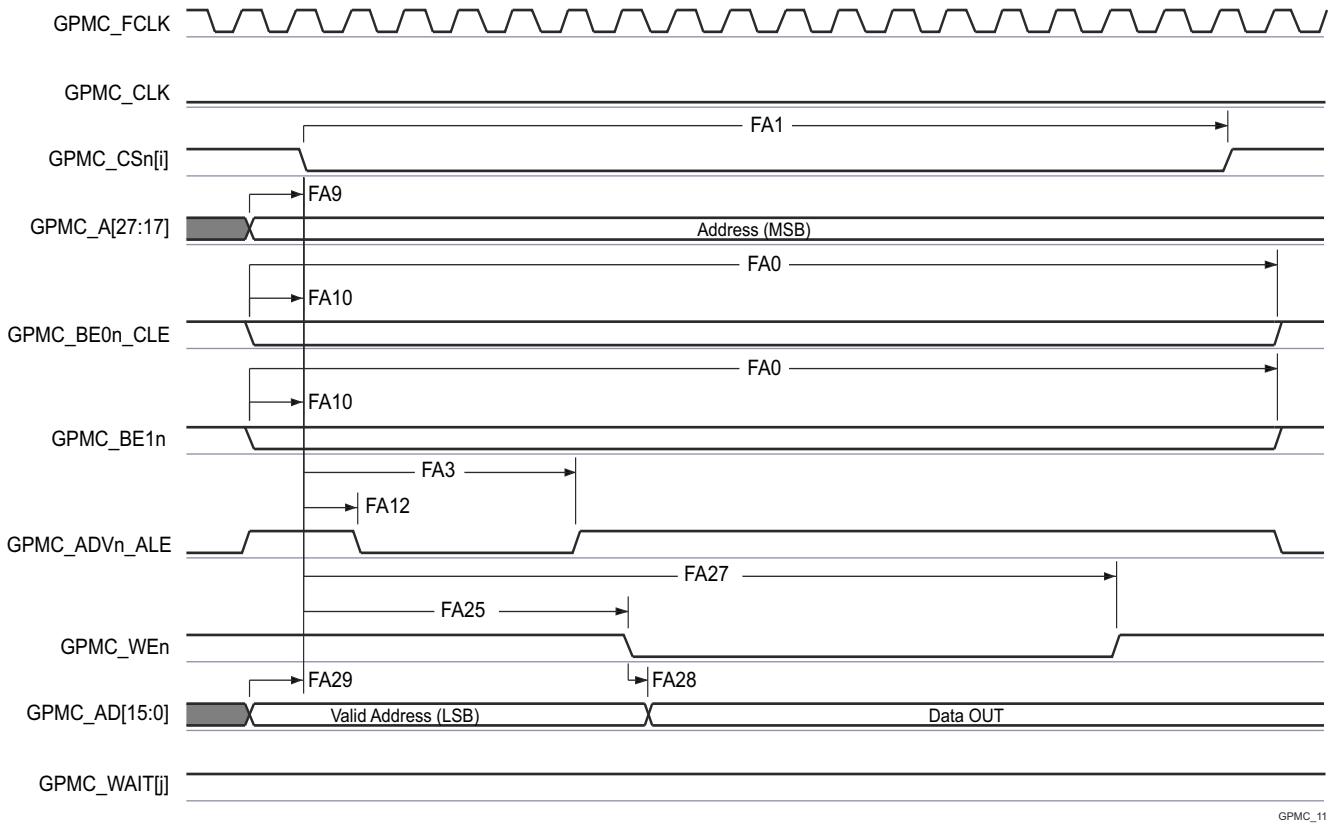
図 6-54. GPMC and NOR Flash — Asynchronous Write — Single Word

ADVANCE INFORMATION



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

図 6-55. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

図 6-56. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word

ADVANCE INFORMATION

6.11.5.12.3 GPMC and NAND Flash — Asynchronous Mode

表 6-67 and 表 6-68 present timing requirements and switching characteristics for GPMC and NAND Flash — Asynchronous Mode.

表 6-67. GPMC and NAND Flash Timing Requirements – Asynchronous Mode

see 図 6-59

NO.	PARAMETER	DESCRIPTION	MODE[4]	MIN / MAX	UNIT
				133 MHz	
GNF12[1]	$t_{acc(d)}$	Access time, input data GPMC_AD[15:0][3]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J[2]	ns

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
(2) J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[3]
(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(4) For div_by_1_mode:

- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY_X1:

- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

表 6-68. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode

see 図 6-57, 図 6-58, 図 6-59 and 図 6-60

NO.	PARAMETER		MODE[4]	MIN	MAX	UNIT
GNF0	$t_{w(wenV)}$	Pulse duration, output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	A		ns
GNF1	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i][2] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2	B + 2	ns
GNF2	$t_{w(cleH-wenV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2	C + 2	ns
GNF3	$t_{w(wenV-dV)}$	Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2	D + 2	ns
GNF4	$t_{w(wenIV-dIV)}$	Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E - 2	E + 2	ns
GNF5	$t_{w(wenIV-cleIV)}$	Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2	F + 2	ns
GNF6	$t_{w(wenIV-CSn[i]V)}$	Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CSn[i][2] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G - 2	G + 2	ns
GNF7	$t_{w(aleH-wenV)}$	Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2	C + 2	ns

表 6-68. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode (続き)

see 図 6-57, 図 6-58, 図 6-59 and 図 6-60

NO.	PARAMETER		MODE[4]	MIN	MAX	UNIT
GNF8	$t_{w(wenIV-alelV)}$	Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2	F + 2	ns
GNF9	$t_{c(wen)}$	Cycle time, write	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H	ns
GNF10	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i][2] valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I - 2	I + 2	ns
GNF13	$t_{w(oenV)}$	Pulse duration, output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		K	ns
GNF14	$t_{c(oen)}$	Cycle time, read	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L		ns
GNF15	$t_{w(oenIV-CSn[i]V)}$	Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CSn[i][2] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	M - 2	M + 2	ns

(1) A = (WEOffTime - WEOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[3]
(2) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(4) For div_by_1_mode:

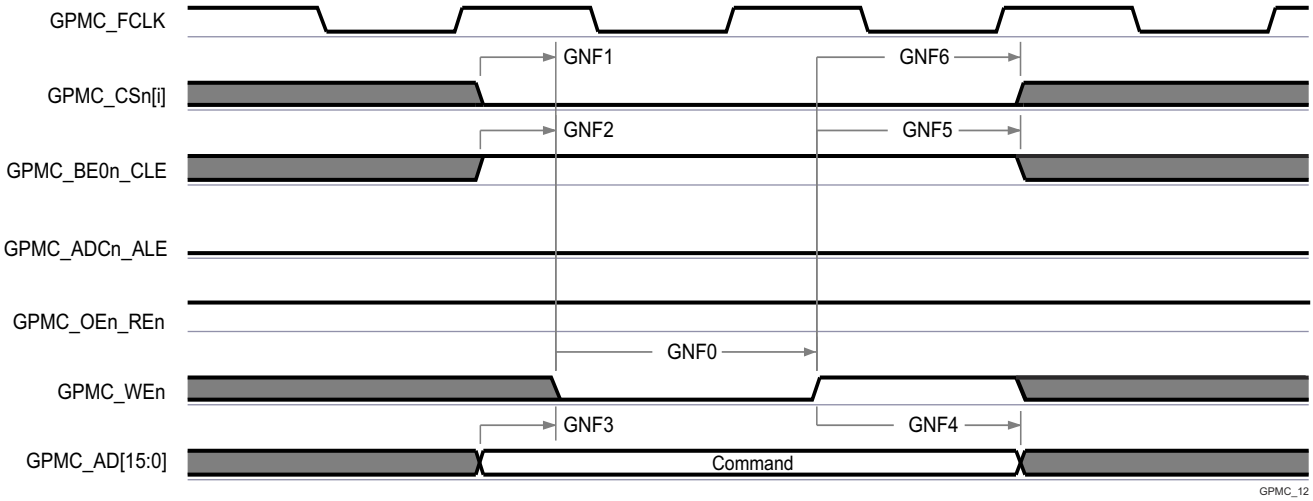
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

For GPMC_FCLK_MUX:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = CPSWHSDIV_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY_X1:

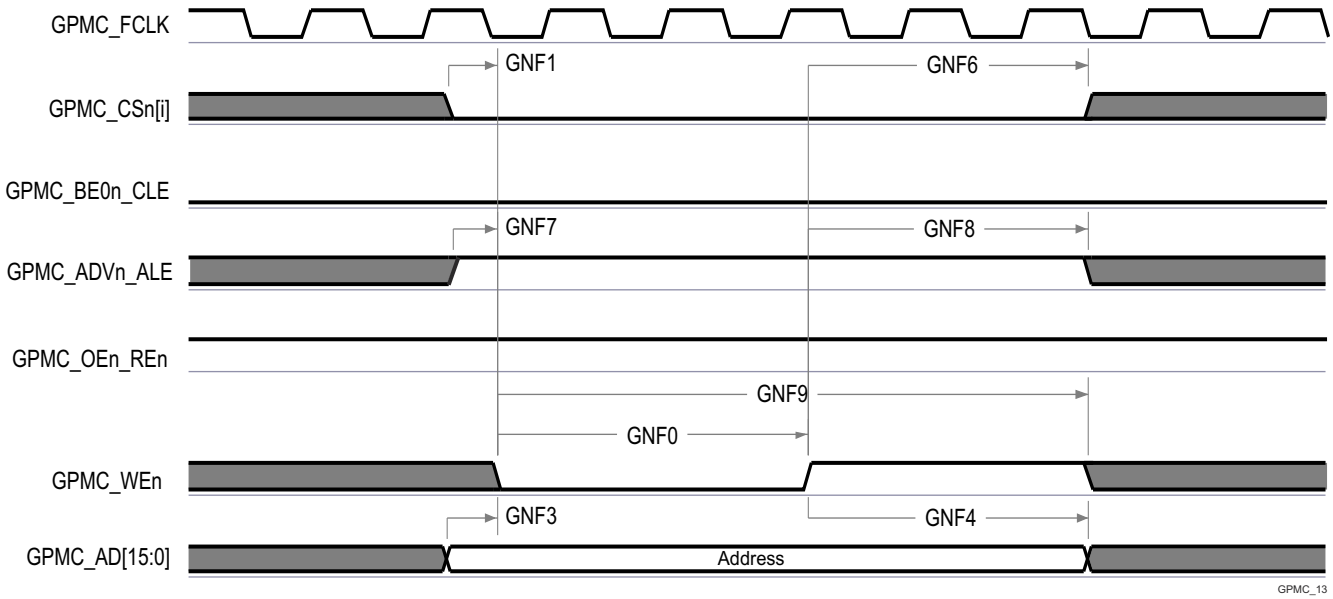
- GPMC_CONFIG1_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

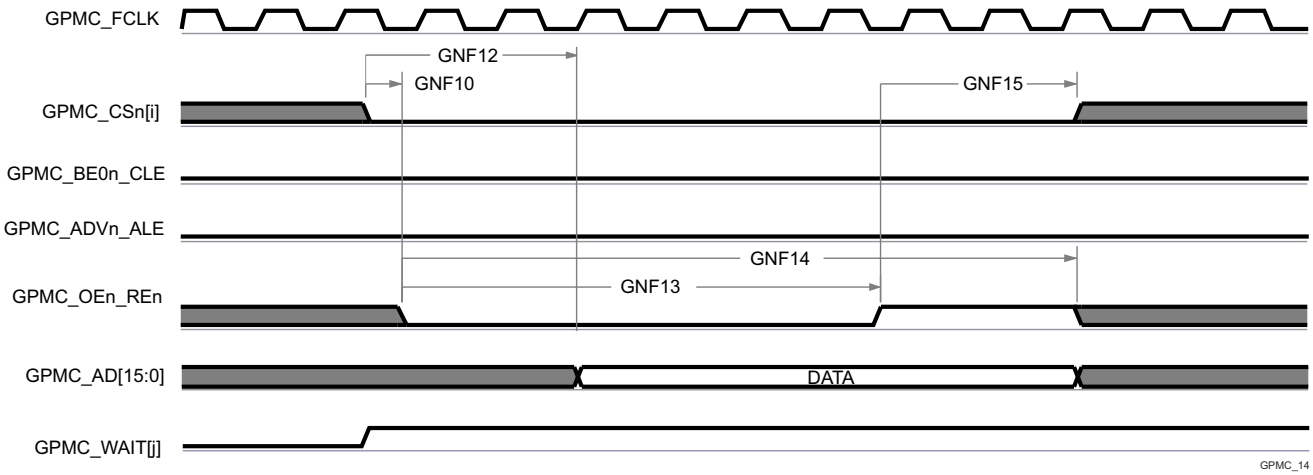
図 6-57. GPMC and NAND Flash — Command Latch Cycle

ADVANCE INFORMATION



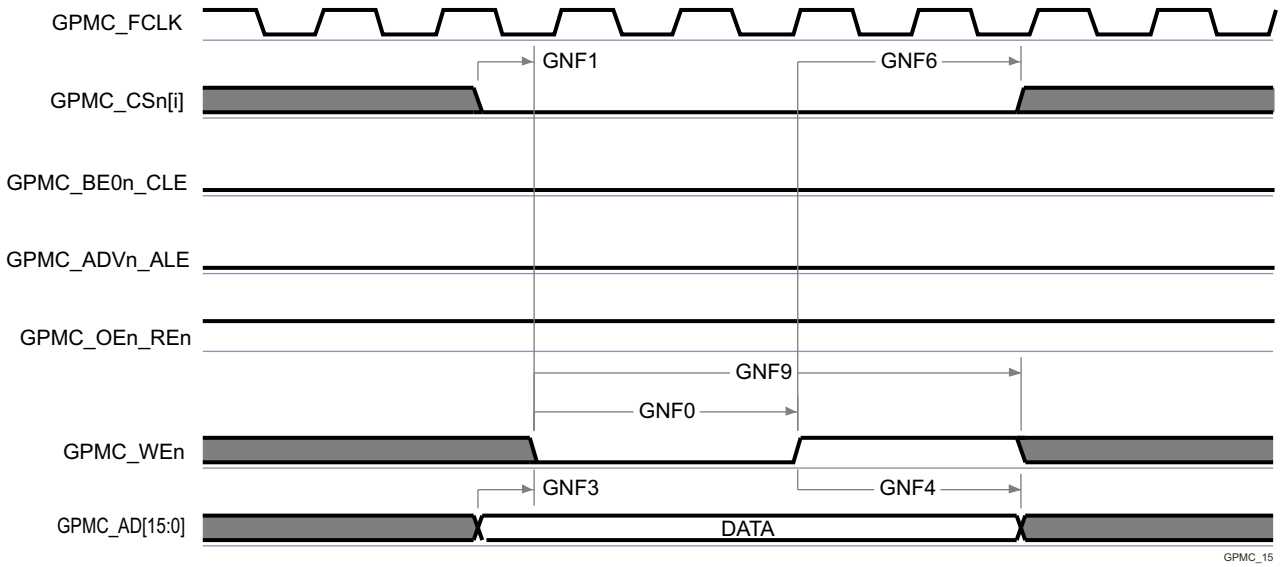
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

図 6-58. GPMC and NAND Flash — Address Latch Cycle



A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
B. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
C. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

図 6-59. GPMC and NAND Flash — Data Read Cycle



A. `In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

図 6-60. GPMC and NAND Flash — Data Write Cycle

6.11.5.13 I2C

The device contains six multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I^{2}C-bus™ specification version 2.1. However, the device IOs are not fully compliant to the I2C electrical specification. The speeds supported and exceptions are described per port below:

- I2C0, I2C1, I2C2, and I2C3
  - Speeds:
    - Standard-mode (up to 100 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Fast-mode (up to 400 Kbits/s)
      - 1.8 V
      - 3.3 V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5 V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.
- MCU_I2C0 and WKUP_I2C0
  - Speeds:
    - Standard-mode (up to 100 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Fast-mode (up to 400 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Hs-mode (up to 3.4 Mbits/s)
      - 1.8 V
  - Exceptions:
    - The IOs associated with these ports were not design to support Hs-mode while operating at 3.3 V. So Hs-mode is limited to 1.8-V operation.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.08 V/ns (or 8E+7 V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.08 V/ns.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5 V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.

注

I2C3 has one or more signals which can be multiplexed to more than one pin. Timing is only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

6.11.5.14 MCAN

表 6-69 and 表 6-70 presents timing conditions and switching characteristics for MCAN.

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

注

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

表 6-69. MCAN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	15	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	5	20	pF

表 6-70. MCAN Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MCAN1	$t_{d(MCAN\_TX)}$	Delay time, transmit shift register to MCANn_TX		10	ns
MCAN2	$t_{d(MCAN\_RX)}$	Delay time, MCANn_RX to receive shift register		10	ns

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

ADVANCE INFORMATION

6.11.5.15 MCASP

注

McASP has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

表 6-71, 表 6-72, 図 6-61, 表 6-73, and 図 6-62 present timing conditions, requirements, and switching characteristics for MCASP.

表 6-71. MCASP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.7	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	10	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	100	1100	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

表 6-72. MCASP Timing Requirements

see 図 6-61

NO.			MODE(1)	MIN	MAX	UNIT
ASP1	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X(4)		20		ns
ASP2	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X(4) high or low		0.5P(2) - 1.53		ns
ASP3	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X(4)		20		ns
ASP4	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X(4) high or low		0.5R(3) - 1.53		ns
ASP5	$t_{su(AFSRX-ACLKRX)}$	Setup time, MCASP[x]_AFSR/X(4) input valid before MCASP[x]_ACLKR/X(4)	ACLKR/X int	9.29		ns
			ACLKR/X ext in/out	4		
ASP6	$t_{h(ACLKRX-AFSRX)}$	Hold time, MCASP[x]_AFSR/X(4) input valid after MCASP[x]_ACLKR/X(4)	ACLKR/X int	-1		ns
			ACLKR/X ext in/out	1.6		
ASP7	$t_{su(AXR-ACLKRX)}$	Setup time, MCASP[x]_AXR(4) input valid before MCASP[x]_ACLKR/X(4)	ACLKR/X int	9.29		ns
			ACLKR/X ext in/out	4		
ASP8	$t_{h(ACLKRX-AXR)}$	Hold time, MCASP[x]_AXR(4) input valid after MCASP[x]_ACLKR/X(4)	ACLKR/X int	-1		ns
			ACLKR/X ext in/out	1.6		

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns. For details on AHCLKR/X clock source options, see the McASP Clocks table in the Multichannel Audio Serial Port (MCASP) section of the Module Integration chapter found in the Technical Reference Manual.
(3) R = ACLKR/X period in ns.
(4) x in MCASP[x]_* is 0, 1 or 2

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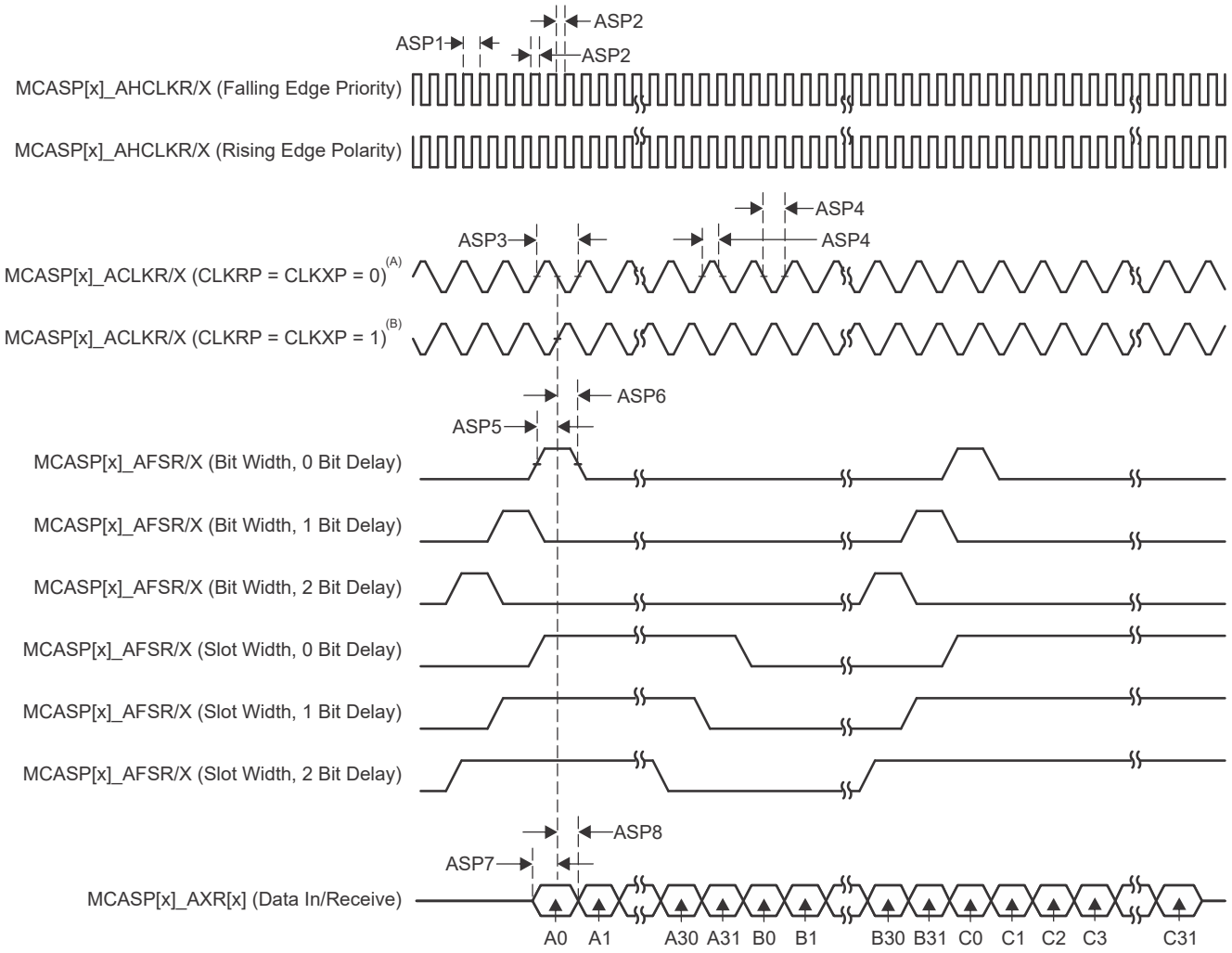


A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

図 6-61. MCASP Timing Requirements

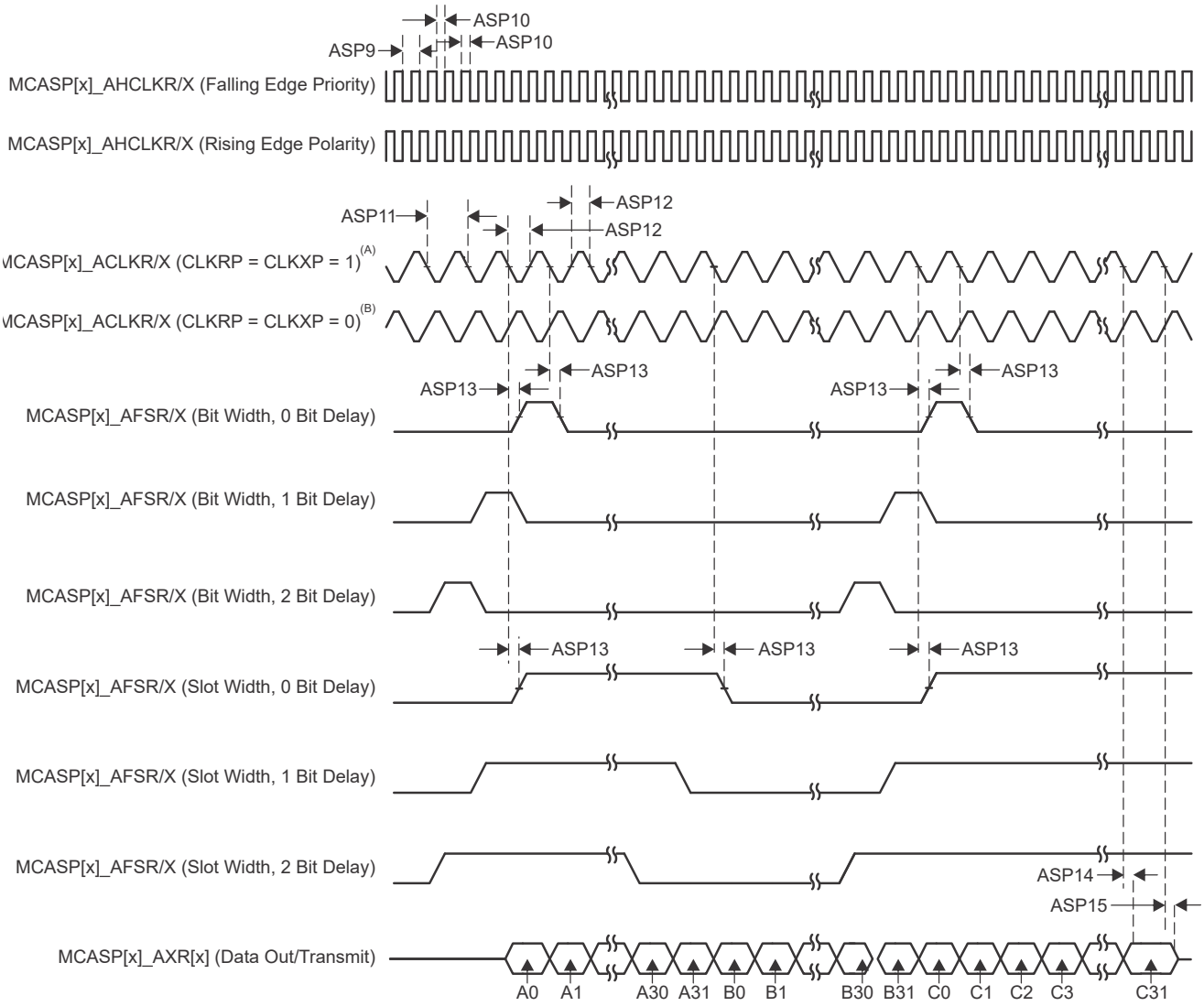
ADVANCE INFORMATION

表 6-73. MCASP Switching Characteristics

see 図 6-62

NO.	PARAMETER	DESCRIPTION	MODE(1)	MIN	MAX	UNIT
ASP9	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X(4)		20		ns
ASP10	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X(4) high or low		0.5P(2) - 2		ns
ASP11	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X(4)		20		ns
ASP12	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X(4) high or low		0.5R(3) - 2		ns
ASP13	$t_{d(ACLKRX-AFSRX)}$	Delay time, MCASP[x]_ACLKR/X(4) transmit edge to MCASP[x]_AFSR/X(4) output valid	ACLKR/X int	-1	7.25	ns
			ACLKR/X ext in/out	-15.29	12.84	
ASP14	$t_{d(ACLKX-AXR)}$	Delay time, MCASP[x]_ACLKX(4) transmit edge to MCASP[x]_AXR(4) output valid	ACLKR/X int	-1	7.25	ns
			ACLKR/X ext in/out	-15.29	12.84	
ASP15	$t_{dis(ACLKX-AXR)}$	Disable time, MCASP[x]_ACLKX(4) transmit edge to MCASP[x]_AXR(4) output high impedance	ACLKR/X int	-1	7.25	ns
			ACLKR/X ext in/out	-14.9	14	

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns. For details on AHCLKR/X clock source options, see the McASP Clocks table in the Multichannel Audio Serial Port (MCASP) section of the Module Integration chapter found in the Technical Reference Manual.
(3) R = ACLKR/X period in ns.
(4) x in MCASP[x]_* is 0, 1 or 2



A. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

図 6-62. MCASP Switching Characteristics

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

ADVANCE INFORMATION

6.11.5.16 MCSPI

注

McSPI has one or more signals which can be multiplexed to more than one pin. Timing requirements and switching characteristics defined in this section are only valid for specific pin combinations known as IOSETs. Valid pin combinations or IOSETs for this interface are defined in the **SysConfig-PinMux Tool**.

For more details about features and additional description information on the device Serial Port Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 6-74 presents timing conditions for MCSPI.

表 6-74. MCSPI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	8.5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	6	12	pF

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

6.11.5.16.1 MCSPI — Controller Mode

表 6-75, 図 6-63, 表 6-76, and 図 6-64 present timing requirements and switching characteristics for SPI – Controller Mode.

表 6-75. MCSPI Timing Requirements – Controller Mode

see 図 6-63

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SM4	$t_{su(POCI-SPICLK)}$	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	2.8		ns
SM5	$t_{h(SPICLK-POCI)}$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	3		ns

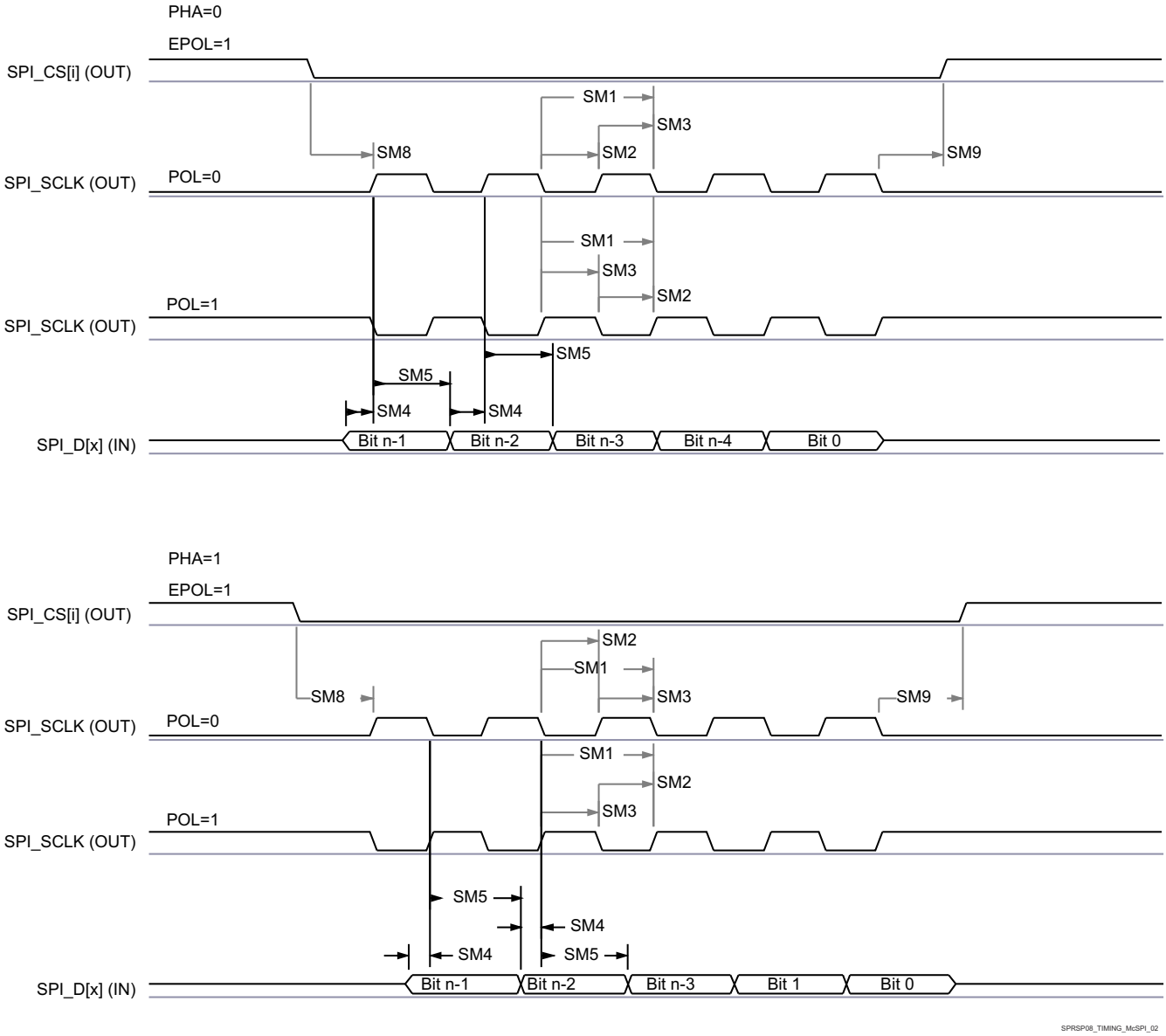


図 6-63. SPI Controller Mode Receive Timing

ADVANCE INFORMATION

表 6-76. MCSPI Switching Characteristics - Controller Mode

see 図 6-64

NO.	PARAMETER			MIN	MAX	UNIT
SM1	$t_{c(SPICLK)}$	Cycle time, SPIn_CLK		20		ns
SM2	$t_{w(SPICLKL)}$	Pulse duration, SPIn_CLK low		0.5P - 1 (1)		ns
SM3	$t_{w(SPICLKH)}$	Pulse duration, SPIn_CLK high		0.5P - 1 (1)		ns
SM6	$t_{d(SPICLK-PICO)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]		-3	2.5	ns
SM7	$t_{d(CS-PICO)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]		5		ns
SM8	$t_{d(CS-SPICLK)}$	Delay time, SPIn_CSi active to SPIn_CLK first edge	PHA = 0	B - 4 (2)		ns
			PHA = 1	A - 4 (3)		ns
SM9	$t_{d(SPICLK-CS)}$	Delay time, SPIn_CLK last edge to SPIn_CSi inactive	PHA = 0	A - 4 (4)		ns
			PHA = 1	B - 4 (5)		ns

(1) P = SPIn_CLK period in ns.

(2) T_ref is the period of the McSPI functional clock in ns. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.
- When Fratio = 1; B = (TCS(i) + 0.5) * T_ref.
- When Fratio ≥ 2 and even value; B = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; B = ((TCS(i) * Fratio) + ((Fratio + 1) / 2)) * T_ref.

(3) T_ref is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.
- When Fratio = 1; A = (TCS(i) + 1) * T_ref.
- When Fratio ≥ 2 and even value; A = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; A = ((TCS(i) * Fratio) + ((Fratio - 1) / 2)) * T_ref.

(4) T_ref is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.
- When Fratio = 1; A = (TCS(i) + 1) * T_ref.
- When Fratio ≥ 2 and even value; A = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; A = ((TCS(i) * Fratio) + ((Fratio + 1) / 2)) * T_ref.

(5) T_ref is the period of the McSPI functional clock. Fratio is the divide ratio of McSPI functional clock frequency to SPIn_CLK clock frequency, controlled by the CLKD and CLKG bit fields in the MSPI_CH(i)CONF register and the EXTCLK bit field in the MSPI_CH(i)CTRL register. TCS(i) is the value programmed into the chip select time control bit field of the MSPI_CH(i)CONF register.
- When Fratio = 1; B = (TCS(i) + 0.5) * T_ref.
- When Fratio ≥ 2 and even value; B = (TCS(i) + 0.5) * Fratio * T_ref.
- When Fratio ≥ 3 and odd value; B = ((TCS(i) * Fratio) + ((Fratio - 1) / 2)) * T_ref.

ADVANCE INFORMATION

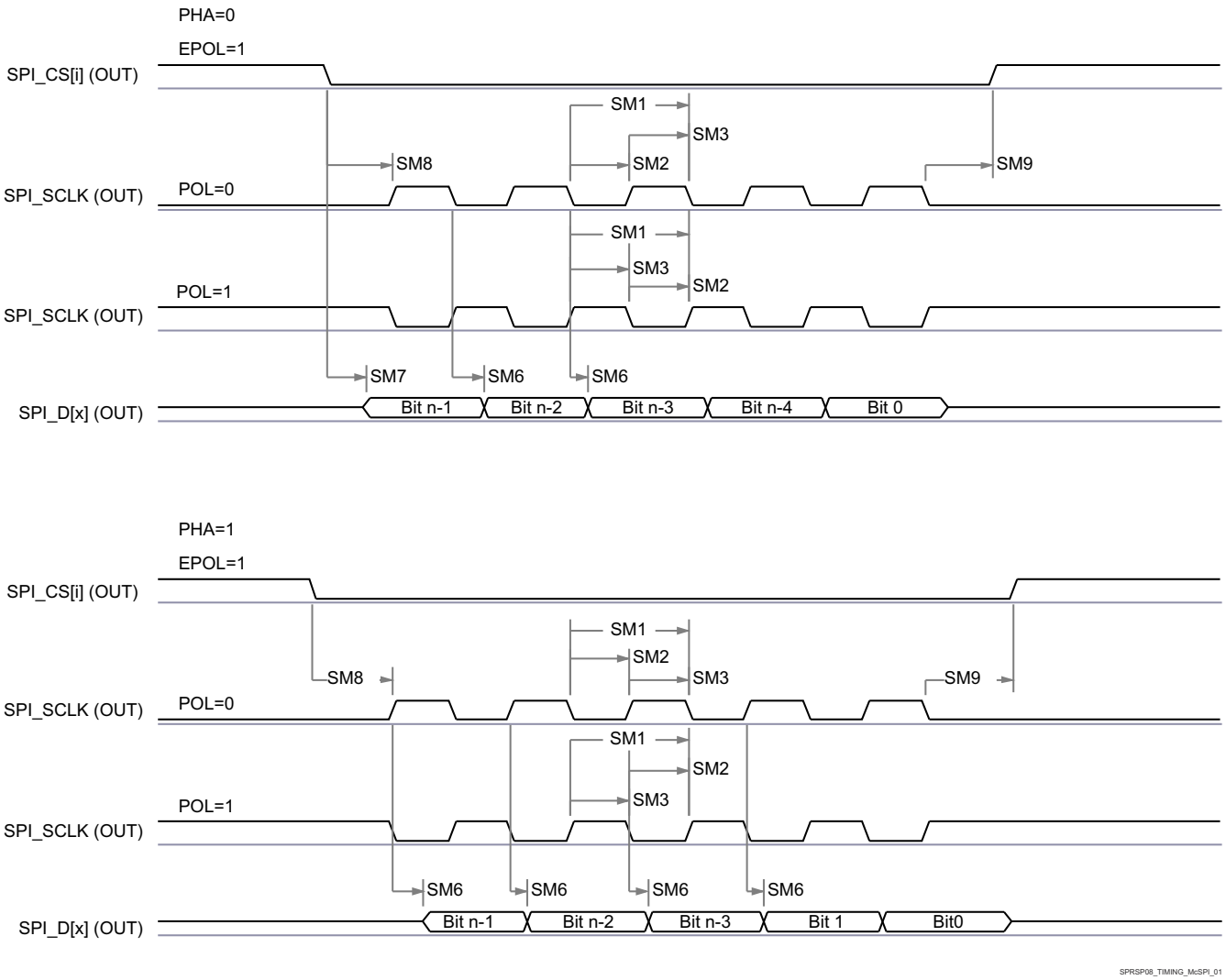


図 6-64. SPI Controller Mode Transmit Timing

ADVANCE INFORMATION

6.11.5.16.2 MCSPI — Peripheral Mode

表 6-77, 図 6-65, 表 6-78, and 図 6-66 present timing requirements and switching characteristics for SPI – Peripheral Mode.

表 6-77. MCSPI Timing Requirements – Peripheral Mode

see 図 6-65

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS1	$t_{c(SPICLK)}$	Cycle time, SPIn_CLK	20		ns
SS2	$t_{w(SPICLKL)}$	Pulse duration, SPIn_CLK low	0.45P(1)		ns
SS3	$t_{w(SPICLKH)}$	Pulse duration, SPIn_CLK high	0.45P(1)		ns
SS4	$t_{su(PICO-SPICLK)}$	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	5		ns
SS5	$t_{h(SPICLK-PICO)}$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	5		ns
SS8	$t_{su(CS-SPICLK)}$	Setup time, SPIn_CSi valid before SPIn_CLK first edge	5		ns
SS9	$t_{h(SPICLK-CS)}$	Hold time, SPIn_CSi valid after SPIn_CLK last edge	5		ns

(1) P = SPIn_CLK period in ns.

ADVANCE INFORMATION

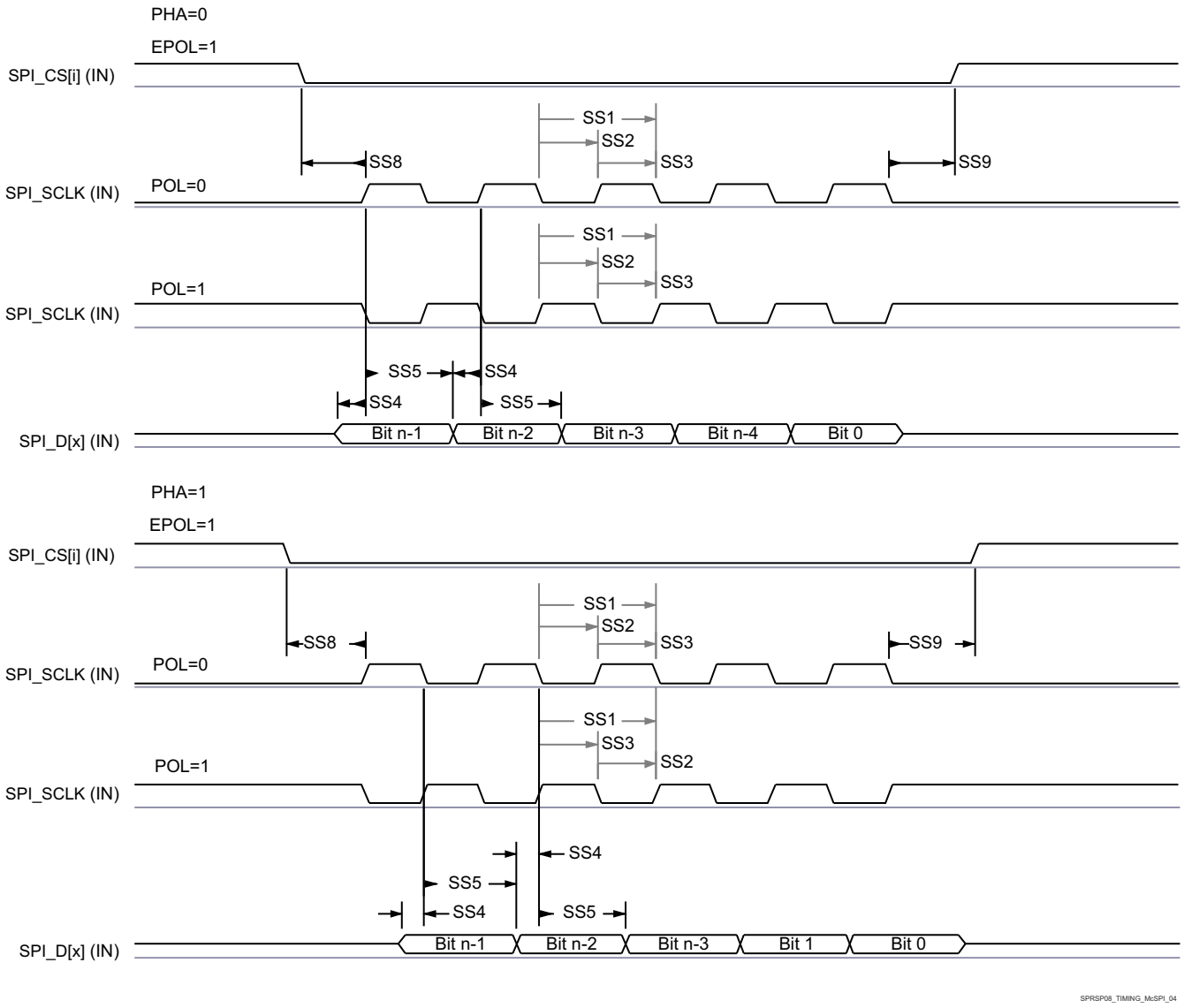


図 6-65. SPI Peripheral Mode Receive Timing

表 6-78. MCSPI Switching Characteristics – Peripheral Mode

see 図 6-66

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS6	$t_{d(SPICLK-POCI)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]	2	17.12	ns
SS7	$t_{sk(CS-POCI)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]	20.95		ns

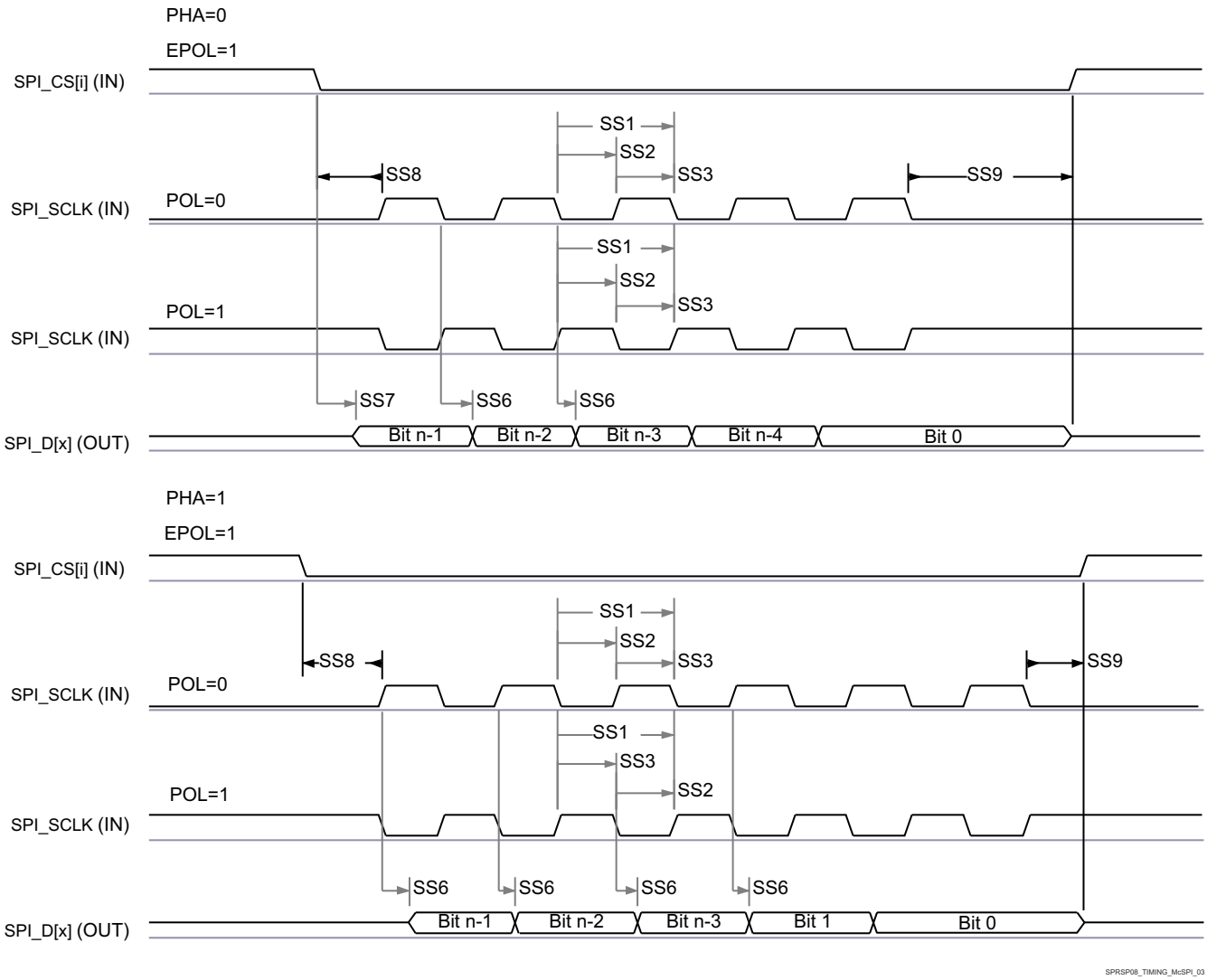


図 6-66. SPI Peripheral Mode Transmit Timing

ADVANCE INFORMATION

6.11.5.17 MMCSD

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the corresponding MMC0, MMC1, and MMC2 subsections within *Signal Descriptions* and *Detailed Description* sections.

注

Some operating modes require software configuration of the MMC DLL delay settings, as shown in 表 6-79 and 表 6-90.

The modes which show a value of "Tuning" in the ITAPDLYSEL column of 表 6-79 and 表 6-90 require a tuning algorithm to be used for optimizing input timing. Refer to the MMCSD Programming Guide in the device TRM for more information on the tuning algorithm and configuration of input delays required to optimize input timing.

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

6.11.5.17.1 MMC0 - eMMC Interface

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and it supports the following eMMC applications:

- Legacy SDR
- High Speed SDR
- High Speed DDR
- HS200
- HS400

表 6-79 presents the required DLL software configuration settings for MMC0 timing modes.

表 6-79. MMC0 DLL Delay Mapping for all Timing Modes

REGISTER NAME		MMCSD0_SS_PHY_CTRL_x_REG								
		x = 4					x = 5			x = 1
BIT FIELD		[31:24]	[20]	[15:12]	[8]	[4:0]	[17:16]	[10:8]	[2:0]	[1]
BIT FIELD NAME		STRBSEL	OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	SELDLYTXCLK SELDLYRXCLK	FRQSEL	CLKBUFSEL	ENDLL
MODE	DESCRIPTION	STROBE DELAY	OUTPUT DELAY ENABLE	OUTPUT DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DLL DELAY CHAIN SELECT	DLL REF FREQUENCY	DELAY BUFFER DURATION	ENABLE DLL
Legacy SDR	8-bit PHY operating 1.8 V, 25 MHz	0x0	0x1	0x1	0x1	0x10	0x3	NA(1)	0x7	0x0
High Speed SDR	8-bit PHY operating 1.8 V, 50 MHz	0x0	0x1	0x1	0x1	0xA	0x3	NA(1)	0x7	0x0
High Speed DDR	8-bit PHY operating 1.8 V, 50 MHz	0x0	0x1	0x6	0x1	0x3	0x0	0x4	NA(1)	0x1
HS200	8-bit PHY operating 1.8 V, 200 MHz	0x0	0x1	0x8	0x1	Tuning(2)	0x0	0x0	NA(1)	0x1
HS400	8-bit PHY operating 1.8 V, 200 MHz	0x77	0x1	0x5	0x1	Tuning(2)	0x0	0x0	NA(1)	0x1

(1) NA means Not Applicable
(2) Tuning means this mode requires a tuning algorithm to be used for optimal input timing

ADVANCE INFORMATION

表 6-80 presents timing conditions for MMC0.

表 6-80. MMC0 Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	Legacy SDR High Speed SDR	0.3	0.9	V/ns
		High Speed DDR (CMD)	0.3	0.9	V/ns
		High Speed DDR (DAT)	0.45	0.9	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	HS400	1	6	pF
		All other modes	1	12	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	All modes	126	756	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	HS200 HS400		8	ps
		High Speed DDR		20	ps
		All other modes		100	ps

ADVANCE INFORMATION

6.11.5.17.1.1 Legacy SDR Mode

表 6-81, 図 6-67, 表 6-82, and 図 6-68 present timing requirements and switching characteristics for MMC0 – Legacy SDR Mode.

表 6-81. MMC0 Timing Requirements – Legacy SDR Mode

see 図 6-67

NO.			MIN	MAX	UNIT
LSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	1.56		ns
LSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	5.44		ns
LSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	1.56		ns
LSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	5.44		ns

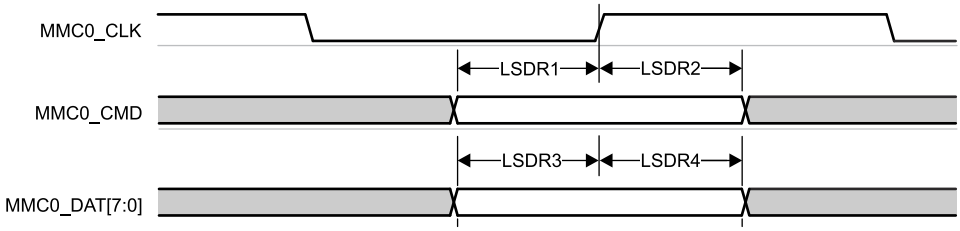


図 6-67. MMC0 – Legacy SDR – Receive Mode

表 6-82. MMC0 Switching Characteristics – Legacy SDR Mode

see 図 6-68

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		25	MHz
LSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	40		ns
LSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	18.7		ns
LSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	18.7		ns
LSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	-2.3	2.9	ns
LSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	-2.3	2.9	ns

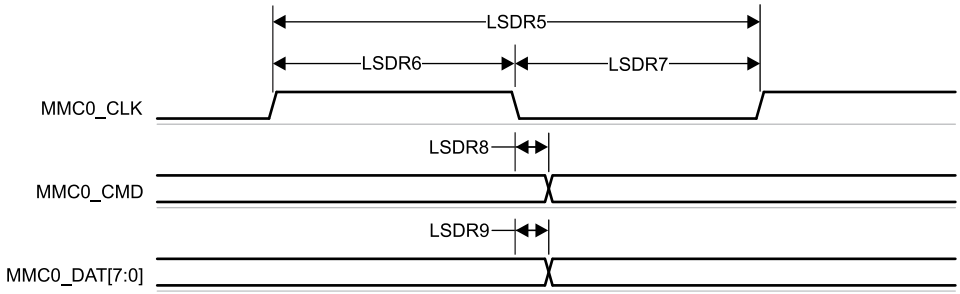


図 6-68. MMC0 – Legacy SDR – Transmit Mode

6.11.5.17.1.2 High Speed SDR Mode

表 6-83, 図 6-69, 表 6-84, and 図 6-70 present timing requirements and switching characteristics for MMC0 – High Speed SDR Mode.

表 6-83. MMC0 Timing Requirements – High Speed SDR Mode

see 図 6-69

NO.			MIN	MAX	UNIT
HSSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.24		ns
HSSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.67		ns
HSSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	2.24		ns
HSSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	2.67		ns

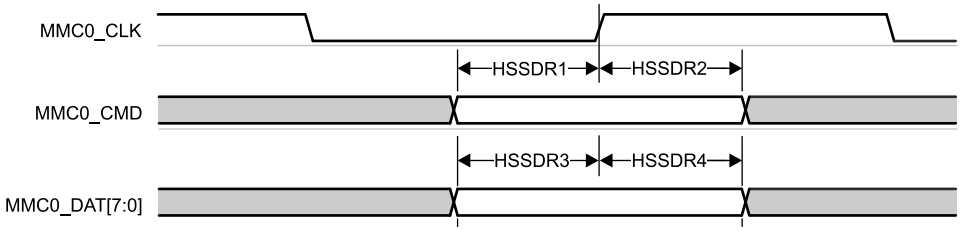


図 6-69. MMC0 – High Speed SDR Mode – Receive Mode

表 6-84. MMC0 Switching Characteristics – High Speed SDR Mode

see 図 6-70

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
HSSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
HSSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
HSSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
HSSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	-2.3	2.9	ns
HSSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	-2.3	2.9	ns

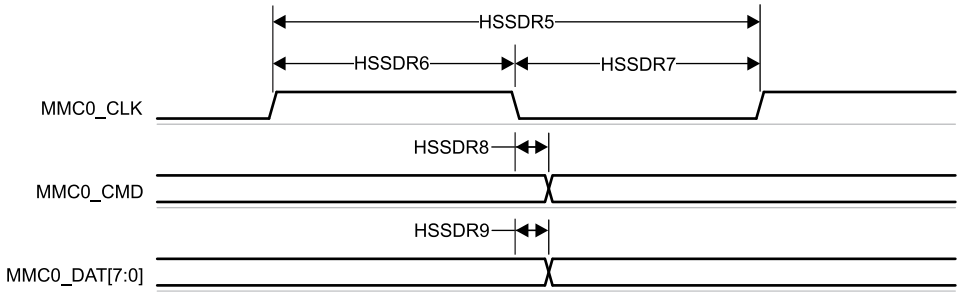


図 6-70. MMC0 – High Speed SDR Mode – Transmit Mode

ADVANCE INFORMATION

6.11.5.17.1.3 High Speed DDR Mode

表 6-85, 図 6-71, 表 6-86, and 図 6-72 present timing requirements and switching characteristics for MMC0 – High Speed DDR Mode.

表 6-85. MMC0 Timing Requirements – High Speed DDR Mode

see 図 6-71

NO.			MIN	MAX	UNIT
HSDDR1	$t_{su(cmdV-clk)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	1.62		ns
HSDDR2	$t_{h(clk-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.52		ns
HSDDR3	$t_{su(dV-clk)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK transition	0.82		ns
HSDDR4	$t_{h(clk-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK transition	1.75		ns

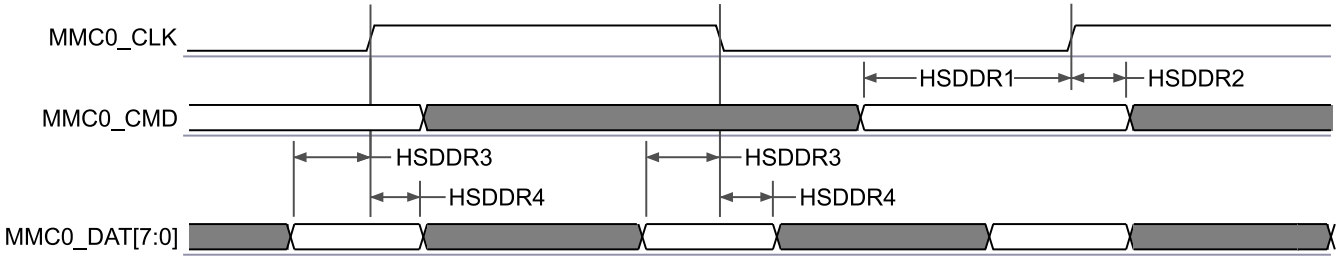


図 6-71. MMC0 – High Speed DDR Mode – Receive Mode

表 6-86. MMC0 Switching Characteristics – High Speed DDR Mode

see 図 6-72

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
HSDDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
HSDDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
HSDDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
HSDDR8	$t_{d(clk-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	3.32	7.64	ns
HSDDR9	$t_{d(clk-dV)}$	Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition	2.82	6.93	ns

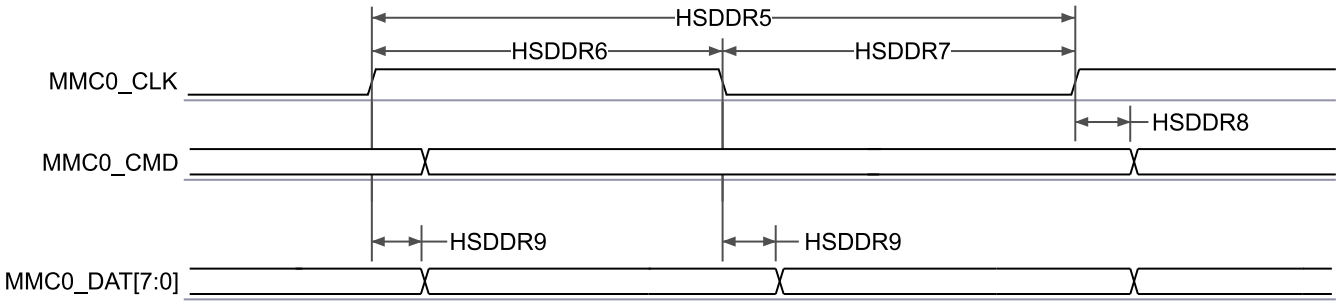


図 6-72. MMC0 – High Speed DDR Mode – Transmit Mode

6.11.5.17.1.4 HS200 Mode

表 6-87 and 図 6-73 present switching characteristics for MMC0 – HS200 Mode.

表 6-87. MMC0 Switching Characteristics – HS200 Mode

see 図 6-73

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
HS2005	$t_{c(clk)}$	Cycle time, MMC0_CLK	5		ns
HS2006	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.12		ns
HS2007	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.12		ns
HS2008	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.07	3.21	ns
HS2009	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[7:0] transition	1.07	3.21	ns

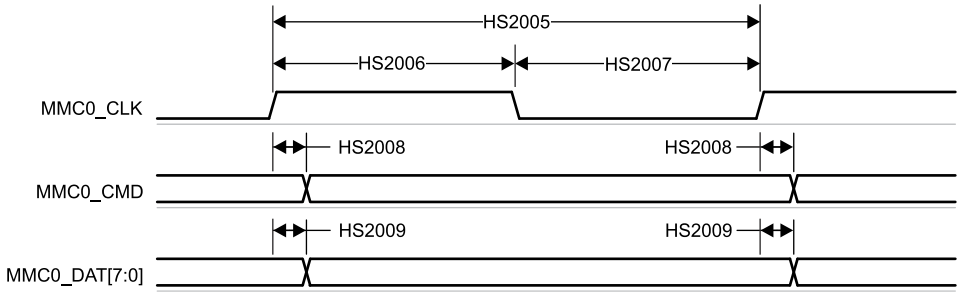


図 6-73. MMC0 – HS200 Mode – Transmit Mode

ADVANCE INFORMATION

6.11.5.17.1.5 HS400 Mode

表 6-88, 図 6-74, 表 6-89, and 図 6-75 present timing requirements and switching characteristics for MMC0 – HS400 Mode.

表 6-88. MMC0 Timing Requirements – HS400 Mode

see 図 6-74

NO.			MIN	MAX	UNIT
HS4000	t_{DSMPW}	Pulse width, MMC0_DS	2.0		ns
HS4001	t_{RQ_DAT}	Input skew, MMC0_DS to MMC0_DAT valid		500	ps
HS4002	t_{RQH_DAT}	Input skew hold, MMC0_DAT invalid to MMC0_DS		500	ps
HS4003	t_{RQ_CMD}	Input skew, MMC0_DS to MMC0_CMD valid		500	ps
HS4004	t_{RQH_CMD}	Input skew hold, MMC0_CMD invalid to MMC0_DS		500	ps

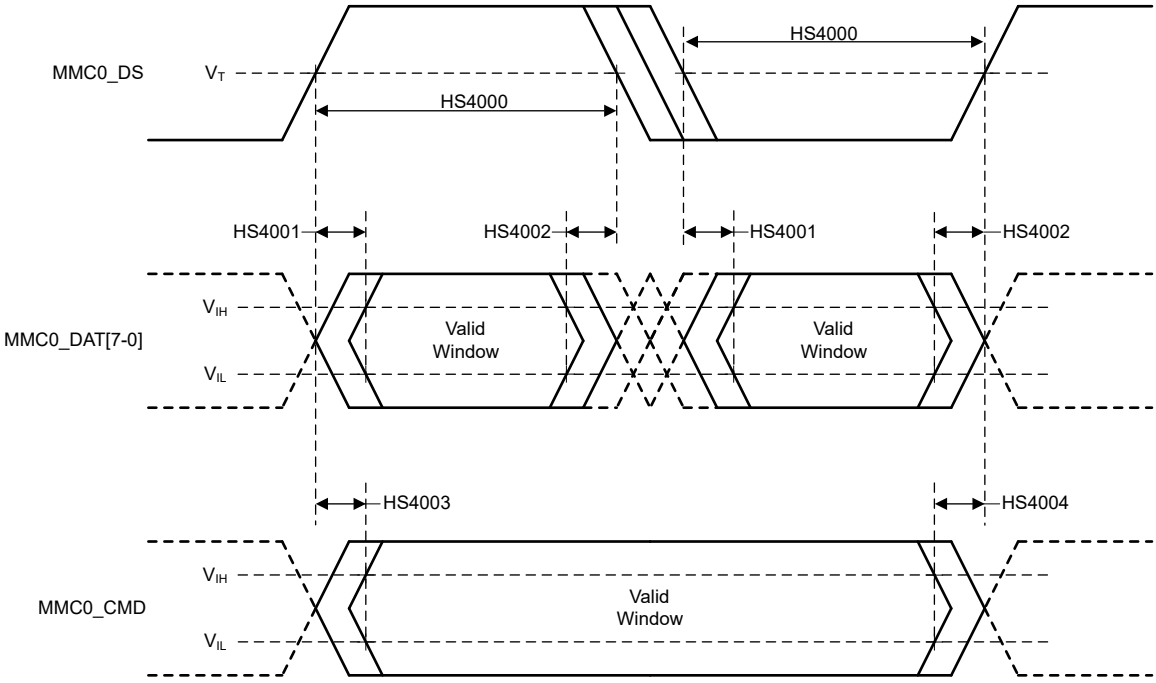


図 6-74. MMC0 – HS400 – Receive Mode

表 6-89. MMC0 Switching Characteristics – HS400 Mode

see 図 6-75

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
HS4005	$t_{c(clkH)}$	Cycle time, MMC0_CLK	5		ns
HS4006	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.24		ns
HS4007	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.24		ns
HS4008	$t_{d(clkH-cmdV)}$	Delay time, MMC0_CLK rising clock edge to MMC0_CMD transition	0.99	3.28	ns
HS4009	$t_{d(clk-dV)}$	Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition	0.59	1.84	ns

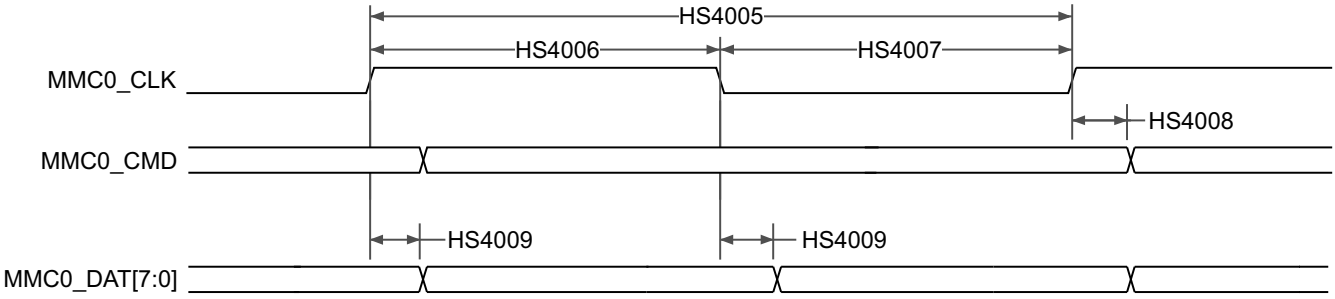


図 6-75. eMMC in – HS400 Mode – Transmitter Mode

ADVANCE INFORMATION

6.11.5.17.2 MMC1/MMC2 - SD/SDIO Interface

MMC1/MMC2 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications:

- Default speed
- High speed
- UHS–I SDR12
- UHS–I SDR25
- UHS–I SDR50
- UHS–I DDR50
- UHS–I SDR104

表 6-90 presents the required DLL software configuration settings for MMC1/2 timing modes.

表 6-90. MMC1/MMC2 DLL Delay Mapping for all Timing Modes

REGISTER NAME		MMCSD1_SS_PHY_CTRL_4_REG/ MMCSD2_SS_PHY_CTRL_4_REG				MMCSD1_SS_PHY_CTRL_5_REG/ MMCSD2_SS_PHY_CTRL_5_REG
BIT FIELD		[20]	[15:12]	[8]	[4:0]	[2:0]
BIT FIELD NAME		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL
MODE	DESCRIPTION	DELAY ENABLE	DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DELAY BUFFER DURATION
Default Speed	4-bit PHY operating 3.3 V, 25 MHz	0x1	0x0	0x1	0x0	0x7
High Speed	4-bit PHY operating 3.3 V, 50 MHz	0x1	0x0	0x1	0x0	0x7
UHS-I SDR12	4-bit PHY operating 1.8 V, 25 MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR25	4-bit PHY operating 1.8 V, 50 MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR50	4-bit PHY operating 1.8 V, 100 MHz	0x1	0xC	0x1	Tuning(1)	0x7
UHS-I DDR50	4-bit PHY operating 1.8 V, 50 MHz	0x1	0x9	0x1	Tuning(1)	0x7
UHS-I SDR104	4-bit PHY operating 1.8, V 200 MHz	0x1	0x6	0x1	Tuning(1)	0x7

(1) Tuning means this mode requires a tuning algorithm to be used for optimal input timing

ADVANCE INFORMATION

表 6-91 presents timing conditions for MMC1.

表 6-91. MMC1/MMC2 Timing Conditions

PARAMETER			MIN	MAX	UNIT
Input Conditions					
SR_I	Input slew rate	Default Speed High Speed	0.69	2.06	V/ns
		UHS–I SDR12 UHS–I SDR25	0.34	1.34	V/ns
		UHS–I DDR50	1	2	V/ns
Output Conditions					
C_L	Output load capacitance	All modes	1	10	pF
PCB Connectivity Requirements					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	UHS–I DDR50	239	1134	ps
		All other modes	126	1386	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	High Speed UHS–I SDR104		8	ps
		UHS–I DDR50		20	ps
		All other modes		100	ps

ADVANCE INFORMATION

6.11.5.17.2.1 Default Speed Mode

表 6-92, 図 6-76, 表 6-93, and 図 6-77 present timing requirements and switching characteristics for MMC1/MMC2 – Default Speed Mode.

表 6-92. Timing Requirements for MMC1/MMC2 – Default Speed Mode

see 図 6-76

NO.			MIN	MAX	UNIT
DS1	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	2.15		ns
DS2	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	1.67		ns
DS3	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	2.15		ns
DS4	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	1.67		ns

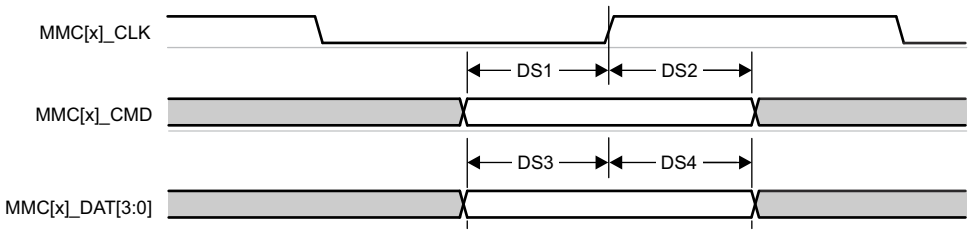


図 6-76. MMC1/MMC2 – Default Speed – Receive Mode

表 6-93. Switching Characteristics for MMC1/MMC2 – Default Speed Mode

see 図 6-77

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		25	MHz
DS5	$t_{c(clk)}$	Cycle time, MMCx_CLK	40		ns
DS6	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	18.7		ns
DS7	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	18.7		ns
DS8	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK falling edge to MMCx_CMD transition	- 1.8	2.2	ns
DS9	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK falling edge to MMCx_DAT[3:0] transition	- 1.8	2.2	ns

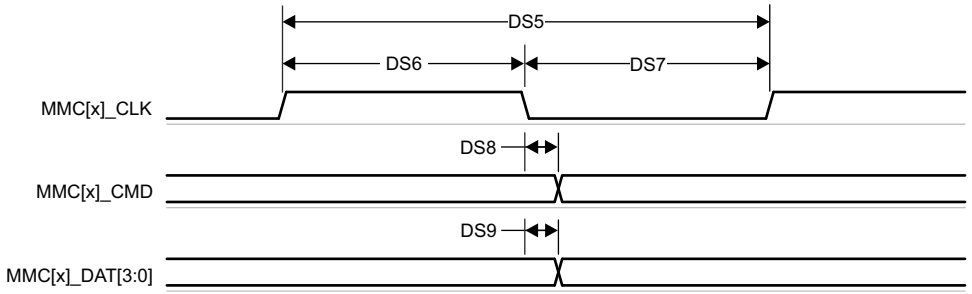


図 6-77. MMC1/MMC2 – Default Speed – Transmit Mode

6.11.5.17.2.2 High Speed Mode

表 6-94, 図 6-78, 表 6-95, and 図 6-79 present timing requirements and switching characteristics for MMC1/MMC2 – High Speed Mode.

表 6-94. Timing Requirements for MMC1/MMC2 – High Speed Mode

see 図 6-78

NO.			MIN	MAX	UNIT
HS1	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	2.24		ns
HS2	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	1.66		ns
HS3	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	2.24		ns
HS4	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	1.66		ns

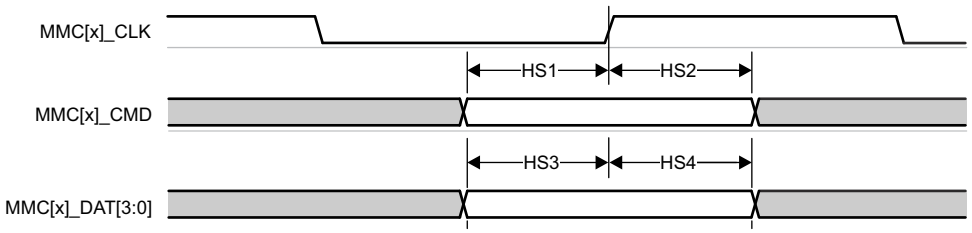


図 6-78. MMC1/MMC2 – High Speed – Receive Mode

表 6-95. Switching Characteristics for MMC1/MMC2 – High Speed Mode

see 図 6-79

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		50	MHz
HS5	$t_{c(clk)}$	Cycle time. MMCx_CLK	20		ns
HS6	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	9.2		ns
HS7	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	9.2		ns
HS8	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK falling edge to MMCx_CMD transition	- 1.8	2.2	ns
HS9	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK falling edge to MMCx_DAT[3:0] transition	- 1.8	2.2	ns

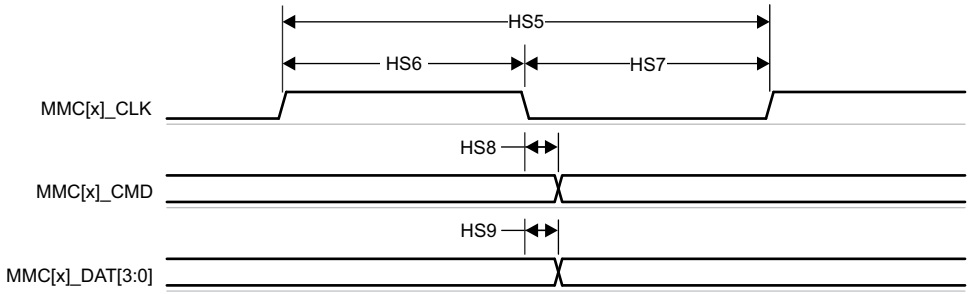


図 6-79. MMC1/MMC2 – High Speed – Transmit Mode

ADVANCE INFORMATION

6.11.5.17.2.3 UHS–I SDR12 Mode

表 6-96, 図 6-80, 表 6-97, and 図 6-81 present timing requirements and switching characteristics for MMC1/MMC2 – UHS-I SDR12 Mode.

表 6-96. Timing Requirements for MMC1/MMC2 – UHS-I SDR12 Mode

see 図 6-80

NO.			MIN	MAX	UNIT
SDR121	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	4.2		ns
SDR122	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	0.87		ns
SDR123	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	4.2		ns
SDR124	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	0.87		ns

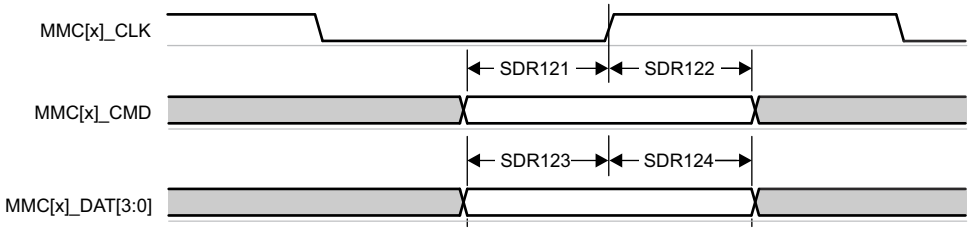


図 6-80. MMC1/MMC2 – UHS-I SDR12 – Receive Mode

表 6-97. Switching Characteristics for MMC1/MMC2 – UHS-I SDR12 Mode

see 図 6-81

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		25	MHz
SDR125	$t_{c(clk)}$	Cycle time, MMCx_CLK	40		ns
SDR126	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	18.7		ns
SDR127	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	18.7		ns
SDR128	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.5	8.6	ns
SDR129	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	1.5	8.6	ns

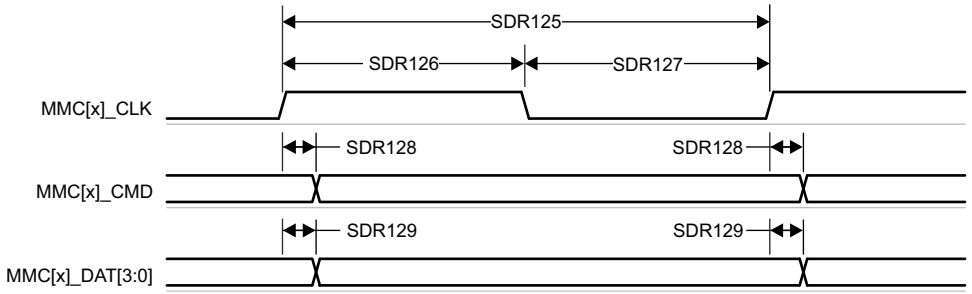


図 6-81. MMC1/MMC2 – UHS-I SDR12 – Transmit Mode

6.11.5.17.2.4 UHS–I SDR25 Mode

表 6-98, 図 6-82, 表 6-99, and 図 6-83 present timing requirements and switching characteristics for MMC1/MMC2 – UHS-I SDR25 Mode.

表 6-98. Timing Requirements for MMC1/MMC2 – UHS-I SDR25 Mode

see 図 6-82

NO.			MIN	MAX	UNIT
SDR251	$t_{su(cmdV-clkH)}$	Setup time, MMCx_CMD valid before MMCx_CLK rising edge	2.15		ns
SDR252	$t_{h(clkH-cmdV)}$	Hold time, MMCx_CMD valid after MMCx_CLK rising edge	1.27		ns
SDR253	$t_{su(dV-clkH)}$	Setup time, MMCx_DAT[3:0] valid before MMCx_CLK rising edge	2.15		ns
SDR254	$t_{h(clkH-dV)}$	Hold time, MMCx_DAT[3:0] valid after MMCx_CLK rising edge	1.27		ns

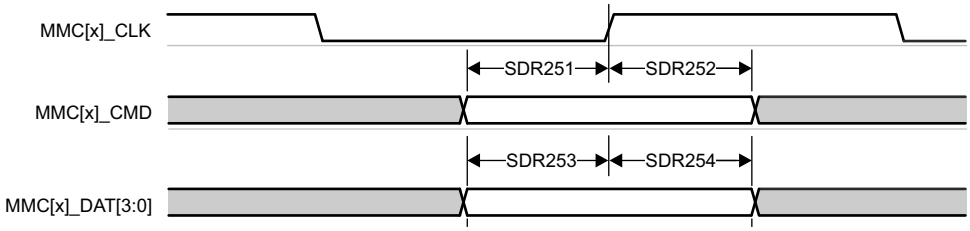


図 6-82. MMC1/MMC2 – UHS-I SDR25 – Receive Mode

表 6-99. Switching Characteristics for MMC1/MMC2 – UHS-I SDR25 Mode

see 図 6-83

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		50	MHz
SDR255	$t_{c(clk)}$	Cycle time, MMCx_CLK	20		ns
SDR256	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	9.2		ns
SDR257	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	9.2		ns
SDR258	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	2.4	8.1	ns
SDR259	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	2.4	8.1	ns

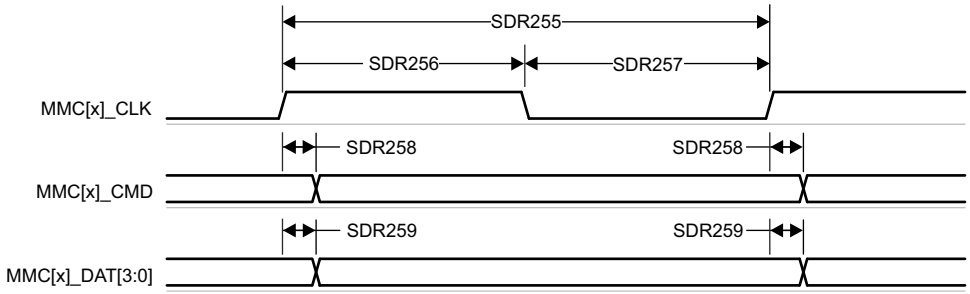


図 6-83. MMC1/MMC2 – UHS-I SDR25 – Transmit Mode

ADVANCE INFORMATION

6.11.5.17.2.5 UHS–I SDR50 Mode

表 6-100 and 図 6-84 presents switching characteristics for MMC1/MMC2 – UHS-I SDR50 Mode.

表 6-100. Switching Characteristics for MMC1/MMC2 – UHS-I SDR50 Mode

see 図 6-84

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		100	MHz
SDR505	$t_{c(clk)}$	Cycle time, MMCx_CLK	10		ns
SDR506	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	4.45		ns
SDR507	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	4.45		ns
SDR508	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.2	6.35	ns
SDR509	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	1.2	6.35	ns

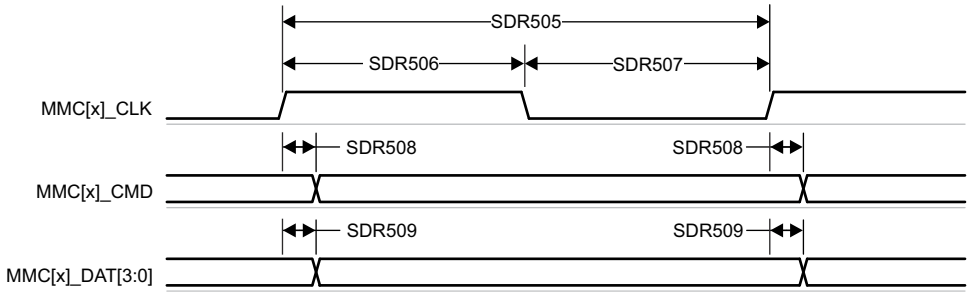


図 6-84. MMC1/MMC2 – UHS-I SDR50 – Transmit Mode

ADVANCE INFORMATION

6.11.5.17.2.6 UHS–I DDR50 Mode

表 6-101 and 図 6-85 present switching characteristics for MMC1/MMC2 – UHS-I DDR50 Mode.

表 6-101. Switching Characteristics for MMC1/MMC2 – UHS-I DDR50 Mode

see 図 6-85

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		50	MHz
DDR505	$t_{c(clk)}$	Cycle time, MMCx_CLK	20		ns
DDR506	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	9.2		ns
DDR507	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	9.2		ns
DDR508	$t_{d(clk-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.12	6.43	ns
DDR509	$t_{d(clk-dV)}$	Delay time, MMCx_CLK transition to MMCx_DAT[3:0] transition	1.12	6.43	ns

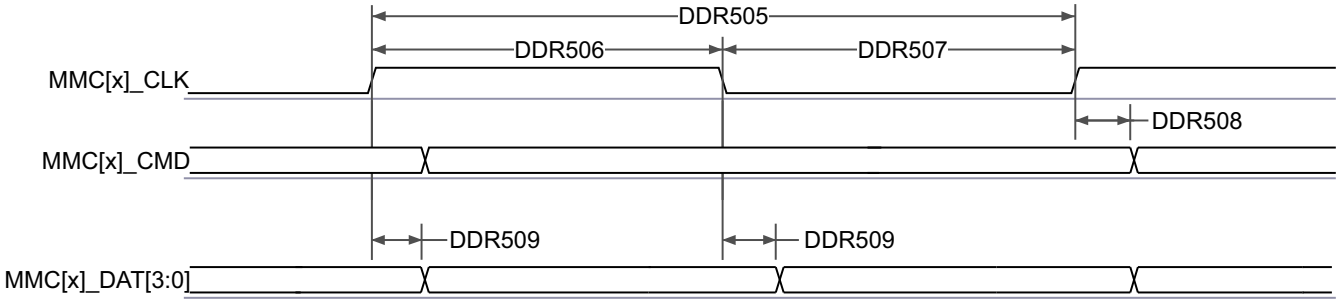


図 6-85. MMC1/MMC2 – UHS-I DDR50 – Transmit Mode

ADVANCE INFORMATION

6.11.5.17.2.7 UHS–I SDR104 Mode

表 6-102 and 図 6-86 present switching characteristics for MMC1/MMC2 – UHS-I SDR104 Mode.

表 6-102. Switching Characteristics for MMC1/MMC2 – UHS-I SDR104 Mode

see 図 6-86

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMCx_CLK		200	MHz
SDR1045	$t_{c(clk)}$	Cycle time, MMCx_CLK	5		ns
SDR1046	$t_{w(clkH)}$	Pulse duration, MMCx_CLK high	2.12		ns
SDR1047	$t_{w(clkL)}$	Pulse duration, MMCx_CLK low	2.12		ns
SDR1048	$t_{d(clkL-cmdV)}$	Delay time, MMCx_CLK rising edge to MMCx_CMD transition	1.07	3.21	ns
SDR1049	$t_{d(clkL-dV)}$	Delay time, MMCx_CLK rising edge to MMCx_DAT[3:0] transition	1.07	3.21	ns

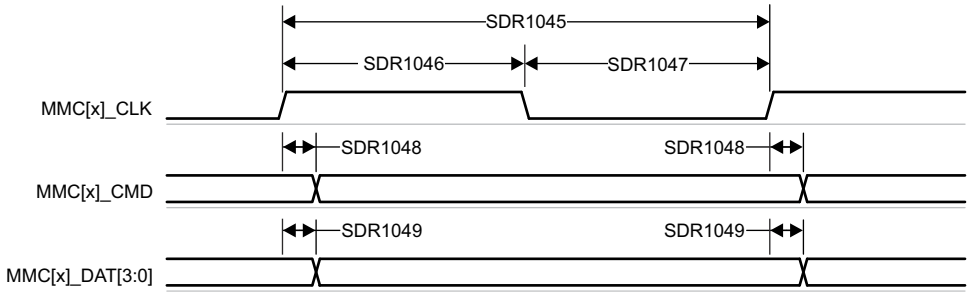


図 6-86. MMC1/MMC2 – UHS-I SDR104 – Transmit Mode

ADVANCE INFORMATION

6.11.5.18 OLDI

6.11.5.18.1 OLDI0 Switching Characteristics

表 6-103 and 図 6-87 present switching characteristics for OLDI0.

表 6-103. OLDI0 Switching Characteristics

NO.	PARAMETER		MODE	MIN	TYP	MAX	UNIT
OLDI1	$t_{t(LHTT)}$	Rise time, OLDI0_CLK[1:0]P, OLDI0_CLK[1:0]N, OLDI0_A[7:0]P, and OLDI0_A[7:0]N	Slow(1)			0.5	ns
			Fast(2)			0.25	ns
OLDI2	$t_{t(HLTT)}$	Fall time, OLDI0_CLK[1:0]P, OLDI0_CLK[1:0]N, OLDI0_A[7:0]P, and OLDI0_A[7:0]N	Slow(1)			0.5	ns
			Fast(2)			0.25	ns
OLDI3	$t_{c(CLK)}$	Cycle time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N		6.06		110.01	ns
OLDI4	$t_{w(BIT)}$	Bit width, OLDI0_A[7:0]P and OLDI0_A[7:0]N			(1/7)OLDI3		ns
OLDI5	$t_{d(BIT1)}$	Bit 1 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		- (0.1)OLDI3		(0.1)OLDI3	ns
OLDI6	$t_{d(BIT0)}$	Bit 0 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(1/7)OLDI3 - (0.1)OLDI3		(1/7) OLDI3 + (0.1)OLDI3	ns
OLDI7	$t_{d(BIT6)}$	Bit 6 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(2/7)OLDI3 - (0.1)OLDI3		(2/7) OLDI3 + (0.1)OLDI3	ns
OLDI8	$t_{d(BIT5)}$	Bit 5 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(3/7)OLDI3 - (0.1)OLDI3		(3/7) OLDI3 + (0.1)OLDI3	ns
OLDI9	$t_{d(BIT4)}$	Bit 4 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(4/7)OLDI3 - (0.1)OLDI3		(4/7) OLDI3 + (0.1)OLDI3	ns
OLDI10	$t_{d(BIT3)}$	Bit 3 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(5/7)OLDI3 - (0.1)OLDI3		(5/7) OLDI3 + (0.1)OLDI3	ns
OLDI11	$t_{d(BIT2)}$	Bit 2 delay time, OLDI0_CLK[1:0]P and OLDI0_CLK[1:0]N to OLDI0_A[7:0]P and OLDI0_A[7:0]N		(6/7)OLDI3 - (0.1)OLDI3		(6/7) OLDI3 + (0.1)OLDI3	ns
OLDI12	$t_{sk(TCCS)}$	Skew, OLDI0_A[7:0]P and OLDI0_A[7:0]N relative to any other OLDI0_A[7:0]P and OLDI0_A[7:0]N				50	ps

(1) Slow mode: TXDRV[3:0] = 0100b without back termination (RTERM_EN = 0b with 100Ω differential termination on far-end only)
(2) Fast mode: TXDRV[3:0] = 1000b with back termination (RTERM_EN = 1b with 100Ω differential termination on far-end only, or RTERM_EN = 0b with 100Ω differential termination on near-end and far-end)

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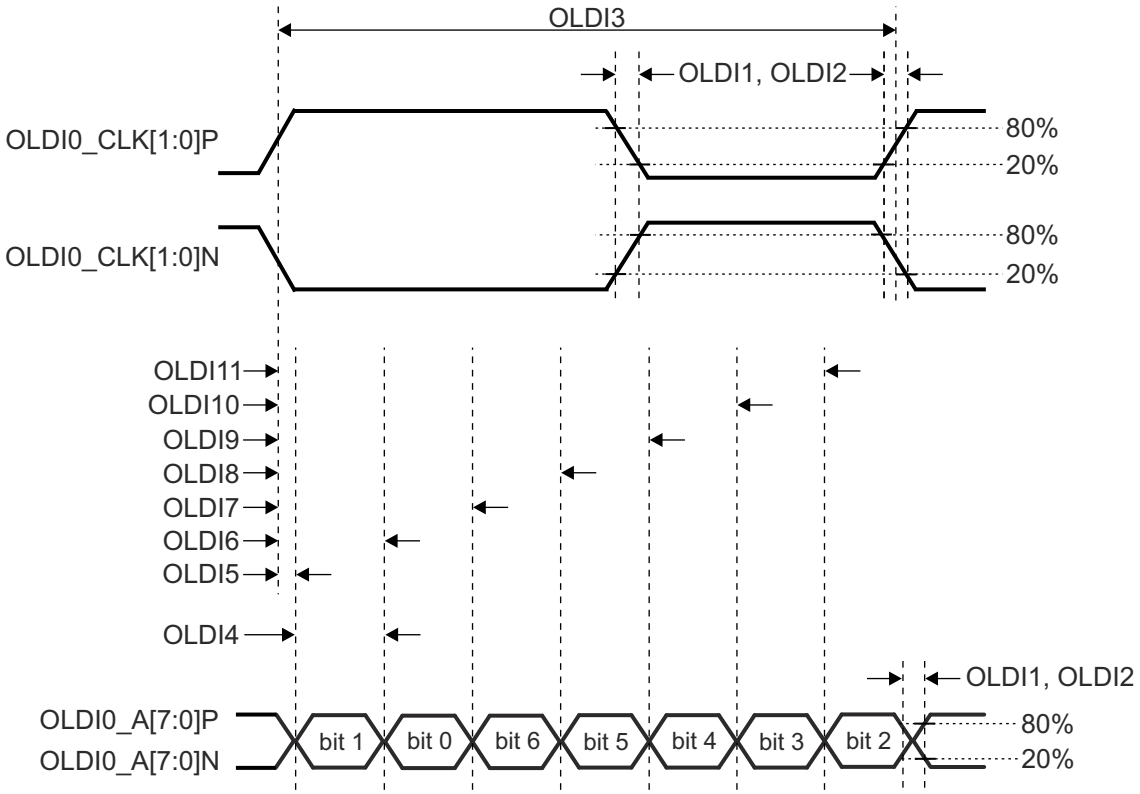


図 6-87. OLDI0 Switching Characteristics

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter in the device TRM.

ADVANCE INFORMATION

6.11.5.19 OSPI

OSPI0 offers two data capture modes, PHY mode and Tap mode.

PHY mode uses an internal reference clock to transmit and receive data via a DLL based PHY, where each reference clock cycle produces a single cycle of OSPI0_CLK for Single Data Rate (SDR) transfers or a half cycle of OSPI0_CLK for Double Data Rate (DDR) transfers. PHY mode supports four clocking topologies for the receive data capture clock. Internal PHY Loopback - uses the internal reference clock as the PHY receive data capture clock. Internal Pad Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_LBCLKO pin as the PHY receive data capture clock. External Board Loopback - uses OSPI0_LBCLKO looped back into the PHY from the OSPI0_DQS pin as the PHY receive data capture clock. DQS - uses the DQS output from the attached device as the PHY receive data capture clock. SDR transfers are not supported when using the Internal Pad Loopback and DQS clocking topologies. DDR transfers are not supported when using the Internal PHY Loopback or Internal Pad Loopback clocking topologies.

Tap mode uses an internal reference clock with selectable taps to adjusted data transmit and receive capture delays relative to OSPI0_CLK, which is a divide by 4 of the internal reference clock for SDR transfers or a divide by 8 of the internal reference clock for DDR transfers. Tap mode only supports one clocking topology for the receive data capture clock. No Loopback - uses the internal reference clock as the Tap receive data capture clock. This clocking topology supports a maximum internal reference clock rate of 200 MHz, which produces an OSPI0_CLK rate up to 50 MHz for SDR mode or 25 MHz for DDR mode.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

セクション 6.11.5.19.1 defines timing requirements and switching characteristics associated with PHY mode and セクション 6.11.5.19.2 defines timing requirements and switching characteristics associated with Tap mode.

表 6-104 presents timing conditions for OSPI0.

表 6-104. OSPI0 Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		1	6	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of OSPI0_CLK trace	No Loopback Internal PHY Loopback Internal Pad Loopback		450	ps
	Propagation delay of OSPI0_LBCLKO trace	External Board Loopback	2L(1) - 30	2L(1) + 30	ps
	Propagation delay of OSPI0_DQS trace	DQS	L(1) - 30	L(1) + 30	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch of OSPI0_D[7:0] and OSPI0_CSn[3:0] relative to OSPI0_CLK	All modes		60	ps

(1) L = Propagation delay of OSPI0_CLK trace

ADVANCE INFORMATION

6.11.5.19.1 OSPI0 PHY Mode

6.11.5.19.1.1 OSPI0 With PHY Data Training

Read and write data valid windows will shift due to variation in process, voltage, temperature, and operating frequency. A data training method may be implemented to dynamically configure optimal read and write timing. Implementing data training enables proper operation across temperature with a specific process, voltage, and frequency operating condition, while achieving a higher operating frequency.

Data transmit and receive timing parameters are not defined for the data training use case since they are dynamically adjusted based on the operating condition.

表 6-105 defines DLL delays required for OSPI0 with Data Training. 表 6-106, 図 6-88, 図 6-89, 表 6-107, 図 6-90, and 図 6-91 present timing requirements and switching characteristics for OSPI0 with Data Training.

表 6-105. OSPI0 DLL Delay Mapping for PHY Data Training

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD,	(1)
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	(2)

(1) Transmit DLL delay value determined by training software
(2) Receive DLL delay value determined by training software

表 6-106. OSPI0 Timing Requirements – PHY Data Training

see 図 6-88, and 図 6-89

NO.			MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	DDR with DQS	(1)		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	DDR with DQS	(1)		ns
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	SDR with External Board Loopback	(1)		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	SDR with External Board Loopback	(1)		ns
	t_{DVW}	Data valid window (O15 + O16)	1.8V, DDR with DQS	1.6		ns
			3.3V, DDR with DQS	2.2		ns
		Data valid window (O21 + O22)	1.8V, SDR with External Board Loopback	2.3		ns
			3.3V, SDR with External Board Loopback	2.9		ns

(1) Minimum setup and hold time requirements for OSPI0_D[7:0] inputs are not defined when Data Training is used to find the optimum data valid window. The t_{DVW} parameter defines the minimum data invalid window required. This parameter is provided in lieu of minimum setup and minimum hold times, where it must be used to check compatibility with the data valid window provided by an attached device.

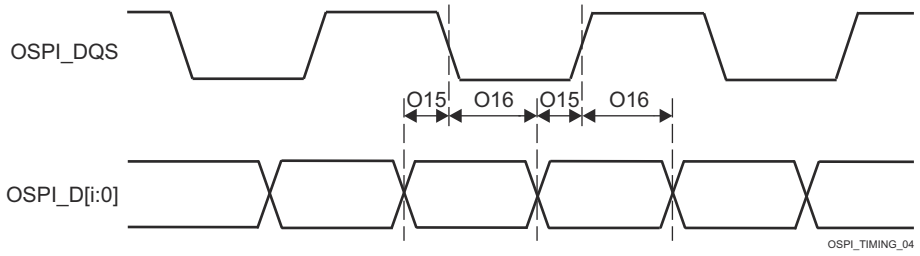


図 6-88. OSPI0 Timing Requirements – PHY Data Training, DDR with DQS

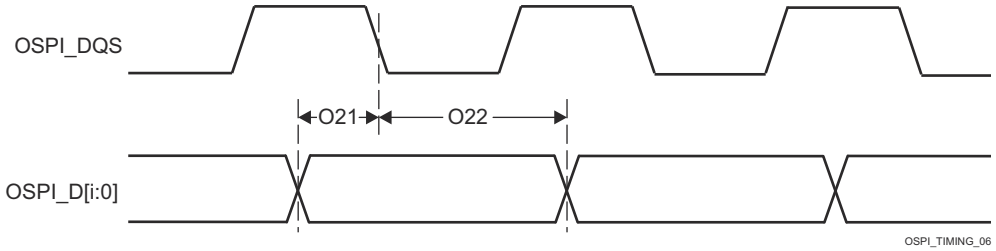


図 6-89. OSPI0 Timing Requirements – PHY Data Training, SDR with External Board Loopback

表 6-107. OSPI Switching Characteristics – PHY Data Training

See 図 6-90 and 図 6-91

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	1.8V, DDR	6.0	10	ns
			3.3V, DDR	7.5	10	ns
O7			1.8V, SDR	6.0	10	ns
			3.3V, SDR	7.5	10	ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low	DDR	((0.475P(1)) - 0.3)		ns
O8			SDR			
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high	DDR	((0.475P(1)) - 0.3)		ns
O9			SDR			
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge	DDR	((0.475P(1)) + (0.975M(2)R(4)) + (0.04TD(5)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + (0.11TD(5)) + 1)	ns
O10			SDR			
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge	DDR	((0.475P(1)) + (0.975N(3)R(4)) - (0.04TD(5)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) - (0.11TD(5)) + 1)	ns
O11			SDR			
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	DDR	(6)	(6)	ns
O12			SDR			
	t_{DIVW}	Data invalid window (O6 Max - Min)	DDR		1.6	ns
		Data invalid window (O12 Max - Min)	SDR			

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns
(5) TD = PHY_CONFIG_TX_DLL_DELAY_FLD
(6) Minimum and maximum delay times for OSPI0_D[7:0] outputs are not defined when Data Training is used to find the optimum data valid window. The t_{DIVW} parameter defines the maximum data invalid window. This parameter is provided in lieu of minimum and maximum delay times, where it must be used to check compatibility with the data valid window requirements of an attached device.

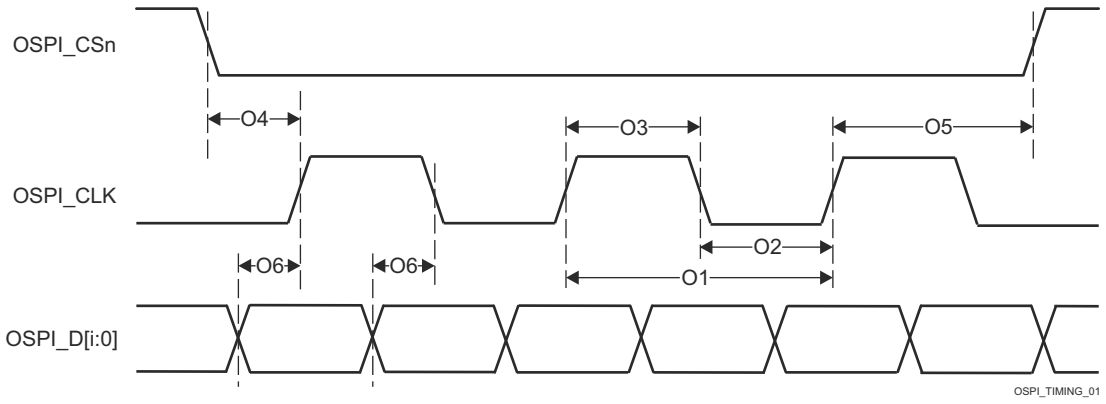


図 6-90. OSPI0 Switching Characteristics – PHY DDR Data Training

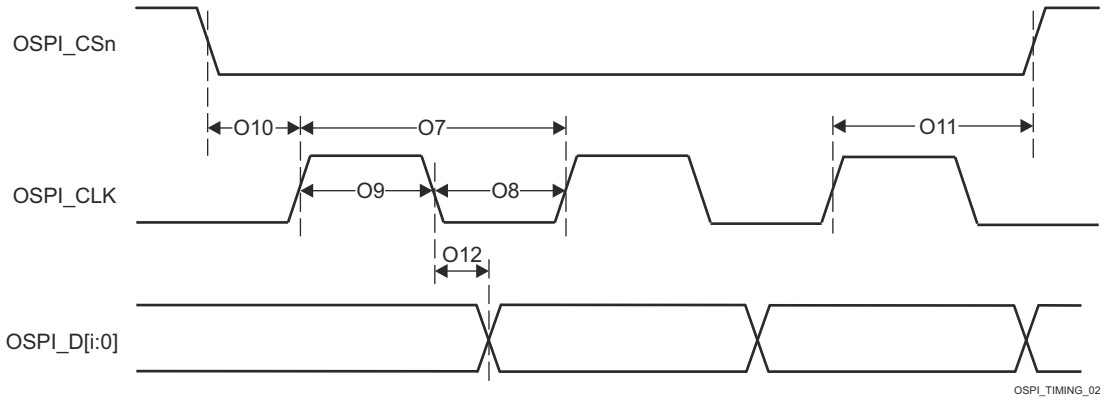


図 6-91. OSPI0 Switching Characteristics – PHY SDR Data Training

ADVANCE INFORMATION

6.11.5.19.1.2 OSPI0 Without Data Training

注

Timing parameters defined in this section are only applicable when data training is not implemented and DLL delays are configured as described in 表 6-108 and 表 6-111.

6.11.5.19.1.2.1 OSPI0 PHY SDR Timing

表 6-108 defines DLL delays required for OSPI0 PHY SDR Mode. 表 6-109, 図 6-92, 図 6-93, 表 6-110, and 図 6-94 present timing requirements and switching characteristics for OSPI0 PHY SDR Mode.

表 6-108. OSPI0 DLL Delay Mapping for PHY SDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD,	0x0
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

表 6-109. OSPI0 Timing Requirements – PHY SDR Mode

see 図 6-92 and 図 6-93

NO.			MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	1.8V, SDR with Internal PHY Loopback	4.8		ns
			3.3V, SDR with Internal PHY Loopback	5.19		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	1.8V, SDR with Internal PHY Loopback	-0.5		ns
			3.3V, SDR with Internal PHY Loopback	-0.5		ns
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	1.8V, SDR with External Board Loopback	0.6		ns
			3.3V, SDR with External Board Loopback	0.9		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	1.8V, SDR with External Board Loopback	1.7		ns
			3.3V, SDR with External Board Loopback	2.0		ns

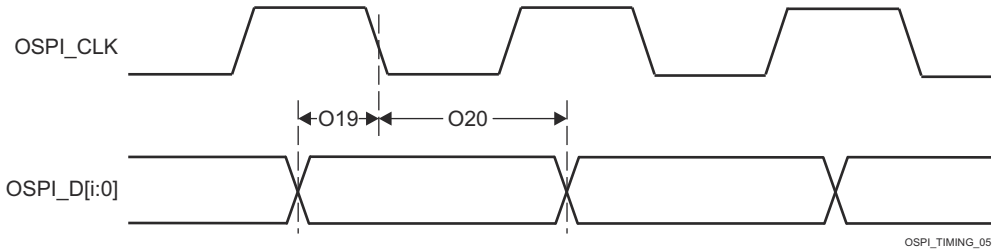


図 6-92. OSPI0 Timing Requirements – PHY SDR with Internal PHY Loopback

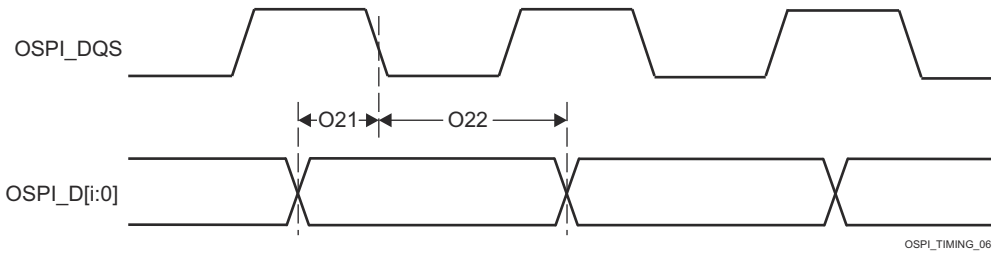


図 6-93. OSPI0 Timing Requirements – PHY SDR with External Board Loopback

ADVANCE INFORMATION

表 6-110. OSPI0 Switching Characteristics – PHY SDR Mode

see 図 6-94

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK	1.8V	7		ns
			3.3V	6.03		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + (0.975M(2)R(4)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + 1)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) + 1)	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	1.8V	-1.16	1.25	ns
			3.3V	-1.33	1.51	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

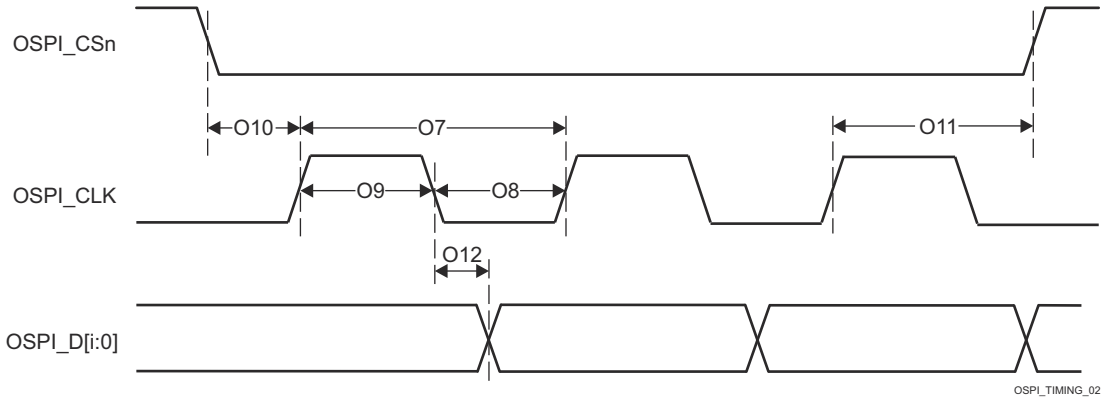


図 6-94. OSPI0 Switching Characteristics – PHY SDR

ADVANCE INFORMATION

6.11.5.19.1.2.2 OSPI0 PHY DDR Timing

表 6-111 defines DLL delays required for OSPI0 PHY DDR Mode. 表 6-112, 図 6-95, 表 6-113, and 図 6-96 present timing requirements and switching characteristics for OSPI0 PHY DDR Mode.

表 6-111. OSPI0 DLL Delay Mapping for PHY DDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
1.8V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x46
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x43
Receive		
1.8V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x15
3.3V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x3A
All other modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

表 6-112. OSPI0 Timing Requirements – PHY DDR Mode

see 図 6-95

NO.			MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_DQS edge	1.8V, DDR with External Board Loopback	0.53		ns
			1.8V, DDR with DQS	-0.46		ns
			3.3V, DDR with External Board Loopback	1.23		ns
			3.3V, DDR with DQS	-0.66		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_DQS edge	1.8V, DDR with External Board Loopback	1.24(1)		ns
			1.8V, DDR with DQS	3.59		ns
			3.3V, DDR with External Board Loopback	1.44(1)		ns
			3.3V, DDR with DQS	7.92		ns

(1) This Hold time requirement is larger than the Hold time provided by a typical OSPI/QSPI/SPI device. Therefore, the trace length between the SoC and attached OSPI/QSPI/SPI device must be sufficiently long enough to ensure that the Hold time is met at the SoC. The length of the SoC's external loopback clock (OSPI0_LBCLKO to OSPI0_DQS) may need to be shortened to compensate.

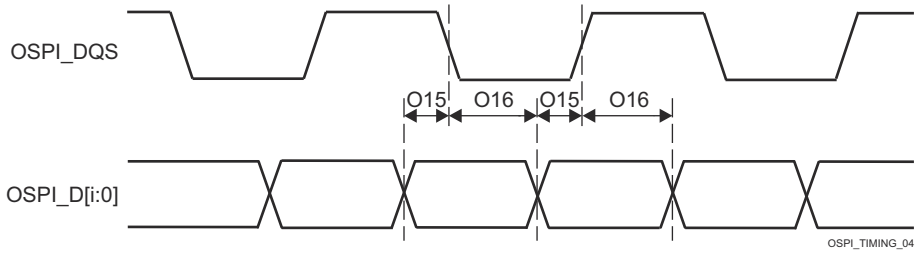


図 6-95. OSPI0 Timing Requirements – PHY DDR with External Board Loopback or DQS

表 6-113. OSPI0 Switching Characteristics – PHY DDR Mode

see 図 6-96

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		19		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) - (0.975M(2)R(4)))	((0.525P(1)) - (1.025M(2)R(4)) + 7)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 7)	((0.525P(1)) + (1.025N(3)R(4)))	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition	1.8V	-7.71	-1.56	ns
			3.3V	-7.71	-1.56	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

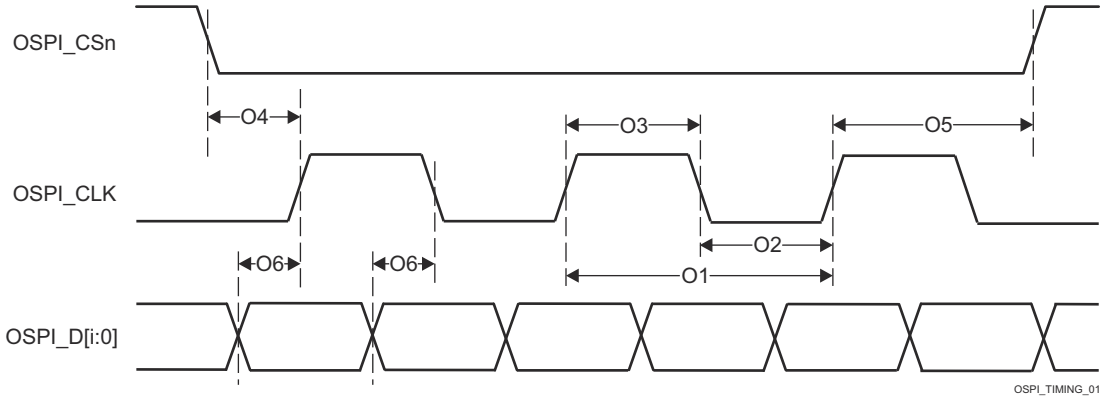


図 6-96. OSPI0 Switching Characteristics – PHY DDR

ADVANCE INFORMATION

6.11.5.19.2 OSPI0 Tap Mode

6.11.5.19.2.1 OSPI0 Tap SDR Timing

表 6-114, 図 6-97, 表 6-115, and 図 6-98 present timing requirements and switching characteristics for OSPI0 Tap SDR Mode.

表 6-114. OSPI0 Timing Requirements – Tap SDR Mode

see 図 6-97

NO.			MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	(15.4 - (0.975T(1)R(2)))		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	(- 4.3 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

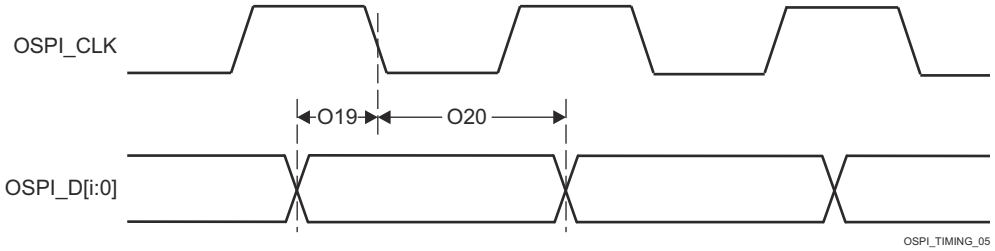


図 6-97. OSPI0 Timing Requirements – Tap SDR, No Loopback

ADVANCE INFORMATION

表 6-115. OSPI0 Switching Characteristics – Tap SDR Mode

see 図 6-98

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		20		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + (0.975M(2)R(4)) - 1)	((0.525P(1)) + (1.025M(2)R(4)) + 1)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1)	((0.525P(1)) + (1.025N(3)R(4)) + 1)	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		- 4.25	7.25	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

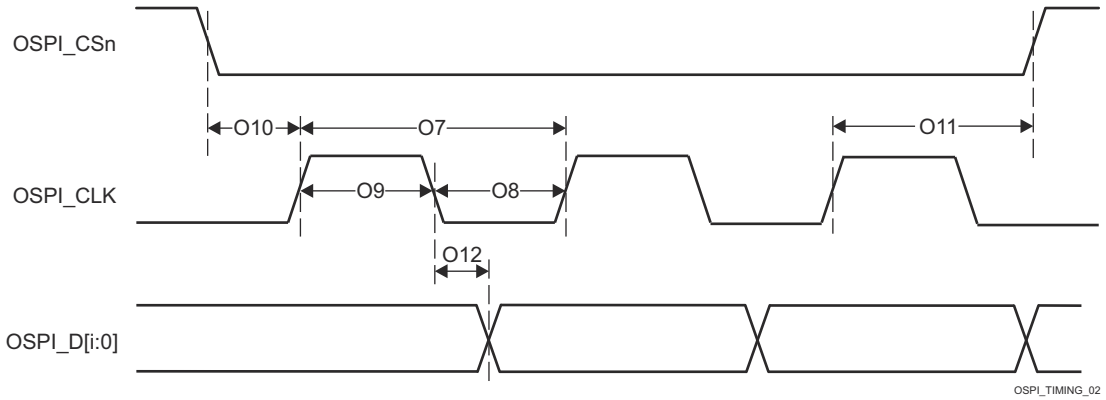


図 6-98. OSPI0 Switching Characteristics – Tap SDR, No Loopback

ADVANCE INFORMATION

6.11.5.19.2.2 OSPI0 Tap DDR Timing

表 6-116, 図 6-99, 表 6-117, and 図 6-100 present timing requirements and switching characteristics for OSPI0 Tap DDR Mode.

表 6-116. OSPI0 Timing Requirements – Tap DDR Mode

see 図 6-99

NO.			MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, OSPI0_D[7:0] valid before active OSPI0_CLK edge	No Loopback	(17.04 - (0.975T(1)R(2)))		ns
O14	$t_{h(CLK-D)}$	Hold time, OSPI0_D[7:0] valid after active OSPI0_CLK edge	No Loopback	(- 3.16 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

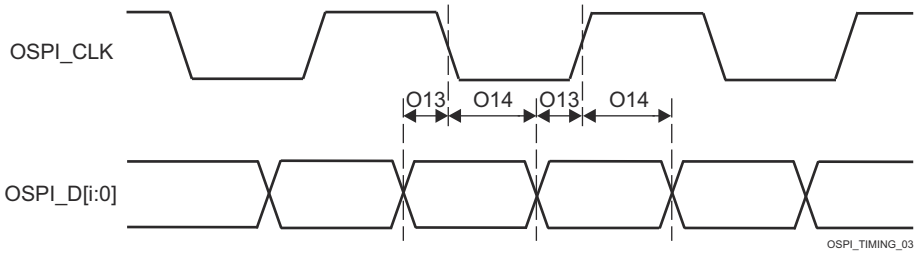


図 6-99. OSPI0 Timing Requirements – Tap DDR, No Loopback

表 6-117. OSPI0 Switching Characteristics – Tap DDR Mode

see 図 6-100

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0_CLK		40		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0_CLK low		((0.475P(1)) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0_CLK high		((0.475P(1)) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0_CSn[3:0] active edge to OSPI0_CLK rising edge		((0.475P(1)) + ((0.975M(2)R(5)) - 1)	((0.525P(1)) + (1.025M(2)R(5)) + 1)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0_CLK rising edge to OSPI0_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(5)) - 1)	((0.525P(1)) + (1.025N(3)R(5)) + 1)	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0_CLK active edge to OSPI0_D[7:0] transition		(- 5.04 + (0.975(T(4) + 1)R(5)) - (0.525P(1)))	(3.64 + (1.025(T(4) + 1)R(5)) - (0.475P(1)))	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) T = OSPI_RD_DATA_CAPTURE_REG[DDR_READ_DELAY_FLD]
(5) R = reference clock cycle time in ns

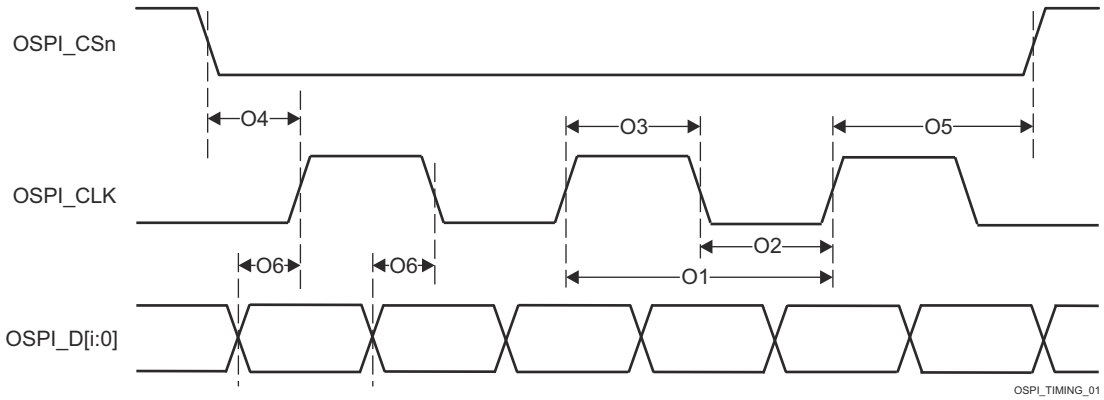


図 6-100. OSPI0 Switching Characteristics – Tap DDR, No Loopback

ADVANCE INFORMATION

6.11.5.20 Timers

For more details about features and additional description information on the device Timers, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 6-118. Timer Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	10	pF

表 6-119. Timer Input Timing Requirements

see 図 6-101

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T1	$t_{w(TINPH)}$	Pulse duration, high	CAPTURE	4P(1)+ 2.5		ns
T2	$t_{w(TINPL)}$	Pulse duration, low	CAPTURE	4P(1)+ 2.5		ns

(1) P = functional clock period in ns.

表 6-120. Timer Output Switching Characteristics

see 図 6-101

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T3	$t_{w(TOUTH)}$	Pulse duration, high	PWM	4P(1) - 2.5		ns
T4	$t_{w(TOUTL)}$	Pulse duration, low	PWM	4P(1) - 2.5		ns

(1) P = functional clock period in ns.

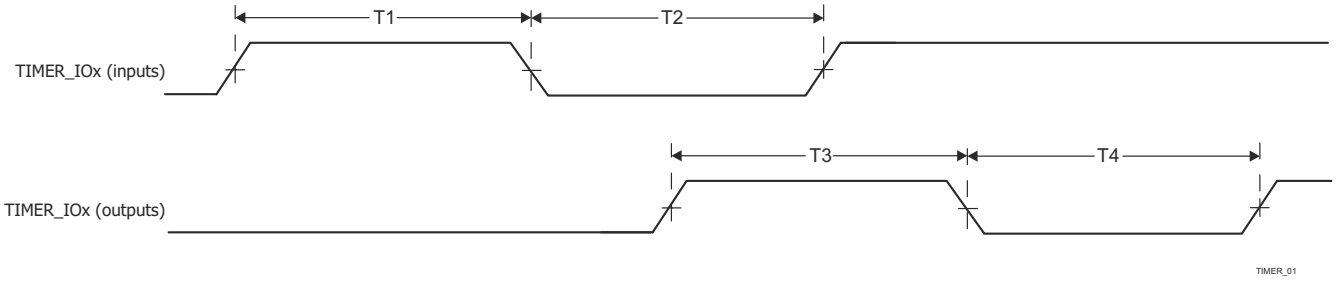


図 6-101. Timer Timing Requirements and Switching Characteristics

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

6.11.5.21 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

表 6-121. UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	30(1)	pF

(1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

表 6-122. UART Timing Requirements

see 図 6-102

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	$t_{w(RXD)}$	Pulse width, receive data bit high or low	0.95U(1) (2)	1.05U(1) (2)	ns
2	$t_{w(RXDS)}$	Pulse width, receive start bit low	0.95U(1) (2)		ns

(1) U = UART baud time in ns = 1/programmed baud rate.
(2) This value defines the data valid time, where the input voltage is required to be above V_{IH} or below V_{IL}.

表 6-123. UART Switching Characteristics

see 図 6-102

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{(baud)}$	Programmable baud rate for Main Domain UARTs		12	Mbps
		Programmable baud rate for MCU and WKUP Domain UARTs		3.7	Mbps
3	$t_{w(TXD)}$	Pulse width, transmit data bit high or low	U(1) - 2	U(1) + 2	ns
4	$t_{w(TXDS)}$	Pulse width, transmit start bit low	U(1) - 2		ns

(1) U = UART baud time in ns = 1/actual baud rate, where the actual baud rate is defined in the UART Baud Rate Settings table of the device TRM.

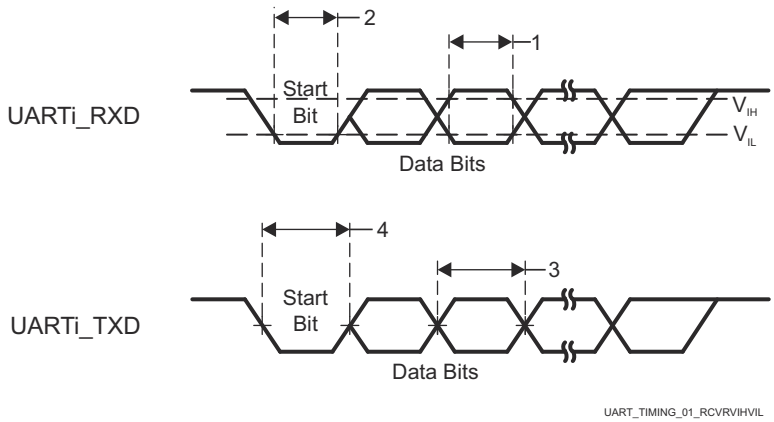


図 6-102. UART Timing Requirements and Switching Characteristics

ADVANCE INFORMATION

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

6.11.5.22 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

7 Detailed Description

7.1 Overview

The AM62Px (P = Plus) is an extension of the existing Sitara™ AM62x low-cost family of application processors built for high-performance embedded 3D display applications. Scalable Arm® Cortex®-A53 performance and embedded features, such as: multi-screen high-definition display support, 3D-graphics acceleration, 4K video acceleration, and extensive peripherals make the AM62Px well-suited for a broad range of automotive and industrial applications, including automotive digital instrumentation, automotive displays, industrial HMI, and more.

Key features and benefits:

- Focus on innovation and fast development with Linux® and Android™ SDKs accompanied with real-time functional safety and security SDKs.
- Address next wave of HMI designs with new generation of 3D GPU and 4K video acceleration.
- Enhance your design connectivity with an extensive set of automotive and high-speed IOs, including: 4x CAN-FD, 3-port Gigabit Ethernet switch (two external ports) with TSN support, and two USB2.0 ports.
- Supports the latest cybersecurity requirements with the built-in Hardware Security Module (HSM).
- Provides intelligent features, such as: facial recognition and touchless HMI with Arm® Cortex®-A53 CPUs and open-source AI software and tools

The AM62Px processors comply with the AEC - Q100 automotive standard and support industrial-grade. ASIL-B and SIL-2 functional safety requirements can be addressed using an integrated Arm Cortex-R5F core and dedicated peripherals, which can all be isolated from the rest of the processor.

7.2 Processor Subsystems

7.2.1 Arm Cortex-A53 Subsystem

The SoC implements one cluster of quad-core Arm® Cortex®-A53 MPCore™, with 32KB L1 instruction, 32KB L1 data, per core and 512KB L2 shared cache.

The Cortex®-A53 cores are general-purpose processors that can be used for running customer applications.

The A53SS is built around the Cortex®-A53 MPCore™ (Arm®-A53 Cluster), which is provided by Arm and configured by TI. It is based on the symmetric multiprocessor (SMP) architecture, and thus, it delivers high performance and optimal power management, debug and emulation capabilities.

The A53 processor is a multi-issue out-of-order superscalar execution engine with integrated L1 Instruction and Data Caches, compatible with Arm®v8-A architecture. It delivers significantly more performance than its predecessors at a higher level of power efficiency.

The Arm®v8-A architecture brings a number of new features. These include 64-bit data processing, extended virtual addressing and 64-bit general purpose registers. The A53 processor is Arm's first Arm®v8-A processor aimed at providing power-efficient 64-bit processing. It features an in-order, 8-stage, dual-issue pipeline, and improved integer, Arm® Neon™, Floating-Point Unit (FPU) and memory performance.

The A53 CPU supports two execution states: AArch32 and AArch64. The AArch64 state gives the A53 CPU its ability to execute 64-bit applications, while the AArch32 state allows the processor to execute existing Arm®v7-A applications.

For more information, see *Arm Cortex-A53 Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

7.2.2 Device/Power Manager

The WKUP_R5FSS is a single-core implementation of the Arm® Cortex®-R5F processor that acts as the Device Manager responsible for boot, resource management, and power management functions. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™™ debug and trace architecture, integrated vectored interrupt manager (VIM), ECC aggregators, and various other modules for protocol conversion and address translation for easy integration into the SoC.

For more information, see *Device Manager Cortex R5F Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

7.2.3 MCU Arm Cortex-R5F Subsystem

The MCU_R5FSS is an Arm® Cortex®-R5F based subsystem that can run safety processing or be used as a general purpose MCU. The processor includes 32KB instruction Cache, 32KB data cache, and 64KB Tightly Coupled Memory.

For more information, see *Cortex R5F Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

7.3 Accelerators and Coprocessors

7.4 Other Subsystems

7.4.1 Dual Clock Comparator (DCC)

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

For more information, see *Dual Clock Comparator* section in *Peripherals* chapter in the device TRM.

7.4.2 Data Movement Subsystem (DMSS)

The DMSS module provides data movement (DMA) and bridges between the CBA switched interconnect and the packet streaming fabric (network on chip) on the device.

The Data Movement Subsystem (DMSS) consists of DMA/Queue Management components and Peripherals:

- Packet DMA
- Block Copy DMA
- Ring Accelerator
- Packet Streaming Interface (PSILSS)
- Infrastructure components such as CBASS, secure proxy, and an interrupt aggregator

7.4.3 Memory Cyclic Redundancy Check (MCRC)

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a pre-determined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system.

For more information, see *Memory Cyclic Redundancy Check* section in *Peripherals* chapter in the device TRM.

7.4.4 Peripheral DMA Controller (PDMA)

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers (MMRs) accessed via a standard non-coherent bus fabric. The PDMA module is located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured transfer request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer DMSS destination channel which then performs the movement of the data into memory. Likewise, a remote DMSS source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (DMSS + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

7.4.5 Real-Time Clock (RTC)

The basic purpose for the RTC is to keep time of day. The other equally important purpose of RTC is for Digital Rights management. Some degree of tamper proofing is needed to ensure that simply stopping, resetting, or corrupting the RTC does not go unnoticed so that if this occurs, the application can re-acquire the time of day from a trusted source.

For more information, see *Real-Time Clock* section in *Peripherals* chapter in the device TRM.

7.5 Peripherals

7.5.1 Gigabit Ethernet Switch (CPSW3G)

The 3-port Gigabit Ethernet Switch (CPSW0) subsystem provides Ethernet packet communication for the device and can be configured as an Ethernet switch.

For more information, see *Gigabit Ethernet Switch* section in *Peripherals* chapter in the device TRM.

7.5.2 Camera Serial Interface Receiver (CSI_RX_IF)

The integration of the CSI_RX_IF module allows the device to stream video inputs from multiple cameras to internal memory.

For more information, see *Camera Serial Interface Receiver* section in *Peripherals* chapter in the device TRM.

7.5.3 Display Subsystem (DSS)

The Display Subsystem (DSS) is a flexible, multi-pipeline subsystem that supports high-resolution display outputs. DSS includes input pipelines providing multi-layer blending with transparency to enable on-the-fly composition. Various pixel processing capabilities are supported, such as color space conversion and scaling, among others. DSS includes a DMA engine, which allows direct access to the frame buffer (device system memory). Display outputs can connect seamlessly to an Open LVDS Display Interface transmitter (OLDI0), Display Serial Interface transmitter (DSITX0), or can directly drive device pads as a Display Parallel Interface (DPI).

For more information, see *Display Subsystem* section in *Peripherals* chapter in the device TRM.

7.5.4 Enhanced Capture (ECAP)

The ECAP module provides accurate timing of events. When not being used for event capture, its resources can be used to generate a single channel of asymmetrical PWM waveforms.

The Enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

For more information, see *Enhanced Capture* section in *Peripherals* chapter in the device TRM.

7.5.5 Error Location Module (ELM)

The ELM extracts error addresses from generated syndrome polynomials.

The ELM is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

For more information, see *Error Location Module* section in *Peripherals* chapter in the device TRM.

7.5.6 Enhanced Pulse Width Modulation (EPWM)

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single channel modules with separate resources and that can

operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

For more information, see *Enhanced Pulse Width Modulation* section in *Peripherals* chapter in the device TRM.

7.5.7 Error Signaling Module (ESM)

The Error Signaling Module (ESM) aggregates events and/or errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with an event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in a safe, known state.

For more information, see *Error Signaling Module* section in *Peripherals* chapter in the device TRM.

7.5.8 Enhanced Quadrature Encoder Pulse (EQEP)

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

For more information, see *Enhanced Quadrature Encoder Pulse* section in *Peripherals* chapter in the device TRM.

7.5.9 General-Purpose Interface (GPIO)

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

For more information, see *General-Purpose Interface* section in *Peripherals* chapter in the device TRM.

7.5.10 General-Purpose Memory Controller (GPMC)

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For more information, see *General-Purpose Memory Controller* section in *Peripherals* chapter in the device TRM.

7.5.11 Global Timebase Counter (GTC)

The GTC module provides a continuous running counter that can be used for time synchronization and debug trace time stamping.

For more information, see *Global Timebase Counter* section in *Peripherals* chapter in the device TRM.

7.5.12 Inter-Integrated Circuit (I2C)

The device contains multicontroller Inter-Integrated Circuit (I2C) controllers each of which provides an interface between a local host (LH), such as an Arm and any I^2C-bus-compatible device that connects via the I^2C serial bus. External components attached to the I^2C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I^2C interface.

Each multicontroller I^2C module can be configured to act like a target or controller I^2C-compatible device.

I^2C instances may be implemented with dedicated, I^2C compliant, open-drain I/O buffers, or with standard LVCMOS I/O buffers. The I^2C instances associated with open-drain I/O buffers can support Hs-mode (up to 3.4 Mbps when the I/O buffers are operating at 1.8 V but limited to 400 kbps when the I/O buffers are operating at 3.3 V).

The I^2C instances associated with standard LVCMOS I/O buffers can support Fast-mode (up to 400 kbps). The LVCMOS I/O buffers being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.

For more information, see *Inter-Integrated Circuit* section in *Peripherals* chapter in the device TRM.

7.5.13 Modular Controller Area Network (MCAN)

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. CAN has high immunity to electrical interference and the ability to self-diagnose and repair data errors. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

For more information, see *Modular Controller Area Network* section in *Peripherals* chapter in the device TRM.

7.5.14 Multichannel Audio Serial Port (MCASP)

This section introduces the Multichannel Audio Serial Port (MCASP) module and describes its main functions and connections in the device.

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although inter-component digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

For more information, see *Multichannel Audio Serial Port* section in *Peripherals* chapter in the device TRM.

7.5.15 Multichannel Serial Peripheral Interface (MCSPI)

The MCSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus.

For more information, see *Multichannel Serial Peripheral Interface* section in *Peripherals* chapter in the device TRM.

7.5.16 Multi-Media Card Secure Digital (MMCSD)

The MMCSD Host Controller provides an interface to eMMC 5.1 (embedded Multi-Media Card), SD 4.10 (Secure Digital), and SDIO 4.0 (Secure Digital IO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness

For more information, see *Multi-Media Card Secure Digital* section in *Peripherals* chapter in the device TRM.

7.5.17 Octal Serial Peripheral Interface (OSPI)

The Octal Serial Peripheral Interface (OSPI) module is a Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices. This module has a memory mapped register interface, which provides a direct memory interface for accessing data from external flash devices, simplifying software requirements.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device controller at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

7.5.18 Timers

All timers include specific functions to generate accurate tick interrupts to the operating system.

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

7.5.19 Universal Asynchronous Receiver/Transmitter (UART)

The UART is a peripheral that utilizes the DMA for data transfer or interrupt polling via host CPU. All UART modules support IrDA and CIR modes when 48 MHz function clock is used. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

For more information, see *Universal Synchronous/Asynchronous Receiver/Transmitter* section in *Peripherals* chapter in the device TRM.

7.5.20 Universal Serial Bus Subsystem (USBSS)

USB (Universal Serial Bus) provides a low-cost connectivity solution for numerous consumer portable devices by implementing a mechanism for data transfer between USB devices.

The device instantiates two independent instances of a third-party USB subsystem (USB2SS) operating at up to USB2.0 speeds (480Mb/s), either of which can be independently configured to act as a USB Host or a USB Device.

For more information, see *Universal Serial Bus Subsystem* section in *Peripherals* chapter in the device TRM.

8 Applications, Implementation, and Layout

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Device Connection and Layout Fundamentals

8.1.1 Power Supply

8.1.1.1 Power Supply Designs

The Power Management IC (PMIC) recommended for the AM62Px family of processors and peripherals, along with its operational details can be found in the *PMIC Solution for AM62Px* application note.

List of benefits when using the recommended PMIC:

- Cost and space optimized PMIC solutions specifically designed to power the AM62Px family of processors
- Supports up to Automotive ASIL-B functional safety applications when powering the AEC – Q100 qualified AM62P-Q1 device
- Supports up to SIL-2 functional safety industrial applications when powering the AM62P device
- Full device performance entitlement as validated on TI Evaluation boards
- Factory programmed configurations support power rail load steps, supply voltage accuracies and maximum load currents with margins
- Factory programmed configurations support LPDDR4 memory
- Integrated ADC in the PMIC provides added benefit of making it easy to measure analog voltages (from temp sensors, ambient light sensors etc.)
- Meets all AM62P and AM62P-Q1 voltage and sequencing requirements, refer to セクション 6.5, *Recommended Operating Conditions* and セクション 6.11.2.2, *Power Supply Sequencing*

8.1.1.2 Power Distribution Network Implementation Guidance

The Sitara Processor Power Distribution Networks: Implementation and Analysis provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI *only* supports designs that follow the board design guidelines contained in the application report.

8.1.2 External Oscillator

For more information about External Oscillators, see the *Clock Specifications* section.

8.1.3 JTAG, EMU, and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For recommendations on JTAG, EMU, and TRACE routing, see the Emulation and Trace Headers Technical Reference Manual

8.1.4 Unused Pins

For more information about Unused Pins, see セクション 5.4, *Pin Connectivity Requirements*.

ADVANCE INFORMATION

8.2 Peripheral- and Interface-Specific Design Information

8.2.1 DDR Board Design and Layout Guidelines

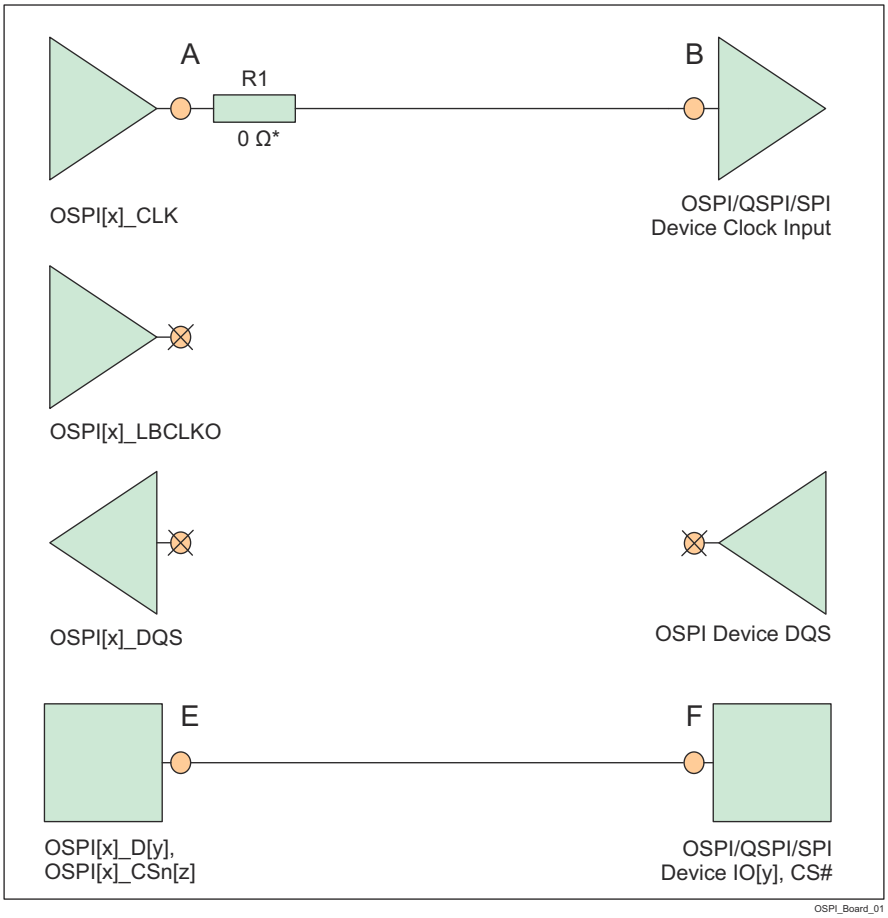
The goal of the *AM62Px DDR Board Design and Layout Guidelines* is to make the DDR system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using LPDDR4 memories that follow the guidelines in this document.

8.2.2 OSPI/QSPI/SPI Board Design and Layout Guidelines

The following section details the PCB routing guidelines that must be observed when connecting OSPI, QSPI, or SPI devices.

8.2.2.1 No Loopback, Internal PHY Loopback, and Internal Pad Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B) must be ≤ 450 ps (~7cm as stripline or ~8cm as microstrip)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 図 8-1
- Propagation delays and matching:
  - (A to B) ≤ 450 ps
  - (E to F, or F to E) = ((A to B) ± 60 ps)



* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is placeholder for fine tuning, if needed.

図 8-1. OSPI Connectivity Schematic for No Loopback, Internal PHY Loopback, and Internal Pad Loopback

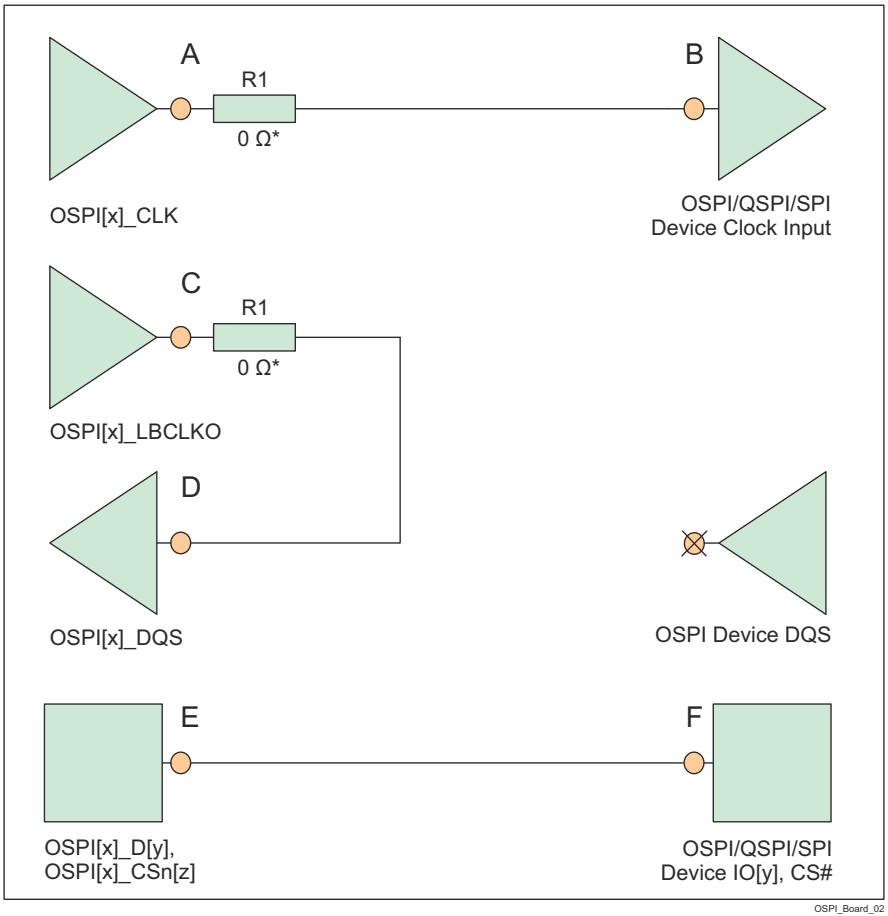
ADVANCE INFORMATION

8.2.2.2 External Board Loopback

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The OSPI[x]_LBCLKO output pin must be looped back to the OSPI[x]_DQS input pin
- The signal propagation delay of the OSPI[x]_LBCLKO pin to the OSPI[x]_DQS pin (C to D) must be approximately twice the propagation delay of the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 図 8-2
- Propagation delays and matching:
  - (C to D) = 2 x ((A to B) ± 30 ps), see the exception note below.
  - (E to F, or F to E) = ((A to B) ± 60 ps)

注

The External Board Loopback hold time requirement (defined by parameter number O16 in the *OSPI0 Timing Requirements - PHY DDR Mode* section) may be larger than the hold time provided by a typical OSPI/QSPI/SPI device. In this case, the propagation delay of OPSI[x]_LBCLKO pin to the OSPI[x]_DQS pin (C to D) can be reduced to provide additional hold time.



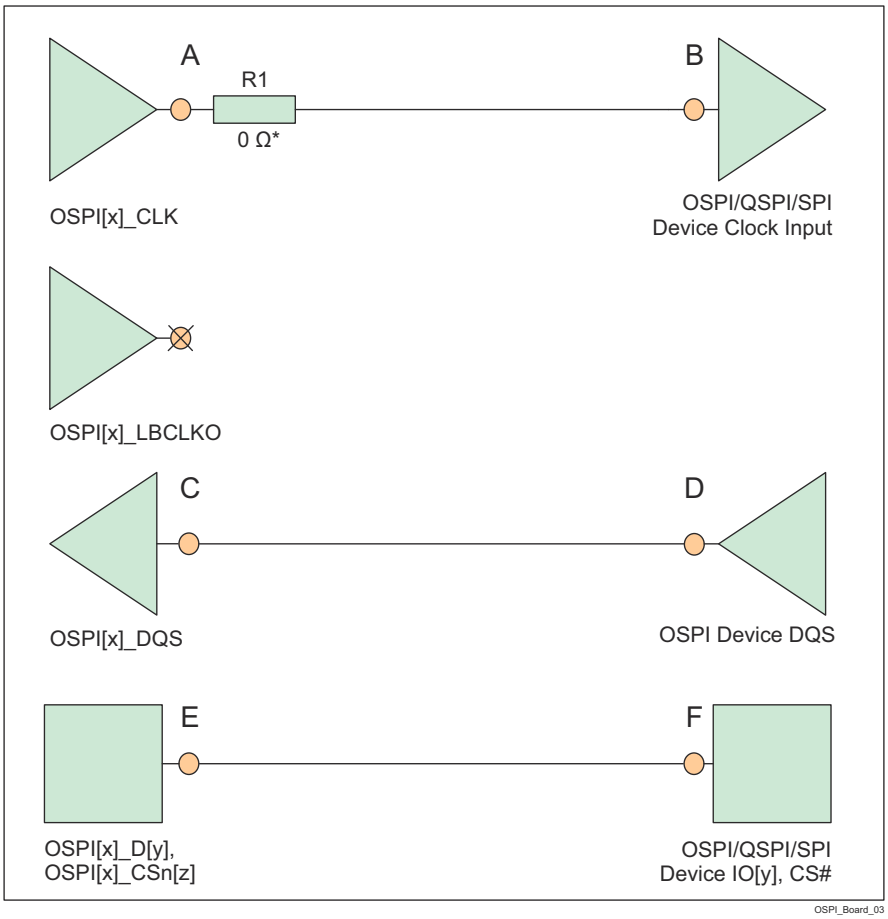
* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK and OSPI[x]_LBCLKO pins, is a placeholder for fine tuning, if needed.

図 8-2. OSPI Connectivity Schematic for External Board Loopback

ADVANCE INFORMATION

8.2.2.3 DQS (only available in Octal SPI devices)

- The OSPI[x]_CLK output pin must be connected to the CLK input pin of the attached OSPI/QSPI/SPI device
- The DQS pin of the attached OSPI/QSPI/SPI device must be connected to OSPI[x]_DQS pin
- The signal propagation delay from the attached OSPI/QSPI/SPI device DQS pin to the OSPI[x]_DQS pin (D to C) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- The signal propagation delay of each OSPI[x]_D[y] and OSPI[x]_CSn[z] pin to the corresponding attached OSPI/QSPI/SPI device data and control pin (E to F, or F to E) must be approximately equal to the signal propagation delay from the OSPI[x]_CLK pin to the attached OSPI/QSPI/SPI device CLK pin (A to B)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 図 8-3
- Propagation delays and matching:
  - (D to C) = ((A to B) ± 30 ps)
  - (E to F, or F to E) = ((A to B) ± 60 ps)



* 0 Ω resistor (R1), located as close as possible to the OSPI[x]_CLK pin, is a placeholder for fine tuning, if needed.

図 8-3. OSPI Connectivity Schematic for DQS

8.2.3 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the 図 8-4), which limits the voltage applied to the actual device pin (USB0_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of Zener diode at 5 V should be less than 100 nA.

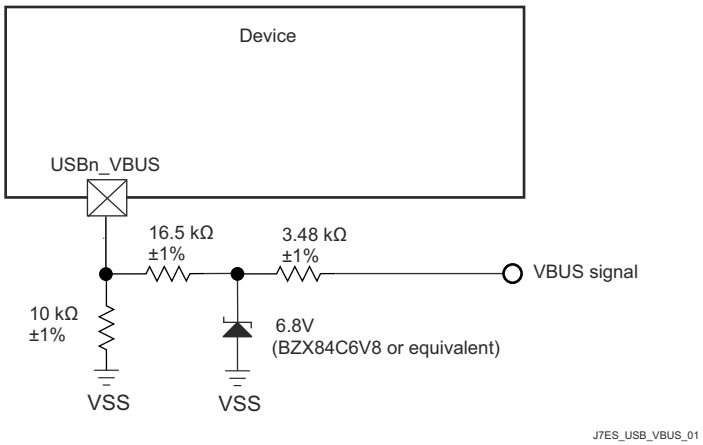


図 8-4. USB VBUS Detect Voltage Divider / Clamp Circuit

The USB0_VBUS pin can be considered to be fail-safe because the external circuit in 図 8-4 limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

8.2.4 System Power Supply Monitor Design Guidelines

The VMON_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system and can be connected to the VMON_VSYS pin via and external resistor divider circuit. This system supply is monitored by comparing the external voltage divider output voltage to an internal voltage reference, where a power fail event is triggered when the voltage applied to VMON_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit.

When designing the resistor divider circuit the designer must understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON_VSYS input threshold which has a nominal value of 0.45 V, with a variation of ±3%. Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON_VSYS input leakage current can be in the range of 10 nA to 2.5 µA when applying 0.45 V.

注

The resistor voltage divider shall be designed such that the output voltage never exceeds the maximum value defined in the *Recommended Operating Conditions* section, during normal operating conditions.

ADVANCE INFORMATION

図 8-5 presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5 V - 10%, or 4.5 V.

For this example, the designer must understand which variables effect the maximum trigger threshold when selecting resistor values. A device which has a VMON_VSYS input threshold of 0.45 V + 3% needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but the contribution to the maximum trigger point is not obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON_VSYS pin is 2.5 µA. When implementing a resistor divider where R1 = 4.81 KΩ and R2 = 40.2 KΩ, the result is a maximum trigger threshold of 4.517 V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45 V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input leakage current is 10 nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.013 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.013 V to 4.517 V. Approximately 250 mV of this range is introduced by VMON_VSYS input threshold accuracy of ±3%, approximately 150 mV of this range is introduced by resistor tolerance of ±1%, and approximately 100 mV of this range is introduced by loading error when VMON_VSYS input leakage current is 2.5 µA.

The resistor values selected in this example produces approximately 100 µA of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above can be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer must also consider implementing a noise filter on the voltage divider output since VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients. This can be done by installing a capacitor across R1 as shown in 図 8-5. However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.

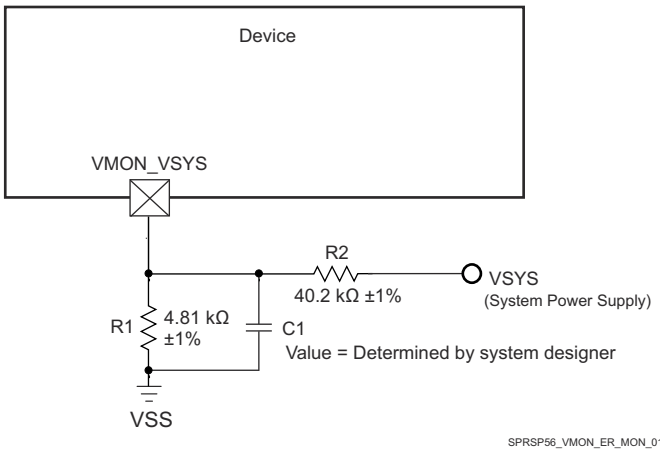


図 8-5. System Supply Monitor Voltage Divider Circuit

VMON_1P8_SOC pin provides a way to monitor external 1.8 V power supplies. This pin must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

VMON_3P3_SOC pin provides a way to monitor external 3.3 V power supplies. This pin must be connected directly to their respective power source. An internal resistor divider with software control is implemented inside

the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

8.2.5 High Speed Differential Signal Routing Guidance

The High Speed Interface Layout Guidelines provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application note.

8.2.6 Thermal Solution Guidance

The Thermal Design Guide for DSP and ARM Application Processors provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application note.

8.3 Clock Routing Guidelines

8.3.1 Oscillator Routing

When designing the printed-circuit board:

- Place all crystal circuit components as close as possible to the respective device pins.
- Route the crystal circuit traces on the outer layer of the PCB and minimize trace lengths to reduce parasitic capacitance and minimize crosstalk from other signals.
- Place a continuous ground plane on the adjacent layer of the PCB such that it is under all crystal circuit components and crystal circuit traces.
- Route a ground guard around the crystal circuit components to shield it from any adjacent signals routed on the same layer as the crystal circuit traces. Insert multiple vias to stitch down the ground guard such that it does not have any unterminated stubs.
- Route a ground guard between the MCU_OSC0_XI and MCU_OSC0_XO signals to shield the MCU_OSC0_XI signal from the MCU_OSC0_X0 signal. Insert multiple vias to stitch down the ground guard such that it does not have any unterminated stubs.
- Connect all crystal circuit ground connections and ground guard connections directly to the adjacent layer ground plane, and the device VSS ground plane if they are implemented separately on different layers of the PCB.

注

Implementing a ground guard between the MCU_OSC0_XI and MCU_OSC0_XO signals is critical to minimize shunt capacitance between the two signals. Routing these two signals adjacent to each other without a ground guard between them will effectively reduce the gain of the oscillator amplifier, which reduces its ability to start oscillation.

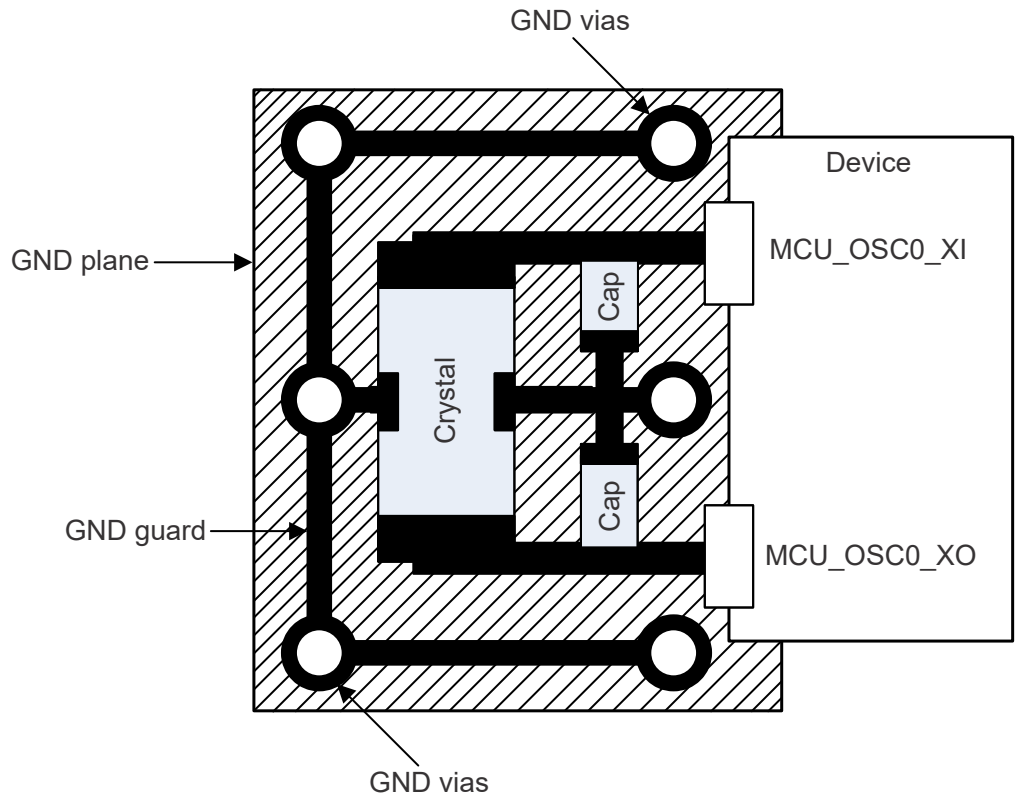


図 8-6. MCU_OSC0 PCB requirements

9 Device and Documentation Support

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, XAM62P54AUMHIAMH). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM62Px devices in the AMH package type, see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

ADVANCE INFORMATION

9.1.1 Standard Package Symbolization

注

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

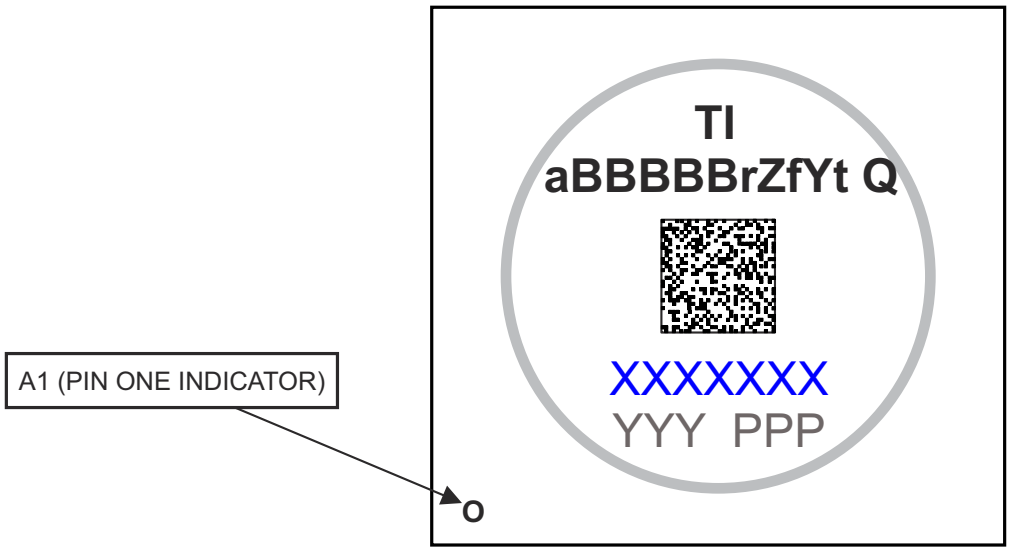


図 9-1. Printed Device Reference

9.1.2 Device Naming Convention

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
TI	Device Manufacturer	TI	Texas Instruments
a	Device evolution stage(1)	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK (null)	Production
–	Part Number Prefix	AM	Not symbolized
BBBBB	Base production part number	62P54	see Device Comparison
		62P52	
		62P34	
		62P32	
r	Device revision	A	SR1.0
Z	Device Speed Grade	O	See Device Speed Grades table
		S	
		U	
f	Features (see Device Comparison)	G	Base
		L	Features supported by G, plus Multimedia JPEG Encoder
		M	Features supported by L, plus Display Subsystem
Y	Security / Functional Safety	1 to 9	Secure with Dummy Key / No Functional Safety
		H to R	Secure with Production Key / No Functional Safety
		S to Z	Secure with Production Key / Functional Safety
t	Temperature(2)	I	–40°C to 125°C - 125°C Industrial and Automotive (see Recommended Operating Conditions)
Q	Automotive Designator	Q	Auto Qualified (AEC - Q100)
		BLANK	Standard
	2D Barcode	Varies	Optional 2D barcode, provides additional device information
		BLANK	
XXXXXXX			Lot Trace Code (LTC)
YYY			Production Code, For TI use only
PPP	Package Designator	AMH	FCBGA (466)
•			Pin one designator

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Prototype devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) Applies to device max junction temperature.

注

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

ADVANCE INFORMATION

9.2 Tools and Software

The following Development Tools support development for TI's Embedded Processing platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. The tool includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig-PinMux Tool The SysConfig-PinMux Tool is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool generates output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements. The **Cloud-based SysConfig-PinMux Tool** is also available.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.3 Documentation Support

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

The following documents describe the AM62Px devices.

Technical Reference Manual

AM62Px Sitara™ Processors Technical Reference Manual: Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM62Px family of devices.

Errata

AM62Px Sitara™ Processors Silicon Errata: Describes the known exceptions to the functional specifications for the device.

9.4 サポート・リソース

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9.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

DATE	REVISION	NOTES
December 2023	*	Initial release.

ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XAM62P54AUMHAAMH	ACTIVE	FCBGA	AMH	466	1	TBD	Call TI	Call TI	-40 to 125		Samples
XAM62P54AUMHIAMH	ACTIVE	FCBGA	AMH	466	90	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

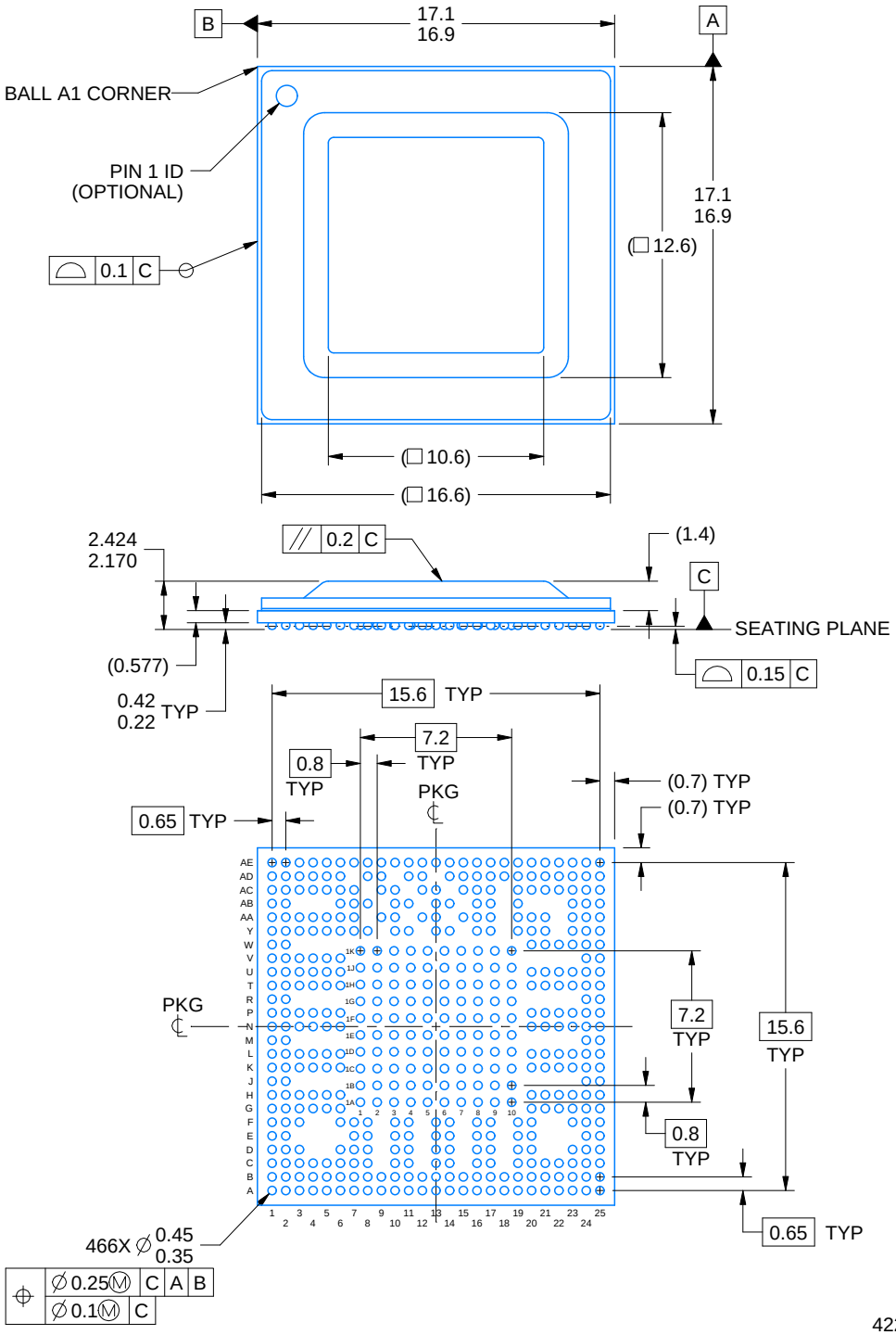
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF AM62P, AM62P-Q1 :

- Catalog : AM62P
- Automotive : AM62P-Q1

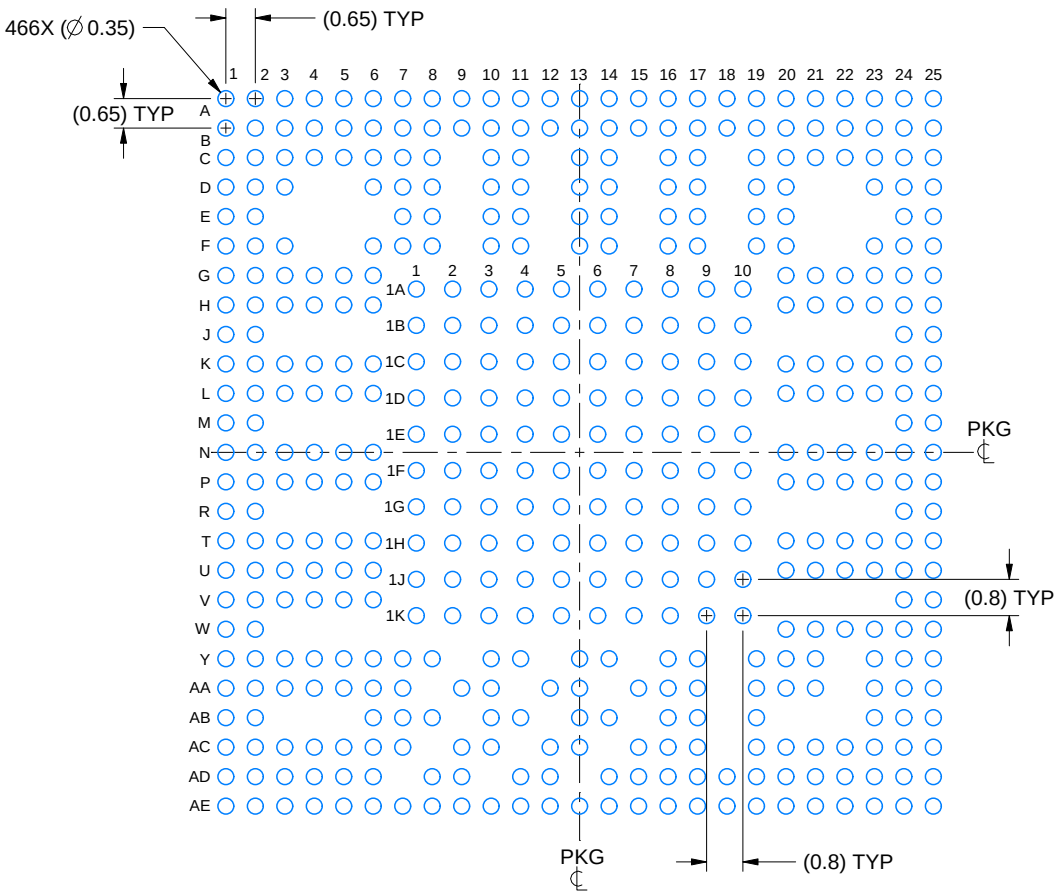
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

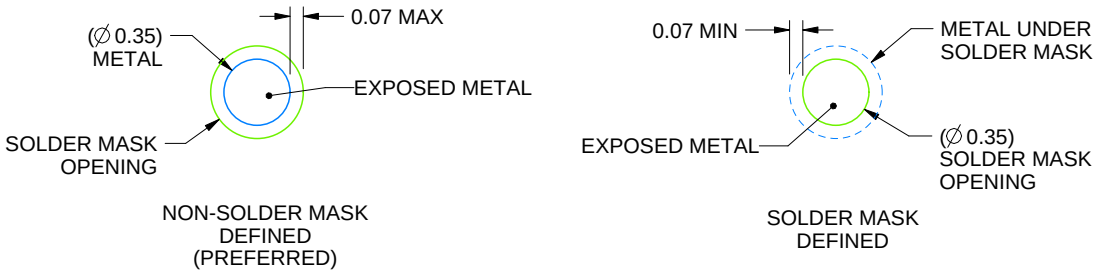


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SNOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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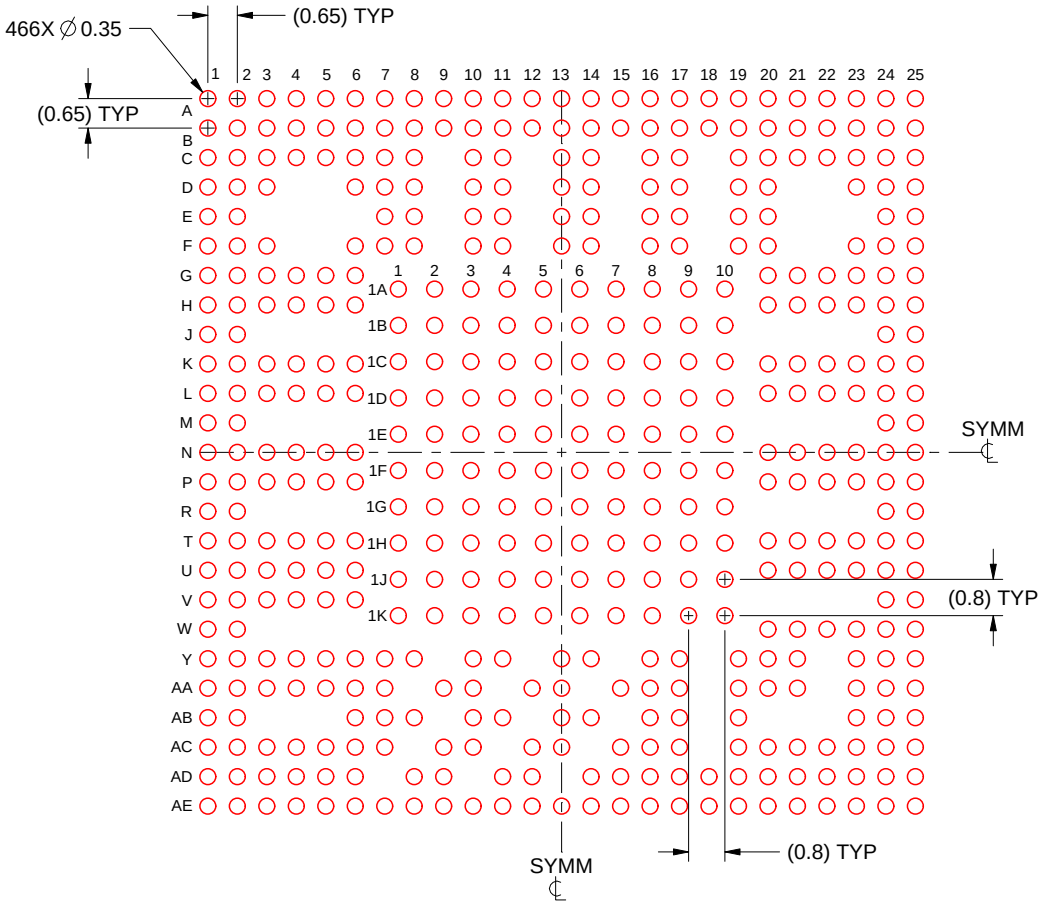
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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