AM26LV32 低電圧、高速、クワッド差動ライン・レシーバ

1 特長

- 最高 32MHz のスイッチング速度
- 3.3V 単一電源で動作
- 非常に低い消費電力:27mW (標準値)
- 開路、短絡、終端 フェイルセーフ
- 同相電圧範囲:−0.3V～5.5V、感度 ± 200mV
- 3.3V V_{CC} で 5V ロジック入力を受容
- 入力ヒステリシス:50mV (標準値)
- 235mW、4 個のレシーバで 32MHz 時
- AM26C32 および AM26LS32 とピン互換

2 アプリケーション

- 高信頼性の車載用アプリケーション
- ファクトリ・オートメーション
- ATM / キャッシュ・カウンタ
- スマート・グリッド
- AC / サーボ・モータ・ドライブ

3 概要

AM26LV32 デバイスは、3 ステート出力を備えた BiCMOS クワッド差動ライン・レシーバで、電源電圧の低下により同相電圧範囲が狭くなり、TIA/EIA-422-B および ITU 勧告 V.11 レシーバと同様に設計されています。

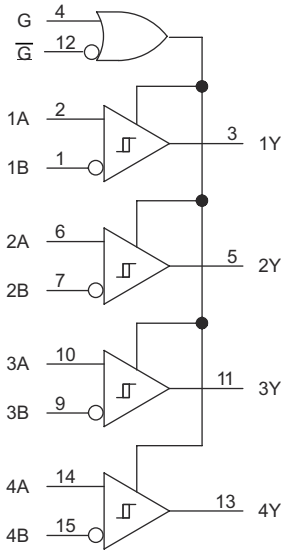
最高 32MHz のスイッチング速度で平衡化されたバス転送を行うように最適化されています。イネーブル機能は 4 つのレシーバすべてに共通で、アクティブ High またはアクティブ Low の入力から選択できます。3 ステート出力によりバス構成システムへの直接接続が可能です。各デバイスは高い入力インピーダンス、ノイズ耐性を高める入力ヒステリシス、−0.3V～5.5V の同相入力電圧範囲にわたって ±200mV の入力感度を備えています。入力が開路のとき、出力は High ロジック状態になります。

AM26LV32C は 0℃～70℃での動作が規定されています。AM26LV32I は -40℃～85℃での動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
AM26LV32	SOIC (16)	9.9mm × 6mm
	SO (16)	10.2mm × 7.8mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



論理図 (正論理)

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (October 2017) to Revision H (August 2023) — **Page**

- 「製品情報」表を「パッケージ情報」表に変更 ... 1
- AM26LV32I の温度を以下のように変更：-45℃～85℃から「概要」で −40℃～85℃ ... 1
- Changed the *Thermal Information* table ... 5
- Changed the *Typical Characteristics* ... 7

Changes from Revision F (November 2016) to Revision G (October 2017) — **Page**

- Changed the MAX value of $t_{sk(p)}$ From: 6 ns To: 14 ns in the *Switching Characteristics* table ... 6
- Changed the MAX value of $t_{sk(o)}$ From: 6 ns To: 14 ns in the *Switching Characteristics* table ... 6

Changes from Revision E (June 2005) to Revision F (November 2016) — **Page**

- 「ESD 定格」表、「熱に関する情報」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1
- 「特長」の一覧から MB570 を削除 ... 1
- 「注文情報」表を削除 (このデータシートの末尾にある「メカニカル、パッケージ、および注文情報」を参照) ... 1
- Deleted Lead temperature (260°C maximum) from *Absolute Maximum Ratings* table ... 4
- Changed Package thermal impedance, $R_{\theta JA}$, values in *Thermal Information* table From: 73°C To: 72.9°C (D) and From: 64°C To: 74°C (NS) ... 5

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5 Pin Configuration and Functions

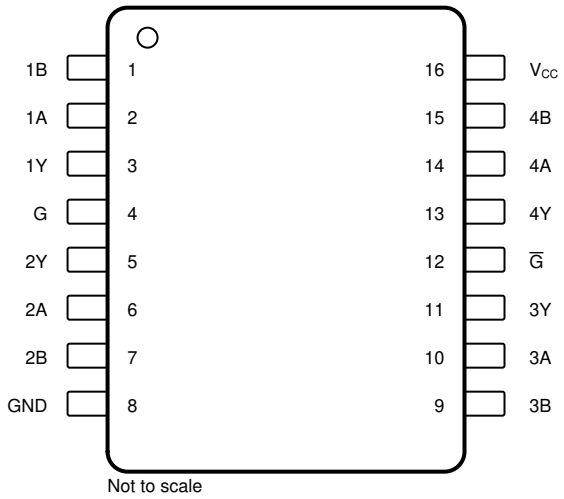

図 5-1. D and NS Package, 16-Pin SOIC and SO (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	RS422, RS485 differential input (noninverting)
1B	1	I	RS422, RS485 differential input (inverting)
1Y	3	O	Logic level output
2A	6	I	RS422, RS485 differential input (noninverting)
2B	7	I	RS422, RS485 differential input (inverting)
2Y	5	O	Logic level output
3A	10	I	RS422, RS485 differential input (noninverting)
3B	9	I	RS422, RS485 differential input (inverting)
3Y	11	O	Logic level output
4A	14	I	RS422, RS485 differential input (noninverting)
4B	15	I	RS422, RS485 differential input (inverting)
4Y	13	O	Logic level output
$\overline{G}$	12	I	Active-low select
G	4	I	Active-high select
GND	8	—	Ground
V_{CC}	16	—	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC} (2)	–0.3	6	V
Input voltage, V_I	–4	8	V
Differential input voltage, V_{ID} (3)		±12	V
Enable input voltage	–0.3	6	V
Output voltage, V_O	–0.3	6	V
Maximum output current, I_O		±25	mA
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, $V_{IH(EN)}$		2			V
Low-level input voltage, $V_{IL(EN)}$				0.8	V
Common-mode input voltage, V_{IC}		–0.3		5.5	V
Differential input voltage, V_{ID}				±5.8	V
High-level output current, I_{OH}				–5	mA
Low-level output current, I_{OL}				5	mA
Operating free-air temperature, T_A	AM26LV32C	0		70	°C
	AM26LV32I	–40		85	

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6.4 Thermal Information

THERMAL METRIC[1] [2]		AM26LV32				
		D (SOIC)	DR (SOIC-Reel)	NS (SO)	NSR (SO-Reel)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.9	84.6	74	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	43.5	31.1	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.4	43.2	34.8	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.4	10.4	5.1	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.1	42.8	34.5	50.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage				0.2	V
V_{IT-}	Differential input low-threshold voltage		–0.2			V
V_{IK}	Enable input clamp voltage	I_I = − 18 mA		–0.8	–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −5 mA	2.4	3.2		V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV, I_{OH} = 5 mA		0.17	0.5	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}			±50	µA
$I_{IH(E)}$	High-level enable input current	V_{CC} = 0 or 3 V, V_I = 5.5 V			10	µA
$I_{IL(E)}$	Low-level enable input current	V_{CC} = 3.6 V, V_I = 0 V			–10	µA
r_I	Input resistance		7	12		kΩ
I_I	Input current	V_I = 5.5 V or − 0.3 V, all other inputs GND			±700	µA
I_{CC}	Supply current	$V_{I(E)}$ = V_{CC} or GND, no load, line inputs open		8	17	mA
C_{pd}	Power dissipation capacitance[2]	One channel		150		pF

(1) All typical values are at V_{CC} = 3.3 V and T_A = 25°C.
(2) C_{pd} determines the no-load dynamic current: $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$.

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See 図 7-1	8	16	20	ns
t_{PHL}	Propagation delay time, high- to low-level output	See 図 7-1	8	16	20	ns
t_t	Transition time (t_r or t_f)	See 図 7-1		5		ns
t_{PZH}	Output-enable time to high level	See 図 7-2		17	40	ns
t_{PZL}	Output-enable time to low level	See 図 7-3		10	40	ns
t_{PHZ}	Output-disable time from high level	See 図 7-2		20	40	ns
t_{PLZ}	Output-disable time from low level	See 図 7-3		16	40	ns
$t_{sk(p)}$ (1)	Pulse skew			4	14	ns
$t_{sk(o)}$ (2)	Pulse skew			4	14	ns
$t_{sk(pp)}$ (3)	Pulse skew (device to device)			6	9	ns

(1) $t_{sk(p)}$ is $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(2) $t_{sk(o)}$ is the maximum difference in propagation delay times between any two channels of the same device switching in the same direction.
(3) $t_{sk(pp)}$ is the maximum difference in propagation delay times between any two channels of any two devices switching in the same direction.

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6.7 Typical Characteristics

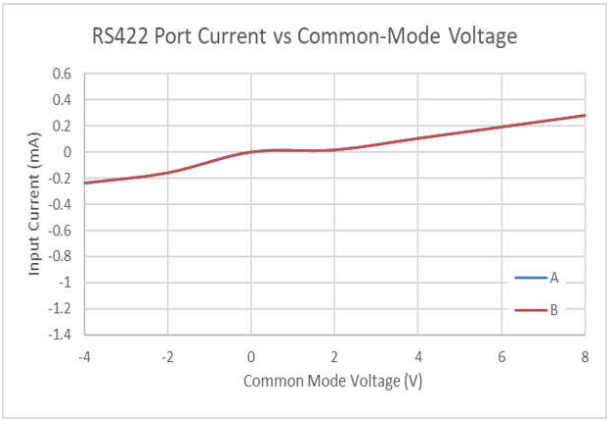


図 6-1. RS422 Port Current vs Common-Mode Voltage

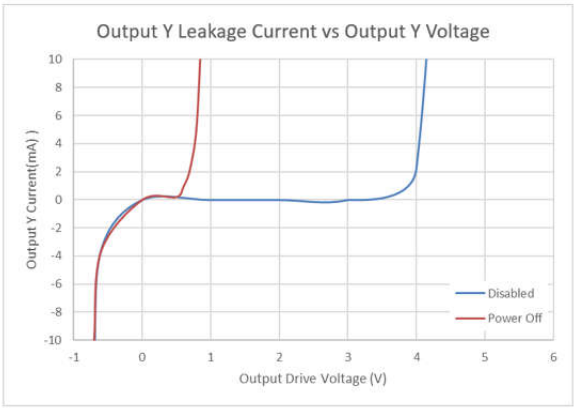


図 6-2. Output Y Leakage Current vs Output Y Voltage

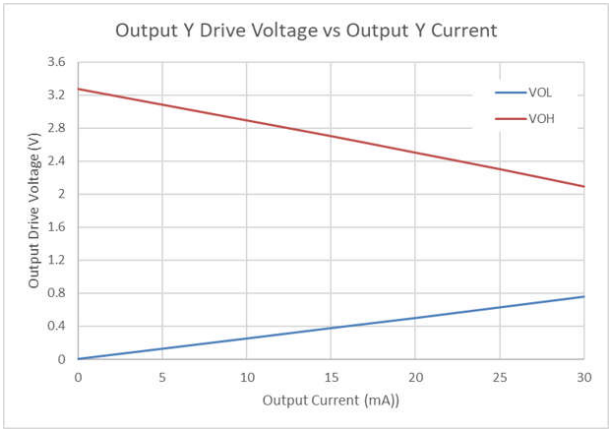
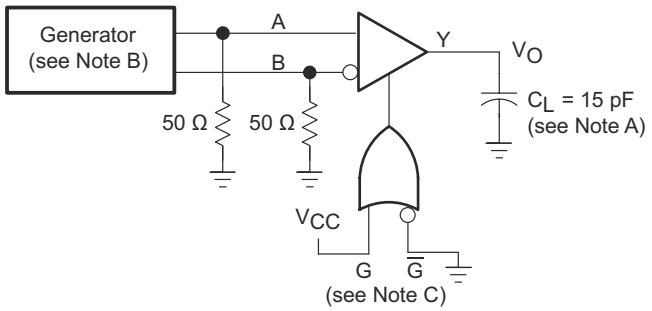


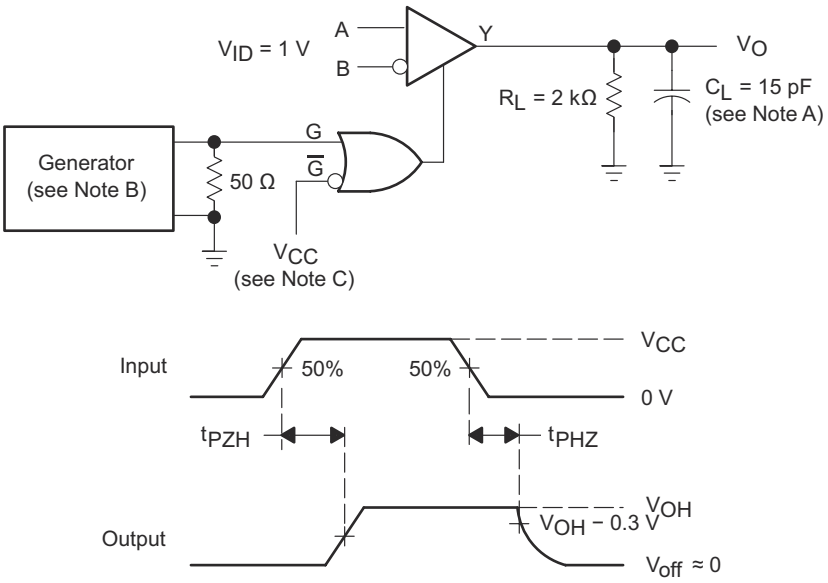
図 6-3. Output Y Drive Voltage vs Output Y Current

7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ≤ 2 ns, 50% duty cycle.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

図 7-1. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ≤ 2 ns, 50% duty cycle.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

図 7-2. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms

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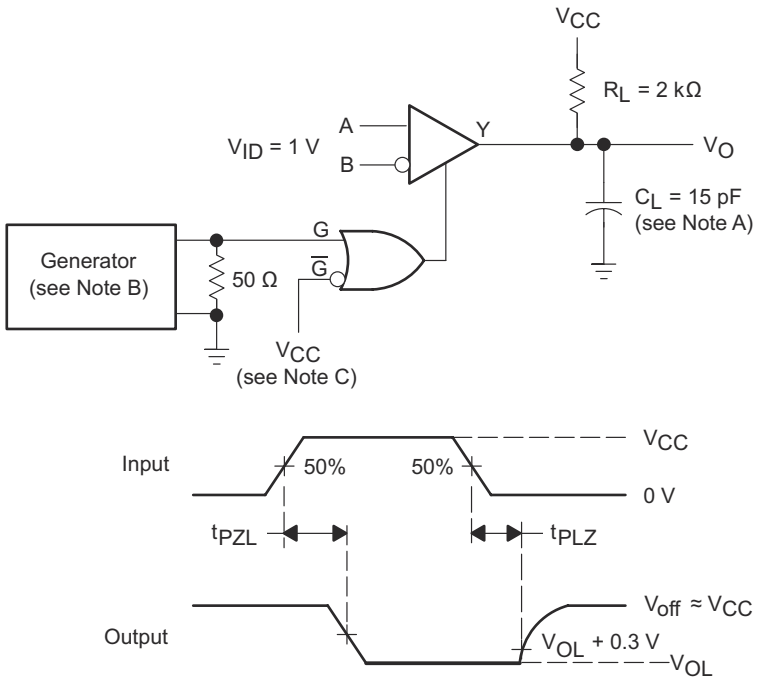

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ≤ 2 ns, 50% duty cycle.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

図 7-3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The AM26LV32 device is a quadruple differential line receiver that meets the necessary requirements for NSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11. This device allows a low-power or low-voltage MCU to interface with heavy machinery, subsystems, and other devices through long wires of up to 1000 m, giving any design a reliable and easy-to-use connection. As with any RS422 interface, the AM26LV32 works in a differential voltage range, which enables very good signal integrity.

8.2 Functional Block Diagram

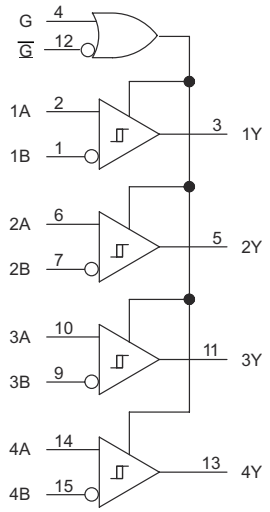

図 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The device can be configured using the G and $\overline{G}$ logic inputs to select receiver output. The high voltage or logic 1 on the G pin allows the device to operate on an active-high, and having a low voltage or logic 0 on the $\overline{G}$ enables active-low operation. These are simple ways to configure the logic to match that of the receiving or transmitting controller or microprocessor.

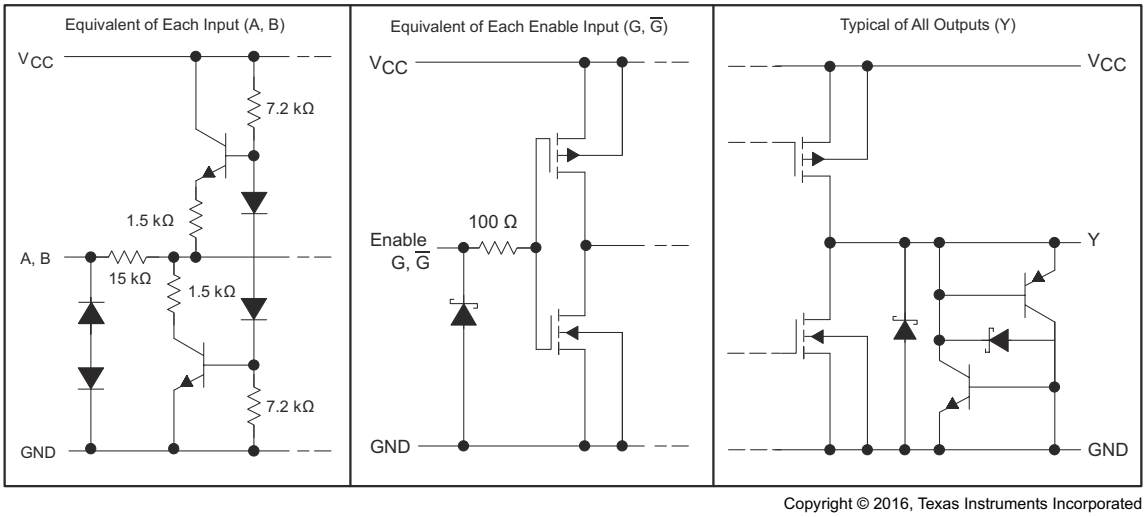

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図 8-2. Schematics of Equivalent Inputs and Outputs

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8.4 Device Functional Modes

The receivers implemented in these RS422 devices can be configured using the G and $\overline{G}$ logic pins to be enabled or disabled. This allows the option to ignore or filter out transmissions as desired. 表 8-1 lists the function of each receiver.

表 8-1. Function Table (Each Receiver)

DIFFERENTIAL INPUT	ENABLES		OUTPUT(1)
	G	$\overline{G}$	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
–0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq$ –0.2 V	H	X	L
	X	L	L
Open, shorted, or terminated(2)	H	X	H
	X	L	H
X	L	H	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate
(2) See *セクション 9* section

8.4.1 Fail-Safe Conditions

The AM26LV32 is a quadruple differential line receiver that is designed to function properly when appropriately connected to active drivers. Applications do not always have ideal situations where all bits are being used, the receiver inputs are never left floating, and fault conditions do not exist. In actuality, most applications have the capability to either place the drivers in a high-impedance mode or power down the drivers altogether, and cables may be purposely (or inadvertently) disconnected, both of which lead to floating receiver inputs. Furthermore, even though measures are taken to avoid fault conditions like a short between the differential signals, this does occur. The AM26LV32 device has an internal fail-safe circuitry which prevents the device from putting an unknown voltage signal at the receiver outputs. In the following three cases, a high-state is produced at the respective output:

1. Open fail-safe: Unused input pins are left open. Do not tie unused pins to ground or any other voltage. Internal circuitry places the output in the high state.
2. 100-Ω terminated fail-safe: Disconnected cables, drivers in high-impedance state, or powered-down drivers does not cause the AM26LV32 to malfunction. The outputs remain in a high state under these conditions. When the drivers are either turned-off or placed into the high-impedance state, the receiver input may still be able to pick up noise due to the cable acting as an antenna. To avoid having a large differential voltage being generated, the use of twisted-pair cable induces the noise as a common-mode signal and is rejected.
3. Shorted fail-safe: Fault conditions that short the differential input pairs together does not cause incorrect data at the outputs. A differential voltage (V_{ID}) of 0 V forces a high state at the outputs. Shorted fail-safe, however, is not supported across the recommended common-mode input voltage (V_{IC}) range. An unwanted state can be induced to all outputs when an input is shorted and is biased with a voltage between −0.3 V and +5.5 V. The shorted fail-safe circuitry functions properly when an input is shorted, but with no external common-mode voltage applied.

8.4.2 Fail-Safe Precautions

The internal fail-safe circuitry was designed such that the input common-mode (V_{IC}) and differential (V_{ID}) voltages must be observed. To ensure the outputs of unused or inactive receivers remain in a high state when the inputs are open-circuited, shorted, or terminated, extra precaution must be taken on the active signal. In applications where the drivers are placed in a high-impedance mode or are powered-down, TI recommends that for 1, 2, or 3 active receiver inputs, the low-level input voltage (V_{IL}) must be greater than 0.4 V. As in all data transmission applications, it is necessary to provide a return ground path between the two remote grounds

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(driver and receiver ground references) to avoid ground differences. 表 8-2 and 図 8-3 through 図 8-5 are examples of active input voltages with their respective waveforms and the effect each have on unused or inactive outputs. Note that the active receivers behave as expected, regardless of the input levels.

表 8-2. Active Receiver Inputs vs Outputs

1, 2, OR 3 ACTIVE INPUTS			SEE FIGURE	1, 2, OR 3 ACTIVE OUTPUTS	3, 2, OR 1 UNUSED OR INACTIVE OUTPUTS
V_{IL}	V_{ID}	V_{IC}			
900 mV	200 mV	1 V	図 8-3	Known state	High state
–100 mV	200 mV	0 V	図 8-4	Known state	?
600 mV	800 mV	1 V	図 8-5	Known state	High state
0 mV	800 mV	400 mV	図 8-6	Known state	?

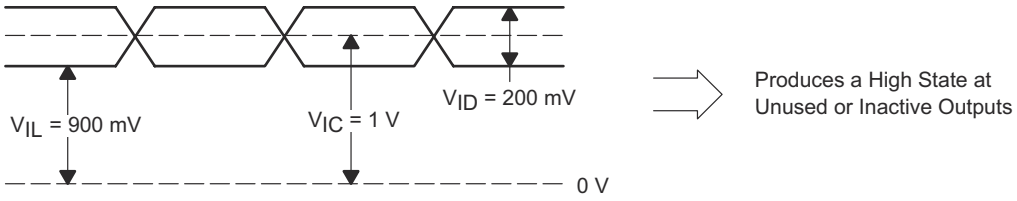

図 8-3. Waveform 1

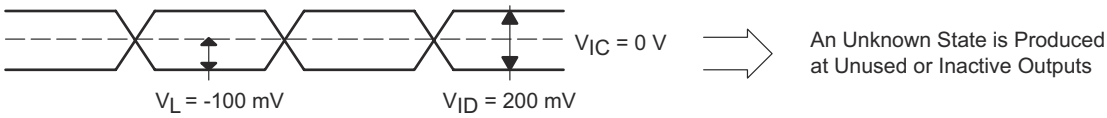

図 8-4. Waveform 2

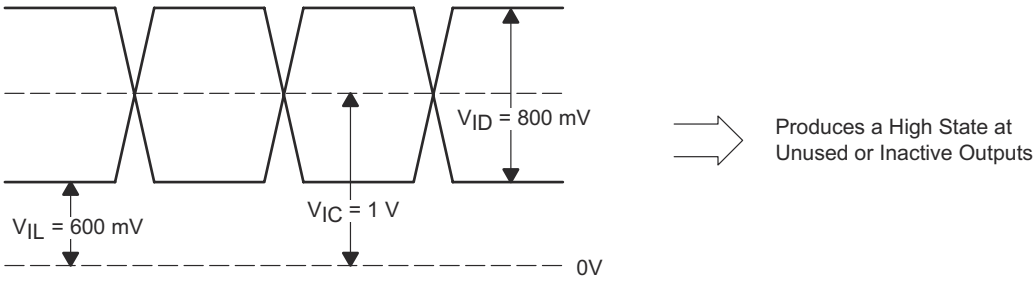

図 8-5. Waveform 3

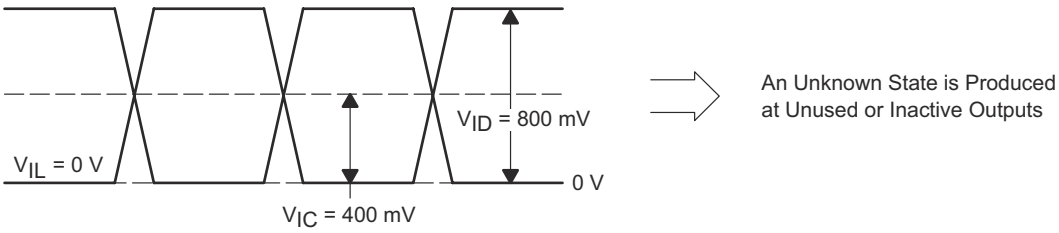

図 8-6. Waveform 4

In most applications, having a common-mode input close to ground and a differential voltage larger than 2 V is not customary. Because the common-mode input voltage is typically around 1.5 V, a 2-V V_{ID} would result in a V_{IL} of 0.5 V, thus satisfying the recommended V_{IL} level of greater than 0.4 V.

図 8-7 plots seven different input threshold curves from a variety of production lots and shows how the fail-safe circuitry behaves with the input common-mode voltage levels. These input threshold curves are representative samples of production devices. The curves specifically illustrate a typical range of input threshold variation. The

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AM26LV32 is specified with ±200 mV of input sensitivity to account for the variance in input threshold. Each data point represents the input's ability to produce a known state at the output for a given V_{IC} and V_{ID}. Applying a differential voltage at or above a certain point on a curve would produce a known state at the output. Applying a differential voltage less than a certain point on a curve would activate the fail-safe circuit and the output would be in a high state. For example, inspecting the top input threshold curve reveals that for a V_{IC} that is approximately 1.6 V, V_{ID} yields around 87 mV. Applying 90 mV of differential voltage to this particular production lot generates a known receiver output voltage. Applying a V_{ID} of 80 mV activates the input fail-safe circuitry and the receiver output is placed in the high state. Texas Instruments specifies the input threshold at ±200 mV, because normal process variations affect this parameter. Note that at common-mode input voltages around 0.2 V, the input differential voltages are low compared to their respective data points. This phenomenon points to the fact that the inputs are very sensitive to small differential voltages around 0.2 V V_{IC}. TI recommends that V_{IC} levels be kept greater than 0.5 V to avoid this increased sensitivity at V_{IC} ≈ 0.2 V. In most applications, because V_{IC} typically is 1.5 V, the fail-safe circuitry functions properly to provide a high state at the receiver output.

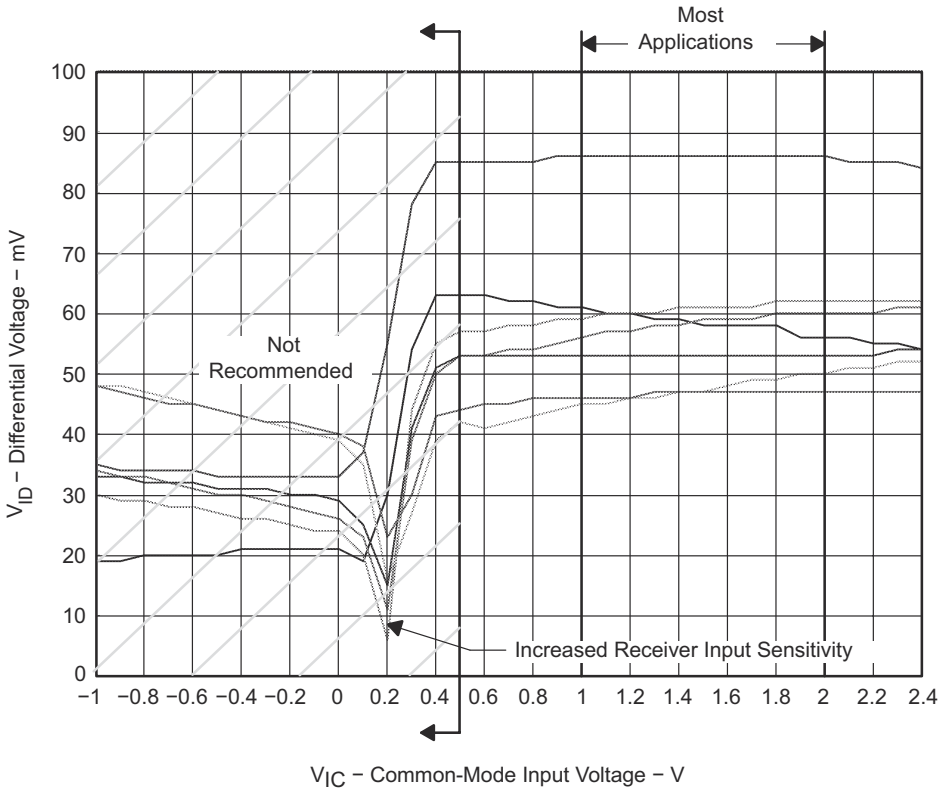

図 8-7. V_{IC} vs V_{ID} Receiver Sensitivity Levels

図 8-8 represents a typical application where two receivers are not used. In this case, there is no need to worry about the output voltages of the unused receivers because these are not connected in the system architecture.

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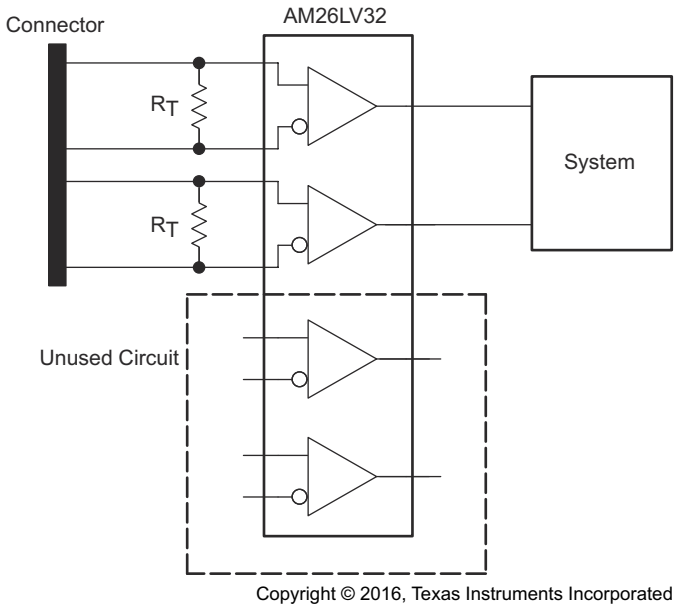

図 8-8. Typical Application With Unused Receivers

図 8-9 shows a common application where one or more drivers are either disabled or powered down. To ensure the inactive receiver outputs are in a high state, the active receiver inputs must have V_{IL} > 0.4 V and V_{IC} > 0.5 V.

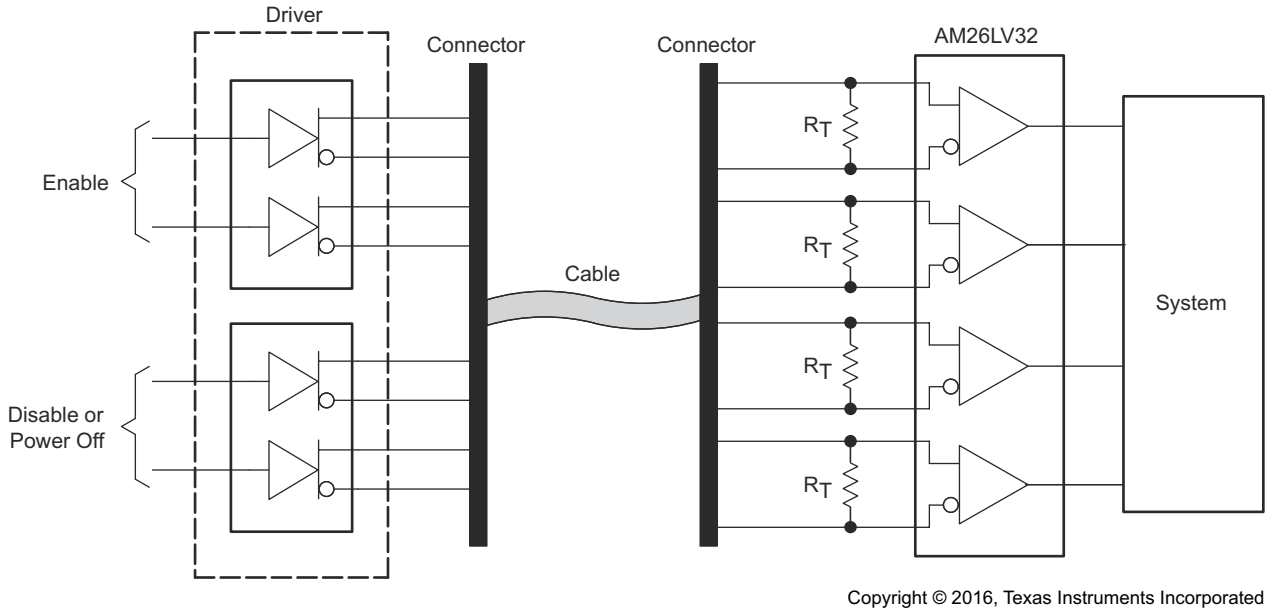

図 8-9. Typical Application Where Two or More Drivers Are Disabled

図 8-10 is an alternative application design to replace the application in 図 8-9. This design uses two AM26LV32 devices instead of one. However, this design does not require the input levels be monitored to ensure the outputs are in the correct state, only that they comply to the RS-232 standard.

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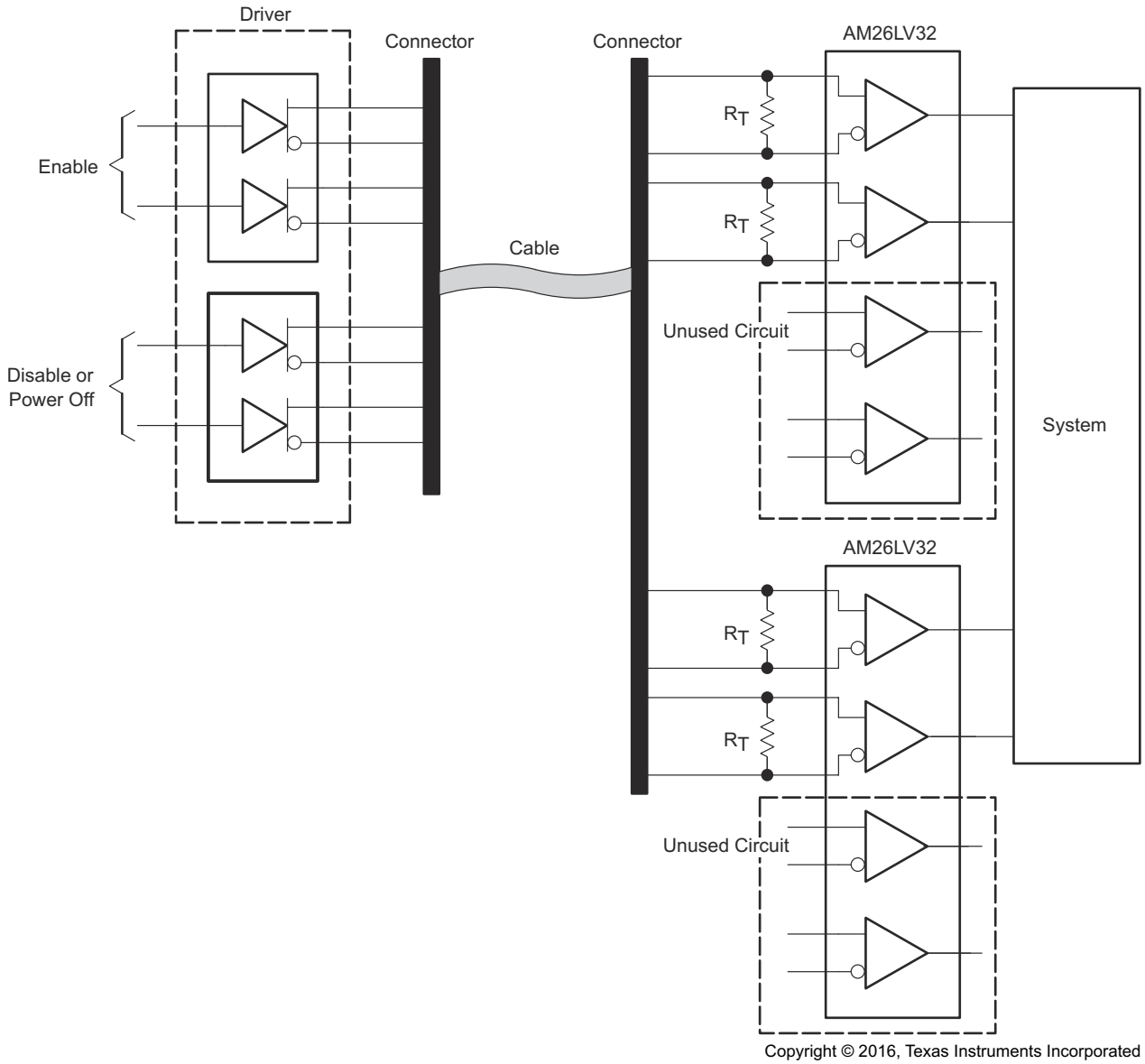

図 8-10. Alternative Solution for 図 8-9

図 8-11 and 図 8-12 show typical applications where a disconnected cable occurs. 図 8-11 illustrates a typical application where a cable is disconnected. Similar to 図 8-9, the active input levels must be monitored to make sure the inactive receiver outputs are in a high state. An alternative solution is shown in 図 8-12.

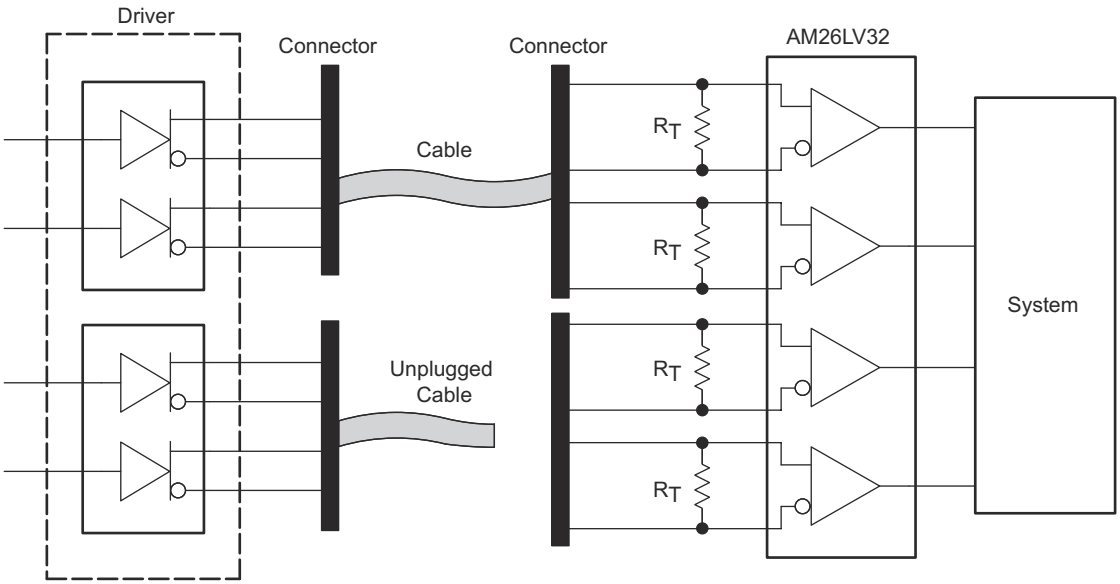

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図 8-11. Typical Application Where Two or More Drivers Are Disconnected

図 8-12 is an alternative solution so the receiver inputs do not have to be monitored. This solution also requires the use of two AM26LV32 devices instead of one.

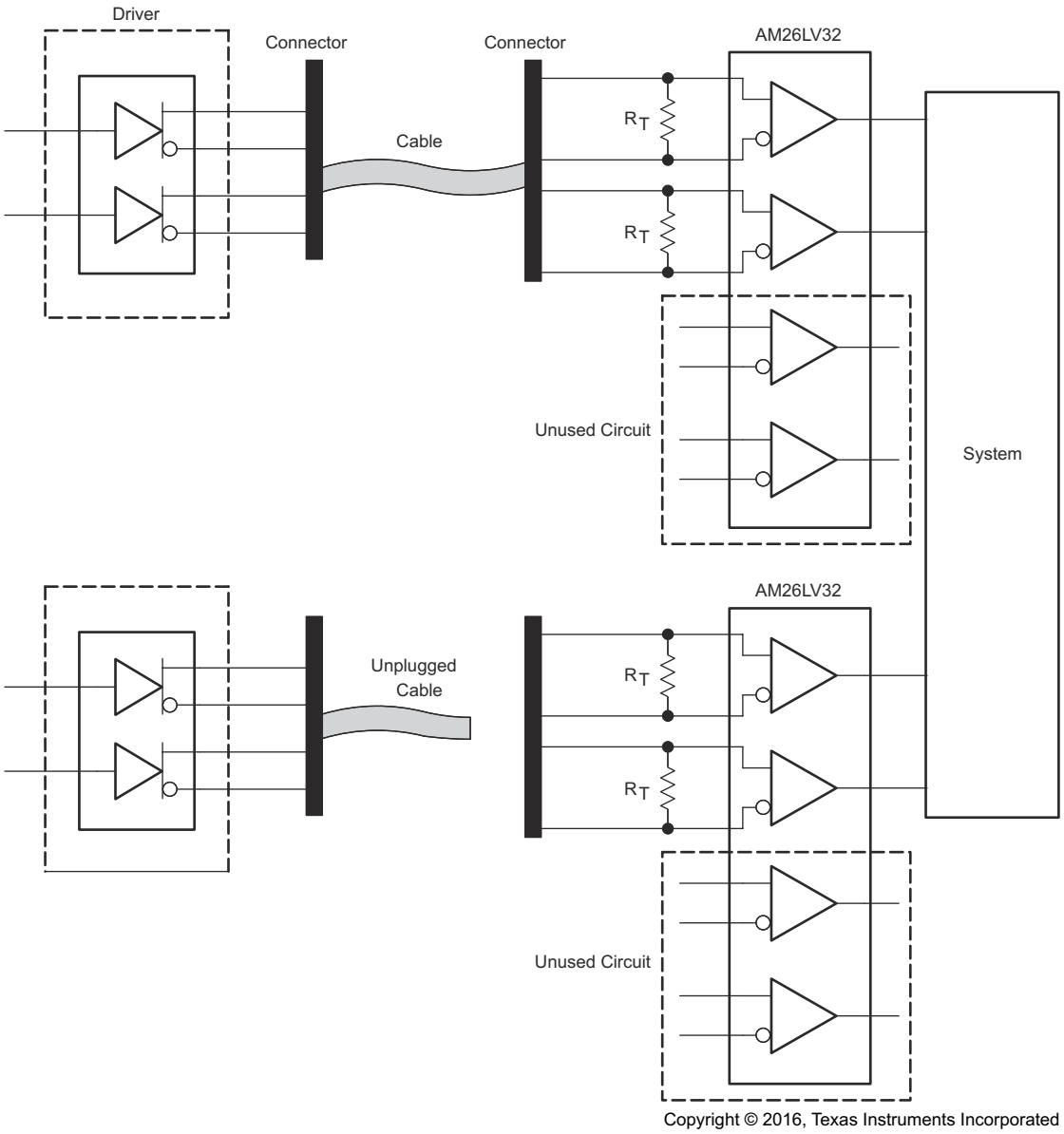

図 8-12. Alternative Solution to 図 8-11

When designing a system using the AM26LV32, the device provides a robust solution where fail-safe and fault conditions are of concern. The RS422-like inputs accept common-mode input levels from −0.3 V to 5.5 V with a specified sensitivity of ±200mV. As previously shown, take care with active input levels because this can affect the outputs of unused or inactive bits. However, most applications meet or exceed the requirements to allow the device to perform properly.

9 Application and Implementation

注

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9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS422 or RS485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques include unterminated lines, parallel termination, ac termination, and multipoint termination.

9.2 Typical Application

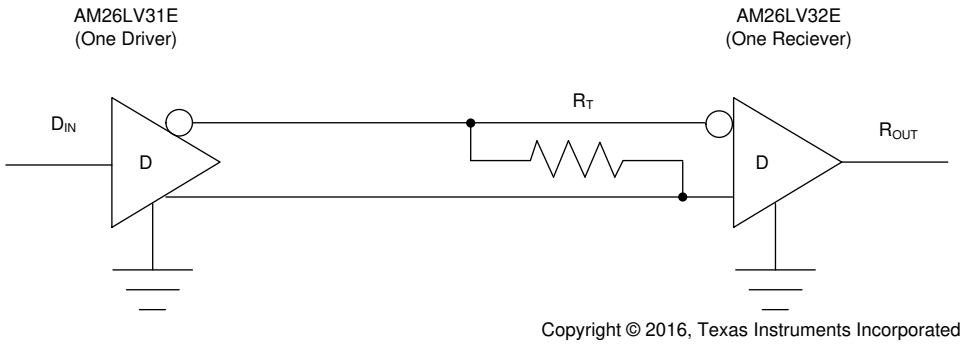

図 9-1. Differential Terminated Configuration

9.2.1 Design Requirements

Resistor and capacitor (if used) termination values vary from system to system. The termination resistor, R_T, must be within 20% of the characteristic impedance, R_{OUT}, of the cable and can vary from about 80 Ω to 120 Ω.

9.2.2 Detailed Design Procedure

図 9-1 shows a configuration with R_T as termination. Although reflections are present at the receiver inputs at a data signaling rate of 200 kbps with no termination, the RS422-compliant receiver reads only the input differential voltage and produces a clean signal at the output.

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9.2.3 Application Curve

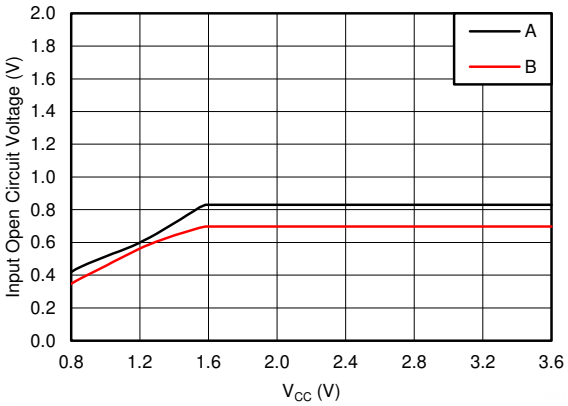

図 9-2. RS422 Port Open-Circuit Voltage vs V_{CC}

9.3 Power Supply Recommendations

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

9.4 Layout

9.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, and pay attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

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9.4.2 Layout Example

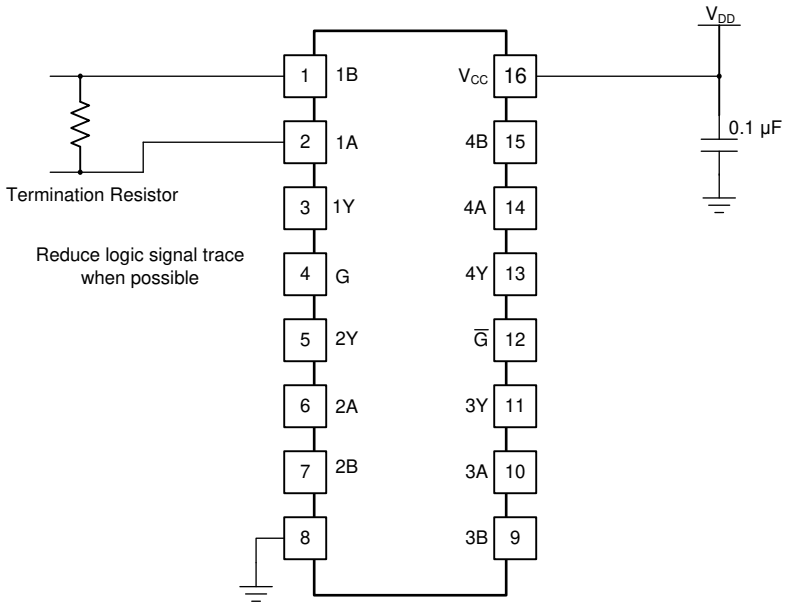

図 9-3. Layout With PCB Recommendations

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10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.5 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26LV32CD	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV32C	
AM26LV32CDE4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV32C	
AM26LV32CDG4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV32C	
AM26LV32CDR	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV32C	
AM26LV32CDRE4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV32C	
AM26LV32CDRG4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26LV32C	
AM26LV32CNSR	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LV32	
AM26LV32CNSRG4	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26LV32	
AM26LV32ID	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV32I	
AM26LV32IDE4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV32I	
AM26LV32IDG4	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV32I	
AM26LV32IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26LV32I	Samples
AM26LV32INS	LIFEBUY	SO	NS	16	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV32I	
AM26LV32INSG4	LIFEBUY	SO	NS	16	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV32I	
AM26LV32INSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26LV32I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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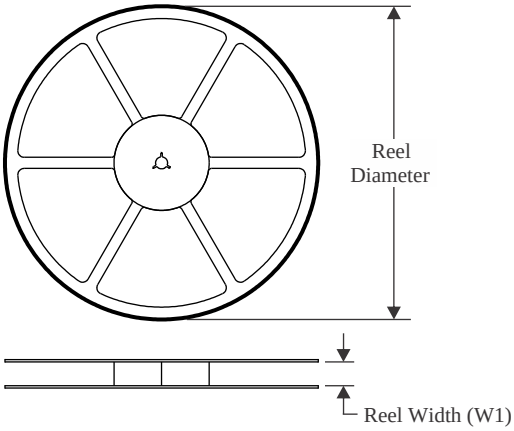
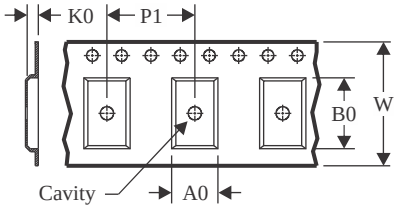
TAPE AND REEL INFORMATION

REEL DIMENSIONS

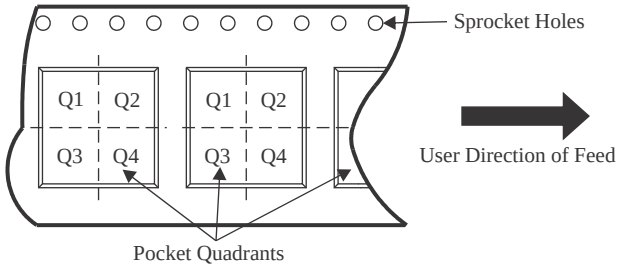


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

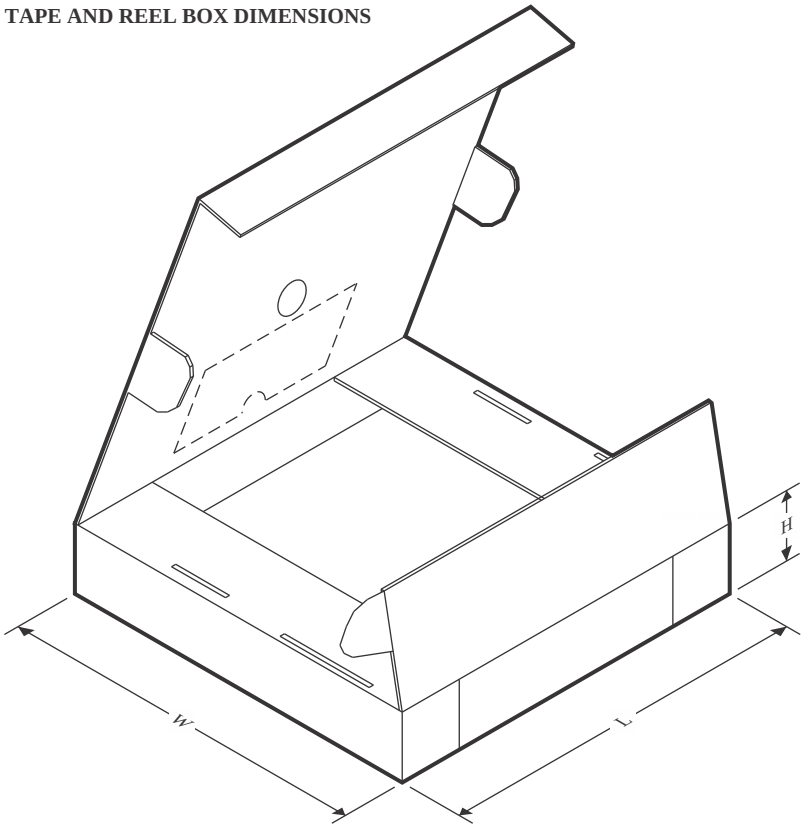
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV32CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV32CDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV32CDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV32CNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV32IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV32IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26LV32INSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26LV32INSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

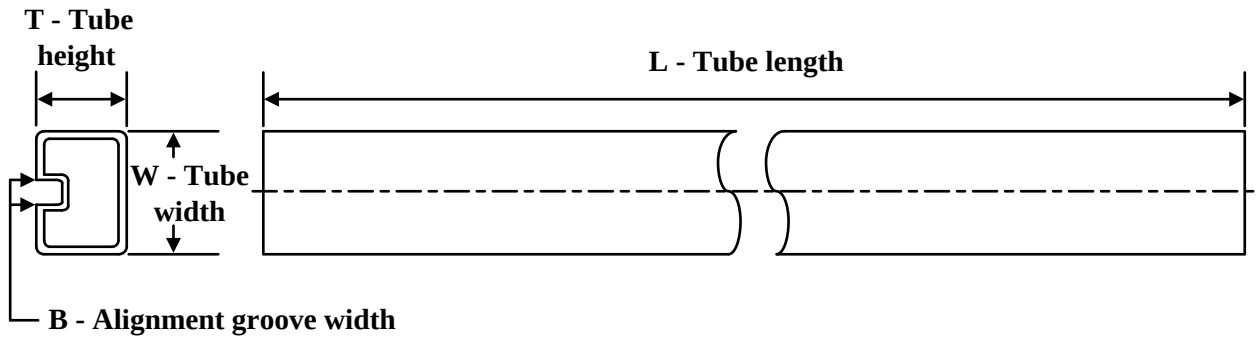
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

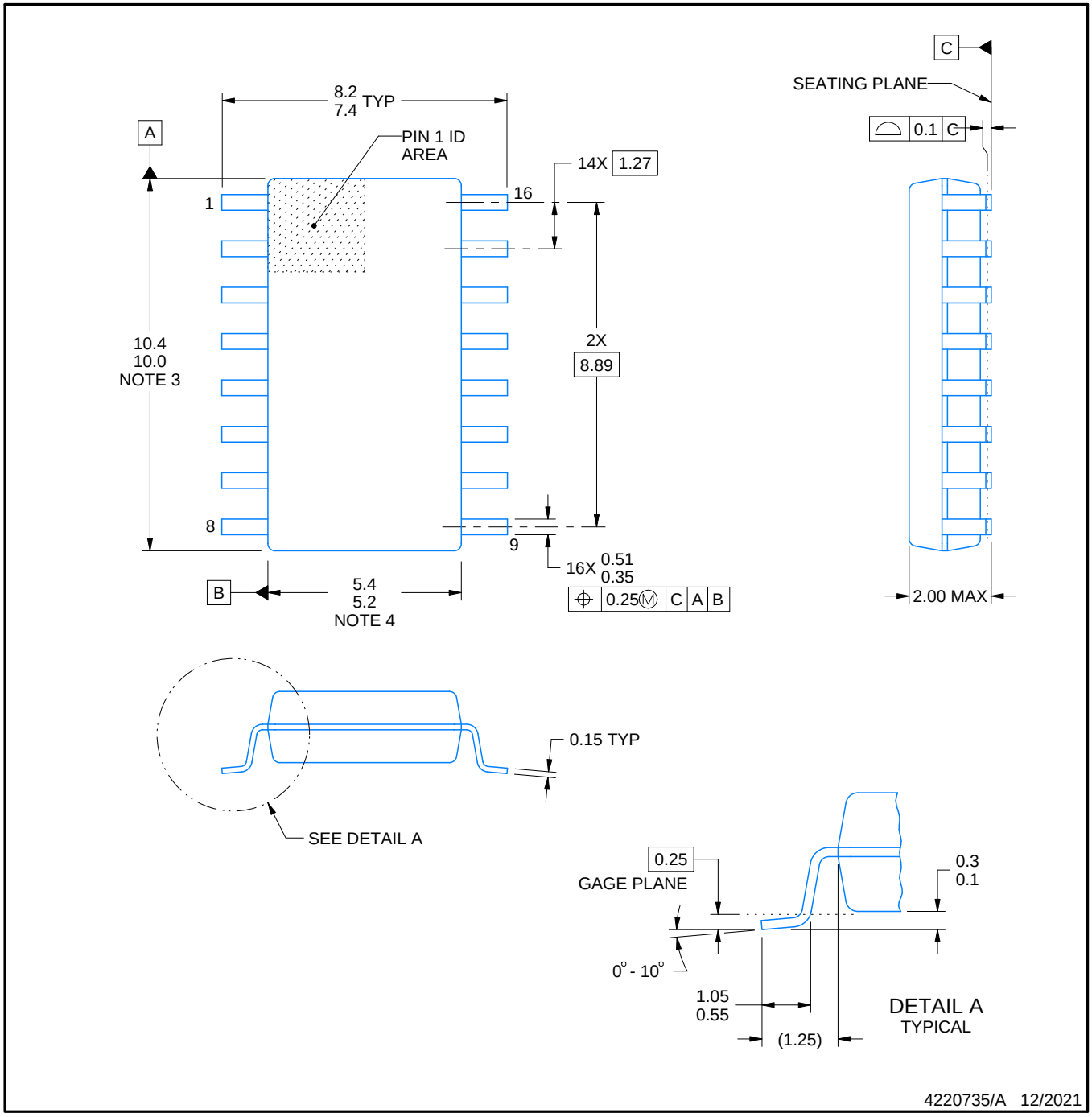
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV32CDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV32CDRG4	SOIC	D	16	2500	356.0	356.0	35.0
AM26LV32CDRG4	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV32CNSR	SO	NS	16	2000	356.0	356.0	35.0
AM26LV32IDR	SOIC	D	16	2500	353.0	353.0	32.0
AM26LV32IDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26LV32INSR	SO	NS	16	2000	367.0	367.0	38.0
AM26LV32INSR	SO	NS	16	2000	353.0	353.0	32.0

TUBE



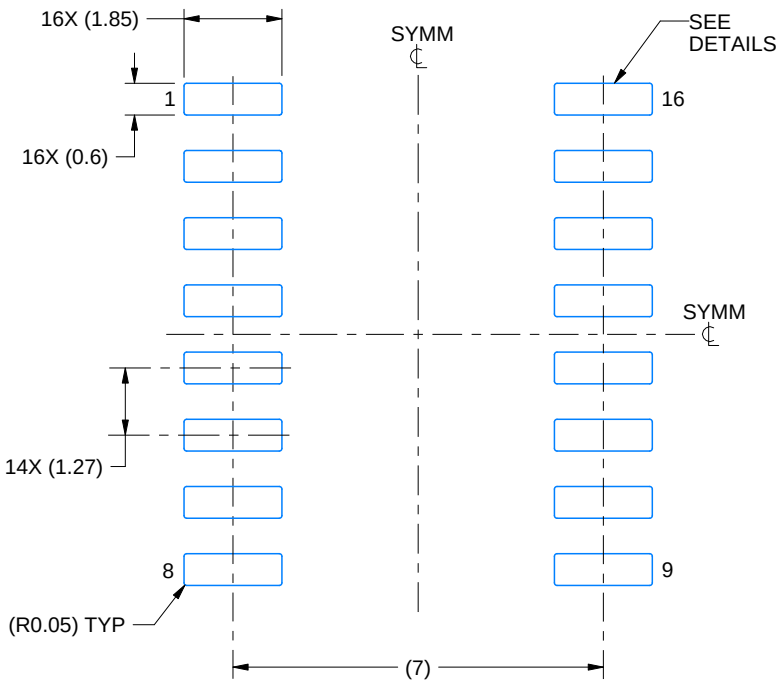
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AM26LV32CD	D	SOIC	16	40	507	8	3940	4.32
AM26LV32CD	D	SOIC	16	40	506.6	8	3940	4.32
AM26LV32CDE4	D	SOIC	16	40	507	8	3940	4.32
AM26LV32CDE4	D	SOIC	16	40	506.6	8	3940	4.32
AM26LV32CDG4	D	SOIC	16	40	507	8	3940	4.32
AM26LV32CDG4	D	SOIC	16	40	506.6	8	3940	4.32
AM26LV32ID	D	SOIC	16	40	507	8	3940	4.32
AM26LV32IDE4	D	SOIC	16	40	507	8	3940	4.32
AM26LV32IDG4	D	SOIC	16	40	507	8	3940	4.32
AM26LV32INS	NS	SOP	16	50	530	10.5	4000	4.1
AM26LV32INSG4	NS	SOP	16	50	530	10.5	4000	4.1

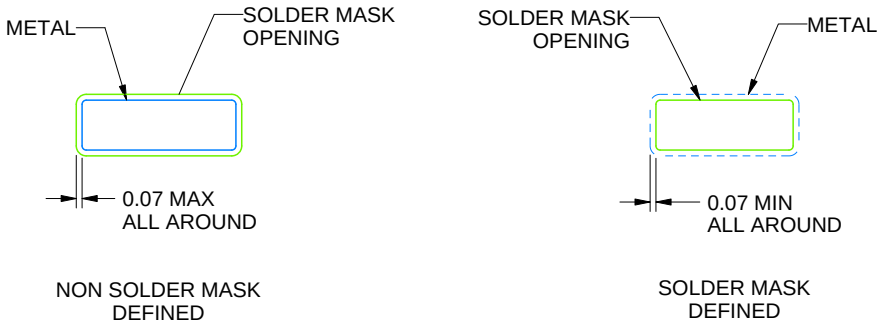


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

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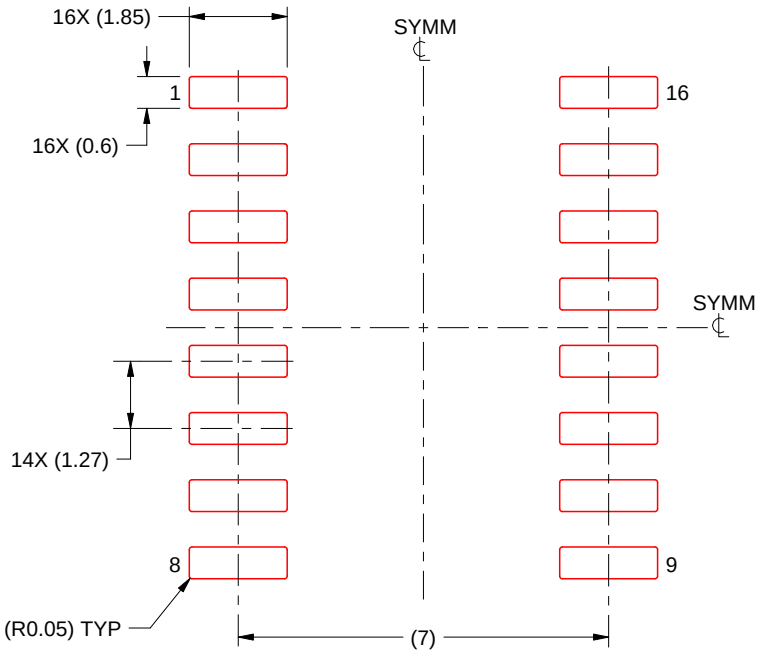
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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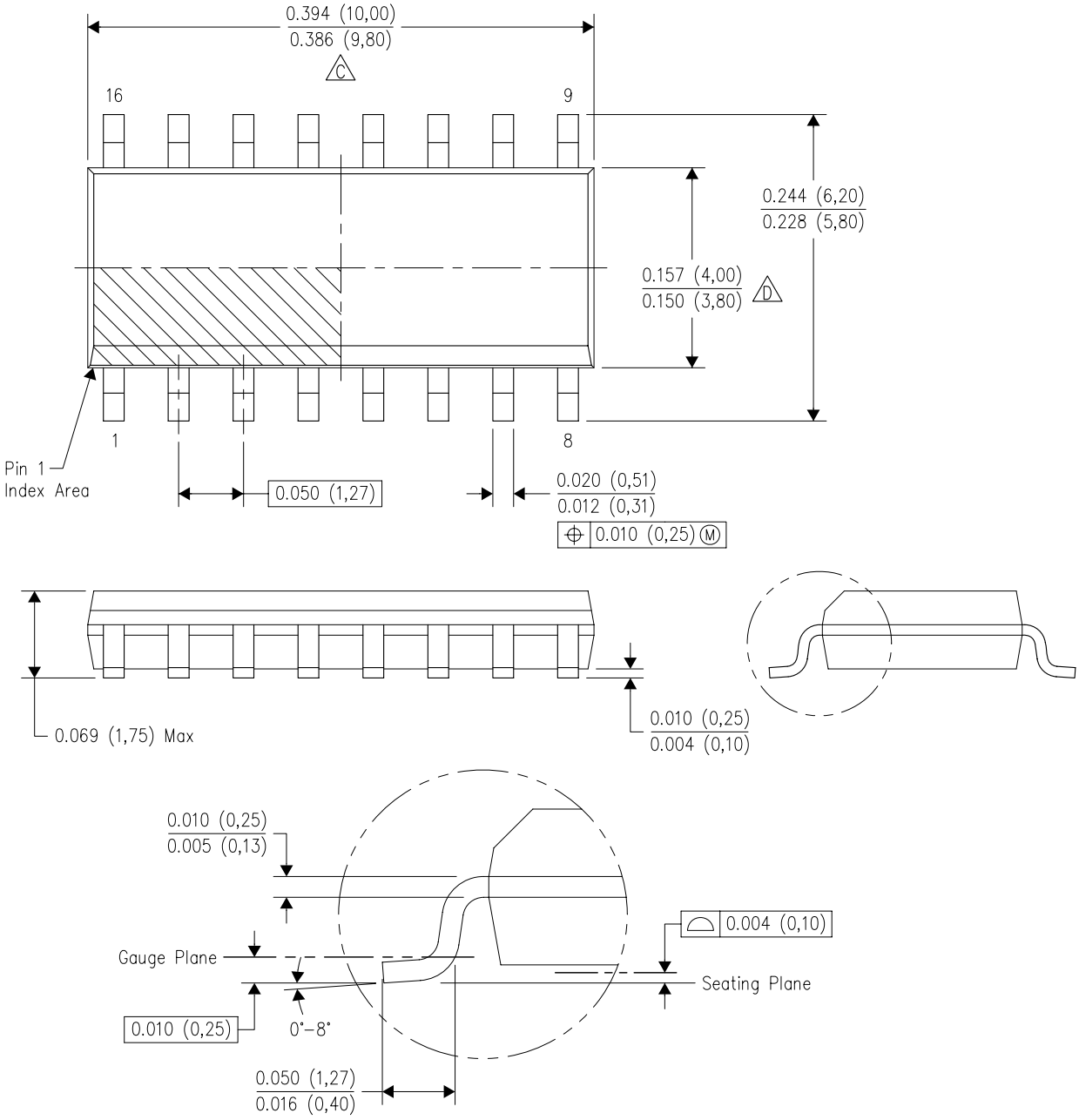
NOTES: (continued)

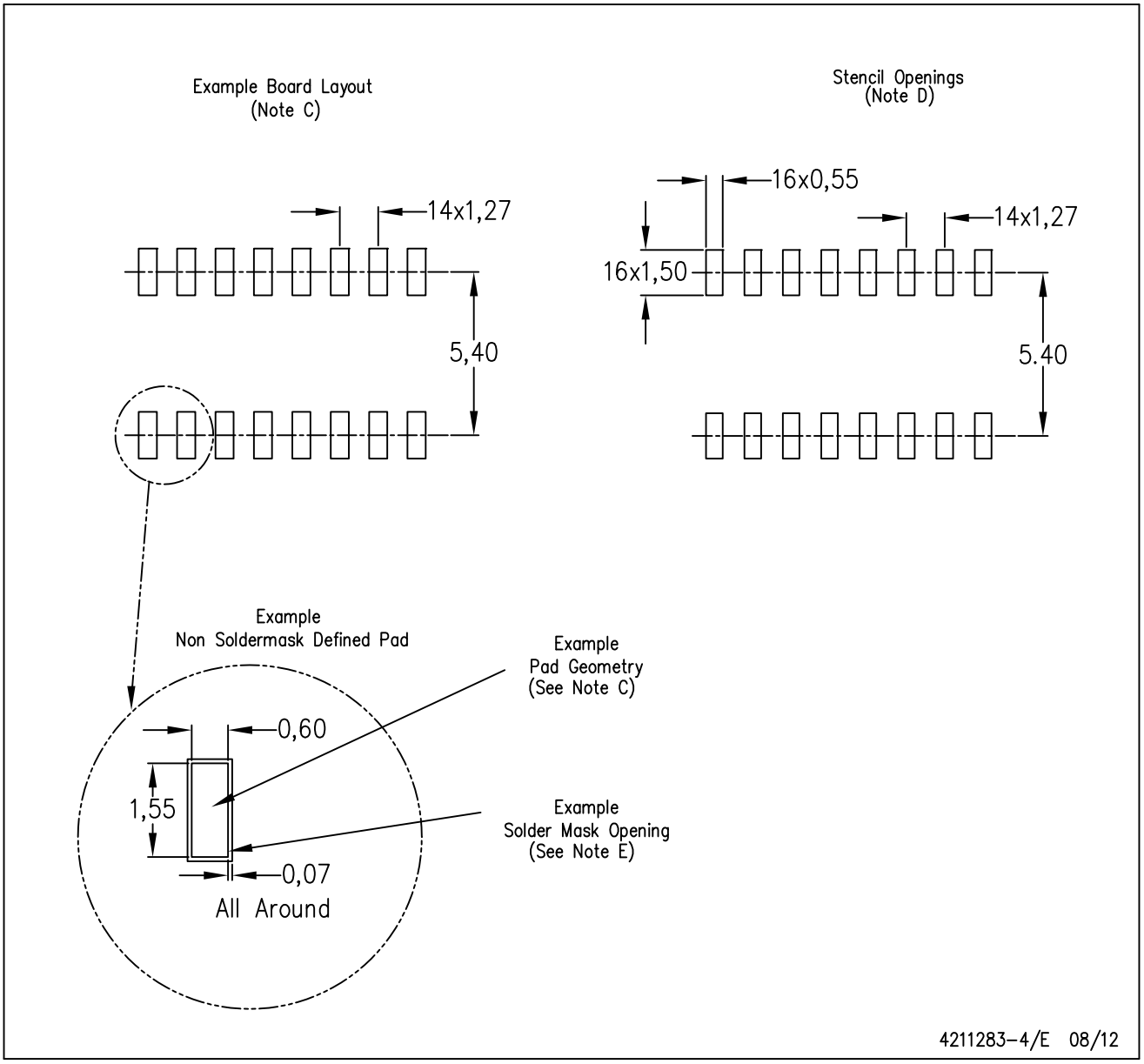
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

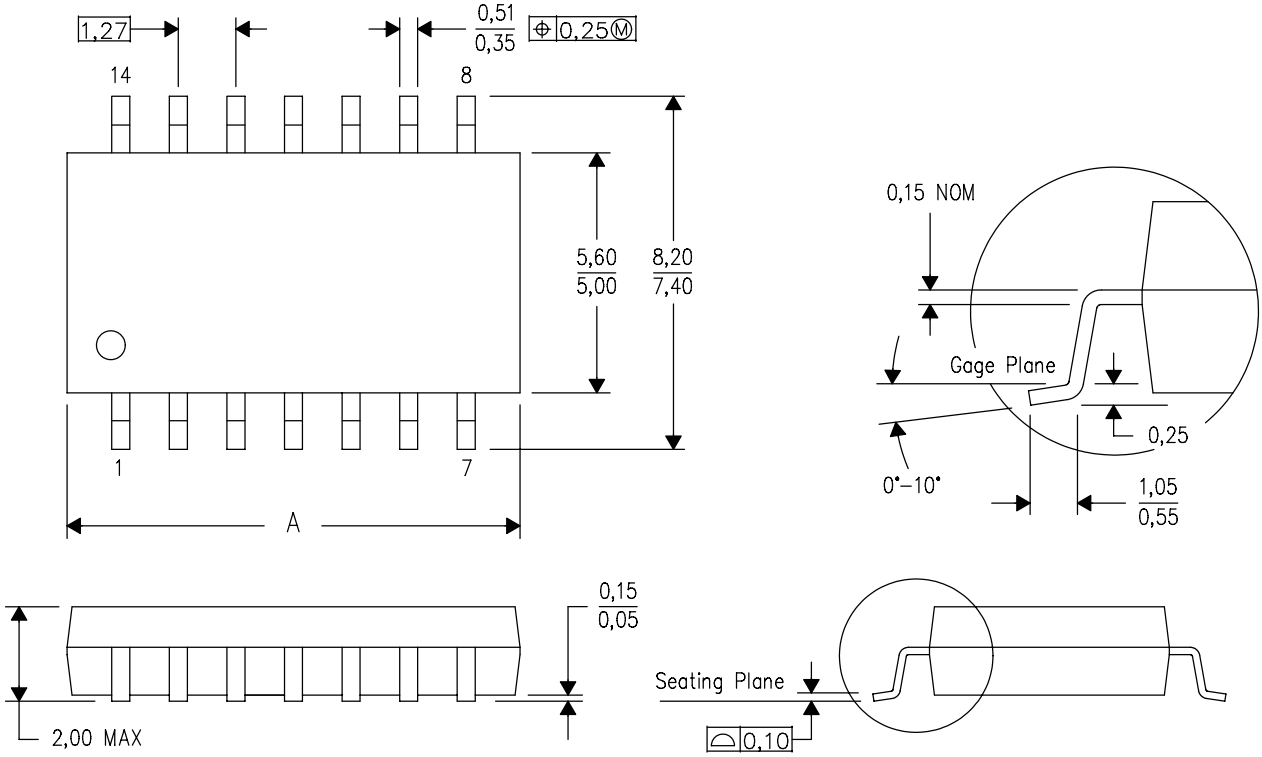


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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