New DSP development environment includes data converter plug-ins

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System designs that include a DSP and one or more data converters consistently increase in complexity. In addition, design engineers are asked to release new applications faster to market. To support both increasing system complexity and shorter design cycles, new development systems had to improve in code generation as well as in efficient debugging capabilities. Therefore, previous compilers were developed in close conjunction with related simulators and hardware emulators. Today all these modules have been integrated into one development system, the Code Composer Studio™ (CCS).

The CCS developments took into consideration the increasing complexity of the on-chip peripheral DSP modules such as serial and parallel ports, timer, memory, and interrupt handler. User functions, written as subroutines that configure the DSP on-chip peripherals, have been combined into libraries, thus enabling the user to execute easily the many configuration options available. In an additional step, subroutines that configure and read or write to analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) have been developed for all major DSP families. The user may generate configuration data using a graphical user interface provided by a CCS plug-in.

Such a plug-in allows the designer to choose from the many options to configure a data converter via a dialog window. The dialog window provides several parameters that allow the ADC configuration to be tailored to the exact needs of the application. Once the parameters have been selected, the tool generates the necessary functions for the C-program that are required to configure the data converter. Functions to initiate the data transfer via the ADC-DSP interface and to read ADC conversion results are also generated. If a subsequent test reveals that another ADC configuration could improve the data transfer—i.e., in data throughput or in power saving—the user can return to the dialog window to select different parameters. The code generation and compilation follow with just a few mouse clicks, so that the interface then can be tested immediately for optimal performance.

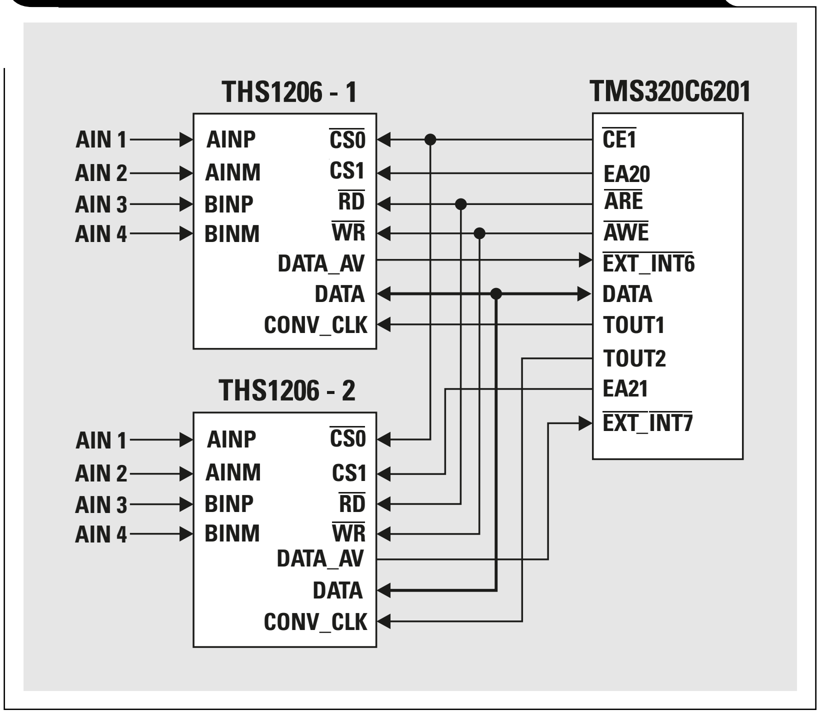
Optimized DSPs for portable and high-performance applications

Texas Instruments offers a variety of DSP architectures optimized for a wide range of applications. In addition to DSPs for motor and process controls, there are low-cost DSPs with floating-point architecture for a variety of industrial systems. To allow for high portability, the processors are often programmed in C, using the highly efficient, optimizing C-compilers.

The C5000 architecture with its many derivatives is designed for extremely low power consumption. Good examples of low-power applications are digital mobile phones such as GSM phones and PCS-1900 phones, whose standby and talk time increase with each generation. Other recent developments using the C5000 family are the Web-phones.

The C6000 DSPs offer processor performance up to several thousand MIPS (million instructions per second). Those devices are mainly used in applications requiring large processing power and high data throughput, such as compression algorithms in the audio and video segment. Typical applications are central office DSL modems as well as GSM base stations, where many data channels need to be processed simultaneously.

Figure 1. Interfacing two THS1206 ADCs to a C6201 DSP



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State-of-the-art data converters offer many options

Besides the increase in DSP performance, new applications also require the increase in data converter performance. For that purpose Texas Instruments recently released the 12-bit ADC, THS1206, used for industrial control applications, and the 16-bit analog interface controller (AIC), TLV320AIC10, for telecom applications.

Modern ADCs, such as the THS1206, provide a vast amount of configuration options that enable the user to configure the ADC optimally to the system application. These options need to be initialized before the actual data transfer begins; however, during operation those options may be reprogrammed to match possible changes in system requirements.

The THS1206 samples the analog input signal at a rate of 6 MSPS (million samples per second). For applications requiring more than one analog channel, the ADC provides four single-ended, analog input channels that can be sampled simultaneously at a rate of up to 1.5 MSPS. To improve the signal-to-noise ratio (SNR), the four single-ended channels can be configured to two differential input channels. Another option is to use one differential channel and two single-ended channels.

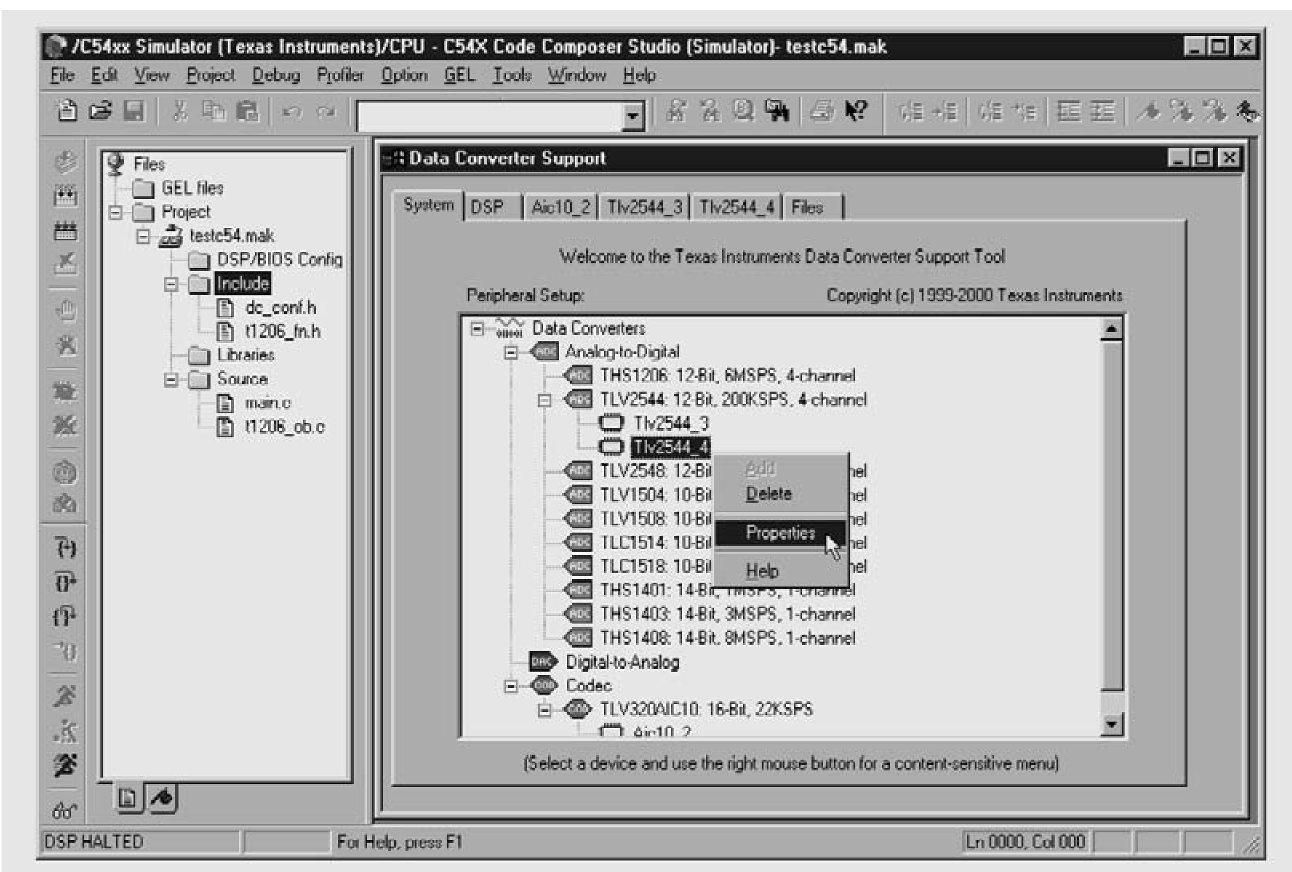
The parallel interface of the ADC can be directly connected to the DSP without external logic. Figure 1 illustrates the interface of two THS1206 ADCs to a C6201 DSP. The DSP addresses both ADCs individually without the need for an address decoder.

The ADC contains an on-chip circular FIFO that improves the data throughput significantly. Without this FIFO, the DSP would have to read each sample separately. At a sample rate of 6 MSPS, the interrupt processing effort would increase enormously, which would not allow the DSP enough time for further signal processing. The on-chip FIFO, however, allows the DSP to read entire blocks of ADC conversion results in burst mode operation. To optimally interface the ADC to various DSPs with different processor speed, at different sample rates, the FIFO provides programmable pointers. This way the DSP is able to read the optimal number of samples after an interrupt occurs.

To optimize the ADC configuration, all available options are programmed via the two 10-bit control registers of the THS1206. The DSP needs to execute two write-cycles to define the register content with the required bit combination. Via the dialog window, Code Composer Studio generates the right bit combinations as well as the program code to initialize the ADC, based on the THS1206 plug-in.

The TLV320AIC10 offers a complete data acquisition system on one chip. The device contains ADC, DAC,

Figure 2. The “Data Converter Support” dialog window within CCS



anti-aliasing filter, and many more programmable functions. The AIC10 interfaces to a DSP via a serial port. A maximum of up to eight AICs can be connected directly to one DSP serial port without external logic.

Code Composer Studio is an integrated development environment (IDE) for the latest TMS320C5000 and C6000 DSP platforms. The basic functions include C-compiler, assembler, linker, simulator, and hardware debugger. In addition, CCS provides DSP/BIOS™ technology and Real-Time Data Exchange (RTDX).

An important element is the anytime-expandable plug-in architecture. This open architecture allows third parties to integrate their specific DSP tools smoothly into CCS. System designers can choose between the plug-ins from Texas Instruments or plug-ins from third parties for a seamless implementation into their own programs. This method reduces the design cycle dramatically, since designers can focus exclusively on their essential development tasks.

Plug-ins for data converters

Texas Instruments uses the plug-in architecture to extend the development environment by gradually implementing the company's product portfolio of DSP-optimized ADCs and DACs. The goal is to simplify the designer's task dramatically, to integrate these data converters from device initialization up to the sample processing into his own algorithm.

When calling the "Data Converter Support" menu option within CCS (see Figure 2), the designer can choose from existing ADC, DAC, and AIC devices. Via the "Add" context menu in the dialog window, the desired converter is added to the system. Selecting "Properties" with the converter selected makes the configuration dialog window appear.

Figure 3 gives an example for the THS1206. This window consists of the following three segments: "Interface Settings," "ADC Settings," and "Current Control Selection." "Interface Settings," for example, includes the definition of the ADC address within the DSP memory space, the polarity of the edge of the interrupt signal, and the format of the transferred data. Within "ADC Settings," the number of analog-input channels and their operation modes is defined. In addition, the user determines the ADC conversion clock and configures the FIFO by setting the trigger level. Finally, "Current Control Selection" provides the resulting bit combination for the two control registers of the THS1206.

The following step automatically generates the source code for the ADC initialization. This code is inserted into the application project via the project manager. This way all functions are callable from the main application program.

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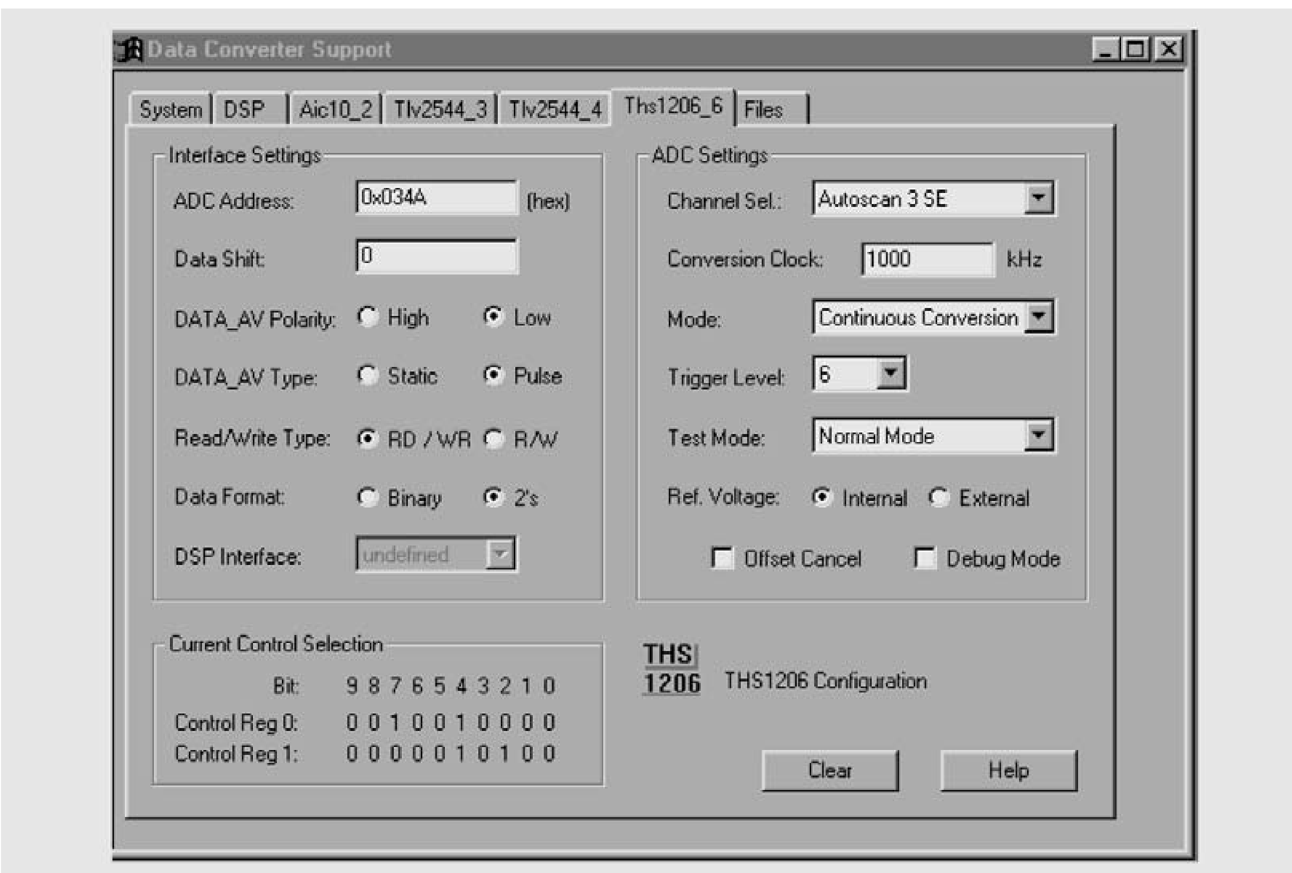
Figure 3. Various options of the THS1206 ADC for data converter setup



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The designer can use these functions in initialization routines as well as in the actual data processing algorithms. After the source code implementation, the overall system test can begin. If the user discovers that different settings are required, he returns to the "Data Converter Support" dialog window and selects new parameters.

Future outlook

The current version of CCS already includes support for 11 data converters. Further devices currently under development will be integrated gradually into the plug-in. An installation program, updated with the latest plug-in, is available for downloads from TI's Web site at www.ti.com/sc/dcplug-in. This program is downward-compatible with previous CCS versions. Every update of the CCS CD-ROM includes the latest plug-in version. Program examples for some of the DSP DSKs and data converter EVMs are also available. Future standard software interfaces for ADCs and DACs are currently under development.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
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