TPSM84203、TPSM84205、TPSM84212 1.5A、28V 输入、TO-220 电源模块

1 特性

- 完全集成的电源解决方案
- 3 引脚 TO-220 封装
- 效率高达 95%
- 固定输出电压选项：3.3V、5V 和 12V
- 400kHz 开关频率
- 高级 Eco-mode™ 脉冲跨周期
- 预偏置输出启动
- 过流保护
- 输出过压保护
- 过热保护
- 工作结温范围：–40°C 至 +125°C
- 工作环境温度范围：-40°C 至 +85°C
- 符合 EN55022 B 类辐射标准
- 使用 TPSM84203 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 12V 和 24V 分布式电源总线供电
- 工业白色家电
- 消费类
  - 音频
  - 机顶盒 (STB)、数字电视 (DTV)
  - 打印机

3 说明

TPSM842xx 电源模块是一种简单易用的集成式电源解决方案，它将 1.5A 直流/直流转换器与功率 MOSFET、电感器和无源器件整合在一个 3 引脚的穿孔插入式封装内。这套完备的电源解决方案只需要增加输入和输出电容器，省去了设计过程中的环路补偿和磁性元件选择。

借助标准 TO-220 引脚，可在这一业界标准封装中更换为明显改善的线性稳压器。TPSM842xx 器件提供更高的效率而无需散热片。

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPSM84203	EAB	10mm x 11mm
TPSM84205		
TPSM84212		

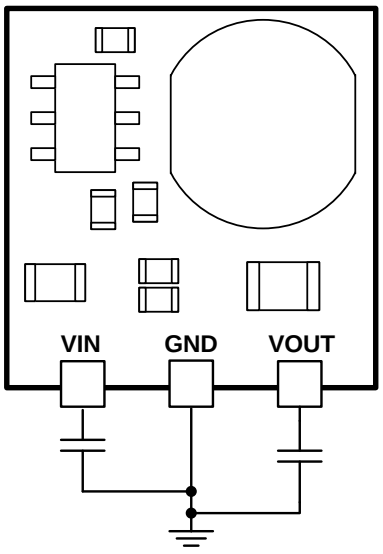
(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

器件比较

器件编号	输出电压
TPSM84203	3.3V
TPSM84205	5.0V
TPSM84212	12.0V

简化应用

TPSM842xx



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4 修订历史记录

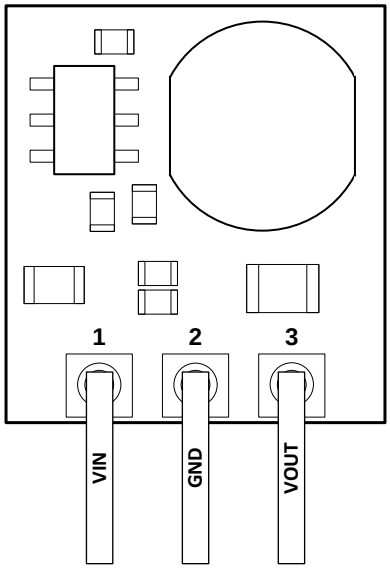
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (July 2017) to Revision A **Page**

- 添加了特性：符合 EN55022 B 类辐射发射标准 ... 1
- Added the *EMI* section ... 16

5 Pin Configuration and Functions

EAB Package
3-Pin Through-Hole
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2		Ground. This is the return current path for the power stage of the device. Connect this pin to the bypass capacitors associated with VIN and VOUT.
VIN	1	I	Input Voltage. This pin supplies voltage to the control circuitry and power switches of the converter. Connect external bypass capacitors between this pin and GND.
VOUT	3	O	Output Voltage. This pin is connected to the internal output inductor. Connect this pin to the output load and connect external bypass capacitors between this pin and GND.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Input Voltage		–0.3	30	V
Output Voltage	TPSM84203	–0.3	3.9	V
	TPSM84205	–0.3	5.7	V
	TPSM84212	–0.3	13.0	V
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1msec, 1/2 sine, mounted		1500	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		10	G
Operating IC Junction Temperature range, T_J (2)		–40	125	°C
Operating Ambient Temperature range, T_A (2)		–40	85	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
V_{IN}	Input voltage	TPSM84203	4.5	28	V
		TPSM84205	7	28	V
		TPSM84212	14.5	28	V
I_{OUT}	Output current		0	1.5	A
T_A	Operating ambient temperature range(1)		–40	85	°C
T_J	Operating junction temperature range(1)		–40	125	°C

(1) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Thermal Information

THERMAL METRIC(1)		TPSM842xx EAB 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	56	°C/W
ψ_{JT}	Junction-to-top characterization parameter (3)	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter (4)	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics paper.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 50 mm × 50 mm double-sided PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the controller IC.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the module board 1 mm from the controller IC.

6.5 Electrical Characteristics

Over -40°C to +85°C free-air temperature range, V_{IN} = 24 V, I_{OUT} = I_{OUT} max, F_{SW} = 400 kHz, C_{IN} = 0.1µF, 50V ceramic; 10µF, 50V ceramic; 100µF, 35V electrolytic, and C_{OUT} = 2 x 47µF, 16V 1210 ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)							
V_{IN}	Input voltage range	Over V_{OUT} range	TPSM84203	4.5(1)		28	V
			TPSM84205	7(1)		28	V
			TPSM84212	14.5(1)		28	V
V_{IN_UVLO}	V_{IN} under voltage lock out	V_{IN} increasing			4.1	4.4	V
		V_{IN} decreasing		3.3	3.6		V
OUTPUT VOLTAGE (VOUT)							
V_{OUT}	Output voltage	Over I_{OUT} range	TPSM84203		3.3		V
			TPSM84205		5.0		V
			TPSM84212		12.0		V
	Set-point voltage tolerance	T_A = 25°C, I_{OUT} = 0 A		–3%		+3%	
	Temperature variation(2)	–40°C ≤ T_A ≤ 85°C, I_{OUT} = 0 A			0.4%		
	Line regulation	Over V_{IN} range, I_{OUT} = 1 A			0.4%		
	Load regulation	Over I_{OUT} range			0.5%		
	Output voltage ripple	20 MHz bandwidth, peak-to-peak, I_{OUT} > 500 mA			15		mV
OUTPUT CURRENT							
I_{OUT}	Output current	See SOA graph for derating over temperature.		0		1.5	A
	Overcurrent threshold				3.1		A
PERFORMANCE							
η	Efficiency(3)	V_{IN} = 5 V, I_{OUT} = 1 A	V_{OUT} = 3.3 V		92%		
		V_{IN} = 12 V, I_{OUT} = 1 A	V_{OUT} = 3.3 V		91%		
			V_{OUT} = 5.0 V		92%		
		V_{IN} = 24 V, I_{OUT} = 1 A	V_{OUT} = 3.3 V		87%		
			V_{OUT} = 5.0 V		90%		
			V_{OUT} = 12.0 V		94%		
	Transient response(2)	1 A/µs load step, 25% to 75% IOUT(max), COUT= 94 µF	V_{OUT} over/undershoot		4%		V_{OUT}
			Recovery time		100		µs

(1) The minimum input voltage is the lowest ensured voltage that will produce the nominal output voltage. See the Drop-Out Voltage section for information on drop-out voltage.
(2) Specified by design. Not production tested.
(3) See the efficiency graphs in the Typical Characteristics section for efficiency over the entire load range.

Electrical Characteristics (continued)

Over -40°C to +85°C free-air temperature range, V_{IN} = 24 V, I_{OUT} = I_{OUT} max, F_{SW} = 400 kHz, C_{IN} = 0.1µF, 50V ceramic; 10µF, 50V ceramic; 100µF, 35V electrolytic, and C_{OUT} = 2 x 47µF, 16V 1210 ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SOFT START							
T_{SS}	Internal soft start time(2)				5		ms
THERMAL SHUTDOWN							
	Rising threshold(2)				165		°C
	Hysteresis(2)				10		°C
CAPACITANCE							
C_{IN}	External input capacitance	Ceramic type		10			µF
		Non-ceramic type		0	100		µF
C_{OUT}	External output capacitance	Ceramic type	TPSM84203	94		470	µF
			TPSM84205				
			TPSM84212	47		470	µF
		Total output capacitance		0		500(4)	µF
		Equivalent series resistance (ESR)				35	mΩ

(4) The maximum output capacitance of 500 µF includes the combination of both ceramic and non-ceramic capacitors.

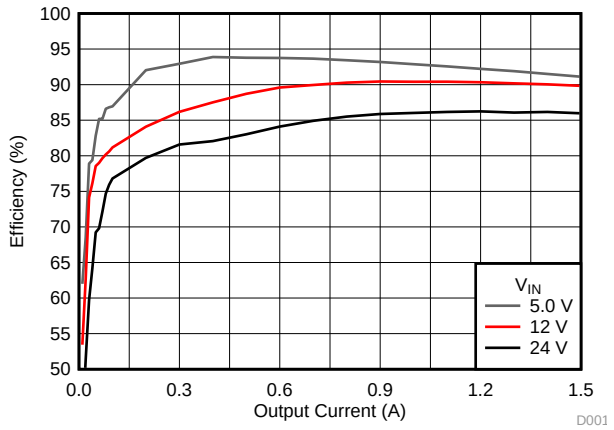
6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{SW}	Switching frequency		290	400	510	kHz

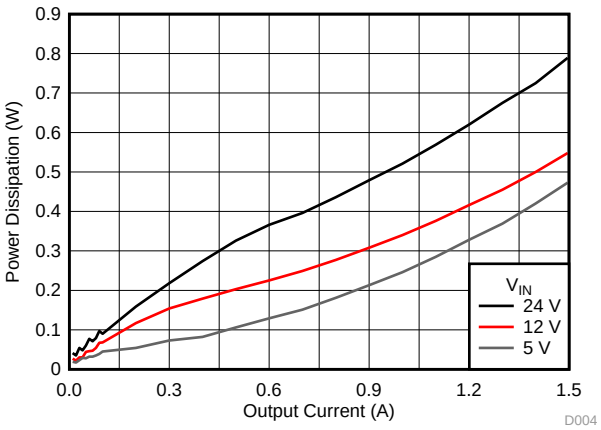
6.7 Typical Characteristics (V_{OUT} = 3.3 V)

Typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device. Safe operating area curves were measured using a Texas Instruments evaluation module (EVM).



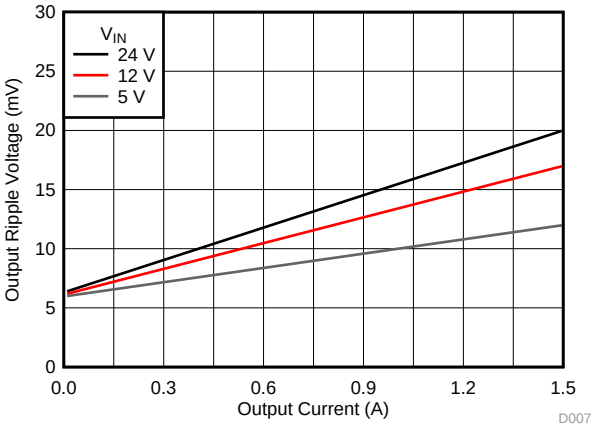
V_{OUT} = 3.3 V

图 1. Efficiency vs Output Current



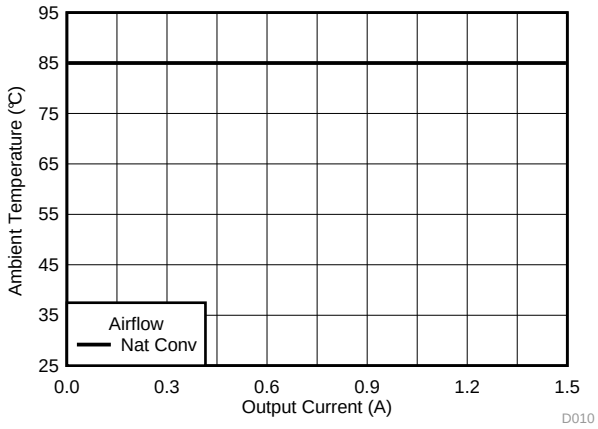
V_{OUT} = 3.3 V

图 2. Power Dissipation vs Output Current



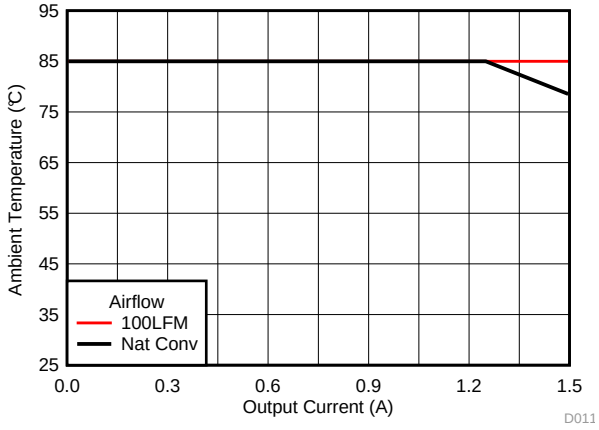
V_{OUT} = 3.3 V C_{OUT} = 2x 47 µF

图 3. Ripple Voltage vs Output Current



V_{OUT} = 3.3 V V_{IN} ≤ 15 V

图 4. Safe Operating Area

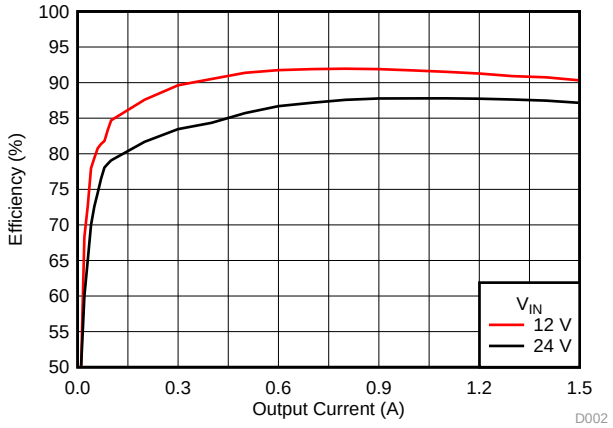


V_{OUT} = 3.3 V V_{IN} = 24 V

图 5. Safe Operating Area

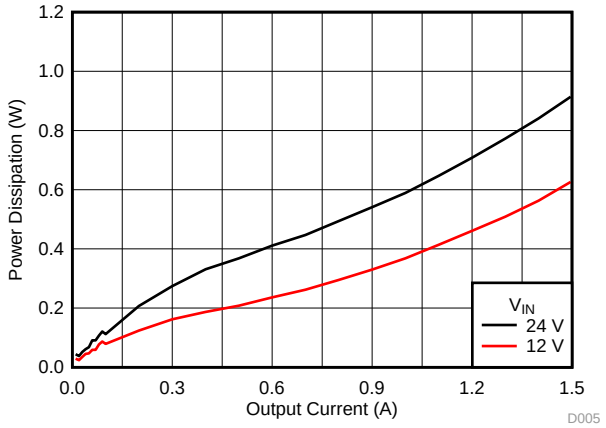
6.8 Typical Characteristics (V_{OUT} = 5 V)

Typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device. Safe operating area curves were measured using a Texas Instruments evaluation module (EVM).



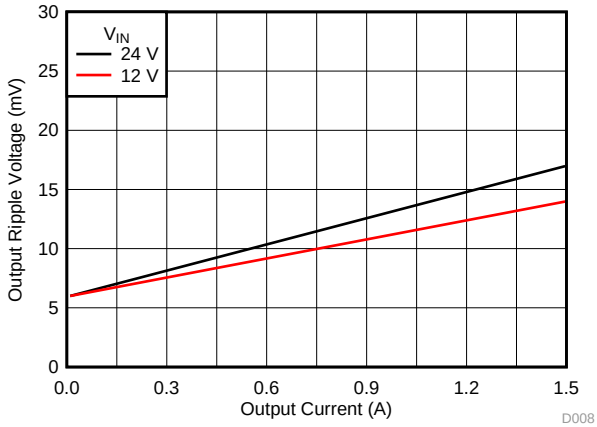
V_{OUT} = 5 V

图 6. Efficiency vs Output Current



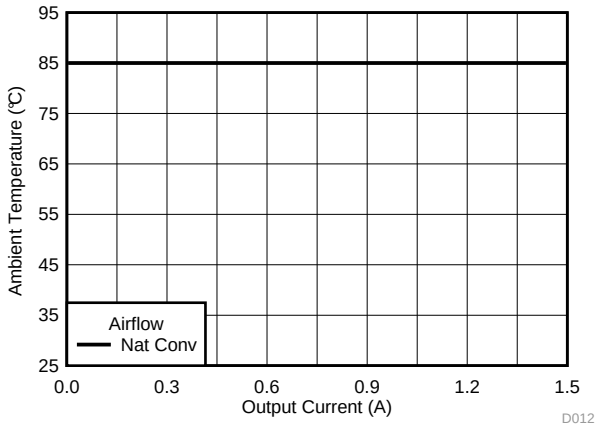
V_{OUT} = 5 V

图 7. Power Dissipation vs Output Current



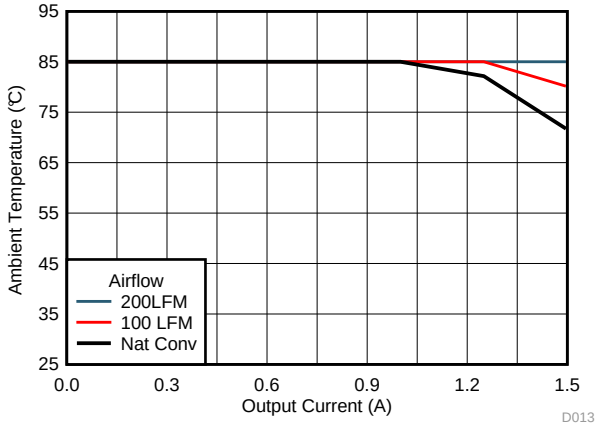
V_{OUT} = 5 V C_{OUT} = 2x 47 µF

图 8. Ripple Voltage vs Output Current



V_{OUT} = 5 V V_{IN} ≤ 15 V

图 9. Safe Operating Area

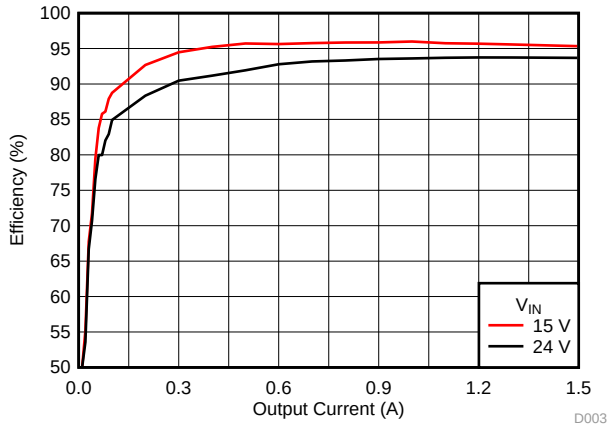


V_{OUT} = 5 V V_{IN} = 24 V

图 10. Safe Operating Area

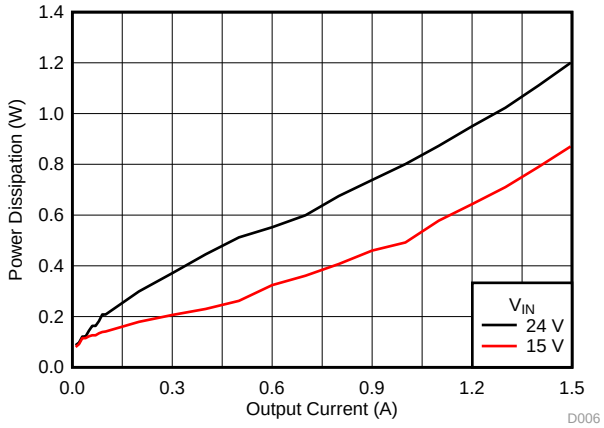
6.9 Typical Characteristics (V_{OUT} = 12 V)

Typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device. Safe operating area curves were measured using a Texas Instruments evaluation module (EVM).



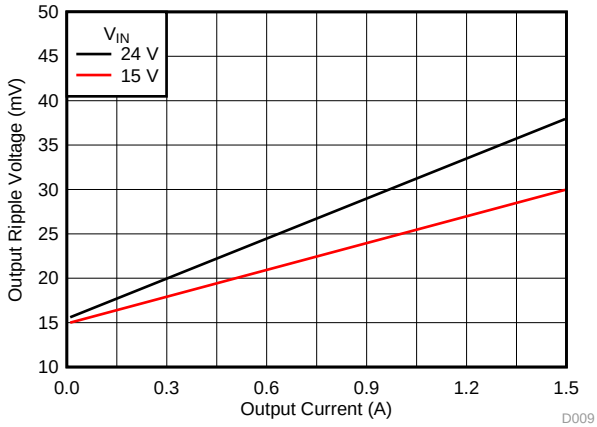
V_{OUT} = 12 V

图 11. Efficiency vs Output Current



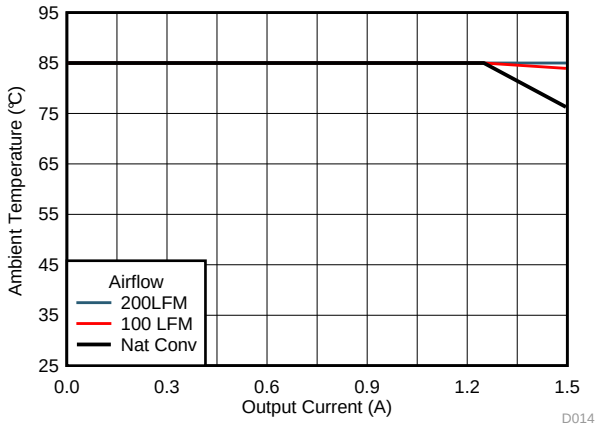
V_{OUT} = 12 V

图 12. Power Dissipation vs Output Current



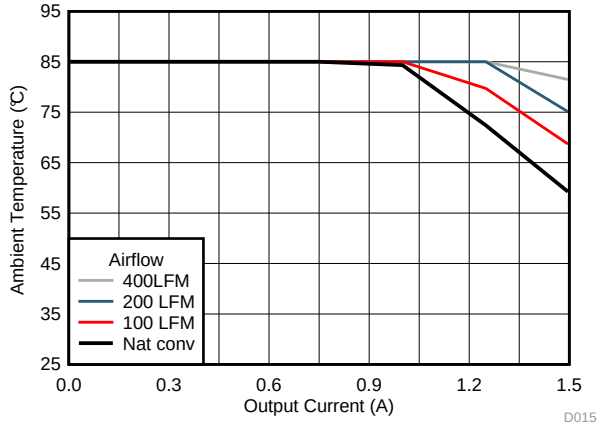
V_{OUT} = 12 V C_{OUT} = 1x 47 µF

图 13. Ripple Voltage vs Output Current



V_{OUT} = 12 V V_{IN} ≤ 15 V

图 14. Safe Operating Area



V_{OUT} = 12 V V_{IN} = 24 V

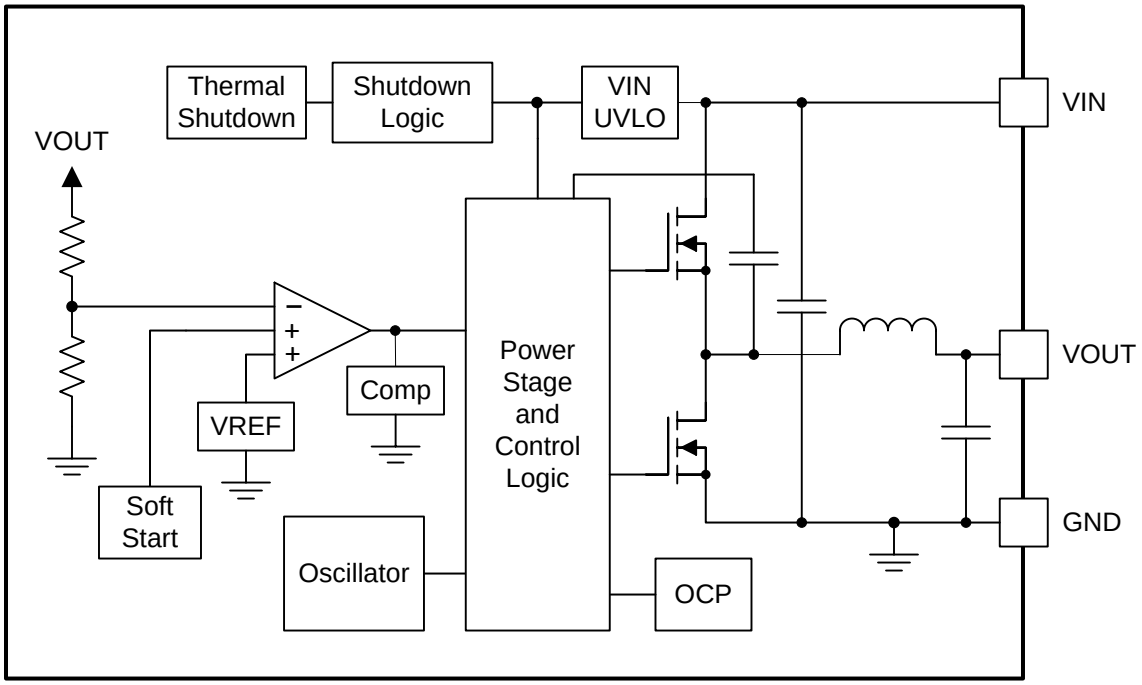
图 15. Safe Operating Area

7 Detailed Description

7.1 Overview

The TPSM84203, TPSM84205, and TPSM84212 devices are 28 V input, 1.5 A, synchronous step down converters with PWM, MOSFETs, inductor, and control circuitry integrated into a TO-220 footprint package. The device integration enables small designs, while improving efficiency over a traditional linear regulator design. The TPSM842xx family provides fixed output voltages of 3.3 V, 5.0 V and 12.0 V. The fixed 400 kHz (typ) switching frequency allows small size and low output voltage ripple. Under light load conditions, these devices are designed to operate in high-efficiency pulse-skipping mode. These devices provide accurate voltage regulation for a variety of loads by using a precision internal voltage reference. These devices have been designed to safely start up into a pre-biased output voltage. Thermal shutdown and current limit features protect the device during an overload condition. The 3-pin, TO-220 footprint package offers improved performance over traditional linear regulators packaged in the standard footprint.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Capacitors

The TPSM842xx devices require a minimum input capacitance of 10 μF of ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. An additional 100 μF of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage.

表 1. Recommended Input Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (2) (μF)	ESR(3) (mΩ)
Murata	X7R	GRM32ER71H475KA88L	50	4.7	2
TDK	X5R	C3225X5R1H106K250AB	50	10	3
Murata	X7R	GRM32ER71H106KA12	50	10	2
TDK	X7R	C3225X7R1H106M250AB	50	10	3
Panasonic	ZA	EEHZA1H101P	50	100	28

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Standard capacitance values
(3) Maximum ESR @ 100kHz, 25°C.

7.3.2 Output Capacitors

The TPSM84203 and TPSM84205 devices require a minimum output capacitance of 94 μF (2x 47 μF) of ceramic type. The TPSM84212 device requires a minimum output capacitance of 47 μF of ceramic type. High-quality X5R or X7R ceramic capacitors with sufficient voltage rating are recommended. Additional output capacitance is recommended for applications with transient load requirements. The voltage rating of output capacitors must be greater than the maximum output voltage.

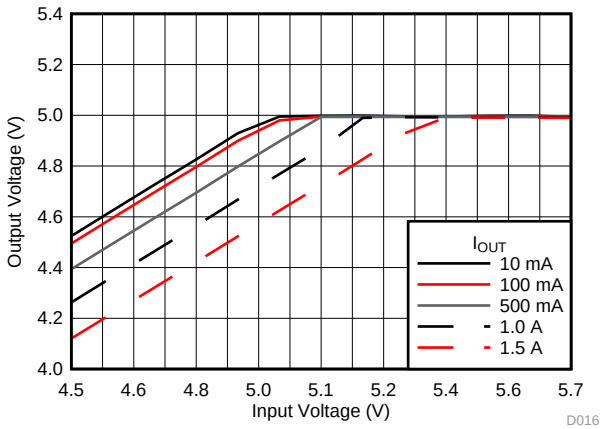
表 2. Recommended Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (2) (μF)	ESR(3) (mΩ)
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER61C476K	16	47	3
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Kemet	X5R	C1210C107M4PAC7800	16	100	2
Panasonic	POSCAP	6TPE100MI	6.3	100	18
Panasonic	POSCAP	6TPF220M9L	6.3	220	9
Panasonic	POSCAP	6TPE220ML	6.3	220	12
Panasonic	POSCAP	6TPF330M9L	6.3	330	9
Panasonic	POSCAP	16TQC47MYFD	16	47	55

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Standard capacitance values.
(3) Maximum ESR @ 100kHz, 25°C.

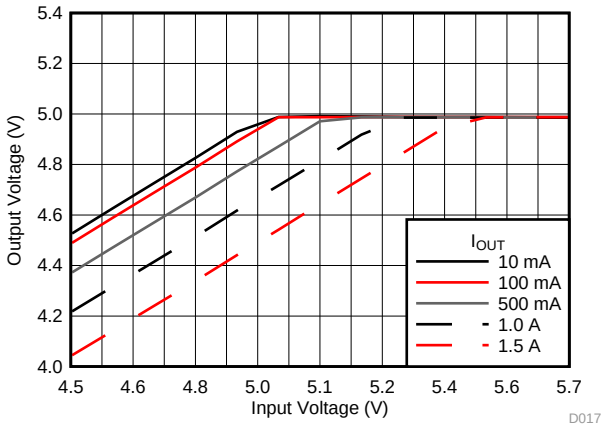
7.3.3 Drop-Out Voltage

The drop-out voltage of a voltage regulator is the difference between the input voltage and the output voltage that is required to maintain regulation. 图 16 and 图 17 show typical drop-out voltage graphs for TPSM84205 at ambient temperatures of 25°C and 85°C. 图 18 and 图 19 show typical drop-out voltage graphs for TPSM84212 at ambient temperatures of 25°C and 85°C.



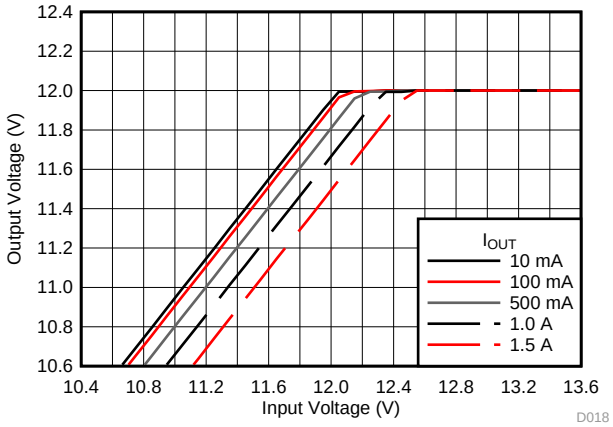
V_{OUT} = 5.0 V T_A = 25°C

图 16. Drop-Out Voltage



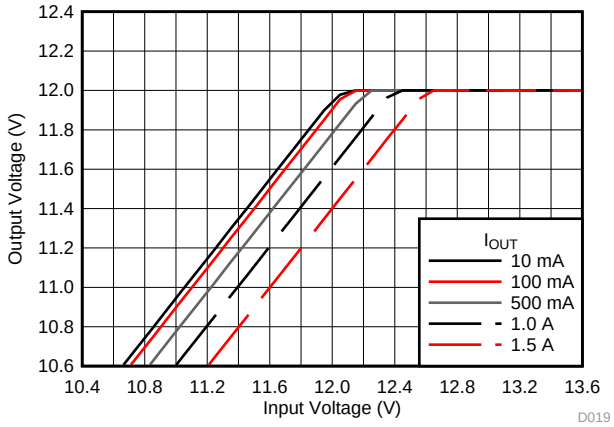
V_{OUT} = 5.0 V T_A = 85°C

图 17. Drop-Out Voltage



V_{OUT} = 12 V T_A = 25°C

图 18. Drop-Out Voltage



V_{OUT} = 12 V T_A = 85°C

图 19. Drop-Out Voltage

7.3.4 Internal Soft-Start

The device starts up under control of the internal soft-start function. The internal soft start time is set to 5 ms typically.

7.3.5 Safe Startup into Pre-Biased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than the internal feedback voltage.

7.3.6 Over-Current Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting. If an output overload condition occurs for more than 1.28 ms, the device shuts down and restarts after approximately 40 ms. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

7.3.7 Output Over-Voltage Protection

An output over voltage protection circuit is incorporated to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. When the output voltage goes above 108% × V_{OUT}, the high-side MOSFET is forced off. When the output voltage falls below 104% × V_{OUT}, the high-side MOSFET is enabled again.

7.3.8 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 165°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 155°C typically.

7.4 Device Functional Modes

7.4.1 Normal Operation

The TPSM842xx devices operate in Normal operation mode when the input voltage is above the minimum input voltage. In Normal operation mode, the device operates in continuous conduction mode (CCM) which occurs when inductor peak current is above 840 mA typically. In CCM, the TPSM842xx devices operate at a fixed frequency of 400 kHz (typ). In addition, to reduce EMI, the devices introduce frequency spread spectrum. The jittering frequency range is ±6% of the switching frequency with a 780 Hz modulation rate.

7.4.2 Eco-mode™ Operation

The TPSM842xx devices operate in Eco-mode operation in light load conditions. Eco-mode is a high-efficiency, pulse-skipping mode under light load conditions. Pulse skipping initiates when the switch current falls to 840 mA typically. During pulse skipping, the low-side FET turns off when the switch current falls to 0 A. The device takes on the characteristics of discontinuous conduction mode (DCM) operation and the apparent switching frequency decreases. As the output current decreases, the perceived time between switching pulses increases.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPSM842xx devices are step down DC-DC power modules. They convert a higher DC voltage to a lower DC voltage of 3.3 V, 5 V, or 12 V with a maximum output current of 1.5 A. The following design procedure can be used to select components for the TPSM842xx devices. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes an iterative design procedure and accesses comprehensive databases of components. Please visit www.ti.com/WEBENCH for more details.

8.2 Typical Application

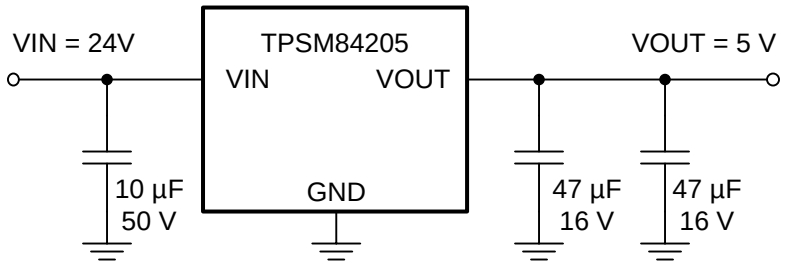


图 20. Typical Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 3 and follow the design procedures below.

表 3. Design Parameters

DESIGN PARAMETER	VALUE
Input Voltage V_{IN}	24-V typical
Output Voltage V_{OUT}	5.0 V
Output Current Rating	1.5 A
Key care-abouts	TO-220 footprint, high efficiency

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM84203 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Input and Output Capacitors

The TPSM842xx devices require both input and output capacitance for proper operation. The minimum required input capacitance for all of the TPSM842xx devices is 10 µF of ceramic capacitance placed directly at the device pins. The minimum required output capacitance for the TPSM84203 and TPSM84205 is 2× 47 µF of ceramic type. The TPSM84212 requires only one 47 µF ceramic output capacitor. Additional capacitance can be added to improve ripple or transient response.

For this application, the minimum required input capacitance of 10 µF, ceramic was added and 2× 47 µF ceramic capacitance was added to the output.

8.2.3 Application Curves

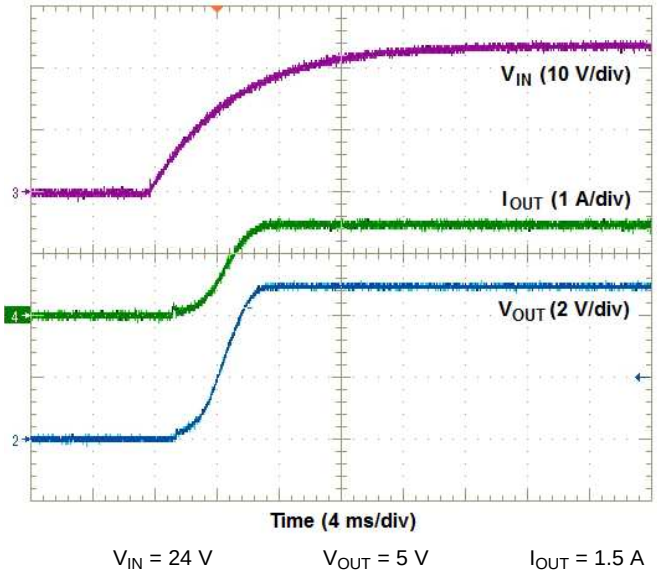


图 21. Start-up Waveforms

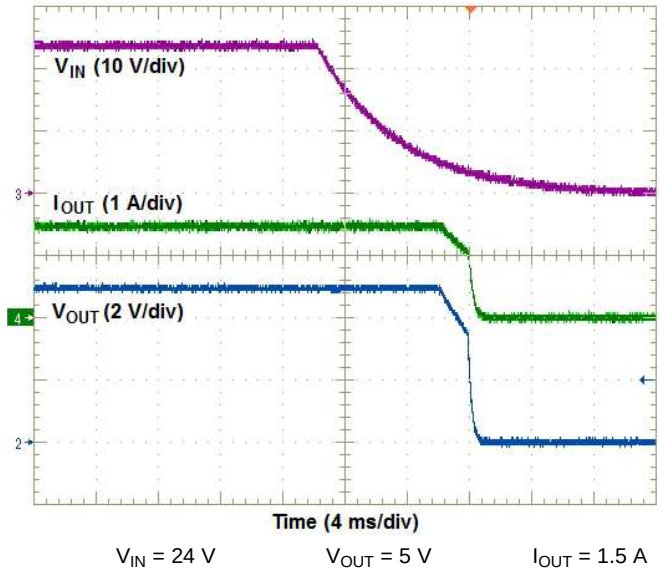


图 22. Shut-down Waveforms

8.2.3.1 EMI

The TPSM842xx devices are all compliant with EN55022 Class B radiated emissions. 图 23 to 图 27 show typical examples of radiated emissions plots for the TPSM842xx devices. The EMI plots were taken using a web-orderable EVM with a resistive load. Input power was provided using a lead acid battery. All graphs show plots of the antenna in the horizontal and vertical positions.

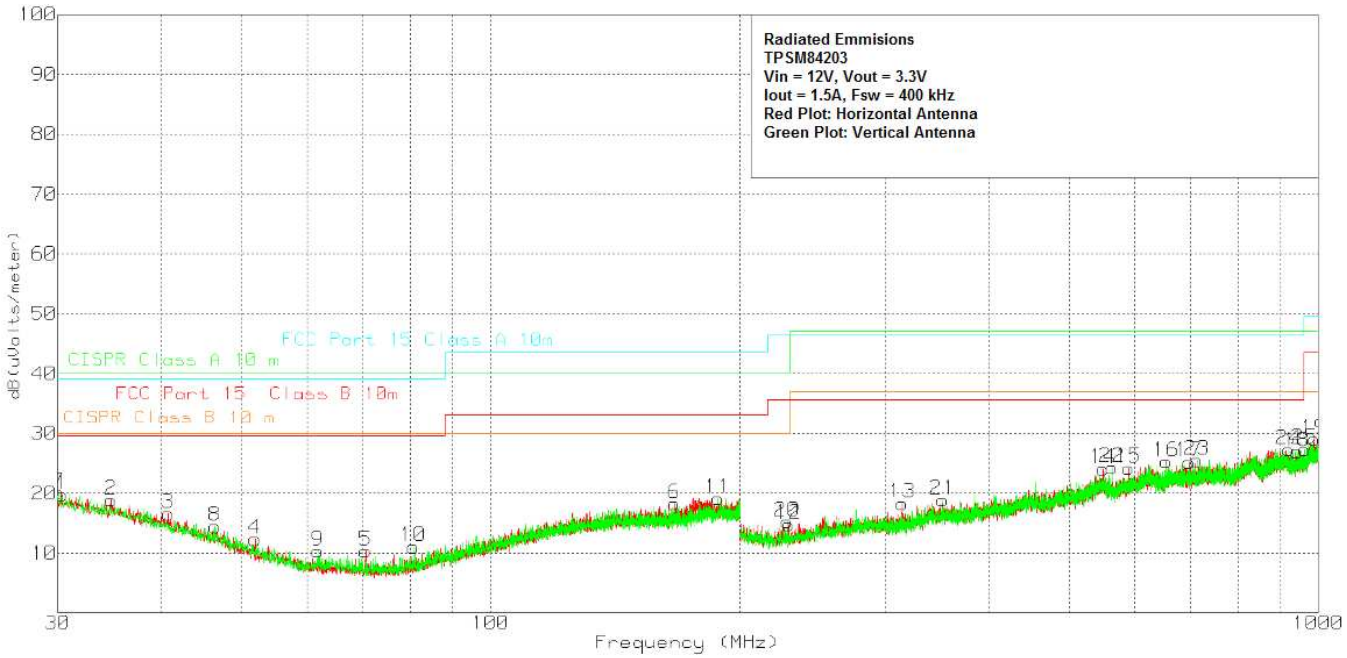


图 23. Radiated Emissions 12-V Input, 3.3-V Output, 1.5-A Load, Horizontal and Vertical Antenna

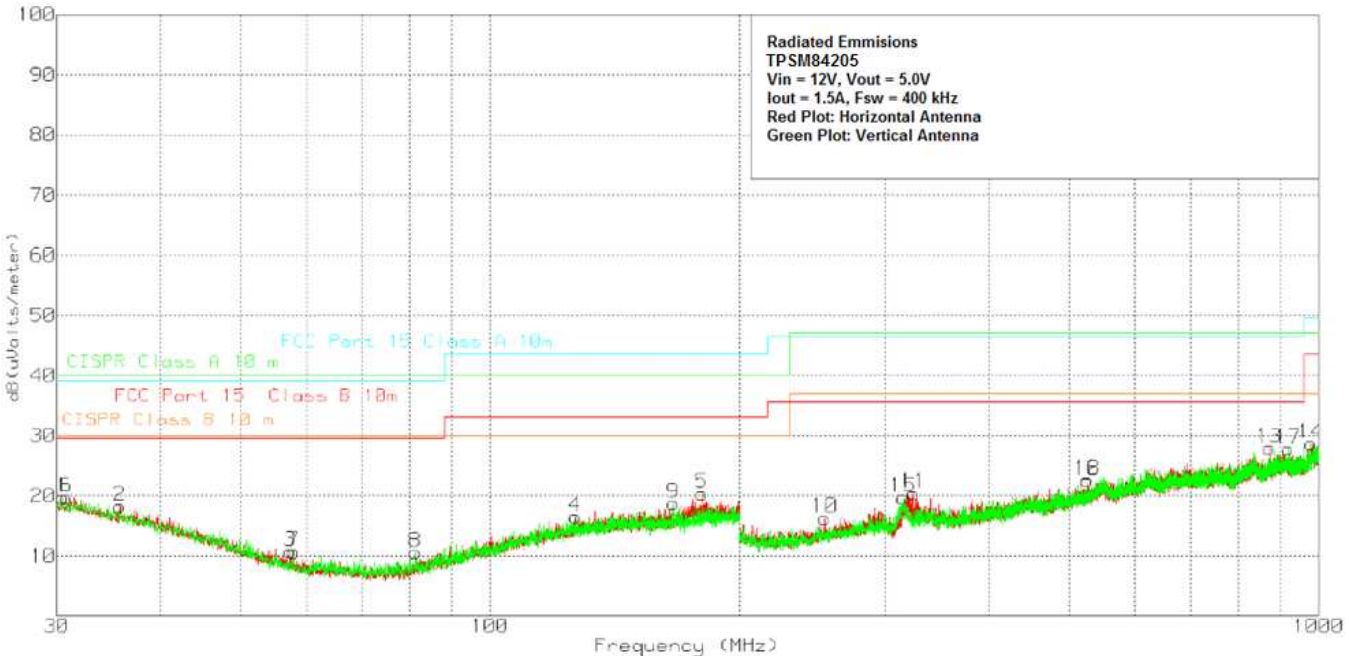


图 24. Radiated Emissions 12-V Input, 5.0-V Output, 1.5-A Load, Horizontal and Vertical Antenna

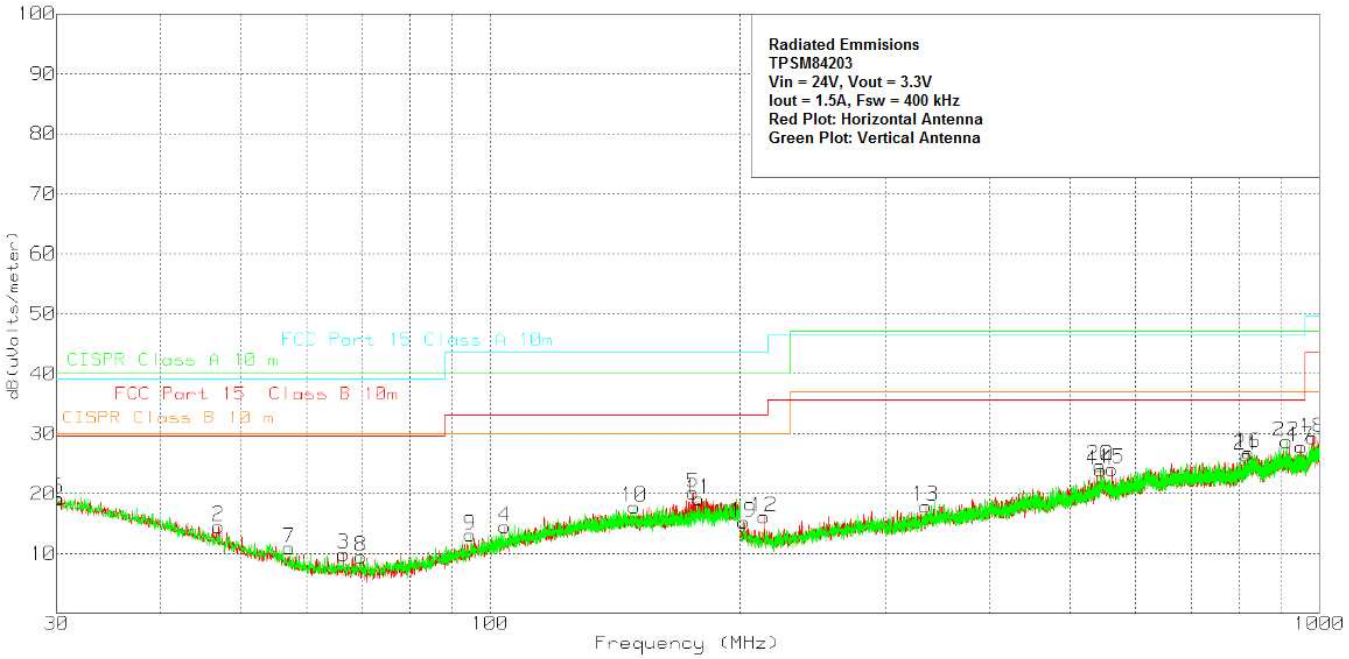


图 25. Radiated Emissions 24-V Input, 3.3-V Output, 1.5-A Load, Horizontal and Vertical Antenna

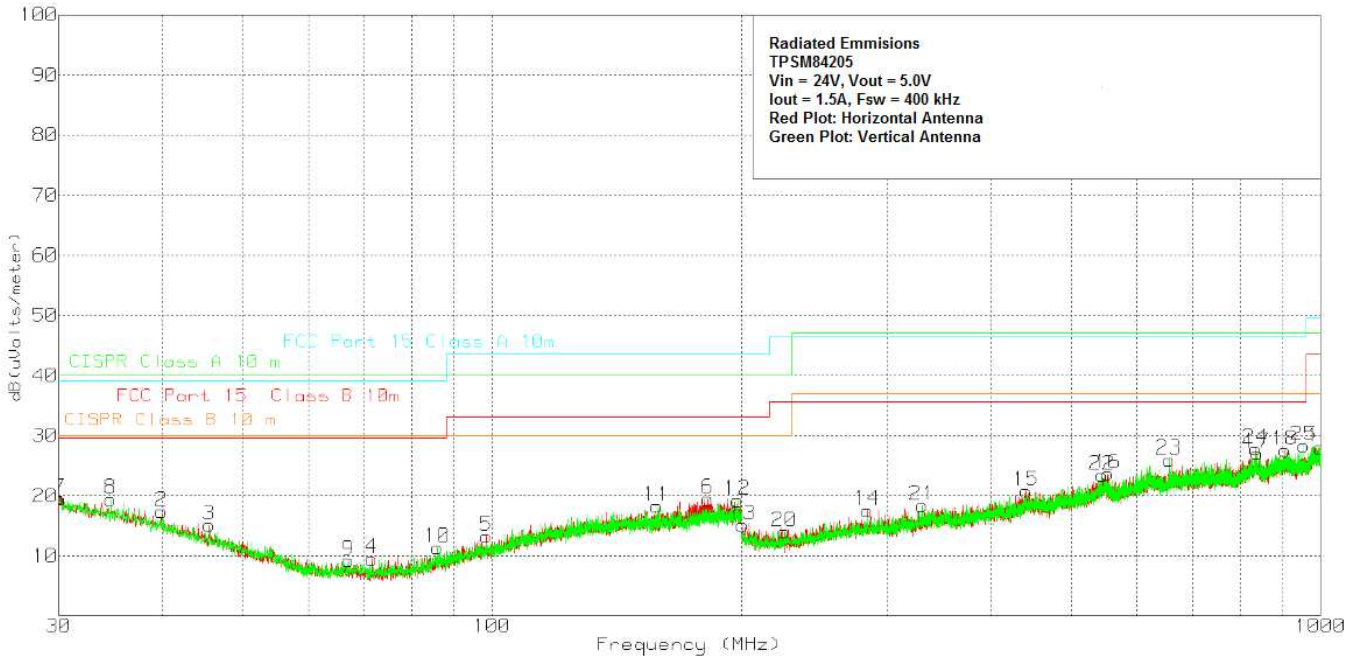


图 26. Radiated Emissions 12-V Input, 5.0-V Output, 1.5-A Load, Horizontal and Vertical Antenna

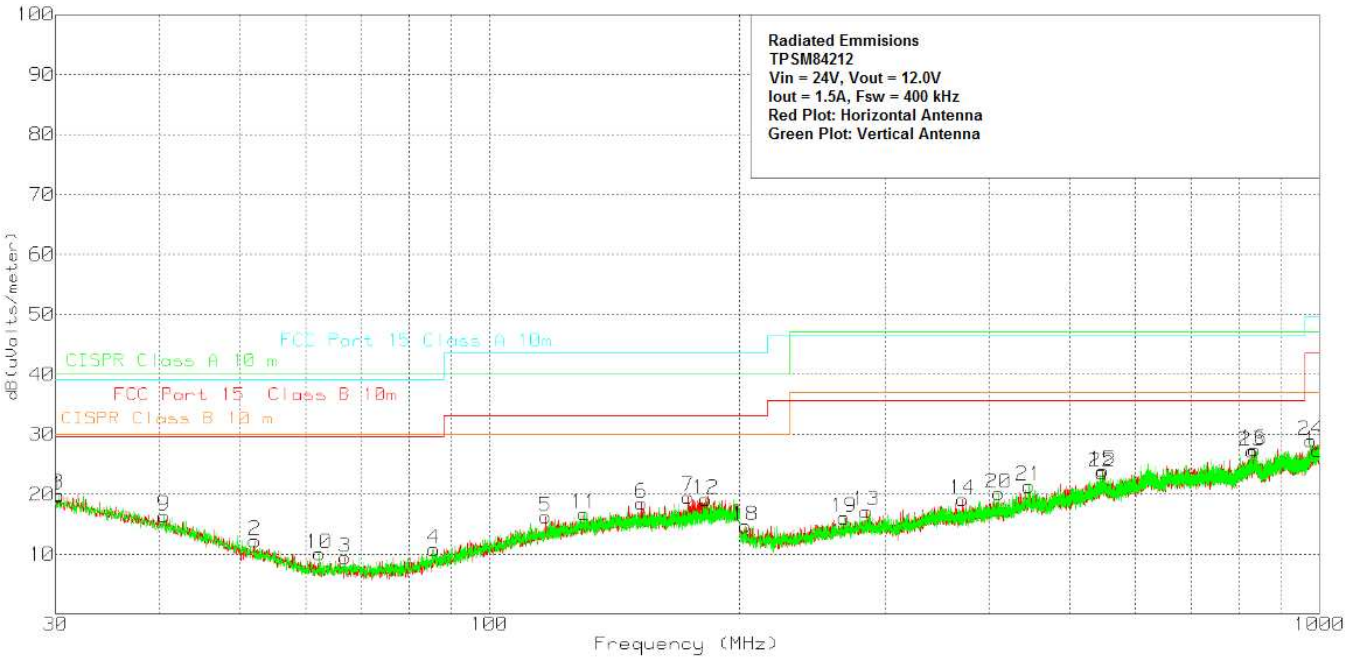


图 27. Radiated Emissions 24-V Input, 12-V Output, 1.5-A Load, Horizontal and Vertical Antenna

9 Power Supply Recommendations

The TPSM842xx devices are designed to operate from an input voltage supply between 4.5 V and 28 V. This supply must be well regulated. Proper bypassing of input supply is critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the Layout section.

10 Layout

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 图 28 shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and GND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

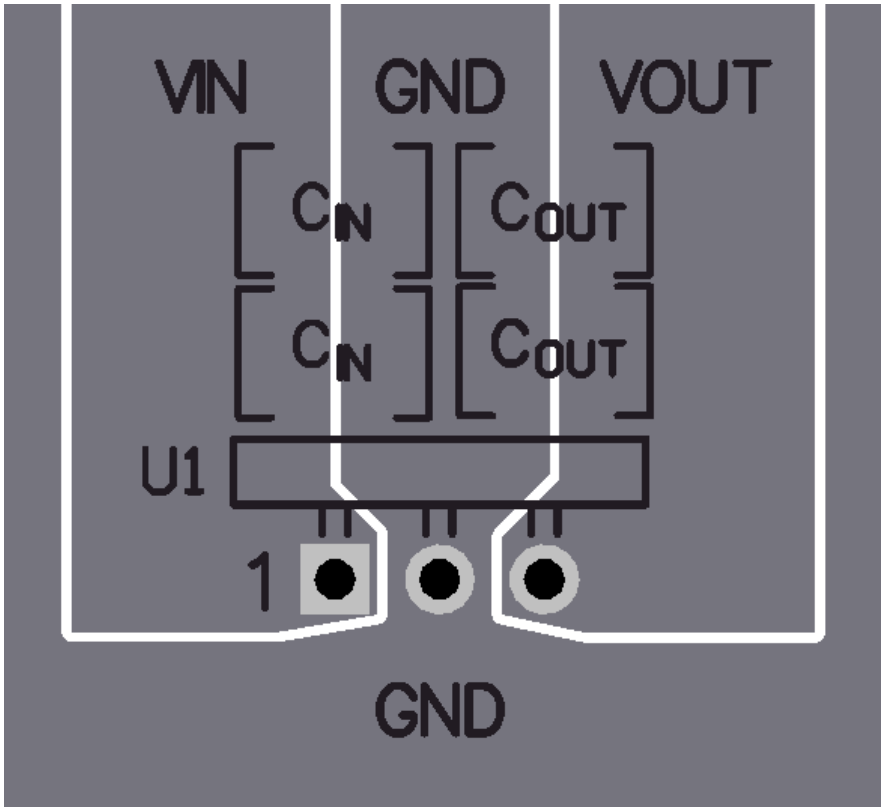


图 28.

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 使用 WEBENCH® 工具创建定制设计

请单击此处，借助 WEBENCH® Power Designer 并使用 TPSM84203 器件创建定制设计方案。

1. 首先键入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键参数设计，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

11.2 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **4.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
TPSM84203	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPSM84205	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPSM84212	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. 有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 Community Resources

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.5 商标

Eco-mode, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM84203EAB	ACTIVE	SIP MODULE	EAB	3	80	RoHS Exempt & Green	SN	N / A for Pkg Type	-40 to 125		Samples
TPSM84205EAB	ACTIVE	SIP MODULE	EAB	3	80	RoHS Exempt & Green	SN	N / A for Pkg Type	-40 to 125		Samples
TPSM84212EAB	ACTIVE	SIP MODULE	EAB	3	80	RoHS Exempt & Green	SN	N / A for Pkg Type	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

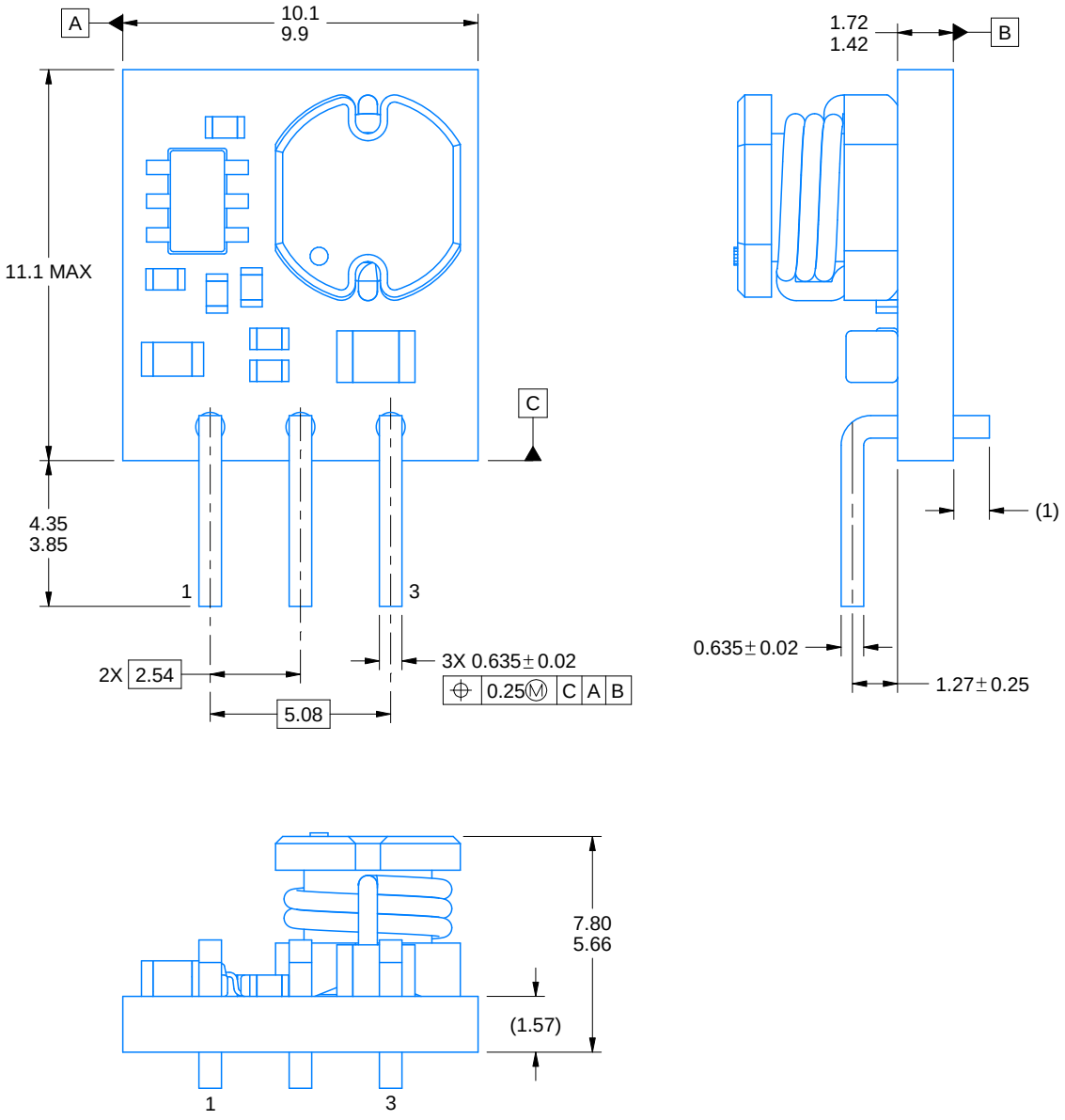
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

EAB0003A

SIPMODULE - 11.1 mm max height

SYSTEM IN PACKAGE MODULE



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NOTES:

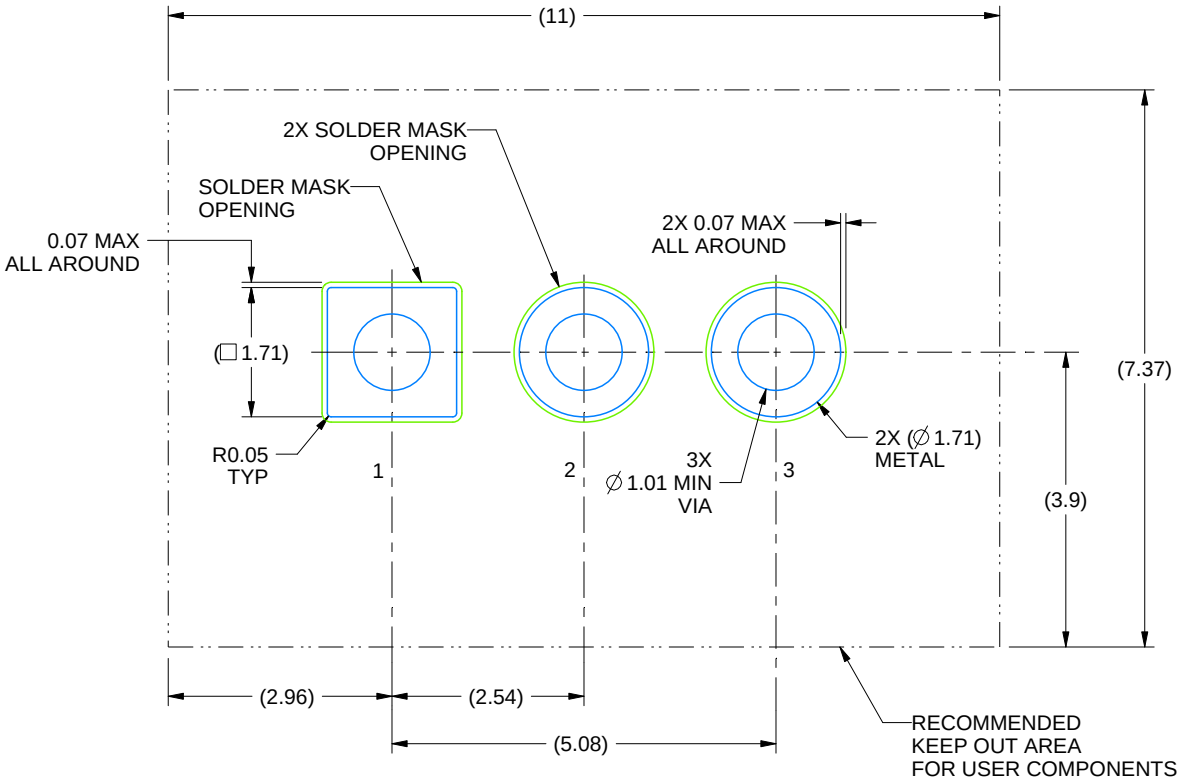
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Location, size and quantity of each component are for reference only and may vary.

EXAMPLE BOARD LAYOUT

EAB0003A

SIPMODULE - 11.1 mm max height

SYSTEM IN PACKAGE MODULE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:10X

4223521/D 04/2024

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2163130	02/07/2017	V. PAKU / T. LEQUANG
B	SIDE VIEW: ADD PIN CENTER TO PCB DIMENSION; REMOVE PIN EDGE TO PCB DIMENSION	2167747	08/14/2017	V. PAKU / K. SINCERBOX
C	4.35/3.85 WAS 4.1/3.5	2169958	11/20/2017	C. FERNANDEZ / K. SINCERBOX
D	1.27± 0.25 WAS 1.27± 0.025;	2208237	04/18/2024	A. VAZQUEZ / K. SINCERBOX

重要声明和免责声明

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