# CSD17571Q2 30V N 沟道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

## 1 特性

- 低 $Q_g$ 和 $Q_{gd}$
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 环保标准
- 无卤素
- 小外形尺寸无引线 (SON) 2mm × 2mm 塑料封装

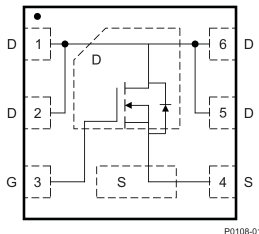
## 2 应用范围

- 针对负载开关应用进行了优化
- 存储、平板电脑和手持设备
- 针对控制场效应晶体管 (FET) 应用进行了优化

## 3 说明

这款 30V、20mΩ、SON 2mm × 2mm NexFET™ 功率 MOSFET 旨在以最大程度降低功率转换和负载管理应用中的损耗，同时提供出色的封装散热性能。

顶视图




产品概要

| $T_A$ = 25°C | | 典型值 | | 单位 |
|---|---|---|---|---|
| $V_{DS}$ | 漏源电压 | 30 | | V |
| $Q_g$ | 栅极电荷总量 (4.5V) | 2.4 | | nC |
| $Q_{gd}$ | 栅极电荷（栅极到漏极） | 0.6 | | nC |
| $R_{DS(on)}$ | 漏源导通电阻 | $V_{GS}$ = 4.5V | 24 | mΩ |
| | | $V_{GS}$ = 10V | 20 | mΩ |
| $V_{GS(th)}$ | 阈值电压 | 1.6 | | V |

订购信息(1)

| 器件 | 介质 | 数量 | 封装 | 出货 |
|---|---|---|---|---|
| CSD17571Q2 | 7 英寸卷带 | 3000 | SON 2mm x 2mm 塑料封装 | 卷带封装 |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

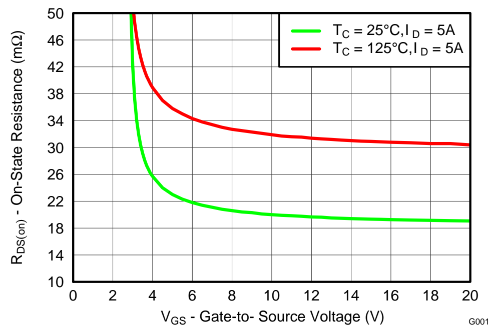
绝对最大额定值

| $T_A$ = 25°C | | 值 | 单位 |
|---|---|---|---|
| $V_{DS}$ | 漏源电压 | 30 | V |
| $V_{GS}$ | 栅源电压 | ±20 | V |
| $I_D$ | 持续漏极电流（受封装限制） | 22 | A |
| | 持续漏极电流(1) | 7.6 | A |
| $I_{DM}$ | 脉冲漏极电流，$T_A$ = 25°C 时测得(2) | 39 | A |
| $P_D$ | 功率耗散(1) | 2.5 | W |
| $T_J$，$T_{stg}$ | 运行结温和储存温度范围 | -55 至 150 | °C |
| $E_{AS}$ | 雪崩能量，单一脉冲 $I_D$ = 12A，L = 0.1mH，$R_G$ = 25Ω | 7.2 | mJ |

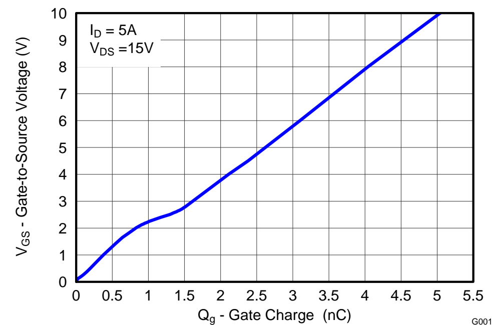
(1) $R_{\theta JA}$ = 50，这是在厚度为 0.060" 的环氧树脂 (FR4) 印刷电路板 (PCB) 上 1 in²（2 盎司）铜焊盘上测得的典型值

(2) 脉冲持续时间 10μs，占空比 ≤ 2%

$R_{DS(on)}$ 与 $V_{GS}$ 间的关系




栅极电荷



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 修订历史记录

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| • Updated Figure #8 | 6 |


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# 5 Specifications

## 5.1 Electrical Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-Source Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 30 | | | V |
| $I_{DSS}$ | Drain-to-Source Leakage Current | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | | | 1 | μA |
| $I_{GSS}$ | Gate-to-Source Leakage Current | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate-to-Source Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 250 μA | 1.3 | 1.6 | 2 | V |
| $R_{DS(on)}$ | Drain-to-Source On-Resistance | $V_{GS}$ = 4.5 V, $I_{DS}$ = 5 A | | 24 | 29 | mΩ |
| | | $V_{GS}$ = 10 V, $I_{DS}$ = 5 A | | 20 | 24 | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 15 V, $I_{DS}$ = 5 A | | 43 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{ISS}$ | Input Capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 15 V, $f$ = 1 MHz | | 360 | 468 | pF |
| $C_{OSS}$ | Output Capacitance | | | 101 | 131 | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 9 | 12 | pF |
| $R_g$ | Series Gate Resistance | | | 3.8 | 7.6 | Ω |
| $Q_g$ | Gate Charge Total (4.5 V) | $V_{DS}$ = 15 V, $I_{DS}$ = 5 A | | 2.4 | 3.1 | nC |
| $Q_{gd}$ | Gate Charge – Gate-to-Drain | | | 0.6 | | nC |
| $Q_{gs}$ | Gate Charge Gate-to-Source | | | 0.9 | | nC |
| $Q_{g(th)}$ | Gate Charge at $V_{th}$ | | | 0.6 | | nC |
| $Q_{OSS}$ | Output Charge | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V | | 3.4 | | nC |
| $t_{d(on)}$ | Turn On Delay Time | $V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_{DS}$ = 5 A<br>$R_G$ = 2 Ω | | 5.3 | | ns |
| $t_r$ | Rise Time | | | 19 | | ns |
| $t_{d(off)}$ | Turn Off Delay Time | | | 8 | | ns |
| $t_f$ | Fall Time | | | 2.6 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode Forward Voltage | $I_{DS}$ = 5 A, $V_{GS}$ = 0 V | | 0.8 | 1 | V |
| $Q_{rr}$ | Reverse Recovery Charge | $V_{DD}$ = 15 V, $I_F$ = 5 A, di/dt = 300 A/μs | | 2.3 | | nC |
| $t_{rr}$ | Reverse Recovery Time | | | 11 | | ns |

## 5.2 Thermal Information

$T_A$ = 25°C unless otherwise specified

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{θJC}$ | Junction-to-Case Thermal Resistance (1) | | | 6.2 | °C/W |
| $R_{θJA}$ | Junction-to-Ambient Thermal Resistance (1) (2) | | | 65 | |

(1) $R_{θJC}$ is determined with the device mounted on a 1 inch$^2$ (6.45 cm$^2$), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1 inch$^2$ (6.45 cm$^2$), 2 oz. (0.071 mm thick) Cu.

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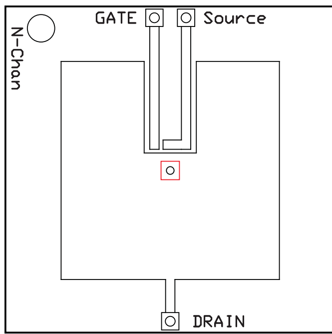
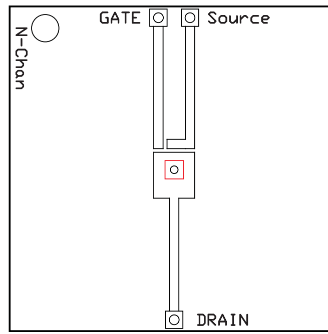



Max $R_{\theta JA}$ = 65 when mounted on 1 inch$^2$ (6.45 cm$^2$) of 2 oz. (0.071 mm thick) Cu.




Max $R_{\theta JA}$ = 235 when mounted on minimum pad area of 2 oz. (0.071 mm thick) Cu.

## 5.3 Typical MOSFET Characteristics

$T_A$ = 25°C unless otherwise specified

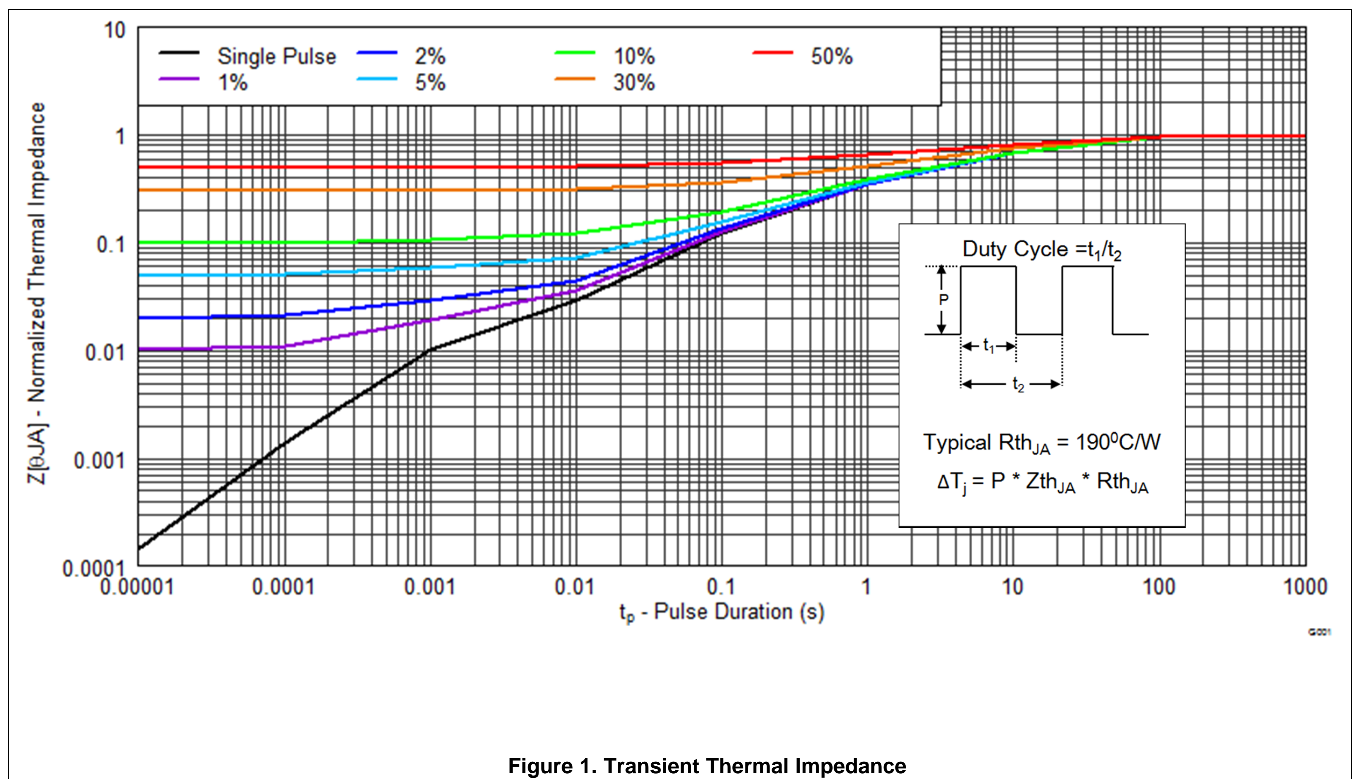



**Figure 1. Transient Thermal Impedance**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## Typical MOSFET Characteristics (continued)

$T_A$ = 25°C unless otherwise specified

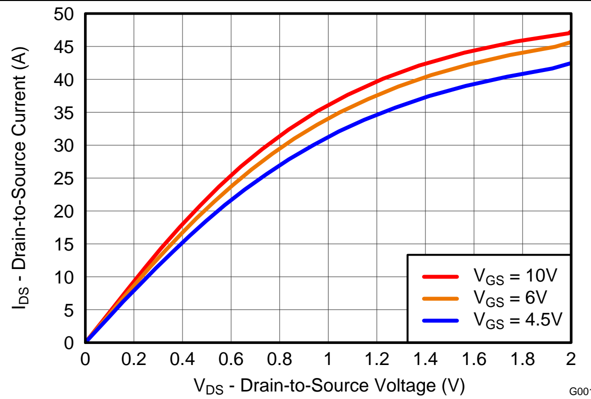


**Figure 2. Saturation Characteristics**

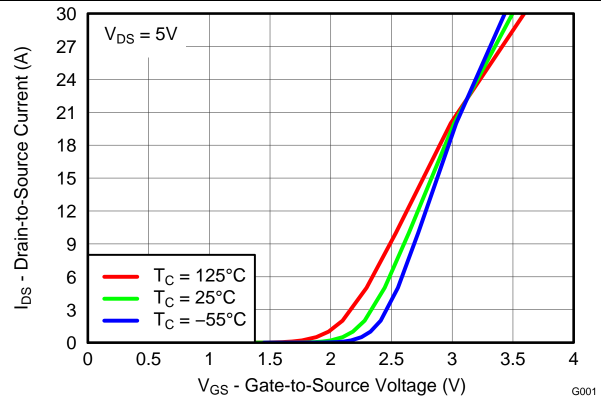


**Figure 3. Transfer Characteristics**

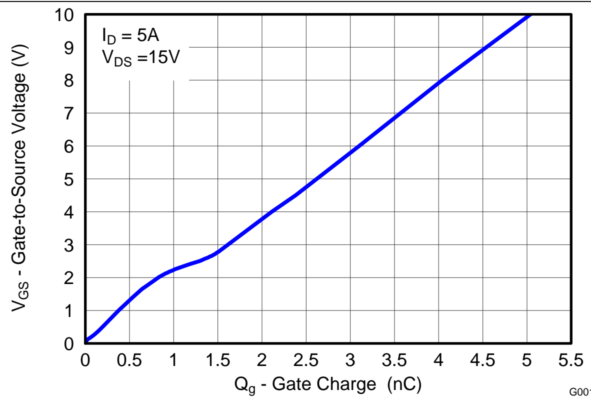


**Figure 4. Gate Charge**

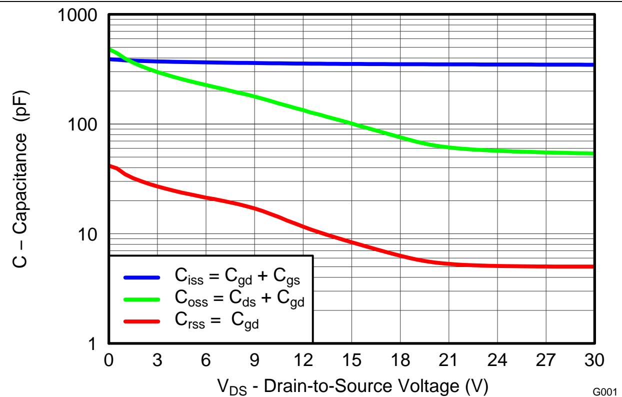


**Figure 5. Capacitance**

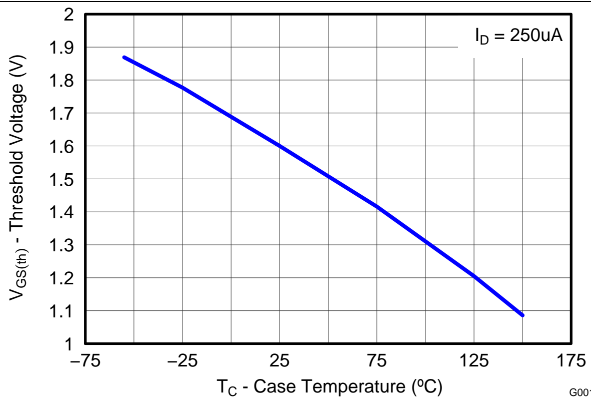


**Figure 6. Threshold Voltage vs Temperature**

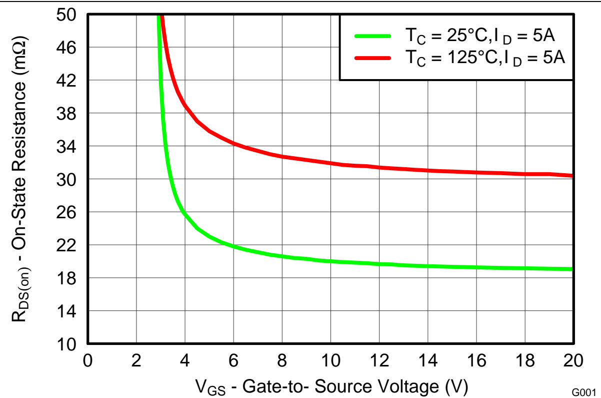


**Figure 7. On-State Resistance vs Gate-to-Source Voltage**

## Typical MOSFET Characteristics (continued)

$T_A$ = 25°C unless otherwise specified

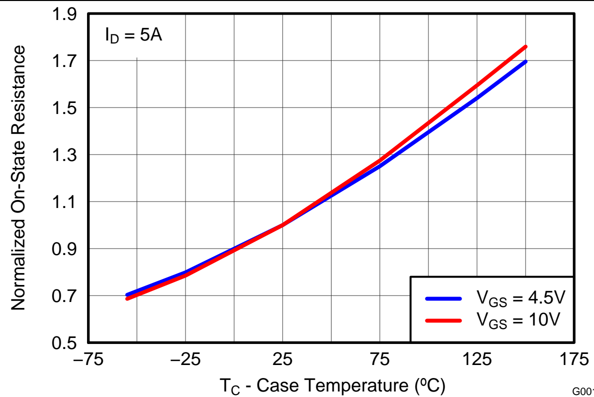


Figure 8. Normalized On-State Resistance vs Temperature

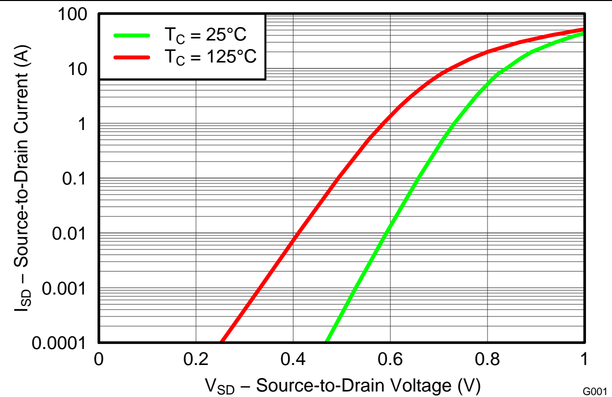


Figure 9. Typical Diode Forward Voltage

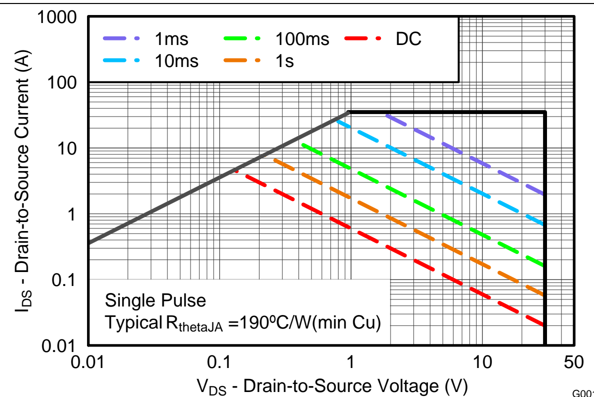


Figure 10. Maximum Safe Operating Area

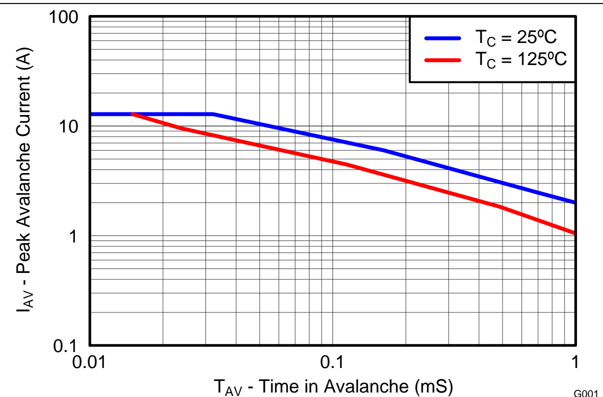


Figure 11. Single Pulse Unclamped Inductive Switching

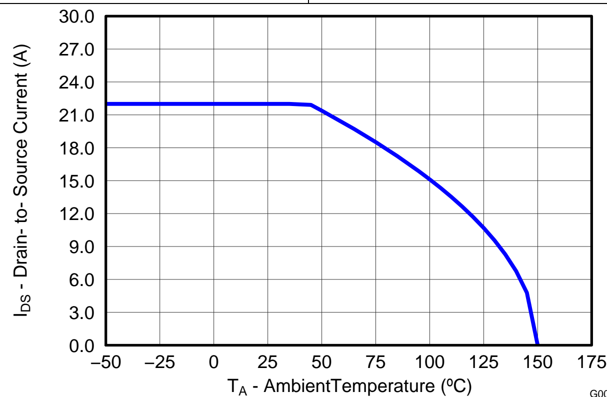


Figure 12. Maximum Drain Current vs Temperature


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# 6 器件和文档支持

## 6.1 商标

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 6.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 6.3 术语表

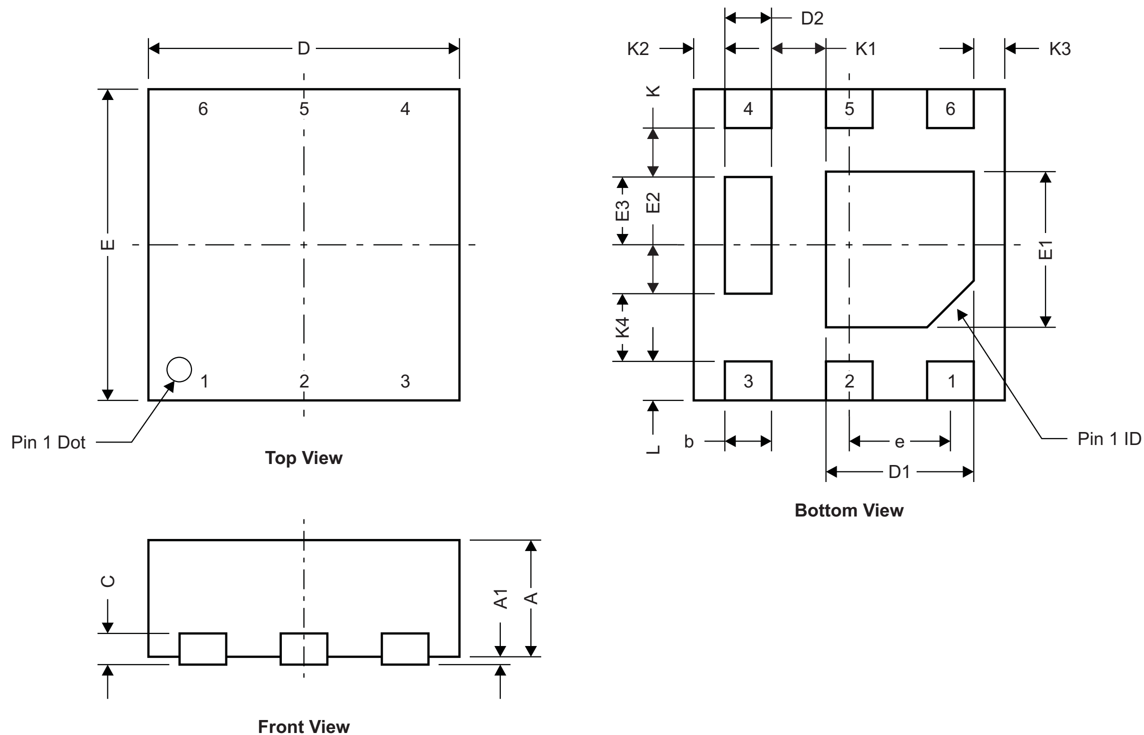
SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

# 7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## 7.1 Q2 封装尺寸




| DIM | 毫米 | | | 英寸 | | |
|---|---|---|---|---|---|---|
| | 最小值 | 标称值 | 最大值 | 最小值 | 标称值 | 最大值 |
| A | 0.700 | 0.750 | 0.800 | 0.028 | 0.030 | 0.032 |
| A1 | 0.000 | | 0.050 | 0.000 | | 0.002 |
| b | 0.250 | 0.300 | 0.350 | 0.010 | 0.012 | 0.014 |
| C | | 0.203 典型值 | | | 0.008 典型值 | |
| D | | 2.000 典型值 | | | 0.080 典型值 | |
| D1 | 0.900 | 0.950 | 1.000 | 0.036 | 0.038 | 0.040 |
| D2 | | 0.300 典型值 | | | 0.012 典型值 | |
| E | | 2.000 典型值 | | | 0.080 典型值 | |
| E1 | 0.900 | 1.000 | 1.100 | 0.036 | 0.040 | 0.044 |
| E2 | | 0.280 典型值 | | | 0.0112 典型值 | |
| E3 | | 0.470 典型值 | | | 0.0188 典型值 | |
| e | | 0.650 BSC | | | 0.026 典型值 | |
| K | | 0.280 典型值 | | | 0.0112 典型值 | |
| K1 | | 0.350 典型值 | | | 0.014 典型值 | |
| K2 | | 0.200 典型值 | | | 0.008 典型值 | |
| K3 | | 0.200 典型值 | | | 0.008 典型值 | |
| K4 | | 0.470 典型值 | | | 0.0188 典型值 | |
| L | 0.200 | 0.25 | 0.300 | 0.008 | 0.010 | 0.012 |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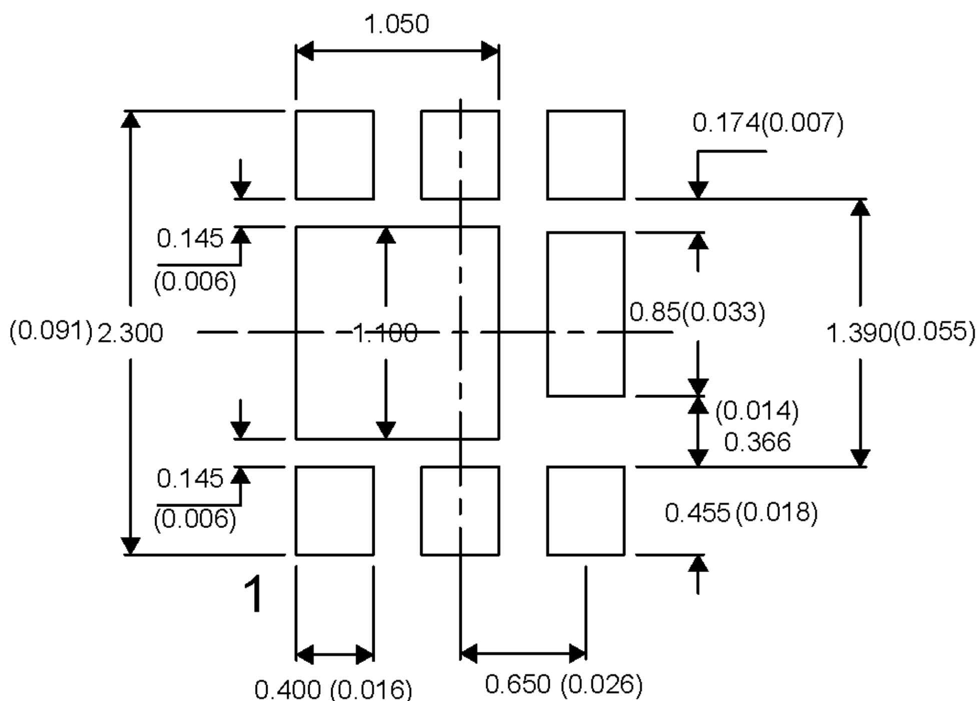
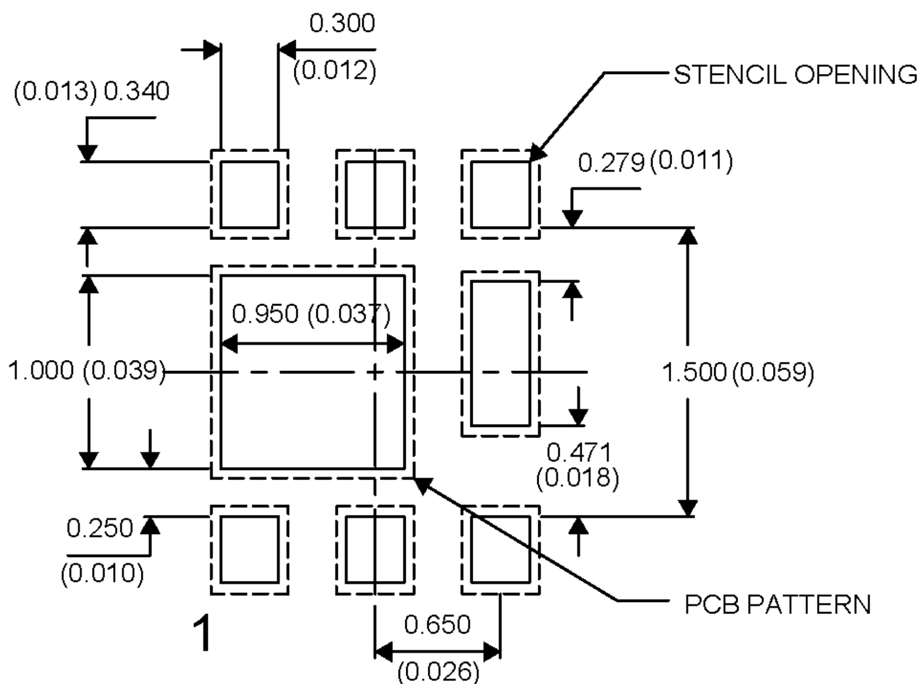
### 7.1.1 建议 PCB 布局




要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

### 7.1.2 建议模板布局




Note: 全部尺寸单位为 mm，除非另外注明。

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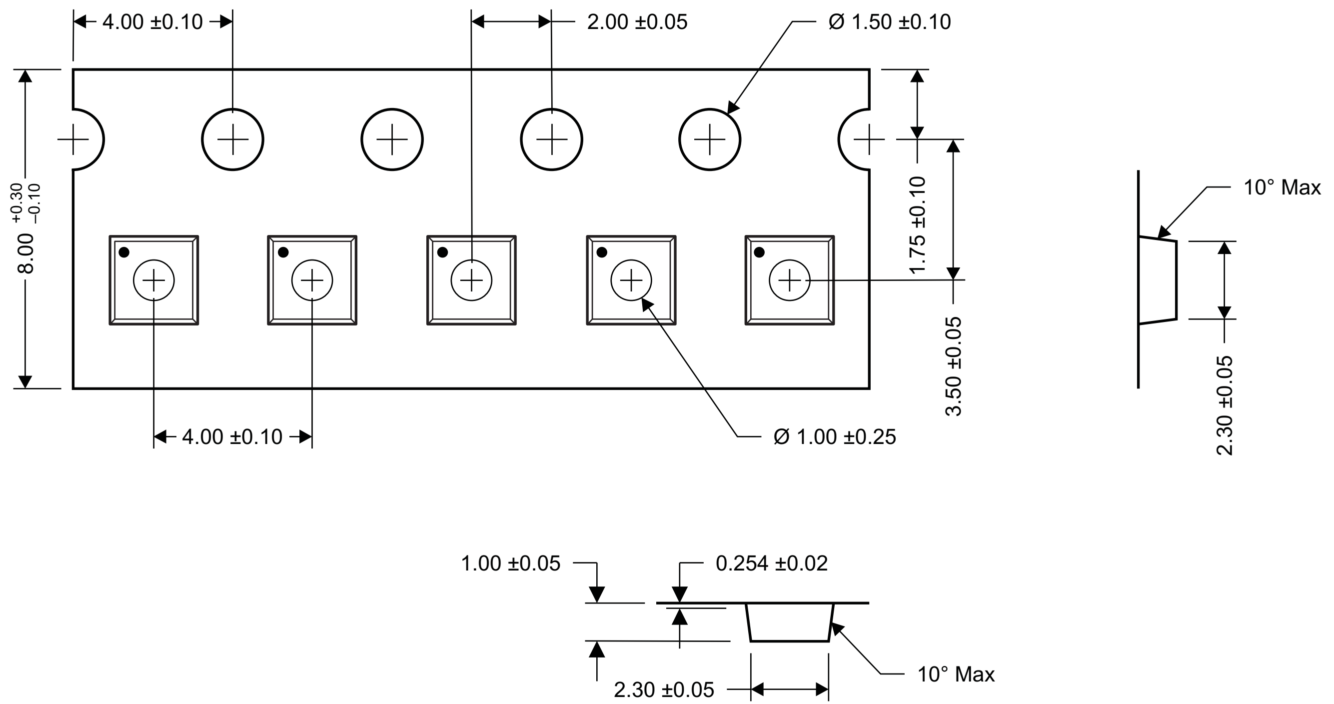
### 7.2 Q2 卷带信息




Notes:
1. 测自链齿孔中心线到孔眼中心线
2. 10 个链齿孔的累积容差为 ±0.20
3. 其他材料可用
4. 卷带的 SR 典型值最大为 $10^9$ OHM/SQ
5. 全部尺寸单位为 mm，除非另外注明。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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD17571Q2 | ACTIVE | WSON | DQK | 6 | 3000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -55 to 150 | 1751 | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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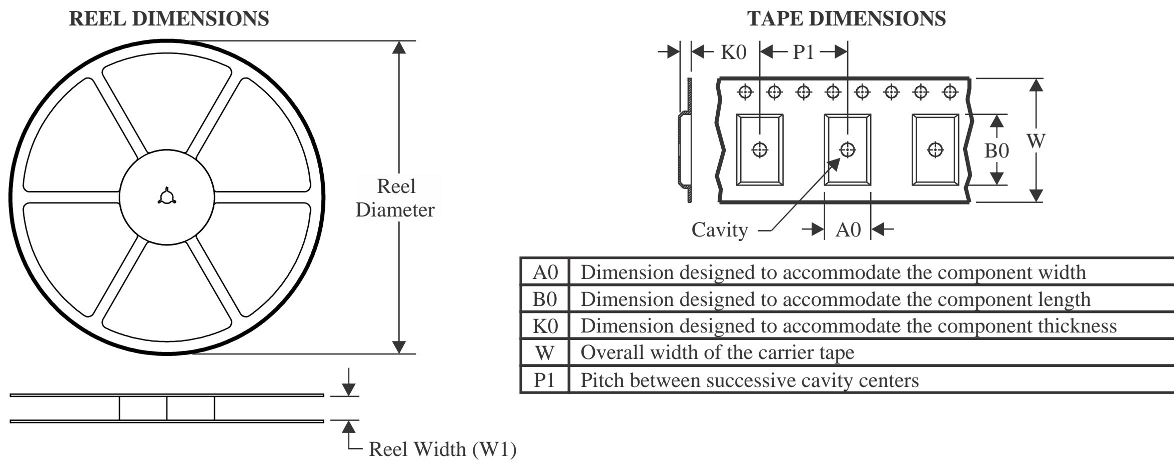
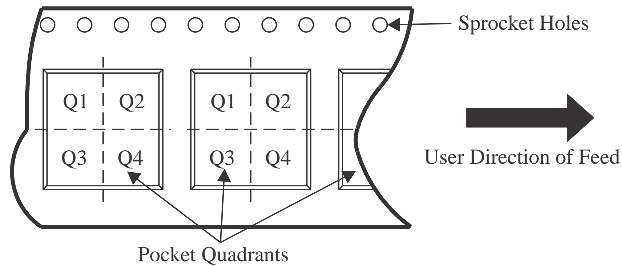
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



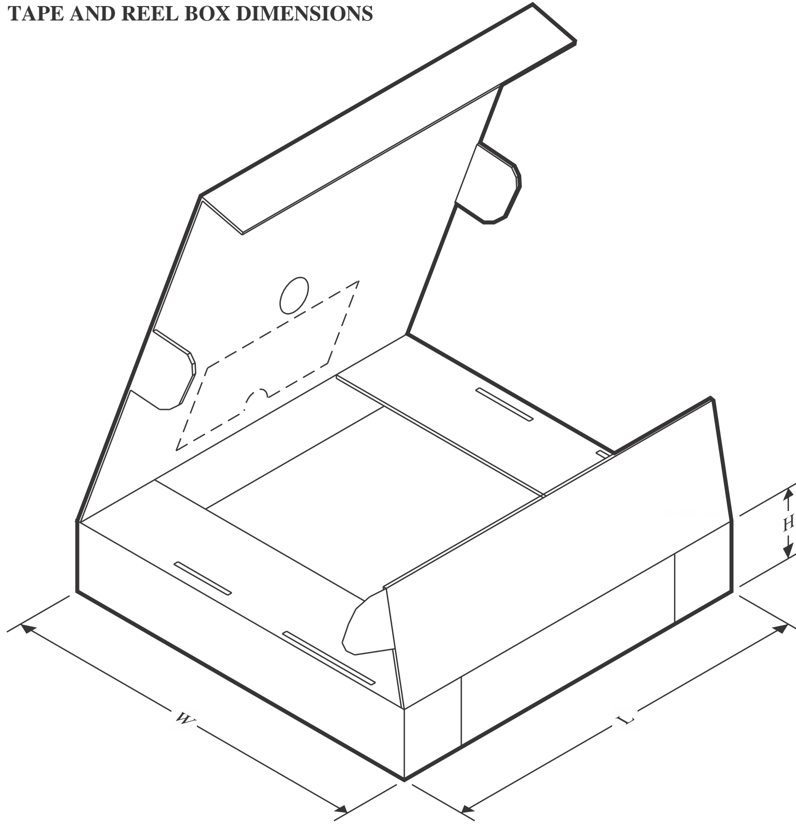

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD17571Q2 | WSON | DQK | 6 | 3000 | 180.0 | 9.5 | 2.3 | 2.3 | 1.0 | 4.0 | 8.0 | Q1 |




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CSD17571Q2 | WSON | DQK | 6 | 3000 | 189.0 | 185.0 | 36.0 |

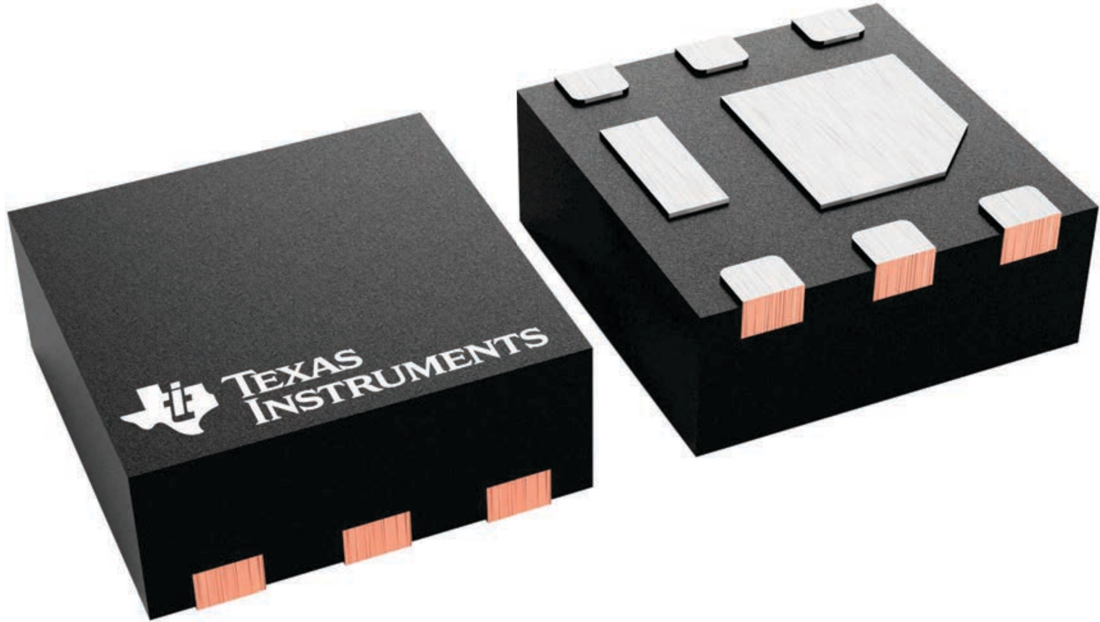
# DQK 6

**WSON - 0.8 mm max height**

**2 x 2, 0.65 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4229807/A

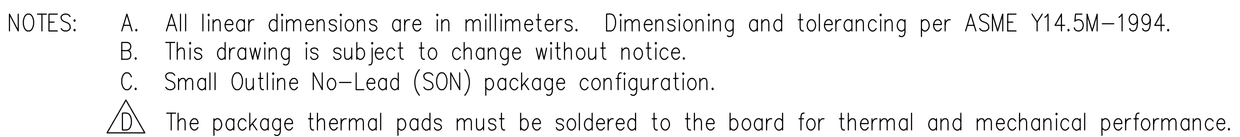
DQK (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

2,10 / 1,90 — A — B — 2,10 / 1,90 — PIN 1 INDEX AREA

0,80 / 0,70 — 0,20 REF. — 0,08 — SEATING PLANE — 0,05 / 0,00

6X 0,30 / 0,20 — 1 — 3 — 6X 0,35 / 0,25 — 0,10 Ⓜ C A B — 6 — 4 — 0,65 — EXPOSED THERMAL PADS D

4210192/B 01/10



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

C. Small Outline No–Lead (SON) package configuration.

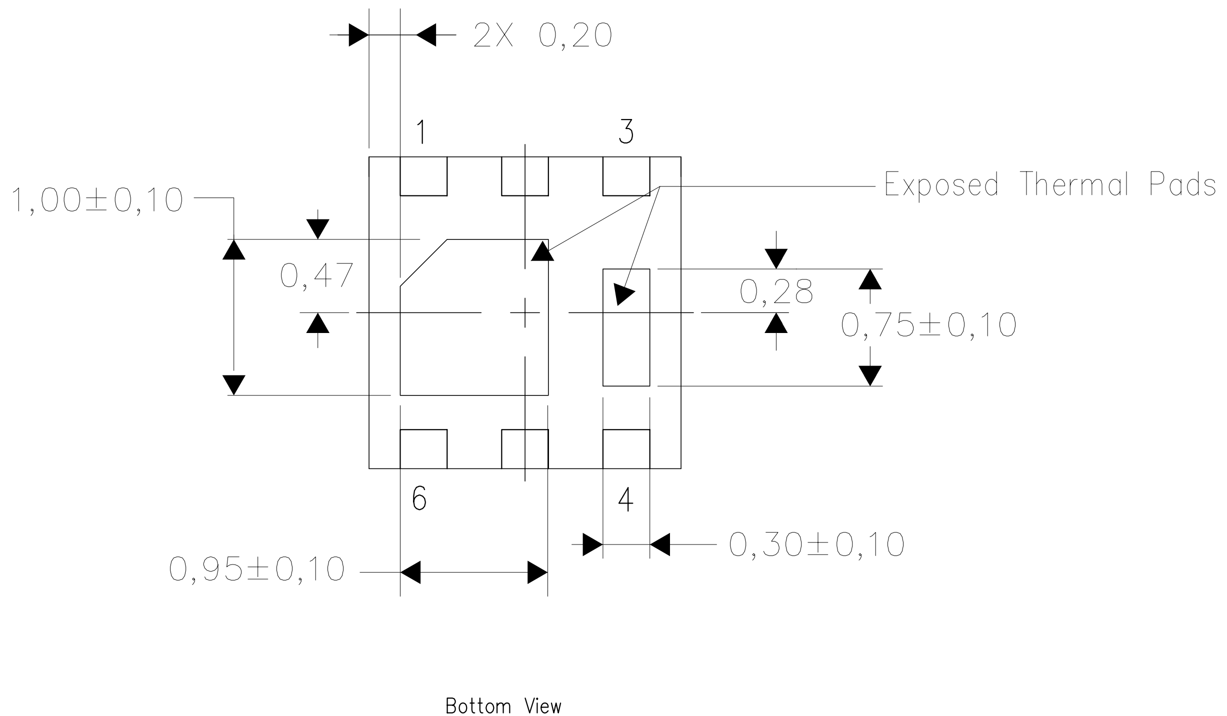
D. The package thermal pads must be soldered to the board for thermal and mechanical performance.

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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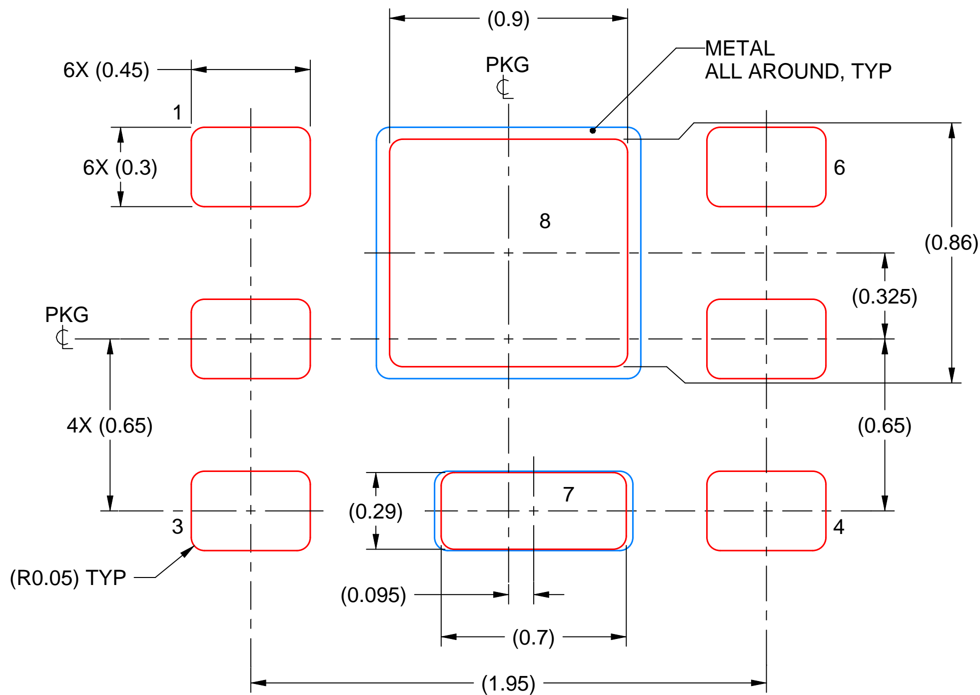
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
PAD 7: 90%, PAD 8: 81%
SCALE:35X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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