

87654321

REVISION HISTORY

REV	DATE	COMMENTS	ENG
1	04/28/17	INITIAL RELEASE	WKM
-	07/19/17	CHANGES PER BUG 2402 & 2435	WAS

REQUIREMENTS

1. MANUFACTURE BOARD IAW (IN ACCORDANCE WITH) IPC-6012, CLASS 2.

2. TOTAL BOARD THICKNESS: 62 MILS +/- 10% ALL MATERIAL SHALL BE RoHS-COMPLIANT FR-4 OR EQUIVALENT

3. COPPER PLATING ON WALL OF PLATED THROUGH HOLES SHALL BE 0.8 MIL MIN FOR CLASS 2.

4. MINIMUM TRACE WIDTH: 5 MILS MINIMUM SPACING: 5 MILS

5. SOLDERMASK:

5.1 LIQUID PHOTOIMAGEABLE (LPI) SOLDERMASK OVER BARE COPPER (SMOBC), TOP AND BOTTOM SIDES

5.2 COLOR: GREEN

5.3 RESIZING FOR OPTIMAL MASK CLEARANCE TO CONDUCTIVE FEATURES PERMISSIBLE.

6. HOLES:

6.1 UNLESS OTHERWISE SPECIFIED ALL HOLE SIZES SHALL BE AS SPECIFIED +/- 3 MILS.

6.2 ALL HOLE SIZES FOR VIAS ARE MAXIMUM DIMENSIONS ONLY.

7. SURFACE FINISH SHALL BE ELECTROLESS NICKEL IMMERSION GOLD (ENIG)

8. DRC'S MUST BE RUN ON GERBERS BEFORE BUILDING BOARDS UNLESS PRIOR APPROVAL IS GIVEN IN WRITING.

9. BOARD SHALL BE ELECTRICALLY TESTED USING IPC-NETLIST FILE GIVEN UNLESS PRIOR APPROVAL IS GIVEN IN WRITING.

10. TOOLING RAILS WITH ROUTE-AND-RETAIN ARE REQUIRED ON PANEL FOR ASSEMBLY, PANELIZATION IS DETERMINED BY VENDOR. ROUGH BOARD EDGES RESULTING FROM DE-PANELIZATION SHALL BE SANDED SMOOTH.

11. SILKSCREEN COLOR: WHITE

12. CONTROLLED IMPEDANCE REQUIREMENTS:

12.1 SINGLE ENDED:

LAYERS: TOP, INNER1, INNER2, BOTTOM

50 OHMS +/- 5 OHMS ON ALL 5 MIL WIDE TRACES

12.2 EDGE-COUPLED DIFFERENTIAL (100 OHMS):

LAYERS: TOP, BOTTOM

100 OHMS +/- 10 OHMS ON 5.01 MIL WIDE TRACES WITH 9 MIL AIRGAP

12.3 EDGE-COUPLED DIFFERENTIAL (90 OHMS):

LAYERS: TOP, BOTTOM

90 OHMS +/- 9 OHMS ON 5.3 MIL WIDE TRACES WITH 6 MIL AIRGAP

13. REMOVAL OF NON-FUNCTIONAL PADS IS PERMISSIBLE.

14. WARP OR TWIST OF BOARD SHALL NOT EXCEED 0.75%

15. REMOVE ALL BURRS AND BREAK SHARP EDGES 10 MILS MAXIMUM.

62.0 + 10%
- 10%

DETAIL A

LAYER STACKING CONFIGURATION

SCALE = NONE

LAYER 1 SILKSCREEN

LAYER 1 SOLDER MASK

LAYER 1 - TOP - 1/2 OZ PLUS PLATING

DIELECTRIC

LAYER 2 - GROUND 1 - 1 OZ

DIELECTRIC

LAYER 3 - INNER 1 - 1/2 OZ

DIELECTRIC

LAYER 4 - GROUND 2 - 1 OZ

DIELECTRIC

LAYER 5 - POWER 1 - 1 OZ

DIELECTRIC

LAYER 6 - POWER 2 - 1 OZ

DIELECTRIC

LAYER 7 - GROUND 3 - 1 OZ

DIELECTRIC

LAYER 8 - INNER 2 - 1/2 OZ

DIELECTRIC

LAYER 9 - GROUND 4 - 1 OZ

DIELECTRIC

LAYER 10 - BOTTOM - 1/2 OZ PLUS PLATING

LAYER 10 SOLDER MASK

LAYER 10 SILKSCREEN

D3

D3 ENGINEERING
1057 E Henrietta Road
Rochester, NY 14623

TITLE
PCB,
TDA3x STARTER KIT,
4-FPD BASEBOARD 2G

DWG
B
SIZE

ITEM NO.
PCB-00C022201

REV
-

DRAWN BY:
W.SENDER

APPROVED BY:
W.MURPHY

DATE:
04/28/17

CAGE CODE 3V6D5

SCALE X/X

SHT 1 OF 2

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