Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR-4 High Tg	5.00mil	4.2	
2	Signal Layer 1		1.40mil		
	Dielectric 2	FR-4 High Tg	24.40mil	4.2	
3	Signal Layer 2		1.40mil		
	Dielectric 3	FR-4 High Tg	5.00mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 10 MIL
MIN. CLEARANCE: 7.874 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 [X] FR-4 High Tg ☐ OTHER _____
THICKNESS: [X] 40 MIL (1.0mm) +/-10% ☐ OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE ☐ OTHER _____
SOLDER RESIST COLOR: [X] GREEN ☐ OTHER _____
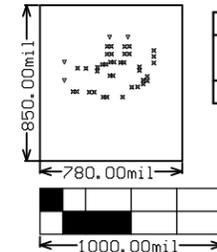[X] MATTE ☐ SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS
TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> ☐ 1 [X] 2 ☐ 3
[X] RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE [X] REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE:
TPS629210-Q1EVM

DESIGNED FOR:
Public Release

FILE NAME:
TIDA_050056.PcbDoc

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
⌑	38	6.00mil (0.152mm)	PTH	Round	Top Layer - Bottom Layer	
▽	4	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer	
	42 Total					

850.00mil
780.00mil
1000.00mil

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = Mechanical Dimensions
PLOT NAME = Fabrication Drawing

BOARD #: TIDA-050056 REV: E1
SVN REV: Not in version control
TID #: .TID
GENERATED : 12/9/2021 6:48:09 PM
TEXAS INSTRUMENTS

ENGINEER:
Nancy Zhang
SCALE: 1.00

LAYOUT BY:
Nancy Zhang
ALTIUM DESIGNER VERSION:
21.2.2.38