



**SAT0027 REV1.0 Test Report (Simple)**  
**6/11/2013**

The following test will evaluate each Source and POL rail for the SAT0027 in the following order.

- A. Overall Board Efficiency
- B. 5V Input Supply (No IC; input of board to each supply)
- C. 12V Input Supply - TPS54339 (5V@2A)
- D. POE Input Supply – TPS23753A (5V@2A)
- E. ARM\_VDD – TPS5432 (1.2V@1.5A)
- F. ARM\_VDD – TPS5432 (1.35V@1.5A)
- G. CORE\_VDD – TPS5432 (1.2V@1.5A)
- H. CORE\_VDD – TPS5432 (1.35V@1.5A)
- I. 1.8V Supply – TPS5432 (1.8V@2A)
- J. 3.3V Supply – TPS63036 (3.3 @1A)

# SAT0027 Test Results Rev. 1

## A. Overall System Efficiency Calculations

The following report is a calculation of overall SAT0027 Board Efficiencies.

<b>Board Efficiency Calculations</b> (Does not take account for routing copper losses)								
<b>1.35V On Core and ARM</b>								
<b>Input</b>	<b>5V Efficiency</b>	<b>Combine Rail Eff</b>	<b>Overall Eff SAT0027</b>					
5V	99%	$(96.7\%+97\%+98\%+93.4\%)/4 = 96.27$	$99\% * 96.27\% = 95.31\%$					
12V	93.60%	$(96.7\%+97\%+98\%+93.4\%)/4 = 96.27$	$93.6\% * 96.27\% = 90.11\%$					
POE (SAT0027)	87.20%	$(96.7\%+97\%+98\%+93.4\%)/4 = 96.27$	$87.20\% * 96.27\% = 83.95\%$					
POE (End-to-End)	85.70%	$(96.7\%+97\%+98\%+93.4\%)/4 = 96.27$	$85.7\% * 96.27\% = 82.5\%$					
<b>1.2V On Core and ARM</b>								
5V	99%	$(96.7\%+97\%+97.8\%+93.4\%)/4 = 96.23$	$99\% * 96.23\% = 95.27\%$					
12V	93.60%	$(96.7\%+97\%+97.8\%+93.4\%)/4 = 96.23$	$93.6\% * 96.23\% = 90.07\%$					
POE (SAT0027)	87.20%	$(96.7\%+97\%+97.8\%+93.4\%)/4 = 96.23$	$87.20\% * 96.23\% = 83.91\%$					
POE (End-to-End)	85.70%	$(96.7\%+97\%+97.8\%+93.4\%)/4 = 96.23$	$85.7\% * 96.23\% = 82.47\%$					

## B. 5V Input Supply

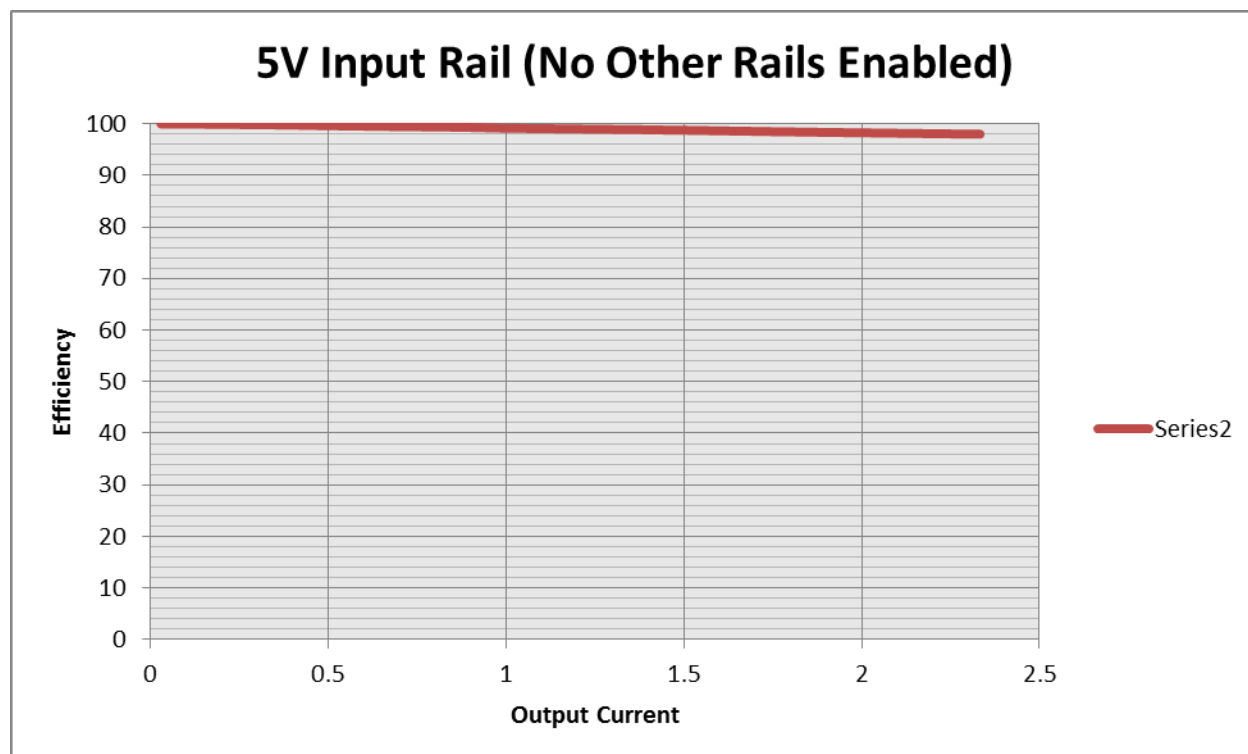
The following test report is for the 5V Input Power Delivered to Subsequent Rails.

The tests performed were as follows: 5V @ 2A

1. Efficiency
2. Load Regulation

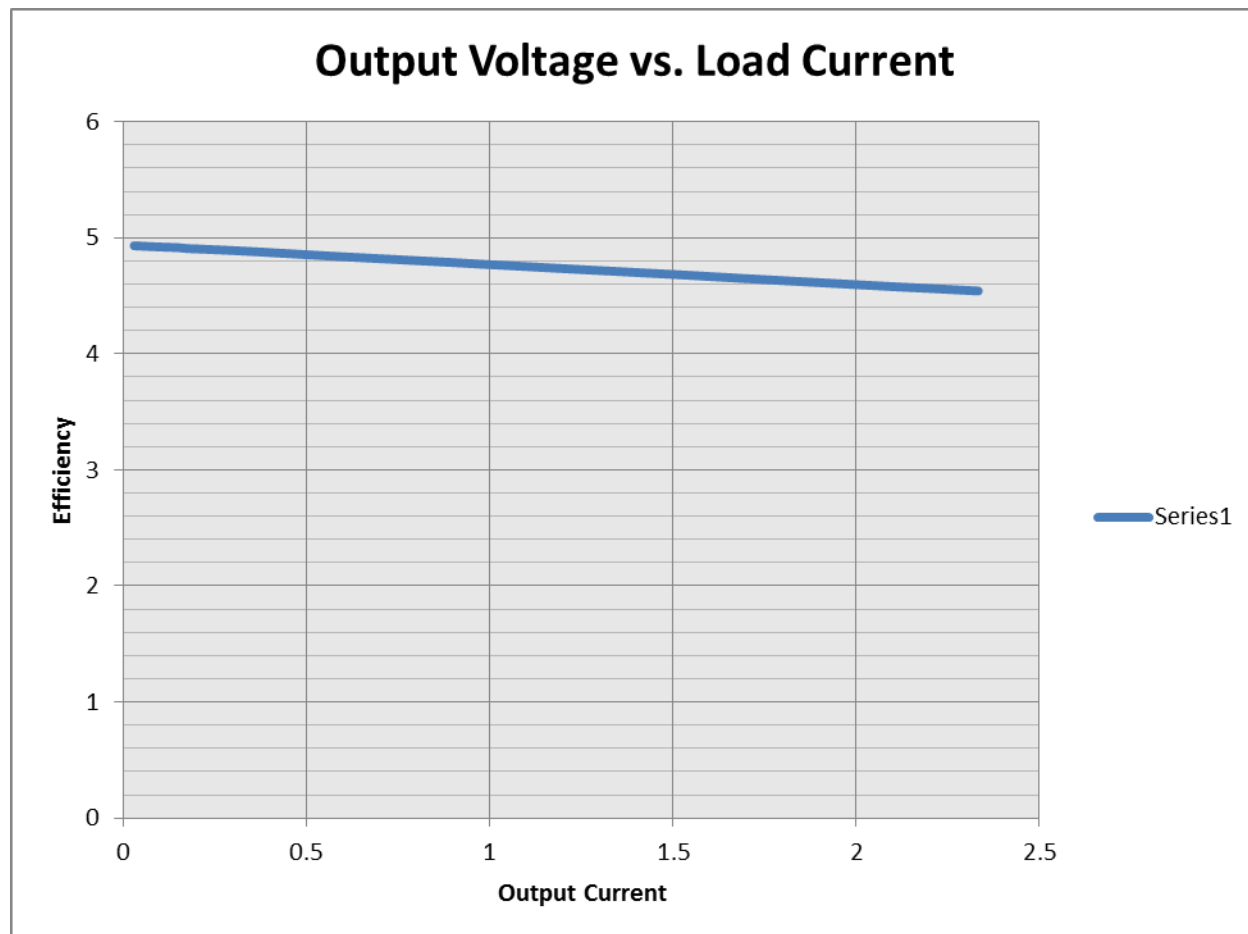
### 1 Efficiency – (5V@2A)

The figure below shows the efficiency of the input supply to the POL rails. The input voltage is 5V.



## 2 Load Regulation – (5V@2A)

The figure below shows the voltage drop to the load. The input voltage is 5V.



## C. 12V Input Supply –TPS5432 (5V @2A)

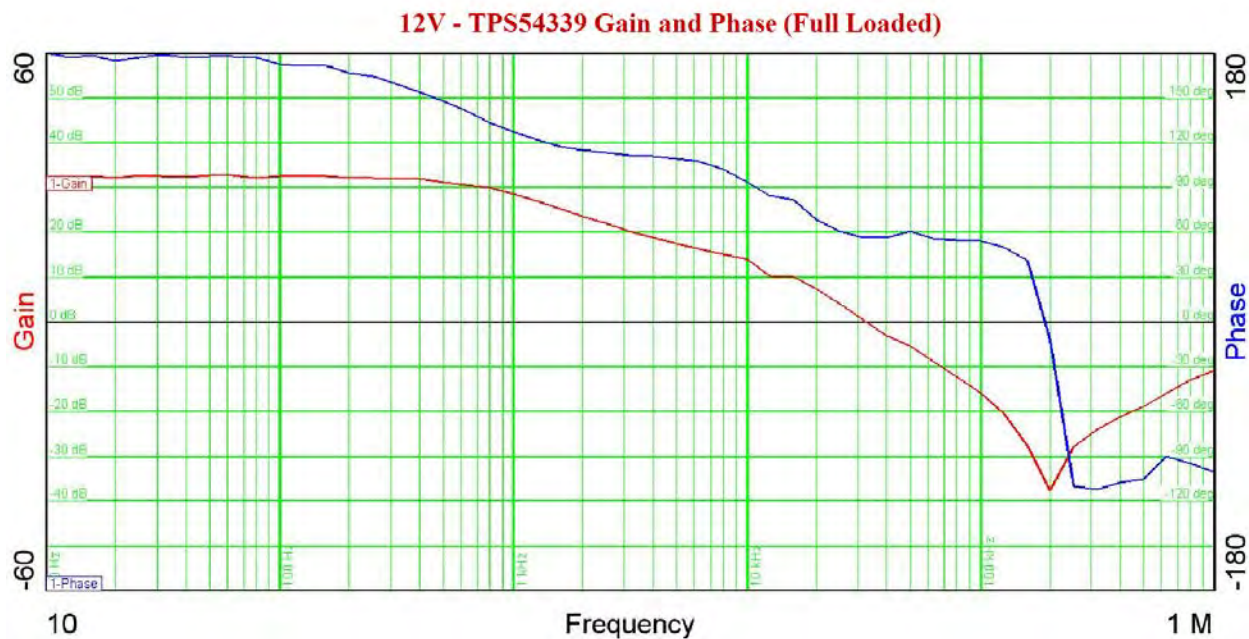
The following test report is for the TPS5432 12V Input Supply.

The tests performed were as follows: 5V @ 2A

1. Bode Plot
2. Efficiency
3. Load Regulation

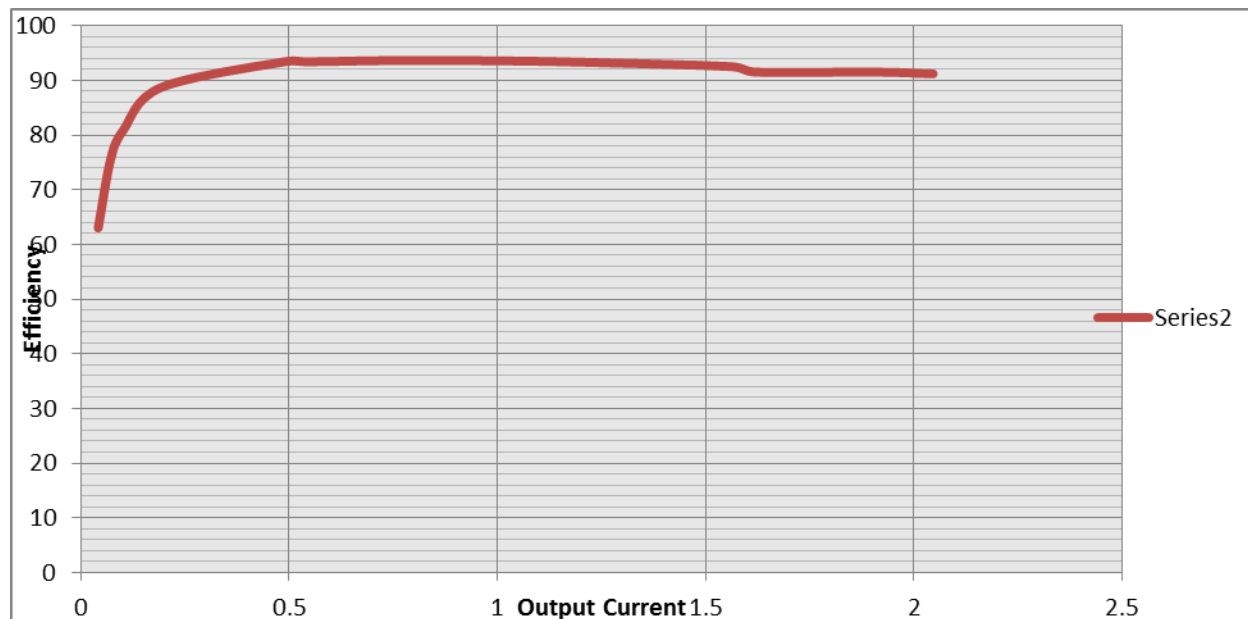
### 1 Bode Plot – (TPS5432 – 5V@2A)

The figure below shows the loop response of the converter. The input voltage is 12V, the output is loaded with 2A.



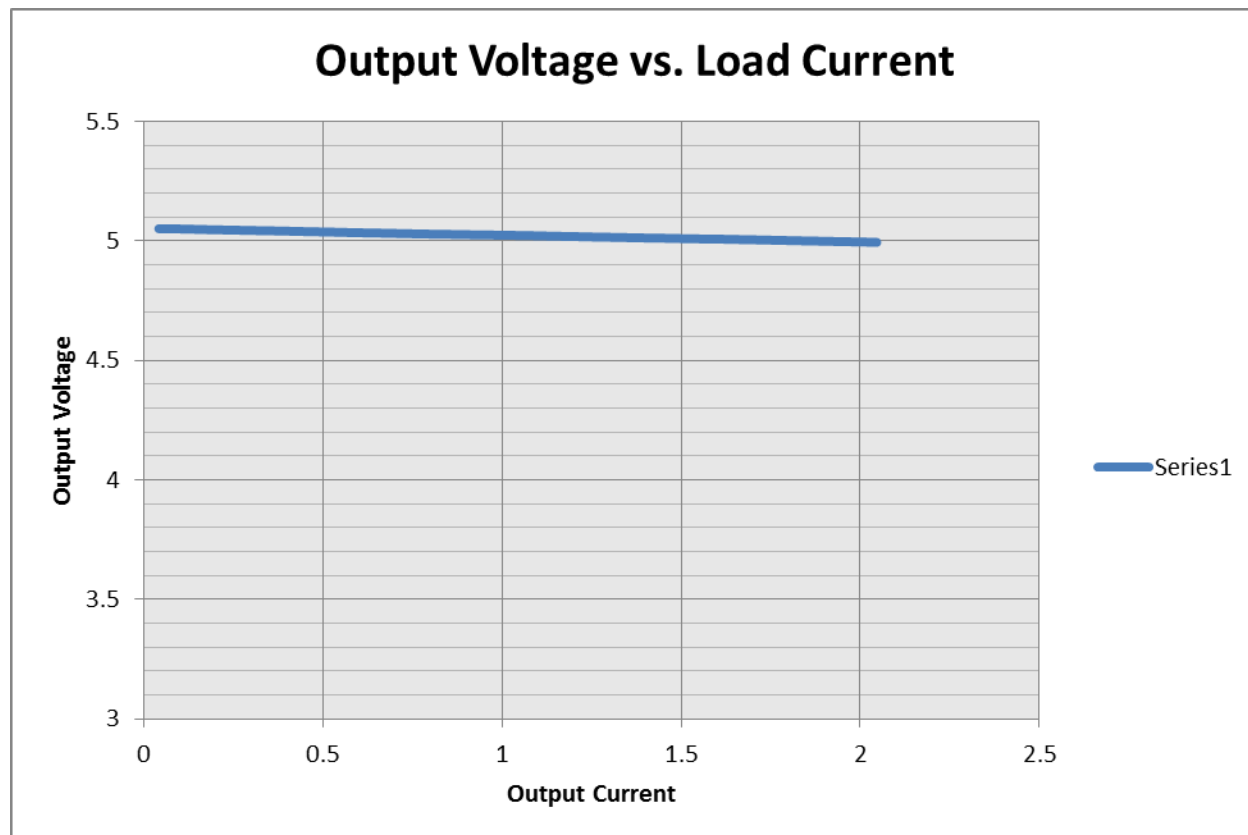
## 2 Efficiency – (TPS5432 – 5V @2A)

The figure below shows the efficiency of the converter. The input voltage is 12V.



### 3 Load Regulation – (TPS5432 – 5V@2A)

The figure below shows the load regulation of the converter. The input voltage is 12V.



## D. Power Over Ethernet –TPS23753A (5V @2A)

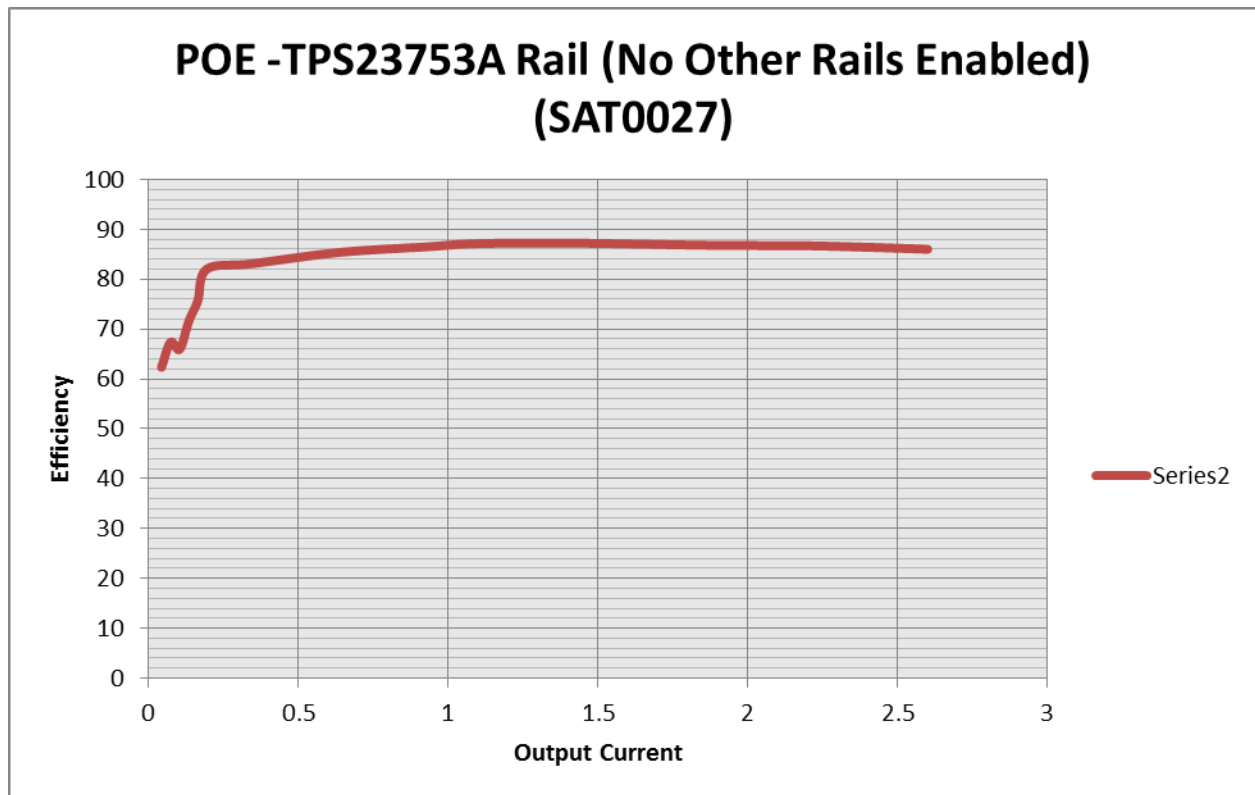
The following test report is for the TPS23753A -50V Input Supply.

The tests performed were as follows: 5V @ 2A

1. Efficiency
2. Load Regulation

### 1 Efficiency - (TPS23753A – 5V@2A)

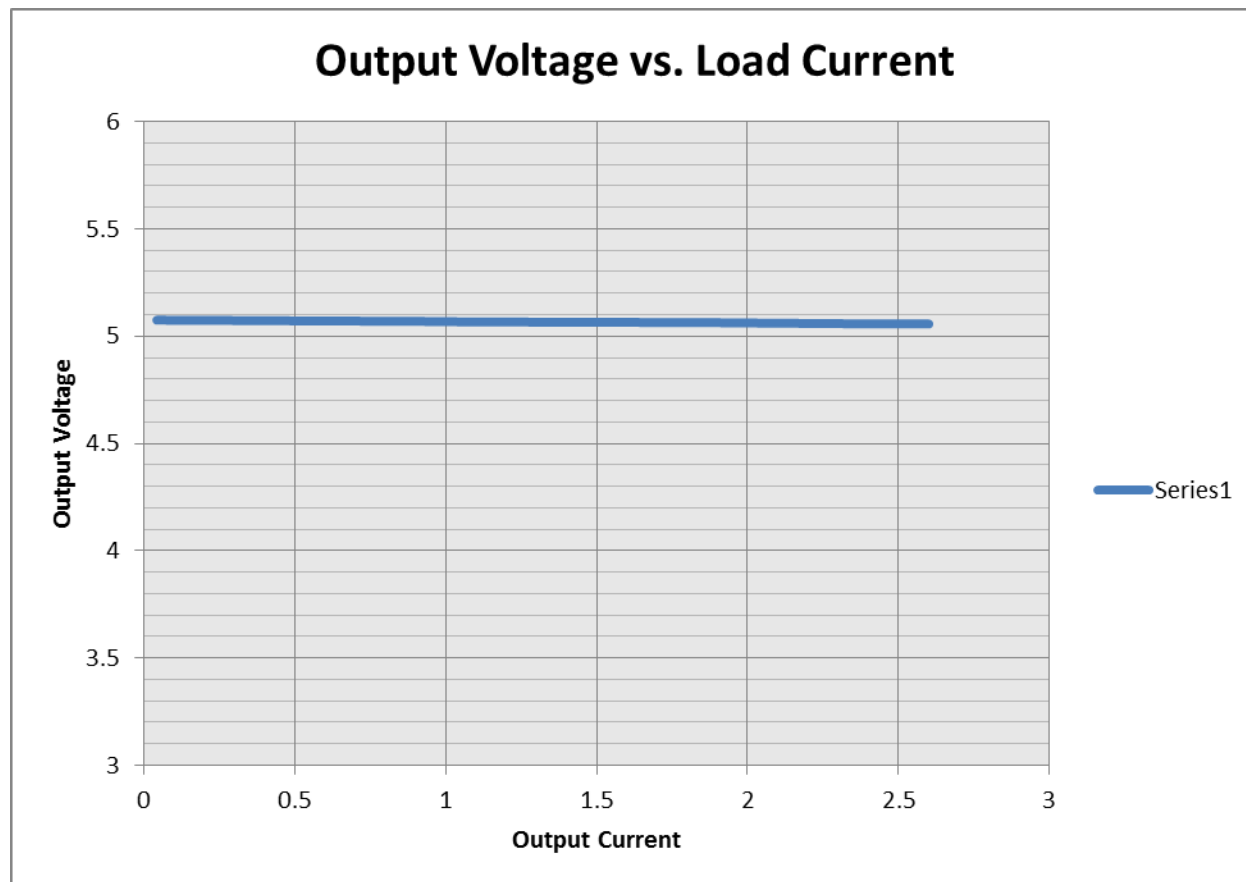
The figure below shows the efficiency of the converter. The input voltage is 50V.





## 2 Load Regulation – (TPS23753A – 5V@2A)

The figure below shows the load regulation of the converter. The input voltage is 50V.



## E. ARM\_VDD –TPS5432 (1.2V @1.5A)

The following test report is for the TPS5432 ARM\_VDD.

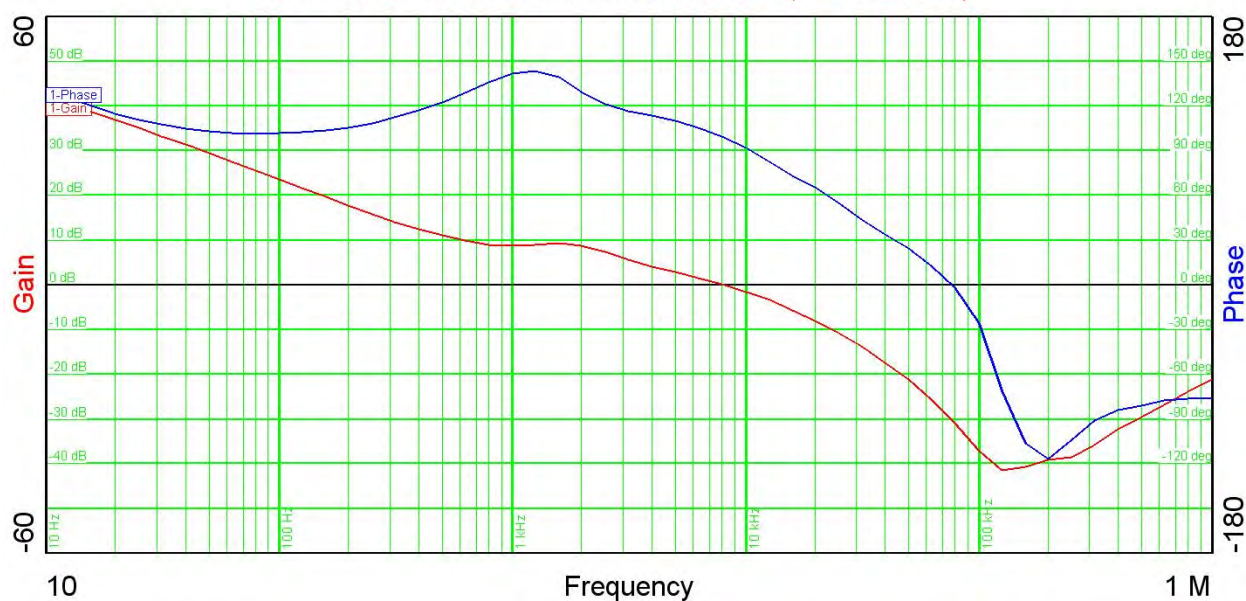
The tests performed were as follows: 1.2V @ 1.5A

1. Bode Plot
2. Efficiency
3. Load Regulation

### 1 Bode Plot – (ARM\_VDD -TPS5432 – 1.2V@1.5A)

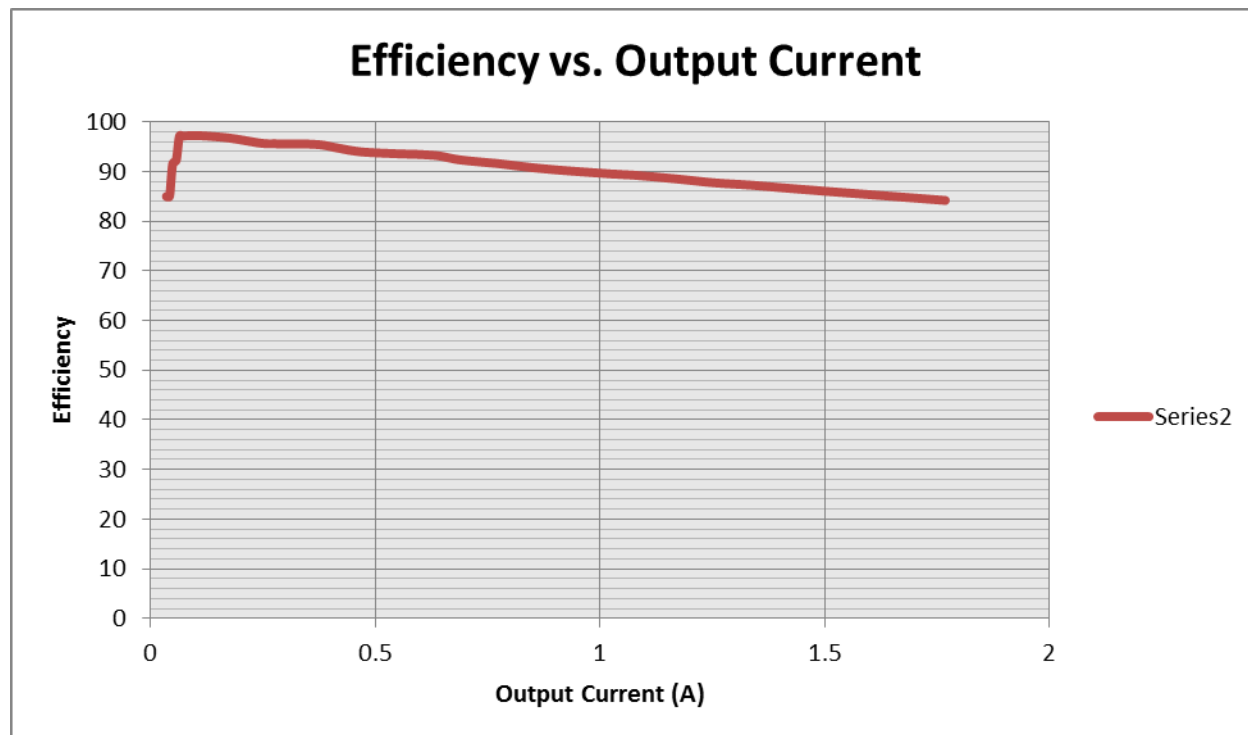
The figure below shows the loop response of the converter. The input voltage is 5V, the output is loaded with 1.5A.

**1.2V ARM-TPS5432 Gain and Phase (Full Loaded)**



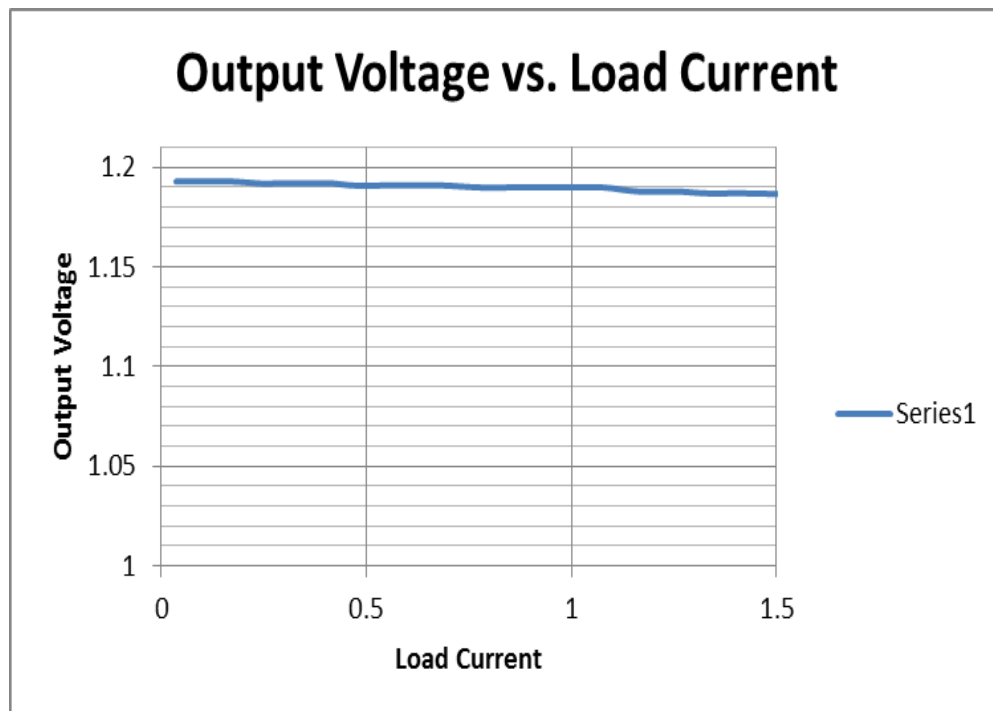
## 2 Efficiency – (ARM\_VDD - TPS5432 – 1.2V@1.5A)

The figure below shows the efficiency of the converter. The input voltage is 5V.



### 3 Load Regulation – (ARM\_VDD - TPS5432 – 1.2V@1.5A)

The figure below shows the load regulation of the converter. The input voltage is 5V.



## F.ARM\_VDD –TPS5432 (1.35V @1.5A)

The following test report is for the TPS5432 ARM\_VDD.

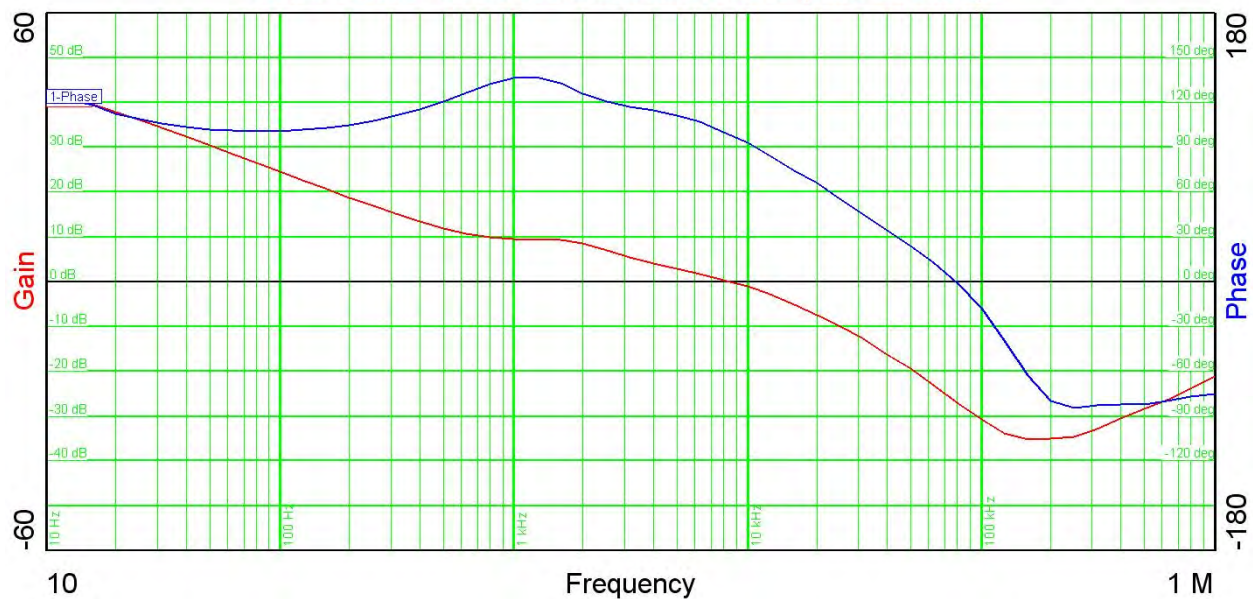
The tests performed were as follows: 1.35V @ 1.5A

1. Bode Plot
2. Efficiency
3. Load Regulation

### 1 Bode Plot – (ARM\_VDD -TPS5432 – 1.35V@1.5A)

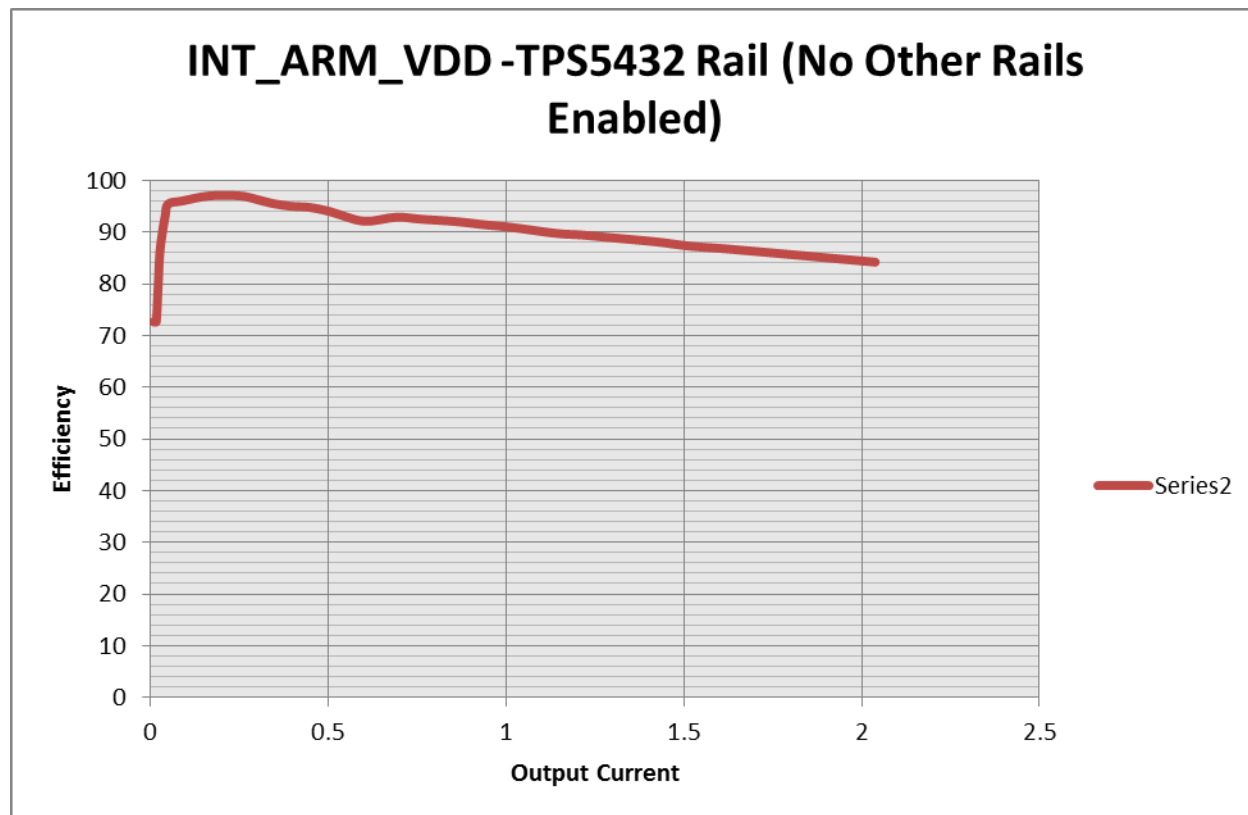
The figure below shows the loop response of the converter. The input voltage is 5V, the output is loaded with 1.5A.

**1.35V ARM -TPS5432 Gain and Phase (Full Loaded)**



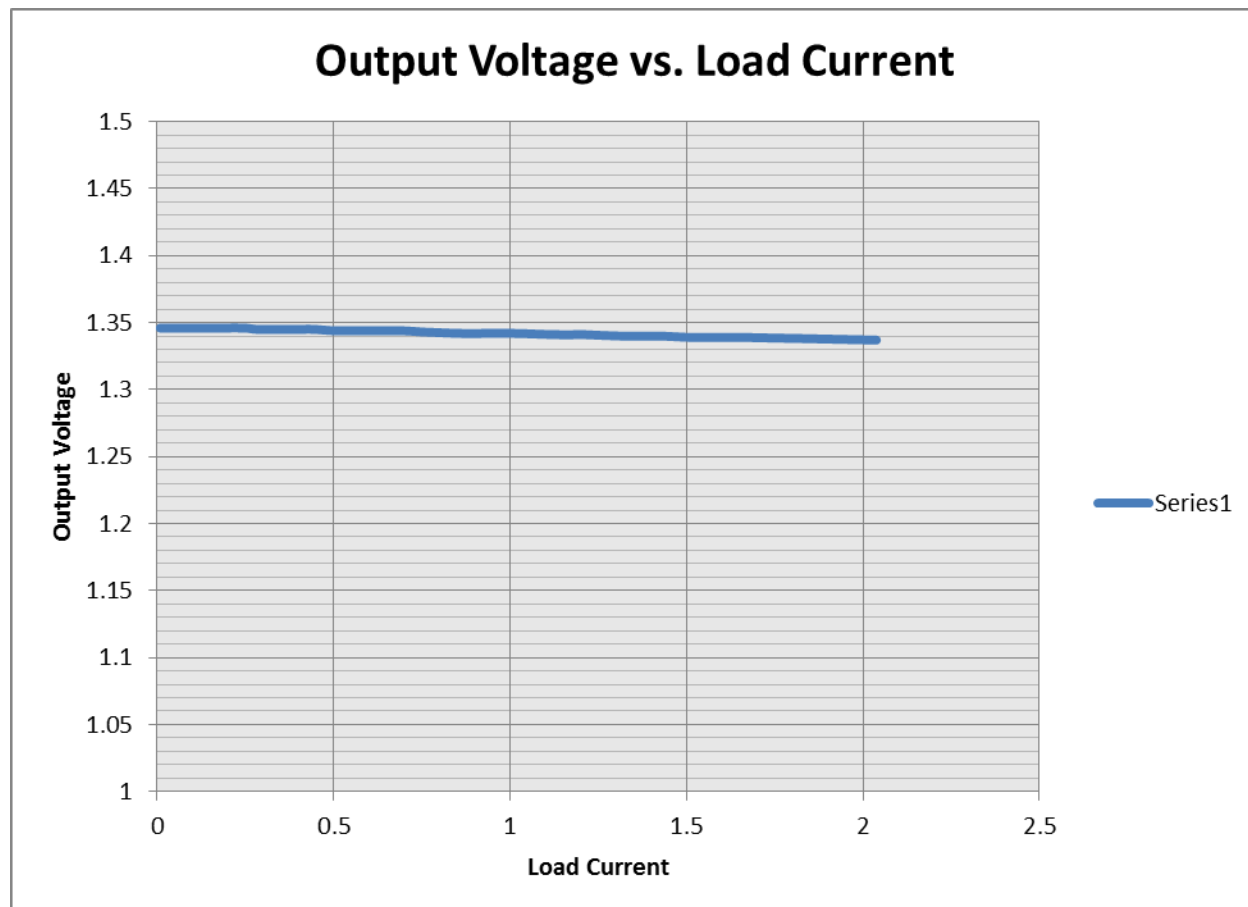
## 2 Efficiency – (ARM\_VDD - TPS5432 – 1.35V@1.5A)

The figure below shows the efficiency of the converter. The input voltage is 5V.



### 3 Load Regulation – (ARM\_VDD - TPS5432 – 1.35V@1.5A)

The figure below shows the load regulation of the converter. The input voltage is 5V.



## G. CORE\_VDD –TPS5432 (1.2V @1.5A)

The following test report is for the TPS5432 CORE\_VDD.

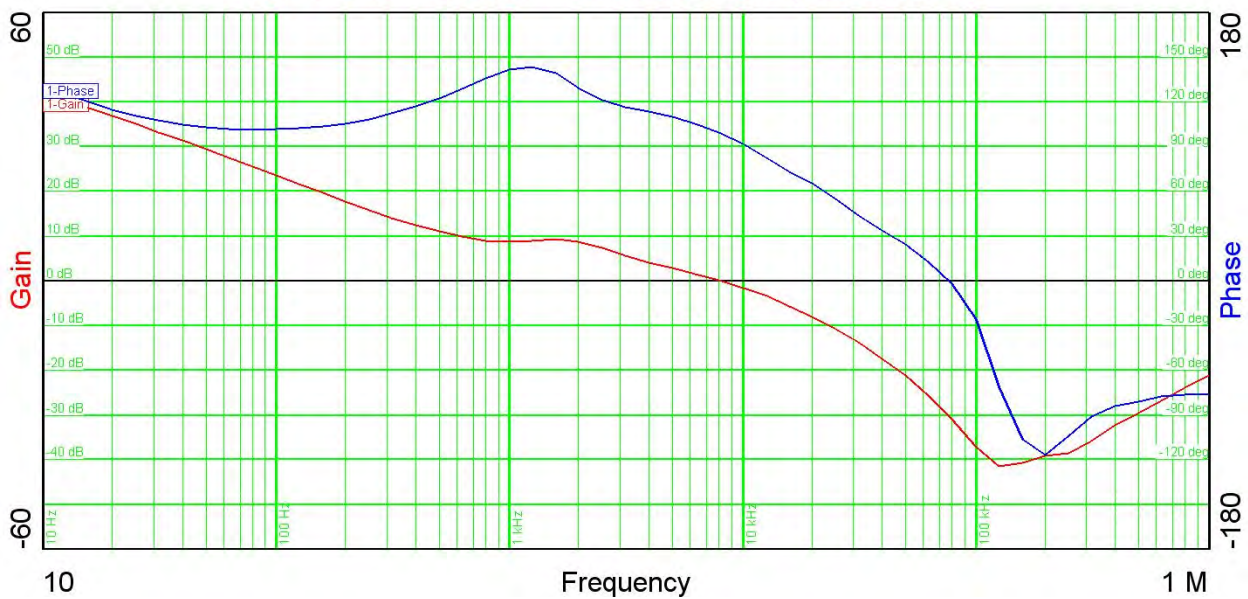
The tests performed were as follows: 1.2V @ 1.5A

1. Bode Plot
2. Efficiency
3. Load Regulation

### 1 Bode Plot – (CORE\_VDD -TPS5432 – 1.2V@1.5A)

The figure below shows the loop response of the converter. The input voltage is 5V, the output is loaded with 1.5A.

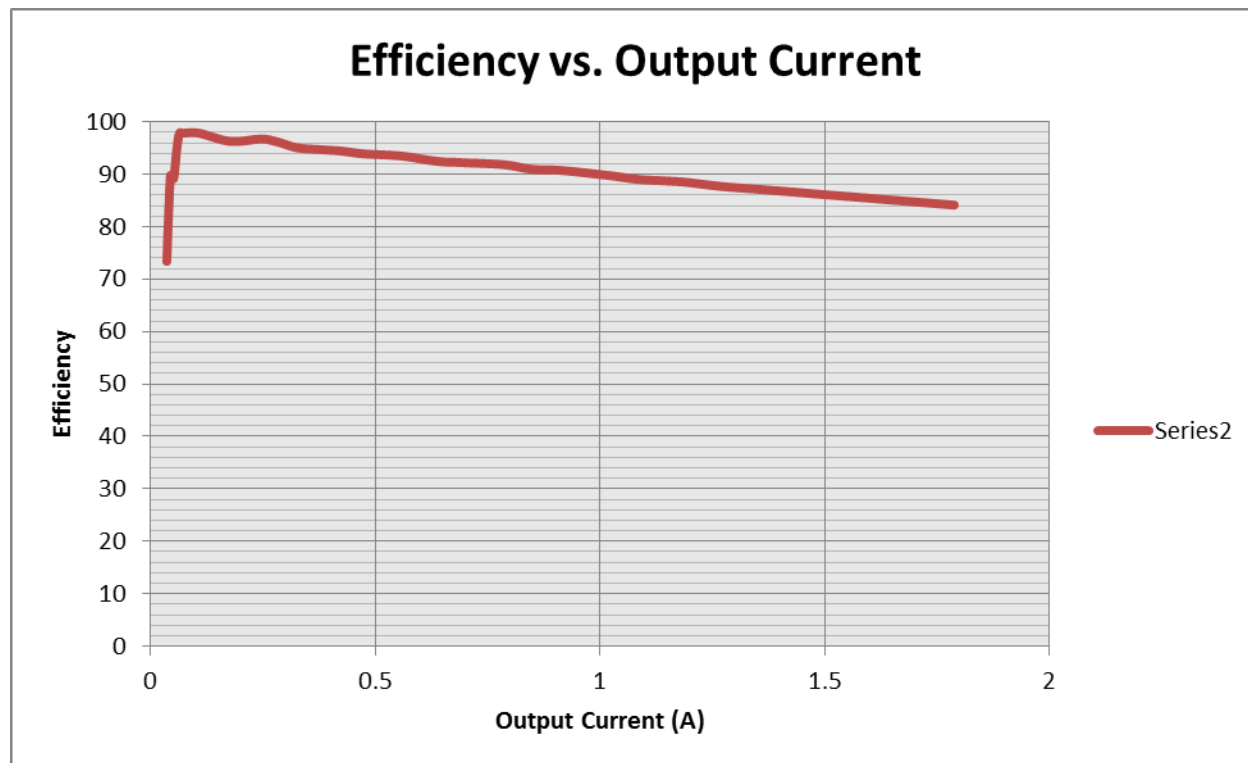
**1.2V CORE -TPS5432 Gain and Phase (Full Loaded)**





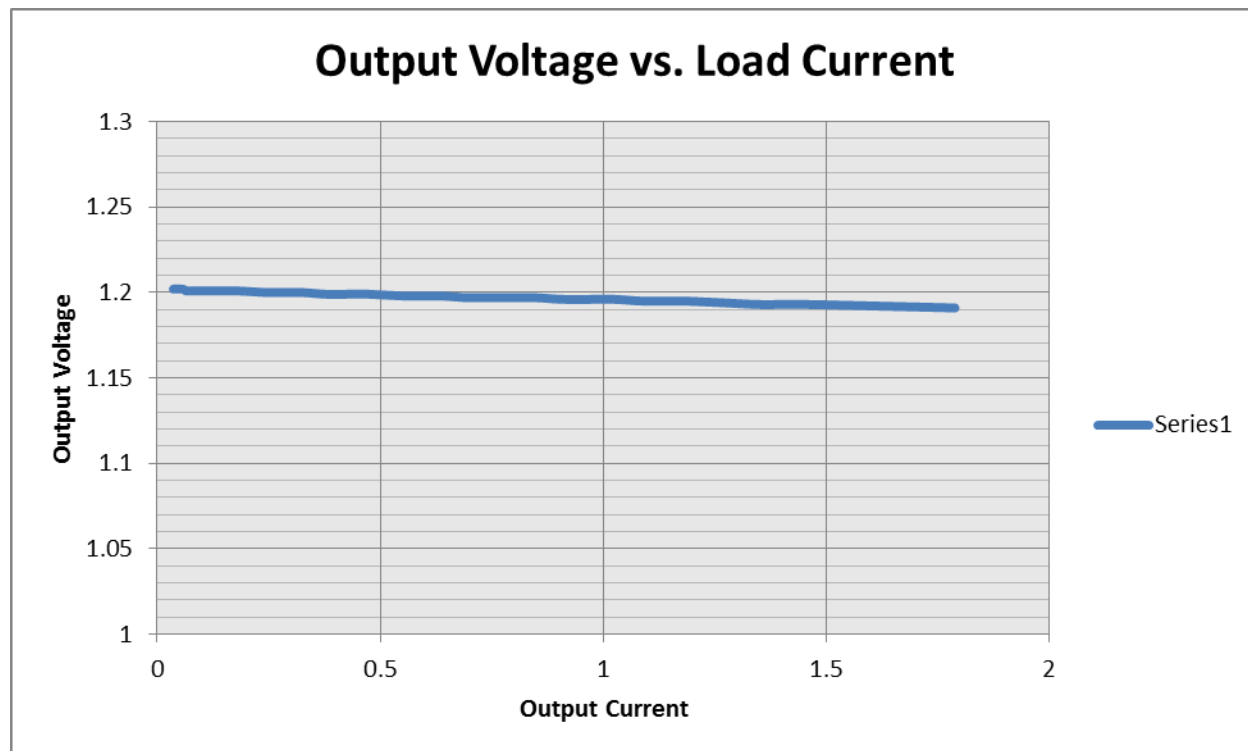
## 2 Efficiency – (CORE\_VDD - TPS5432 – 1.2V@1.5A)

The figure below shows the efficiency of the converter. The input voltage is 5V.



### 3 Load Regulation – (CORE\_VDD - TPS5432 – 1.2V@1.5A)

The figure below shows the load regulation of the converter. The input voltage is 5V.



## H. CORE\_VDD –TPS5432 (1.35V @1.5A)

The following test report is for the TPS5432 CORE\_VDD.

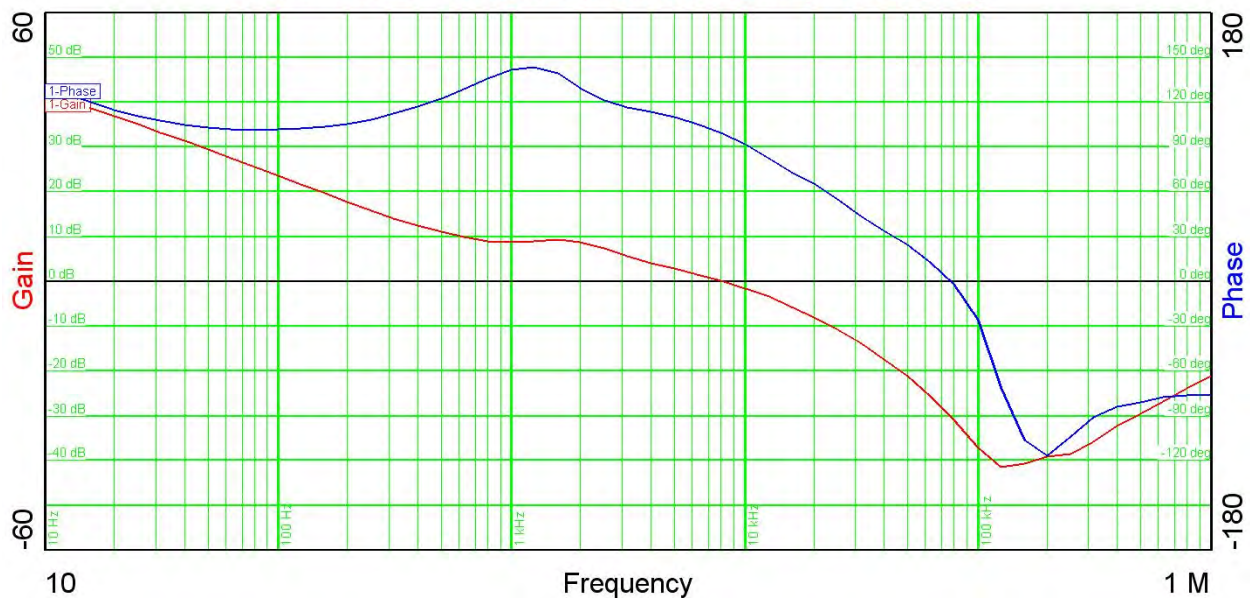
The tests performed were as follows: 1.35V @ 1.5A

1. Bode Plot
2. Efficiency
3. Load Regulation

### 1 Bode Plot – (CORE\_VDD -TPS5432 – 1.35V@1.5A)

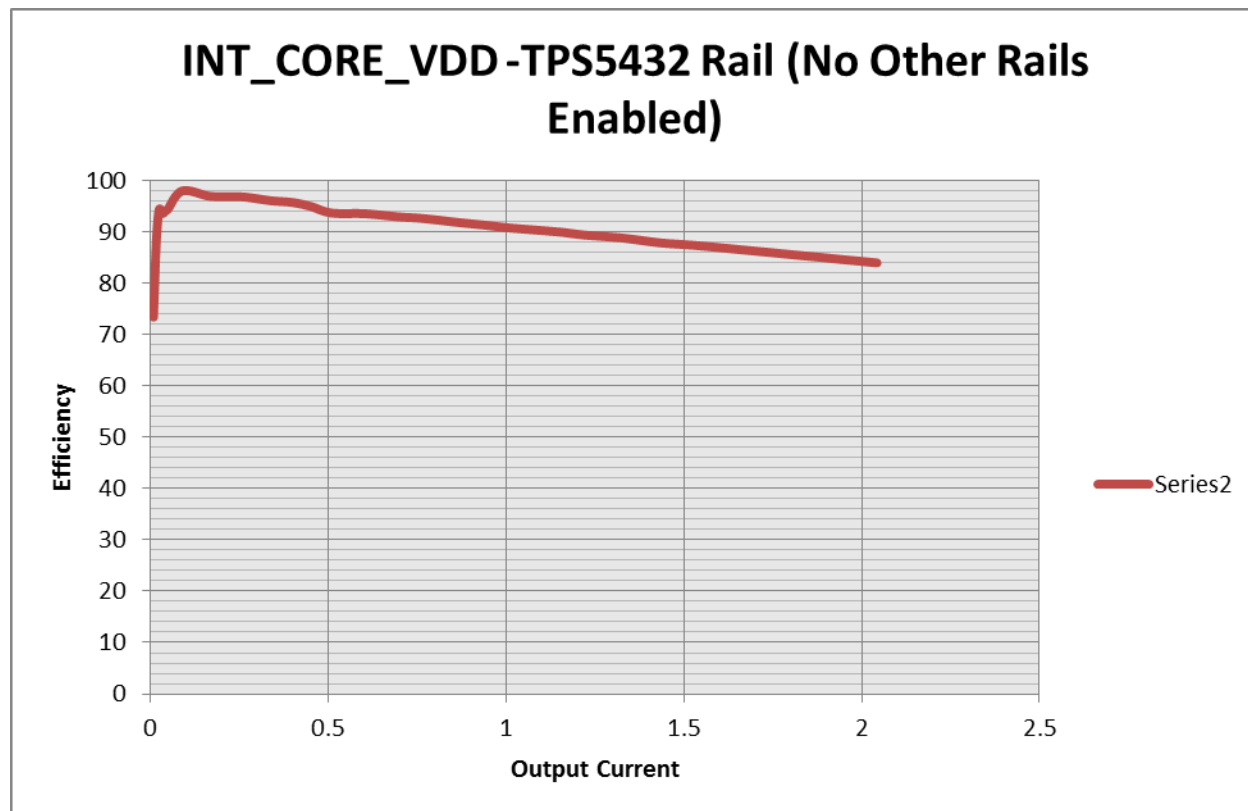
The figure below shows the loop response of the converter. The input voltage is 5V, the output is loaded with 1.5A.

**1.35V CORE -TPS5432 Gain and Phase (Full Loaded)**



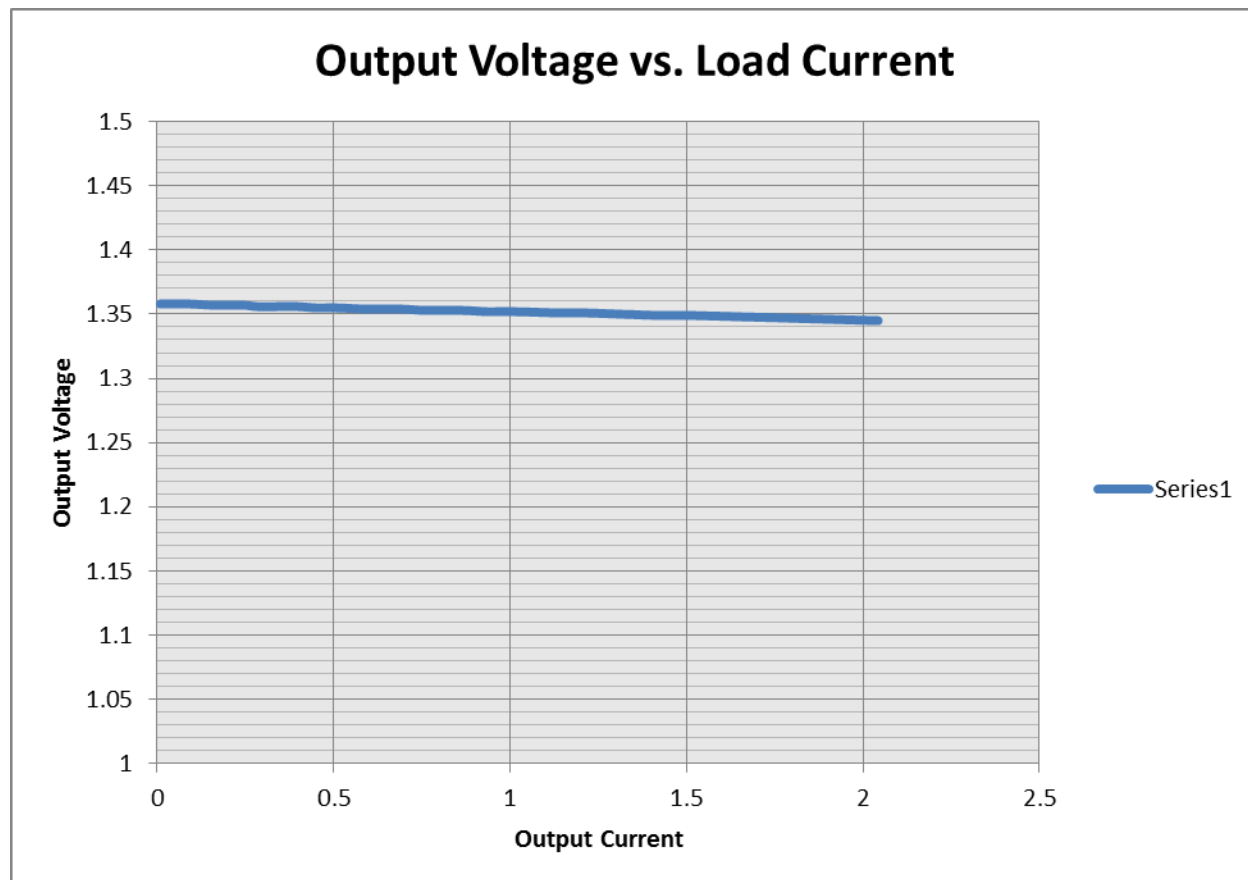
## 2 Efficiency – (CORE\_VDD - TPS5432 – 1.35V@1.5A)

The figure below shows the efficiency of the converter. The input voltage is 5V.



### 3 Load Regulation – (CORE\_VDD - TPS5432 – 1.35V@1.5A)

The figure below shows the load regulation of the converter. The input voltage is 5V.



## I. 1.8V –TPS5432 (1.8V @1.5A)

The following test report is for the TPS5432.

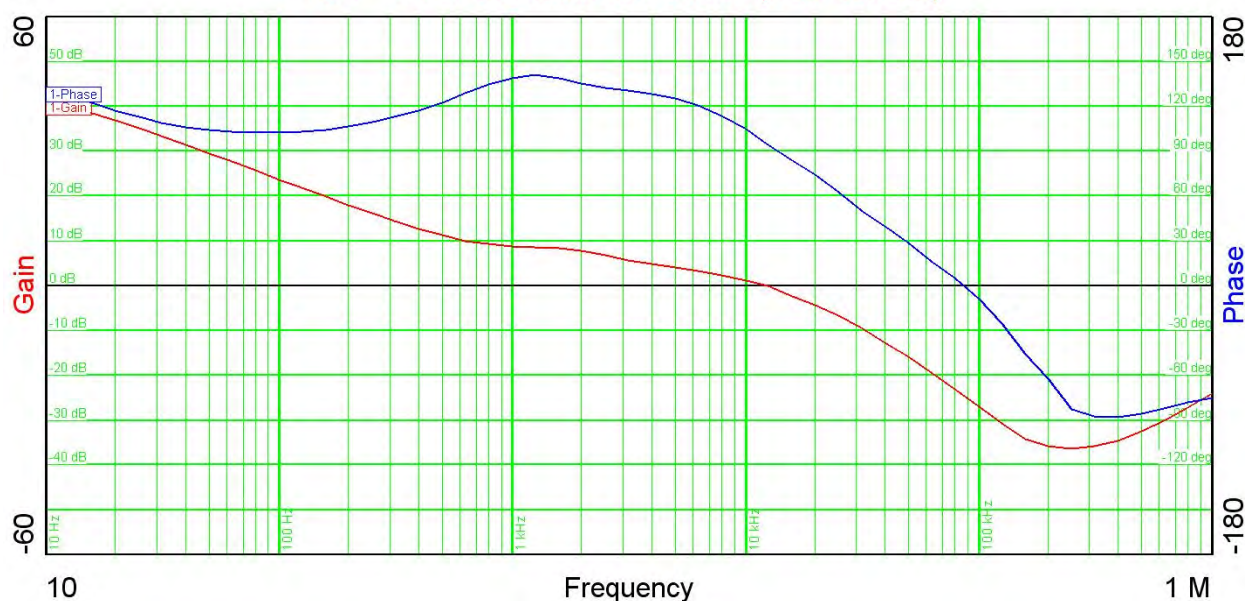
The tests performed were as follows: 1.8V @ 1.5A

1. Bode Plot
2. Efficiency
3. Load Regulation

### 1 Bode Plot – (TPS5432 – 1.8V@1.5A)

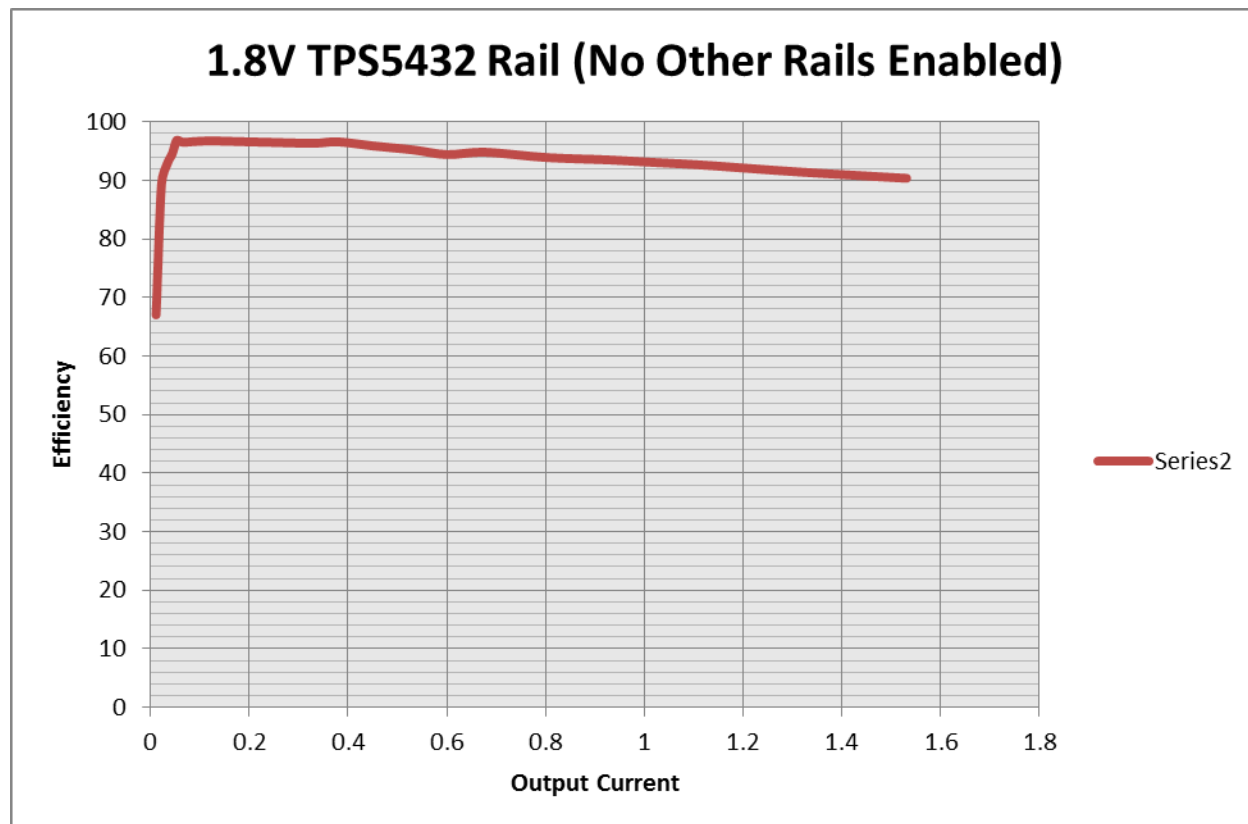
The figure below shows the loop response of the converter. The input voltage is 5V, the output is loaded with 1.5A.

**1.8V - TPS5432 Gain and Phase (Full Loaded)**



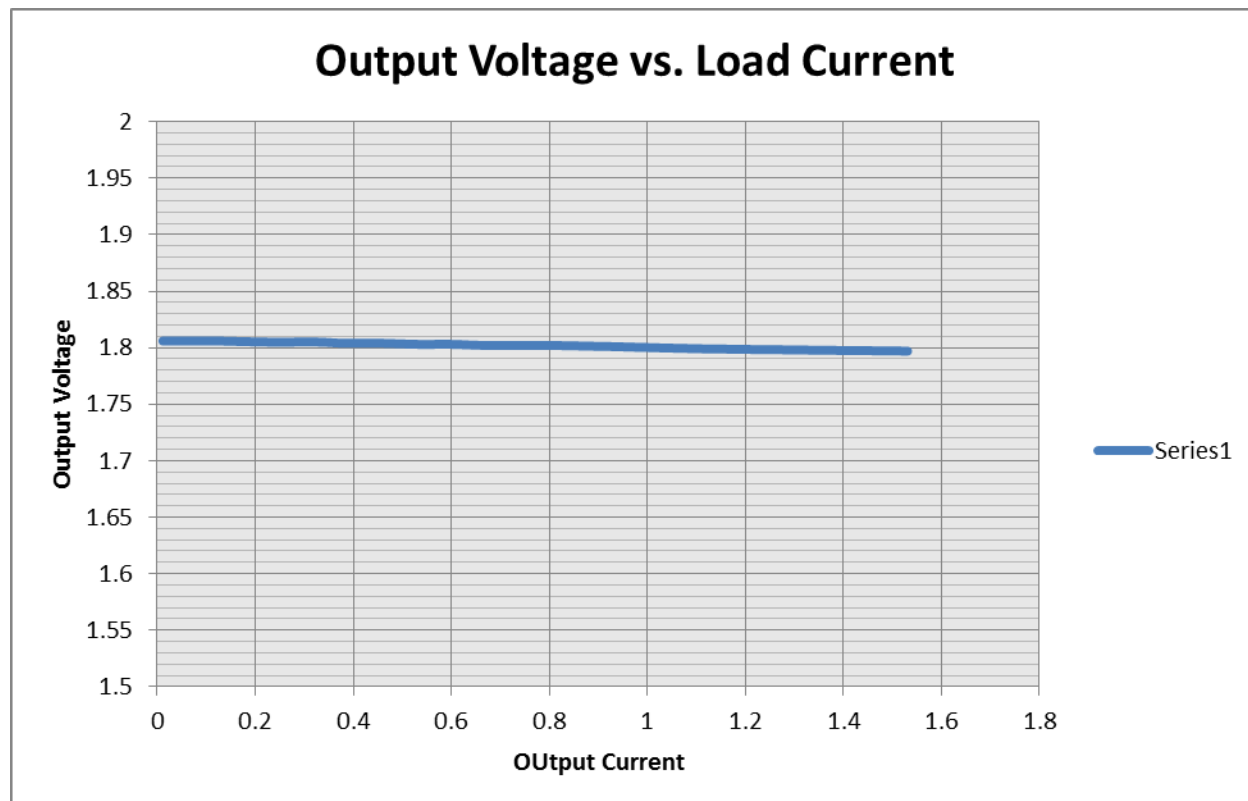
## 2 Efficiency – (TPS5432 – 1.8V@1.5A)

The figure below shows the efficiency of the converter. The input voltage is 5V.



### 3 Load Regulation – (TPS5432 – 1.8V@1.5A)

The figure below shows the load regulation of the converter. The input voltage is 5V.





## J. 3.3V –TPS63036 (3.3V @1.5A)

The following test report is for the TPS63036.

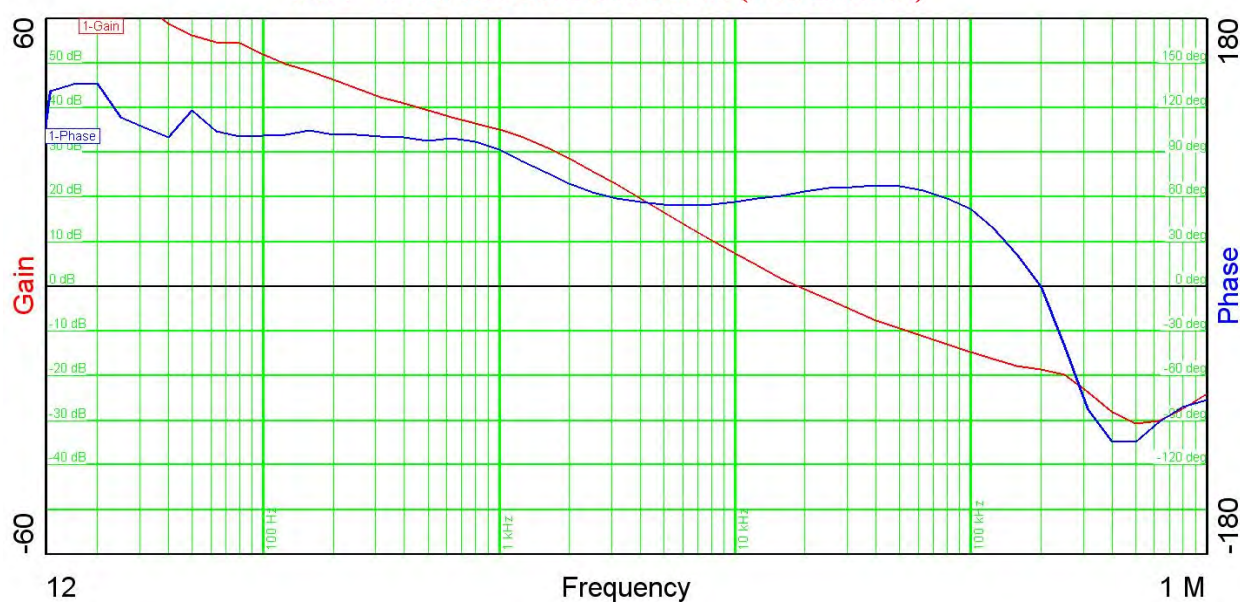
The tests performed were as follows: 3.3V @ 1.5A

1. Bode Plot
2. Efficiency
3. Load Regulation

### 1 Bode Plot – (TPS63036 – 3.3V@1.5A)

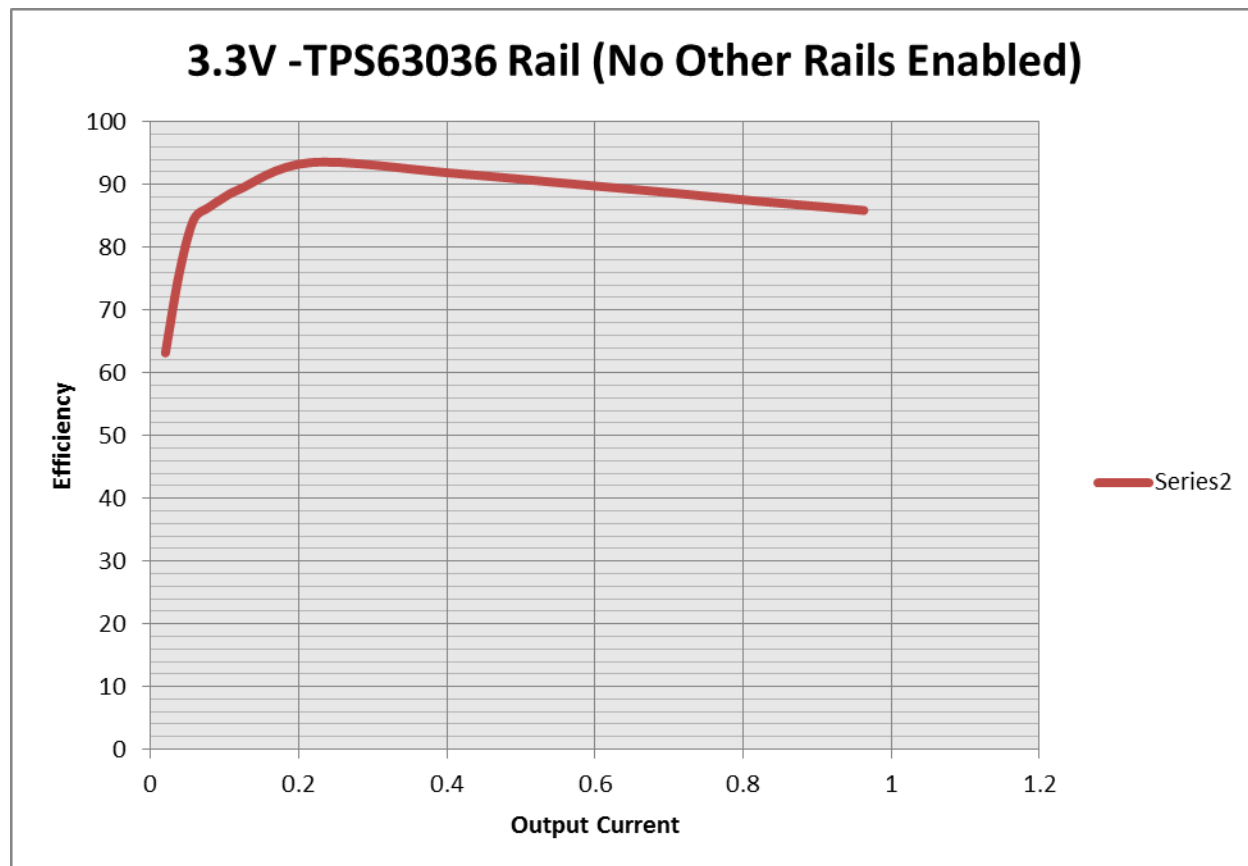
The figure below shows the loop response of the converter. The input voltage is 5V, the output is loaded with 1.5A.

**3.3V -TPS5432 Gain and Phase (Full Loaded)**



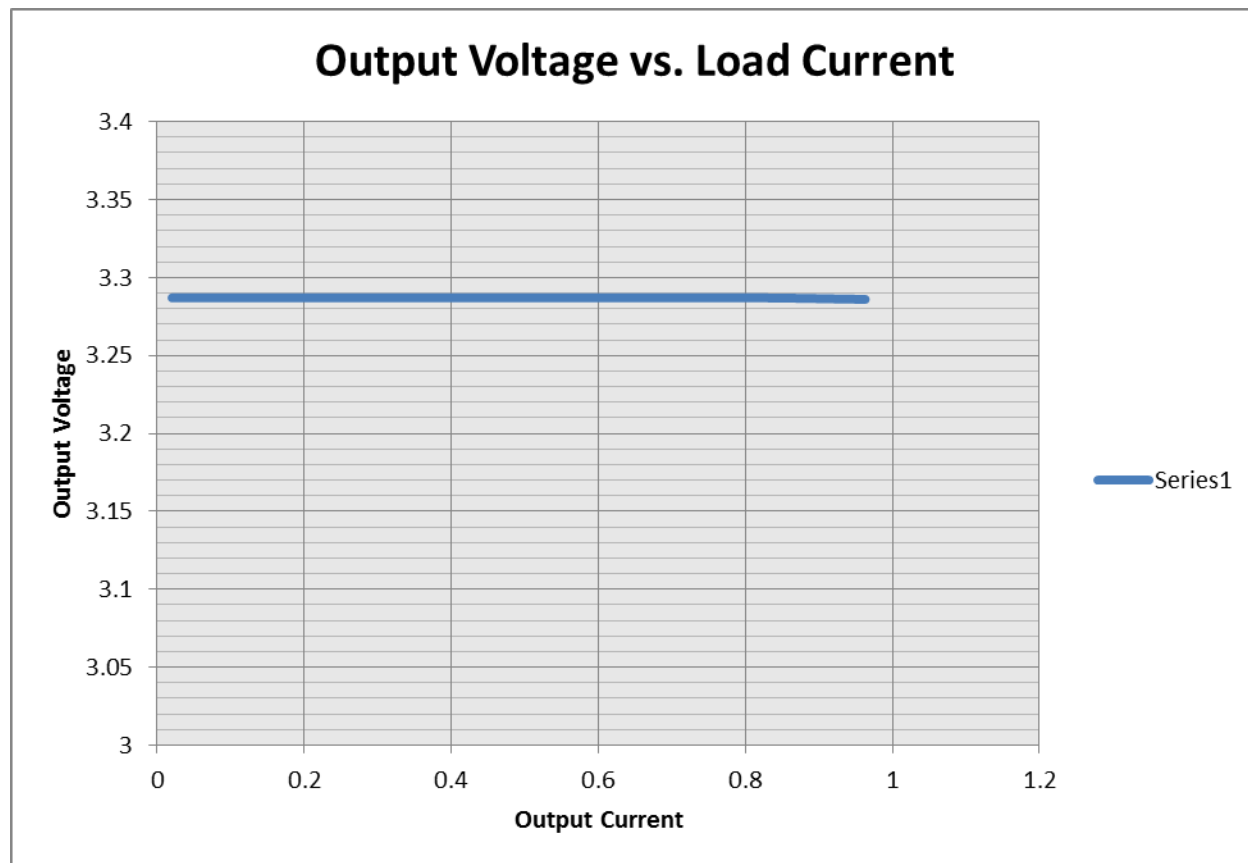
## 2 Efficiency – (TPS63036 – 3.3V@1.5A)

The figure below shows the efficiency of the converter. The input voltage is 5V.



### 3 Load Regulation – (TPS63036 – 3.3V@1.5A)

The figure below shows the load regulation of the converter. The input voltage is 5V.



K.

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