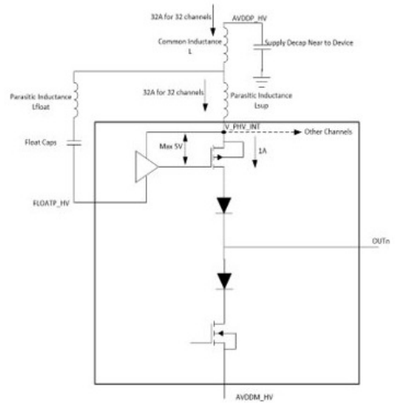
Pulser Output Stage

* Pulser of each channel can give out maximum of 1A current. When all the 32 channels are excited together, device takes 32A current from high voltage power supply.?

* Figure shows simplified diagram of PMOS stage with layout parasitic. ?

* The internal Vgs of PMOS cant go above 5V. Therefore it is important that FLOATP_HV and V_PHV_INT nodes follow each other closely. If supply parasitic cap is higher (Lsup) then it can lead to device abnormal behavior like pulser output is not swinging as expected. Even overall parasitic inductance Lsup of 1nH can give ~2V swing at V_PHV_INT node and can affect device functionality.?

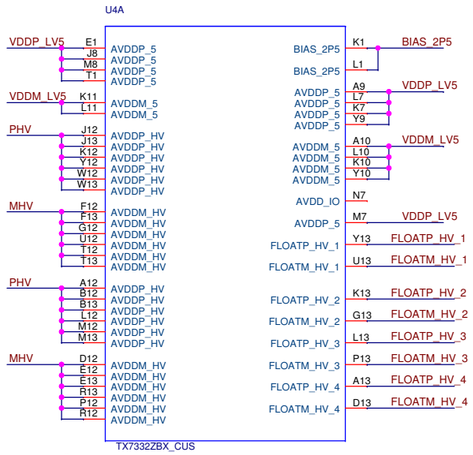
* To avoid this issue, it is recommended to follow the layout guidelines as per given in the datasheet. In layout guidelines the float cap is placed as near to device supply to reduce Lsup inductance.

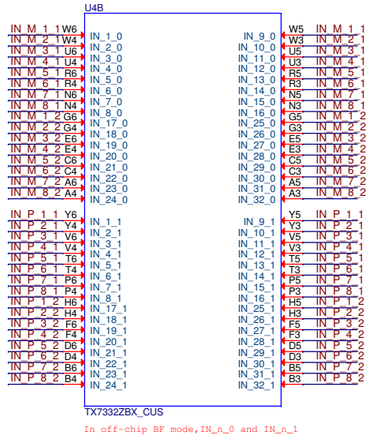


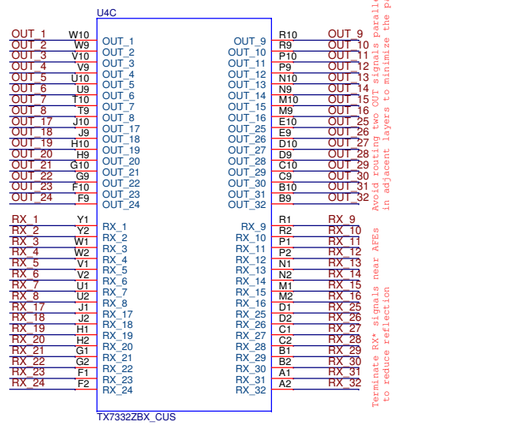
<Variant Name>

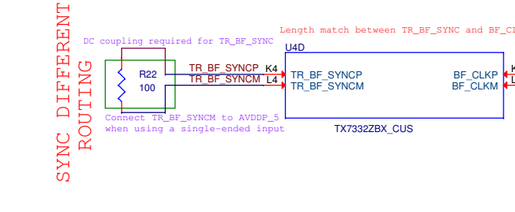
TEXAS INSTRUMENTS	TITLE: DC002_Cover sheet	
Size: C	Variant Name = TX7332	Rev: A
Date: Wednesday, May 27, 2020	Sheet: 01 of 2	

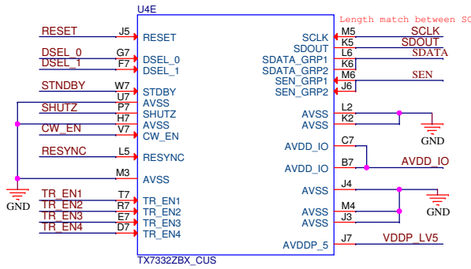
TX7332

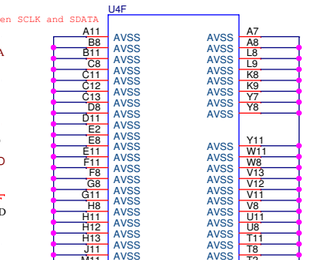






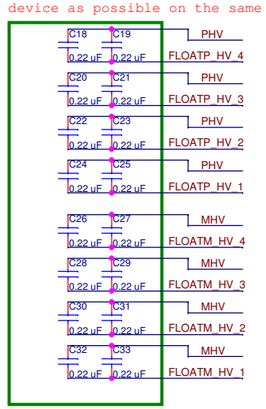






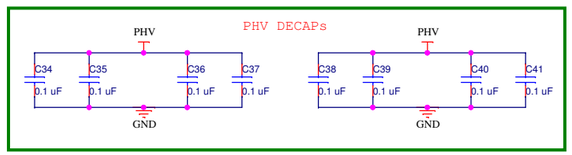
FLOAT DECAPs

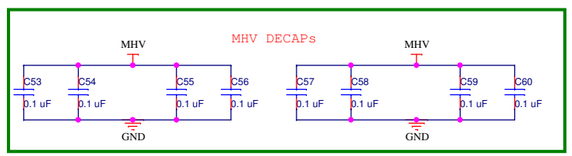
Place the decoupling capacitor as close
to the device as possible on the same layer



HV SUPPLY DECAPS

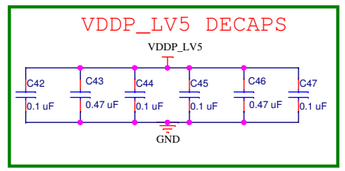
At least one decoupling capacitor for each HV supply pin on the device layer. A HV supply patch just below the device plane is required to ensure the lowest inductance path for supply return current



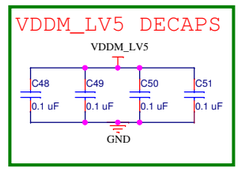


LV SUPPLY DECAPS

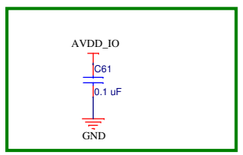
Place at least two decoupling capacitors each of value 0.47 µF on the device layer



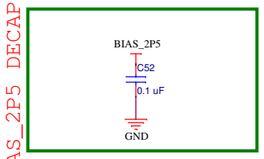
Place at least two decoupling capacitors on the device layer.



AVDD_IO DECAP



BIAS_2P5 DECAP



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TEXAS INSTRUMENTS

TITLE

DC002_Device Pinout

Size		Rev
C	Variant Name =TX7332	A
Date: Wednesday, May 27, 2020	Sheet: 02 of 2	