

TI Designs

Software Defined Radio (SDR) OMAP-L138-Based Reference Platform



TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

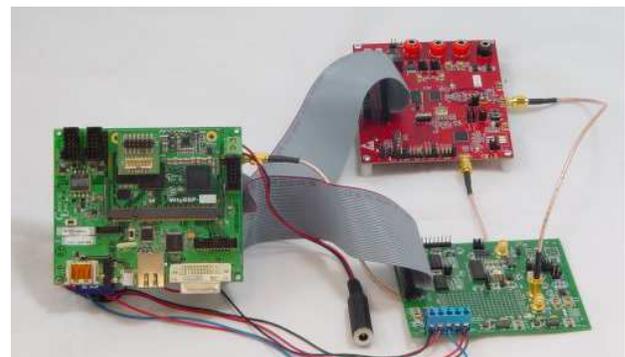
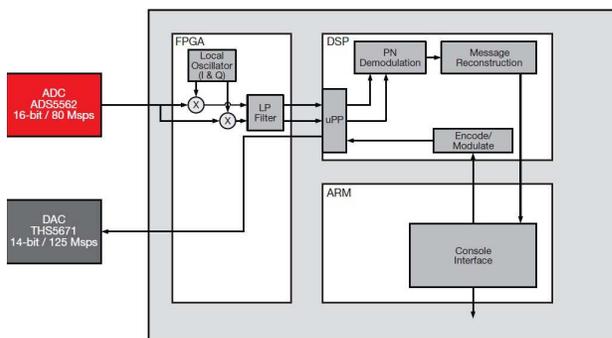
TIDEP0040	Tool Folder Containing Design Files
OMAP-L138	Product Folder
CriticalLink uPP Device Driver	Sample Software
About CriticalLink	TI Design Network
MityDSPOverview	CriticalLink Website
www.CriticalLink.com	CriticalLink Website



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Design Features

- Offers a Software Defined Radio (SDR) platform From Critical Link That Provides a Hardware and Software Framework Designed to Accelerate the Development of SDR Applications
- Includes Both a Xilinx Spartan 6 FPGA and a TI OMAP-L138 Dual Core Processor as Part of Critical Link's Production-ready MityDSP-L138F System on Module (SoM)
- Offers Source Design Files for the Base Industrial Input and Output Card, the ADC Board, and the DAC Board
- Offers an Easy Interface to a OMAP-L138-based SoM
- Offers ARM-based GUI Software
- Offers Sample uPP Software
- Supports Standard Peripherals Including ENET, USB, SATA, and LCD



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1 Overview

Software Defined Radio (SDR) is a popular application within the wireless infrastructure market. This hardware reference design leverages the real time signal processing of the TI DSP, the TI ADC, and the TI DAC. This design offers SDR algorithm developers a platform to enable quick development and demonstration of algorithms and solutions.

2 System Description

Features

- A High Performance MityDSP-L138F CPU
 - TI OMAP™-L138
 - Xilinx Spartan® 6 FPGA
- Linux™ and HMI (Qt)

Expansion

- UART Header (RS232 or RS485)
- WQVGA LCD Interface
- 4 Status LEDs
- 4-Pin GPIO Header

Digital Interfaces

- DVI Video Output
- 10/100 Mbit Ethernet Interface
- Audio Output
- USB Host and OTG
- CAN Bus Interface
- SD/MMC Card Socket

Digital Interfaces

- AC to DC 12-V Adapter
- Ethernet and Serial Cables

3 System Description

Critical Link chose its MityDSP-L138F system-on-module (SOM) as the basis for the SDR because of its processing-horsepower capabilities. These capabilities can save the customer a significant amount of up-front design cost. The MityDSP-L138F module features a TI OMAP-L138 DSP+ARM® processor, which integrated a 456-MHz ARM9™ processing core and a 456-MHz TMS320C674x DSP core. The module also includes a Xilinx Spartan-6 LX16 FPGA, NAND and NOR flash, and DDR2 memory.

For radio front end functionality, we used TI's evaluation kits for the high-speed ADC and DAC for the radio. The design requires data converters capable of converting at 60-MHz sample frequency. For the A/D converter, we selected TI's ADS5562, which converts at 80 Msps with 16 bits of precision. Because spread-spectrum radios must pull signals out of the background noise, high dynamic-range is important for this radio.

For the DAC, we selected TI's THS5671. The THS5671 is a 14-bit, 125-Msps differential current output DAC.

This SDR reference design includes the hardware design files for the Industrial I/O, the ADC and DAC, and links to the Critical Link MityDSP SOM, tools, and sample uPP FPGA and DSP software.

4 Block Diagram

For the key components and interfaces for the SDR reference platform, see [Figure 1](#).

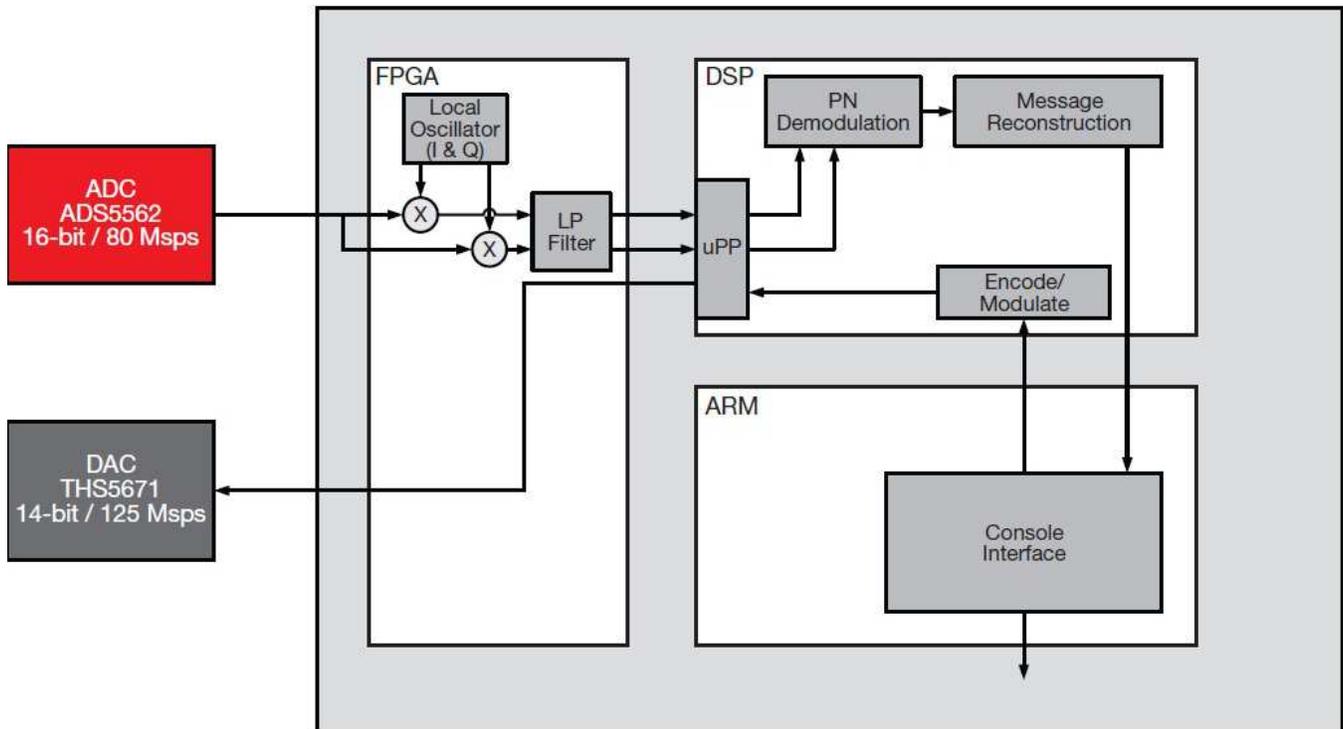


Figure 1. System Block Diagram for FPGA / DSP /ARM

4.1 System Overview

4.1.1 The Data Movement Problem

Many DSP-based applications require high-speed data transfers to let the system acquire and process data or transmit data to an external device. Typical digital signal processors include an asynchronous address or data bus to let the processor read and write to external devices. These interfaces are often move data at low rates but can slow at high speeds. The OMAP-L138 DSP+ARM processor has an address or data bus called the external

Memory Interface A (EMIFA) addresses external memory or devices asynchronously and includes several control pins for varying wait-states, transfer widths, and so forth. Because this interface has a general purpose, each transaction can take multiple clock cycles to complete. The minimum read cycle requires three cycles per 16 bits. Running the EMIFA at 100 MHz, expect a data transfer rate of 66 MBytes/s maximum. Interleaving reads and writes on the bus significantly reduces the data transfer rate because you must add additional turnaround cycles.

The OMAP-L138 processor also includes a more dedicated interface, the universal parallel port (uPP). This interface moves large amounts of data continuously in or out of the memory of the processor. The uPP can clock one data word (8 or 16 bits) per clock cycle (or two per clock for double-data-rate but the clock speed must be half as fast). The uPP clock rate can be no more than half of the processor clock rate. For an OMAP-L138 processor running at 300 MHz, the uPP clock can be as great as 75 MHz, which allows a throughput of a 150 MBytes/s maximum.

The OMAP-L138 processor includes two uPP interfaces you can configure independently. For the SDR application, this capability let us set up one port for transmit and one for receive. This capability removes the contention that would exist on a single bus.

Relating to hardware, the uPP interface is a simple synchronous data interface. The interface includes a clock pin, data pins, and several control pins that indicate valid data and start/wait conditions. You can use the interface with some parallel ADCs and DACs without glue.

4.1.2 The Architecture

Because our SDR requires high-speed data movement to and from the DSP, we implemented the FPGA interface using the uPP ports. We used one port for the transmit side of the interface and one for the receive side. The processing system transmits and receives simultaneously though this feature. This capability let us test and debug by looping the transmitter to the receiver.

For a 10-MHz carrier, the OMAP-L138 processor cannot handle all the processing in the DSP due to the nature of the processing for this type of modulation. For slower applications, the DSP can handle the data rate. Because the customer required the capability to send data at the higher rate, we used the FPGA for some processing tasks.

The FPGA can perform at repetitive tasks well at very high frequencies, so we chose to do the initial demodulation and base-banding process in the FPGA. This choice decimates the data and reduces the data rate to the DSP. When transmitting, the DSP can precompute the final RF signal, so that encoding the payload data takes an inconsequential time. For this reason, the FPGA merely passes the transmit waveform data from the uPP port to the DAC.

The FPGA includes a sine and cosine lookup table in dual-ported RAM, which synthesizes the local oscillator signals for the receiver. Multipliers and accumulators in the FPGA demodulate the signals.

4.1.3 Transmit Processing Chain

The transmit process starts when the software on the ARM microprocessor sends a message packet to the DSP for transmission. The DSP encodes this data into a spread-spectrum modulation sequence and indexes into a precomputed, modulated, sine-wave look-up table. The DSP uses the built-in DMA engine of the uPP to set up the DMA to transfer the data from the DSP memory into the DAC. The FPGA acts as the intermediary, providing a programmable clock to the DAC and uPP to set the transmit sample rate.

4.1.4 Receive Processing Chain

The receive process runs continuously. ADC samples are clocked into the FPGA. In the FPGA, the data is base-banded by multiplying the input samples by quadrature sine and cosine waveforms and integrating to provide in-phase and quadrature samples at a reduced data rate to the DSP. These samples are DMAed into the DSP memory by the uPP DMA engine, where the DSP performs the remaining processing steps for the spread-spectrum demodulation. When the signal is demodulated, the data packet transfers to the ARM processor using TI's DSPLink interprocessor communications library. The ARM software receives the decoded data and presents it to you through the command interface.

The FPGA performs the initial base-banding for the receiver. This action relieves the DSP of enough processing to easily do the remaining demodulation and decoding. If the sample rate of the input signal is significantly lower than the 60 MHz in this system, the DSP can do the base-banding without help from the FPGA.

We used a carrier frequency in the LF band (tens or hundreds of kHz) with this system initially. The FPGA in this initial implementation passed data through to the DSP. The DSP performed the demodulation functions. Though this setup worked well, it was insufficient for applications that require higher sample rates. By base-banding in the FPGA, we can base-band and filter digitally at the full sample rate, which improves the noise performance of the system which is impossible by only under-sampling.

5 Summary

This project resulted in a prototype system used as a proof-of-concept for several applications. The performance of the system is good when compared to the theoretical performance of an ideal spread-spectrum radio. The combination of TI's OMAP-L138 DSP+ARM processor and the FPGA offer a cost-effective solution with outstanding performance. Offloading processing from the DSP to the FPGA let you build the system using a low-cost, low-power processor (rather than requiring a GHz-class DSP to do all the processing). The uPP interface offers simple FPGA interfacing and significant performance advantages to other interfaces on the DSP. By relieving the DSP of data movement by using the DMA in the uPP, DSP cycles are available for more important work. The addition of the ARM processor in the OMAP-L1x platform lets the embedded Linux to provide the communications infrastructure to manage the interface and all housekeeping functions in the system. The system software (ARM, DSP and FPGA) can be field-upgraded using an SD card, a USB drive or an Ethernet connection. The SDR system can remain fully leveraged as processing algorithms evolve.

6 Hardware Design Information

Figure 1 shows that this SDR kit is comprised of three different printed circuit boards (PCB).

You can find design document on each of these boards at the following links:

File Description	File Type	File Location
MityDSP-L138F	Datasheet	http://www.criticallink.com/product/mitydsp-l138f/
Industrial IO	Datasheet	http://www.criticallink.com/product/mitydsp-l138f-dev-kit/
Industrial IO	Schematic	http://www.ti.com/tool/TIDEP0040
Industrial IO	Bill of Materials	http://www.ti.com/tool/TIDEP0040
Industrial IO	Gerbers	http://www.ti.com/tool/TIDEP0040
ADS5562	Schematic	www.ti.com/tool/ADS5562EVM
ADS5562	Bill of Materials	www.ti.com/tool/ADS5562EVM
ADS5562	Gerbers	www.ti.com/tool/ADS5562EVM
THS5671	Schematic	www.ti.com/tool/THS5671EVM
THS5671	Bill of Materials	www.ti.com/tool/THS5671EVM
THS5671	Gerbers	www.ti.com/tool/THS5671EVM

6 Development Tools

This SDR reference platform leverages existing development tools from Xilinx and TI that fit seamlessly within the standard development environment. The development tools are available at the following web link and are summarized below:

- [MityDSPOMAP-L138 Family](#)
- [MityDSP-L138F](#)
- [OMAP-L138 Processor](#)

You can find sample uPP FPGA code at the following link:

https://support.criticallink.com/redmine/projects/indio/wiki/Vision_Framework_Kit

You can find a sample DSP-based uPP device driver at the following link:

[CriticalLink uPP Device Driver](#)

You can find information on MityDSP-L138 topics at the following link:

<http://support.criticallink.com/redmine/projects/arm9-platforms/wiki>

Table 1. Summary of Development Tools

Component	Development Tools	Version	Tool Location
FPGA	Xilinx ISE Webpack Version 13 or Higher	13 or Higher	http://support.criticalink.com/retrieve/projects/arm9-platforms/wiki/FPGA_Development_Tools
	JTAG Programming Cable		http://support.criticalink.com/retrieve/projects/arm9-platforms/wiki/FPGA_Development_Tools
DSP	TI Code Composer (CCS)	5.2 or Higher	http://processors.wiki.ti.com/index.php/Download_CCS
	Spectrum Digital JTAG Emulator	XDS510 Preferred	http://support.criticalink.com/retrieve/projects/arm9-platforms/wiki/DSP_Development_Tools
ARM	Eclipse IDE	Provided with CCS	http://support.criticalink.com/retrieve/projects/arm9-platforms/wiki
	GCC tool chain	Nov 2010	http://support.criticalink.com/retrieve/projects/arm9-platforms/wiki/GCC_Toolchain

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Company Overview

Critical Link is an embedded systems firm specializing in developing electronics for the scientific, industrial, communications, and transportation industries. The business is built around working with industry innovators bringing new products to market, and around leading-edge digital processing platforms. Critical Link's robust methodology, framework of designs, pre-engineered interface cores, device support, and tools help customers bring their applications to market more cost effectively, more rapidly, and with higher quality than if they build from the ground up.

Solutions

MitySOM/MityDSP provides an all-in-one solution for your instrumentation, data collection, and control needs. A product development and production system, MitySOM/MityDSP provides a production-ready core CPU platform that can be quickly and easily customized to meet your specific product requirements through configurable input and output interfaces. The MitySOM/MityDSP includes both hardware and software components that integrate seamlessly into your application, providing a fully customized embedded design that both reduces project technical risk and shortens development cycles and cost.

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