PMP9365 Test Report

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1) Block Diagram

Stratix® V FPGA Power Reference Design

Figure 1. Block Diagram
2) Board Photos

Figure 2. Board Photo Top

Figure 3. Board Photo Bottom

3) Startup Waveforms
Two LM3880's are used for power sequencing as shown in figures 4, 5, and 6. The power up sequence is in the following order: VCC, VCCPD, VCCA_GXB/GTB, VCCT_, VCCIO.

Figure 4. Startup Waveform
Figure 5. Startup Waveform

Ch.1: VIN
Ch.2: VCCPD
Ch.3: VCCA_GXB/GTB
Ch.4: VCCT_
Ch.1: VIN
Ch.2: VCCIO 2.5V
Ch.3: VCCIO_1.8V
Ch.4: VCCIO_1.5V

Figure 6. Startup Waveform

4) Efficiency
The efficiency of the converters is shown in the figures below. The input voltage is set to 12V.
Figure 7. VIN = 12V, VCC Efficiency
Figure 8. VIN = 12V, VCCPD Efficiency
Figure 9. VIN = 12V, VCCA_GXB/GTB Efficiency
Figure 10. VIN = 12V, VCCT Efficiency
Figure 11. VIN = 12V, VCCIO 2.5V Efficiency
Figure 12. VIN = 12V, VCCIO 1.8V Efficiency
5) **Load Regulation**

The images below show the output load regulation. The input voltage is 12V.
Figure 14. VIN = 12V, VCC Load Regulation
Figure 15. VIN = 12V, VCCPD Load Regulation
Figure 16. VIN = 12V, VCCA_GXB/GTB Load Regulation
Figure 17. VIN = 12V, VCCT_ Load Regulation
Figure 18. VIN = 12V, VCCIO 2.5V Load Regulation
Figure 19. VIN = 12V, VCCIO 1.8V Load Regulation
Figure 20. VIN = 12V, VCCIO 1.5V Load Regulation
6) Output Voltage Ripple

The images below shows the output voltage ripple when load is fully applied. The input voltage is 12V.

Figure 21. VIN = 12V, VCC Output Ripple @ IOUT = 20A
Figure 22. VIN = 12V, VCCPD Output Ripple @ IOUT = 3A
Figure 23. VIN = 12V, VCCA_GXB/GTB Output Ripple @ IOUT = 2.2A
Figure 24. VIN = 12V, VCCT Output Ripple @ IOUT = 3A
Figure 25. VIN = 12V, VCCIO 2.5V Output Ripple @ IOUT = 3A
Figure 26. VIN = 12V, VCCIO 1.8V Output Ripple @ IOUT = 3A
Figure 27. VIN = 12V, VCCIO 1.5V Output Ripple @ IOUT = 4A
7) Load Transients

The transient response of the converters is shown below. The input voltage is 12V. The output current is pulsed from 0 to 50% load.

Figure 28. VIN = 12V, VCC Load Transient
Figure 29. VIN = 12V, VCCPD Load Transient
Figure 30. \( \text{VIN} = 12\text{V}, \text{VCCA\_GXB/GTB Load Transient} \)
Figure 31. VIN = 12V, VCCT_Load Transient
Figure 32. VIN = 12V, VCCIO 2.5V Load Transient
Figure 33. VIN = 12V, VCCIO 1.8V Load Transient
8) **Thermal Image**
Thermal images at full load of each device are shown below, the remaining rails are not drawing any current during these tests. The input voltage is 12V.

Figure 34. VIN = 12V, VCCIO 1.5V Load Transient
Figure 35. VIN = 12V, VCC Thermal Image @ Full Load
Figure 36. VIN = 12V, VCCPD Thermal Image @ Full Load
Figure 37. VIN = 12V, VCCA_GXB/GTB Thermal Image @ Full Load
Figure 38. VIN = 12V, VCCT_ Thermal Image @ Full Load
Figure 39. VIN = 12V, VCCIO 2.5V Thermal Image @ Full Load
Figure 40. VIN = 12V, VCCIO 1.8V Thermal Image @ Full Load
Figure 4. VIN = 12V, VCCIO 1.5V Thermal Image @ Full Load
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