Technical Conference Oct 2011

Using Active Clamp Technology to Maximize Efficiency in a Telecom Bus Converter

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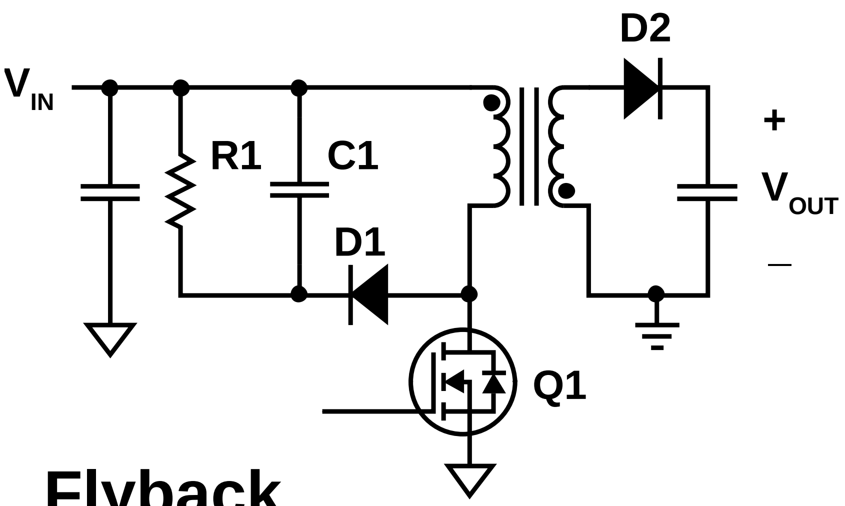
Agenda

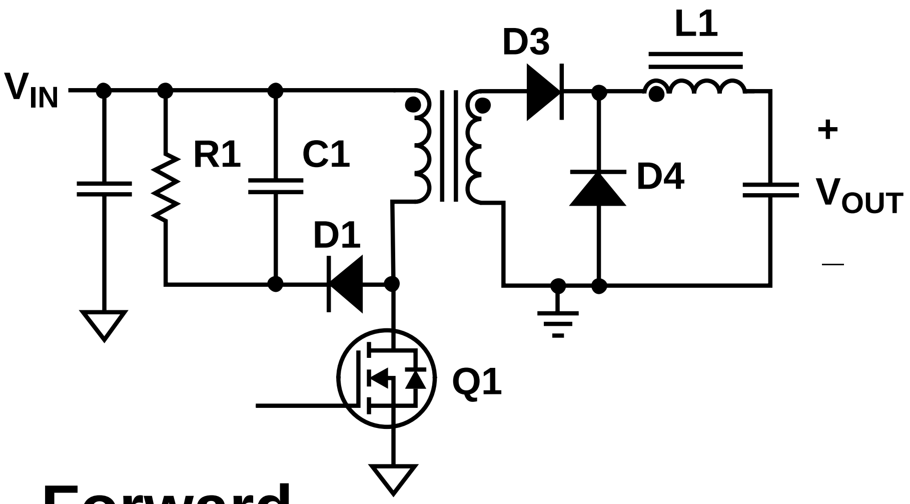
1. **Basic Operation of Flyback and Forward Converters**
2. Active Clamp Operation and Benefits
3. Active Clamp Forward Design
4. Design Review PMP5711

Basic Power Stages



Flyback

- Transformer stores energy
- R1 dissipates leakage and some magnetizing energy
  - Typically 2 to 5% of output power

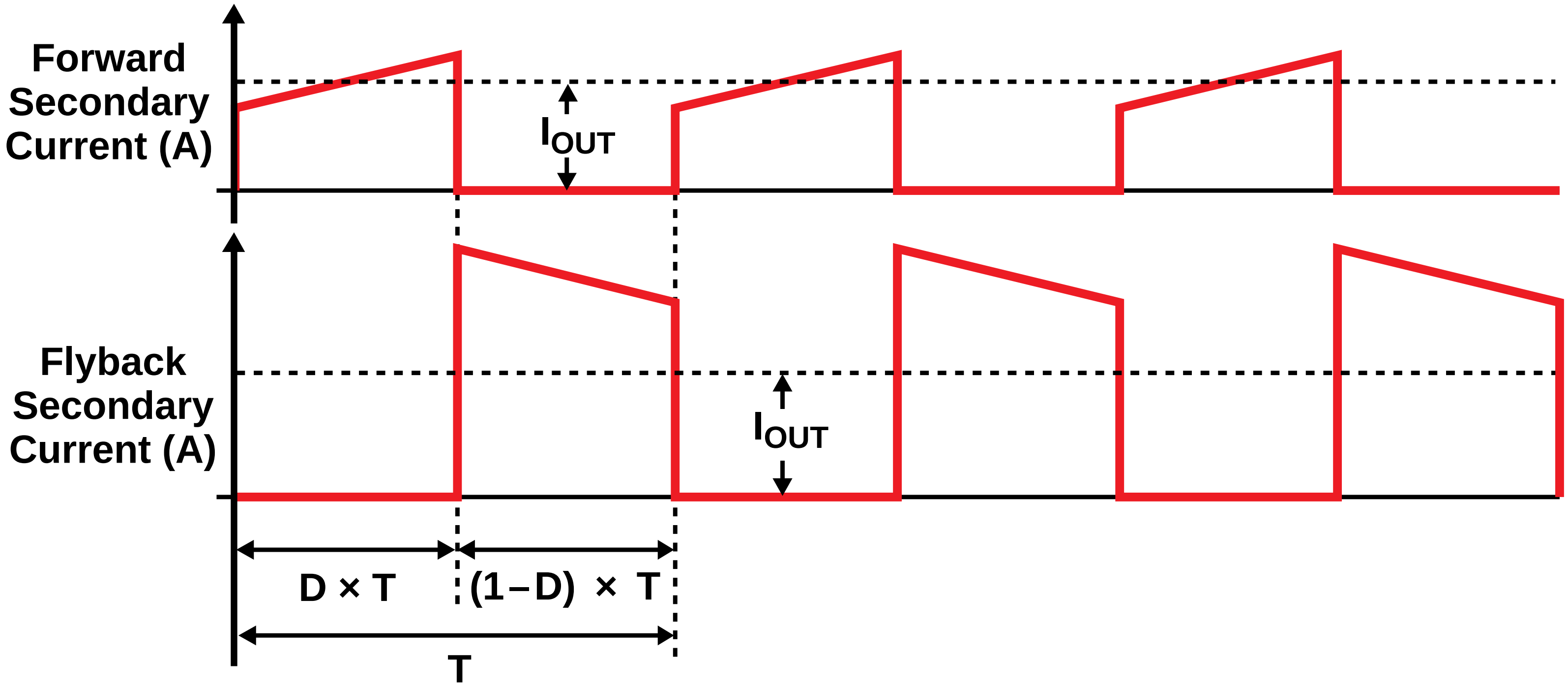


Forward

- Transformer transfers energy
  - Storage is in L1
- R1 dissipates magnetizing plus leakage energy
  - Typically 3 to10% of output power

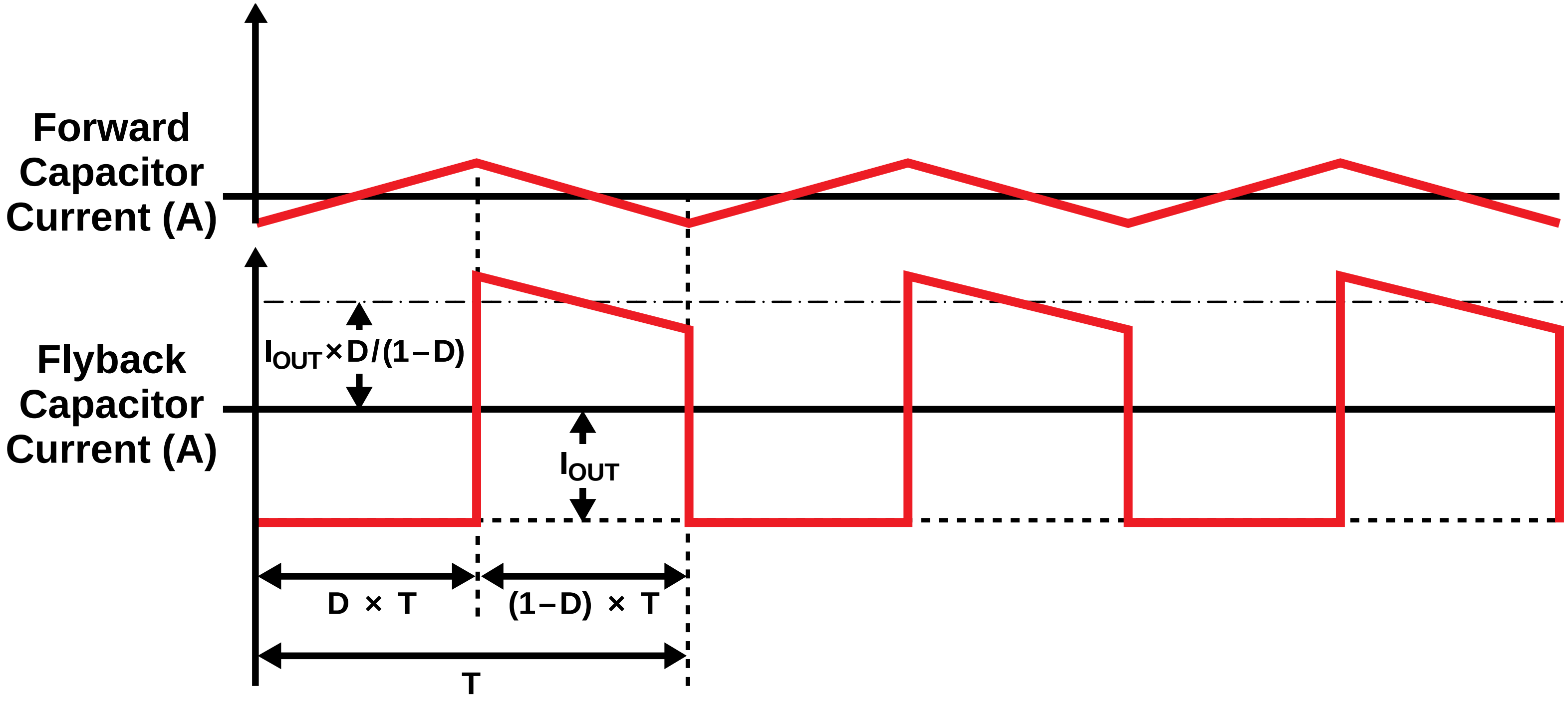
How can we avoid loss in R1?

Secondary Winding Currents



- Assuming 50% duty cycle and CCM
  - Synchronous rectifiers force CCM
- RMS flyback current = 2 X RMS forward current
- For low voltage/high current output, forward is best choice

Output Capacitor Currents



- Flyback output capacitors see much higher current
  - – Higher RMS current increases heating
  - – Higher peak current requires much lower ESR
- Result is more, higher quality capacitors in flyback

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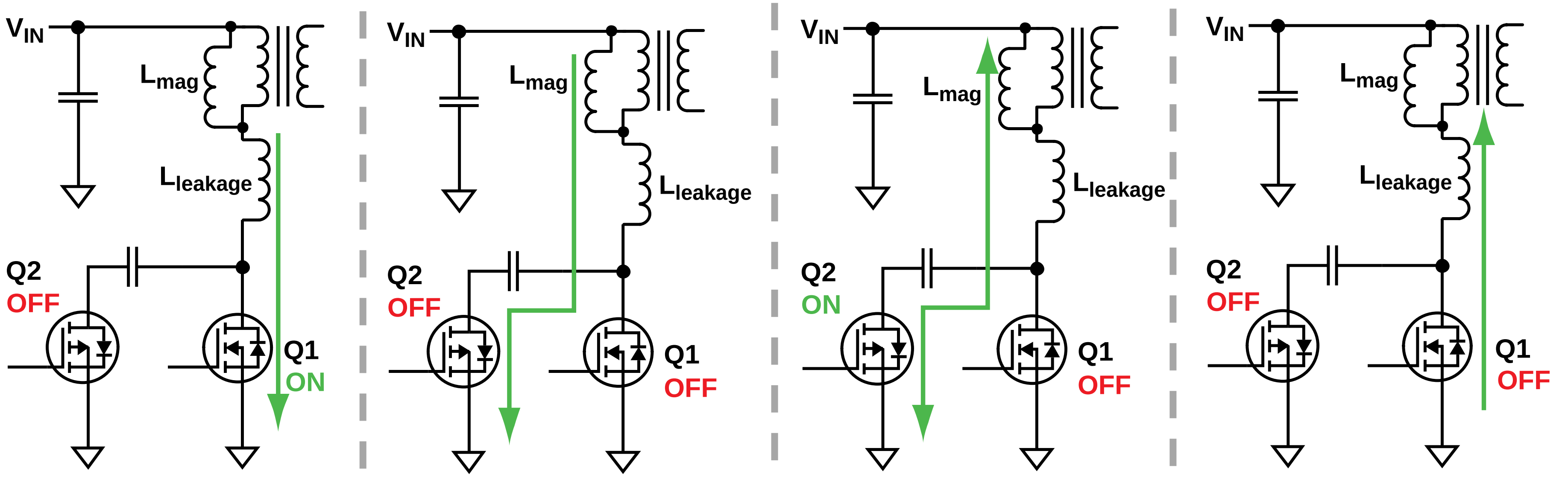
Active Clamp Operation

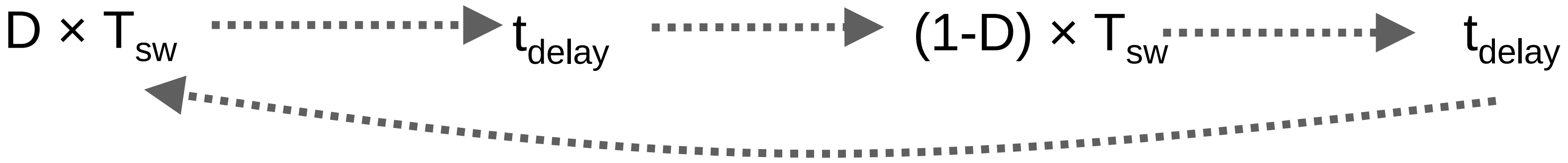


L_{mag} and $L_{leakage}$ are energized

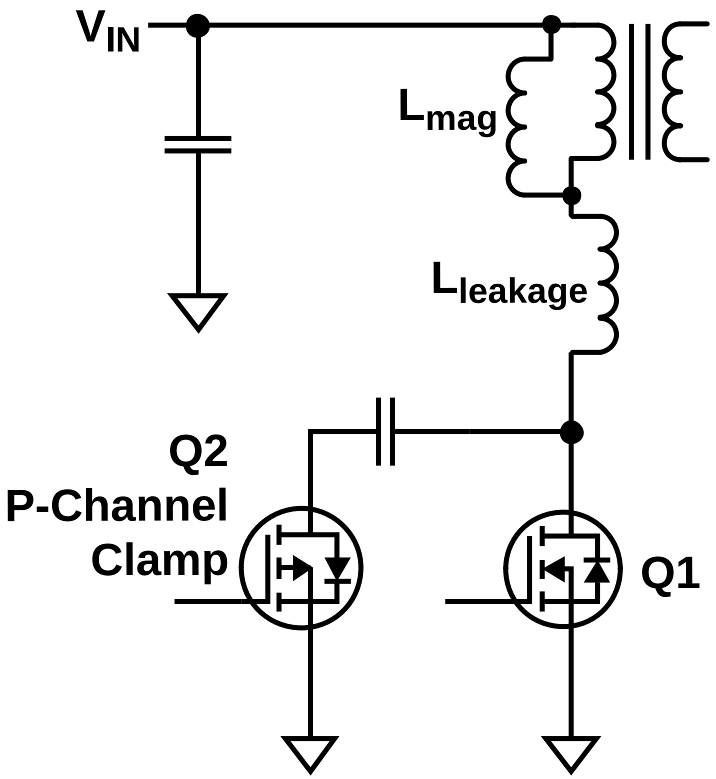
Current commutes to Q2 body diode

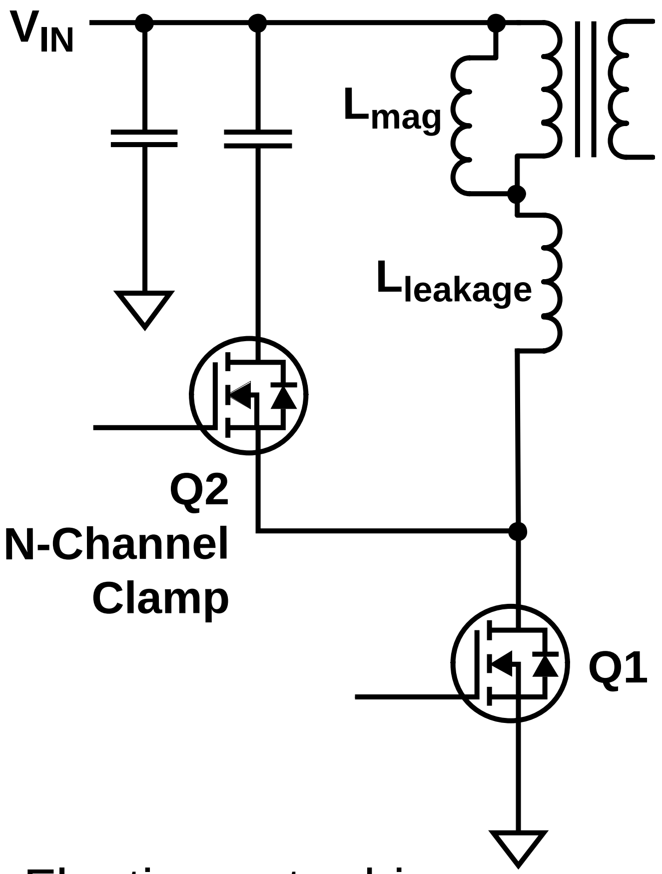
Current resonates, changes direction

Current commutes to Q1 body diode or C_{oss}



Active Clamp Configurations





+ Easy to drive clamp FET

\- Higher capacitor voltage

\- P-channel FET

\- Floating gate drive

+ Lower capacitor voltage

+ N-channel FET

Active Clamp Benefits

RCD Clamp	Active Clamp
• Most of leakage energy is dissipated as heat	• Most of leakage energy is reclaimed
• “Hard” switching results in power losses	• Zero voltage switching reduces losses
• More difficult implementation of self-driven synchronous rectifiers with Forward	• Simple Implementation of self-driven synchronous rectifiers with forward
• Voltage spike on Q1 drain at turn off can be EMI issue	• No voltage spike on Q1 drain at turn off
	• Nearly lossless recovery of magnetizing energy in forward

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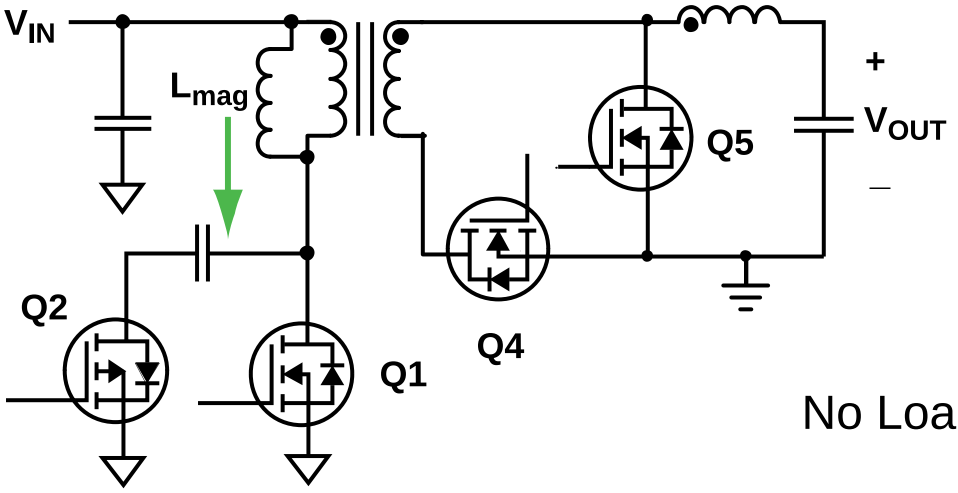
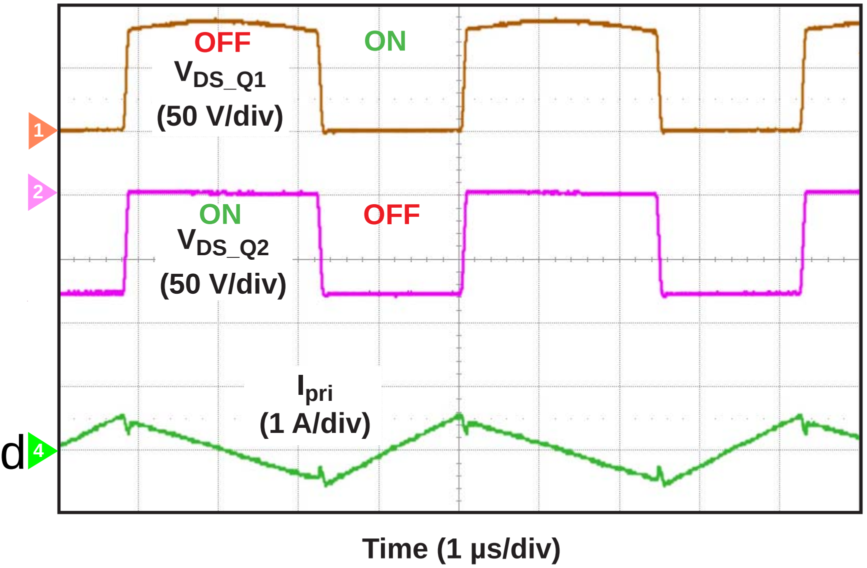
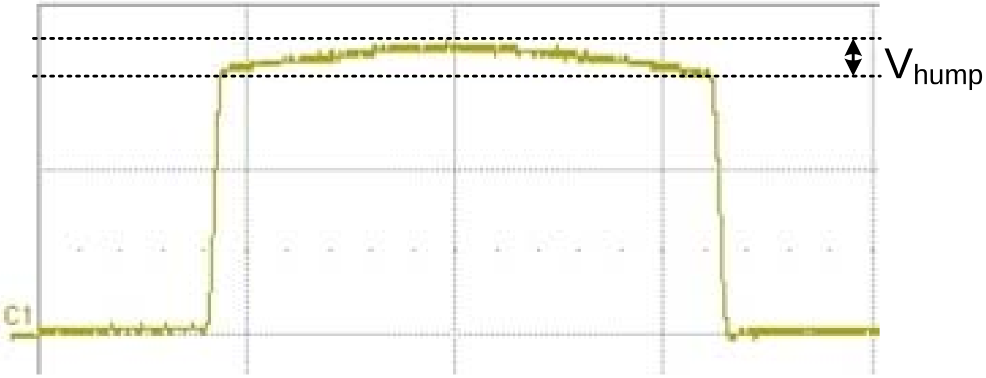
Active Clamp Forward Design





- Reflected primary voltage during reset time allows self driven sync rectifiers
- No leakage spike at Q1 turn off
- Primary current resets to third quadrant resulting in better core utilization
- Unlike flyback, clamp resonant frequency is determined by magnetizing inductance and C_{clamp}

Forward Clamp Circuit



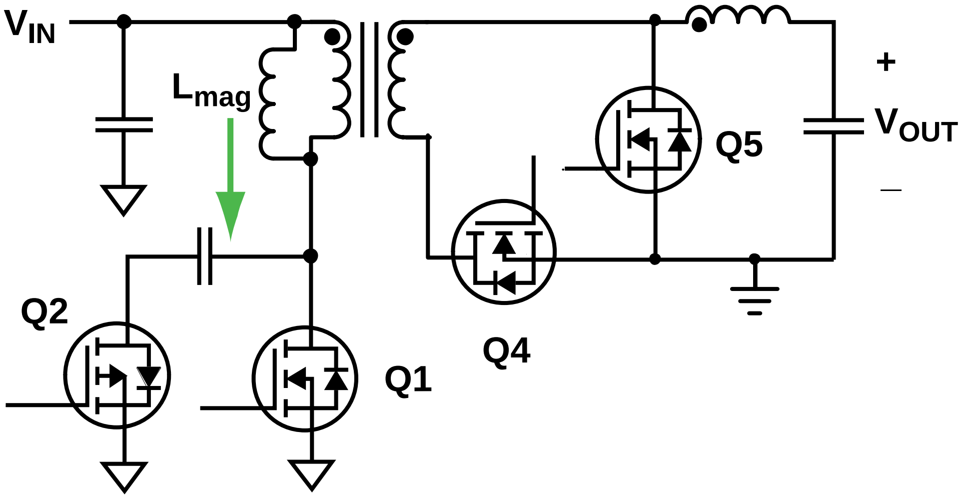
$$f_{clamp} = \frac{1}{2 \times \pi \times \sqrt{L_{magnetizing} \times C_{clamp}}}$$

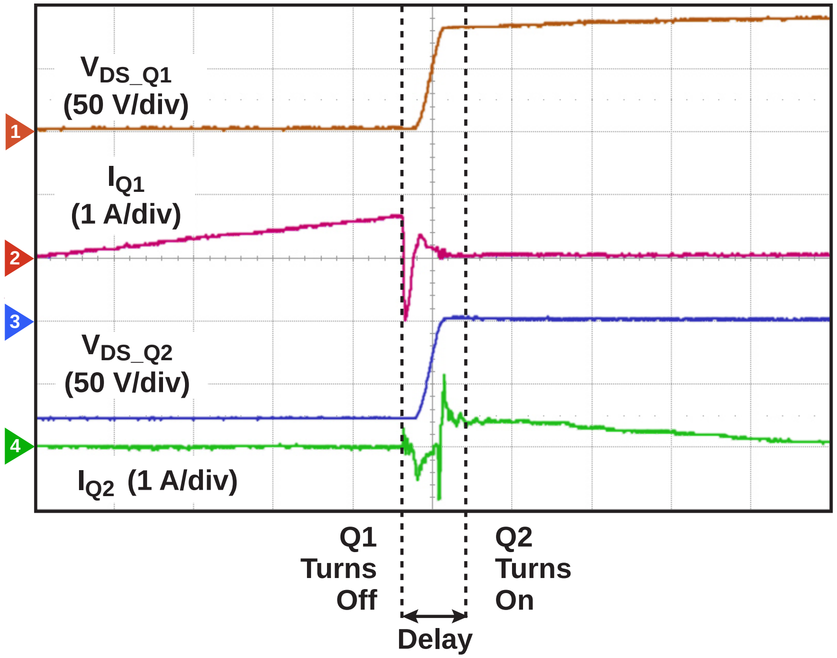
$$V_{hump} = \frac{V_{in} \times D \times (1 - D)}{8 \times L_{magnetizing} \times f_{SW}^{2} \times C_{clamp}}$$

$$I_{Q2\_RMS} = \frac{V_{in} \times D \times \sqrt{1 - D}}{2 \times \sqrt{3} \times L_{magnetizing} \times f_{sw}}$$

(Peak current is I_{mag};
RMS clamp current is
much less than flyback)

Forward Soft Switching – Q1 Turn-Off

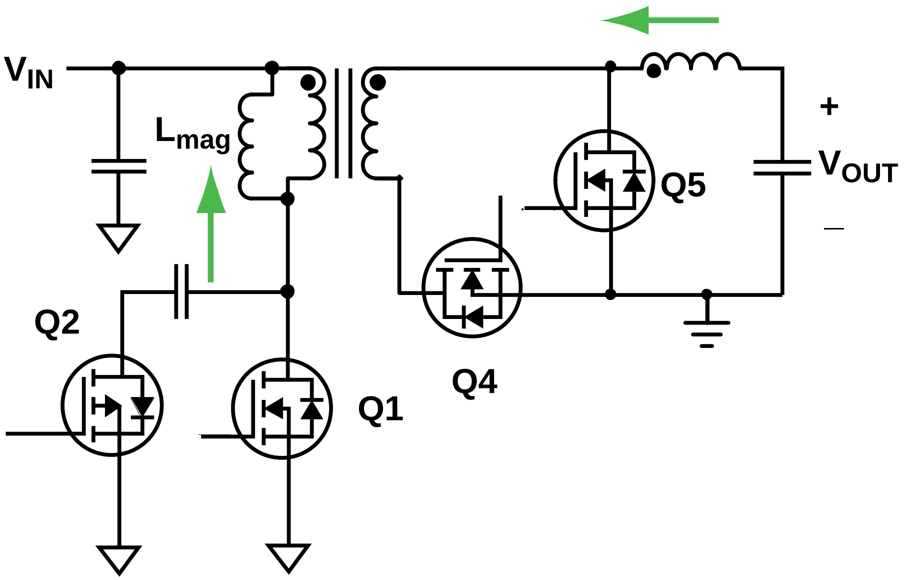


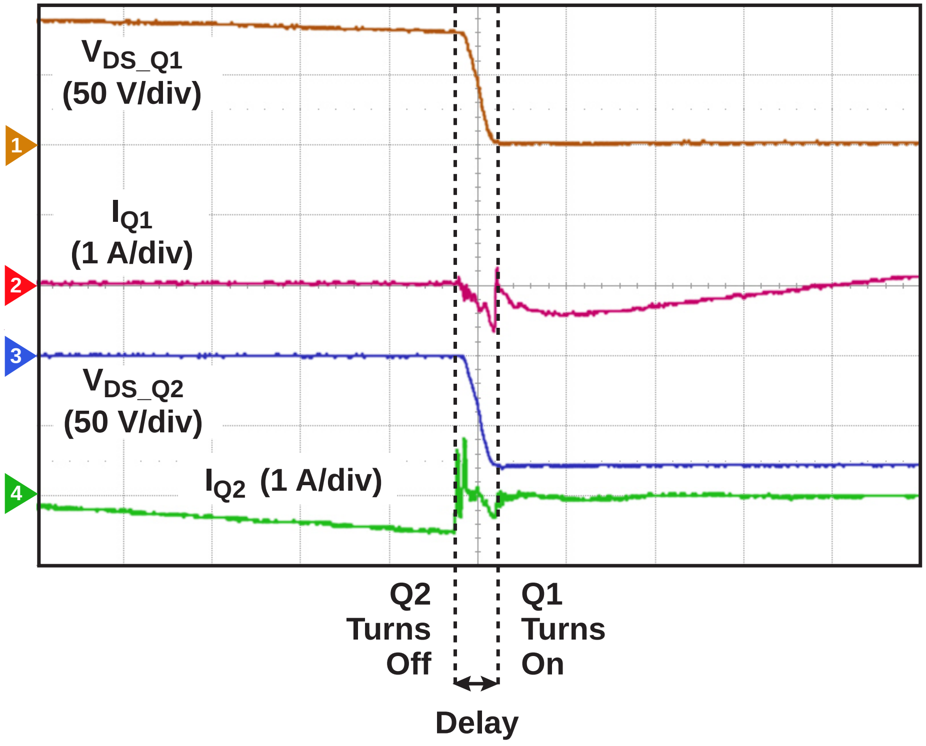


- Magnetizing and reflected load current flowing in Q1
- Transfers to Q2 body diode
  - Delay from Q1 turn-off to Q2 turn-on
- Zero voltage switching of Q2
- Not load or line dependent

Forward Soft Switching – Q1 Turn-On

Light Loads

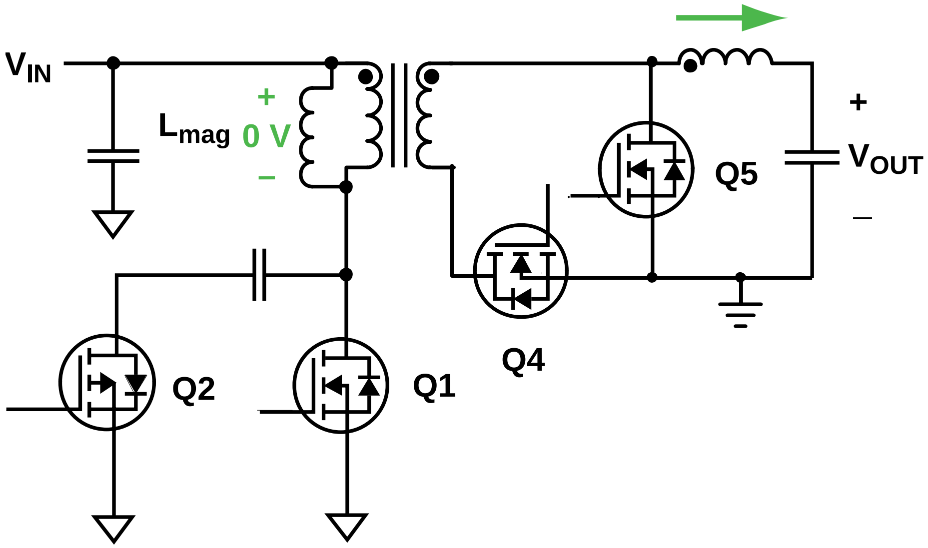


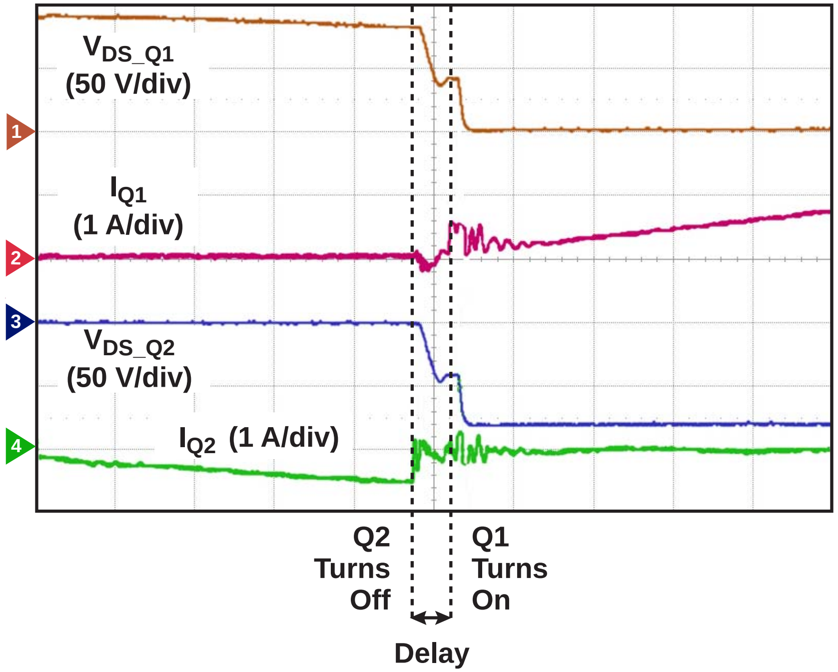


- No current in Q4 or Q5 during delay time
- Allows Q1 to achieve ZVS

Forward Soft Switching – Q1 Turn-On

Heavy Loads



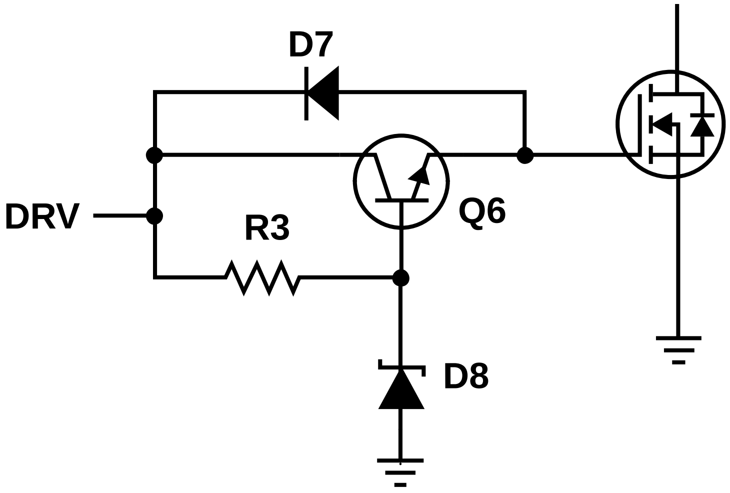


- Current flows in body diodes of Q4 and Q5 during delay time
- Q1 drain voltage = V_{IN} when Q1 turns On
- <u>Partial</u> zero voltage switching

Forward Synchronous Rectifiers

Output Voltage	PRI:SEC Turn Ratio	MAX Sync FET V_{DS} Stress	Sync FET V_{DS} Rating
3.3 V	6:1	12.5 V	20 V
5 V	4.5:1	17 V	30 V
12 V	1.88:1	40 V	60 V

- Turn ratios and voltages for telecom 35- to 75-VDC input
- FET gate rating of 20 V or less
- 3.3-V output can be driven directly from transformer winding
- Outputs >3.3 V require gate protection



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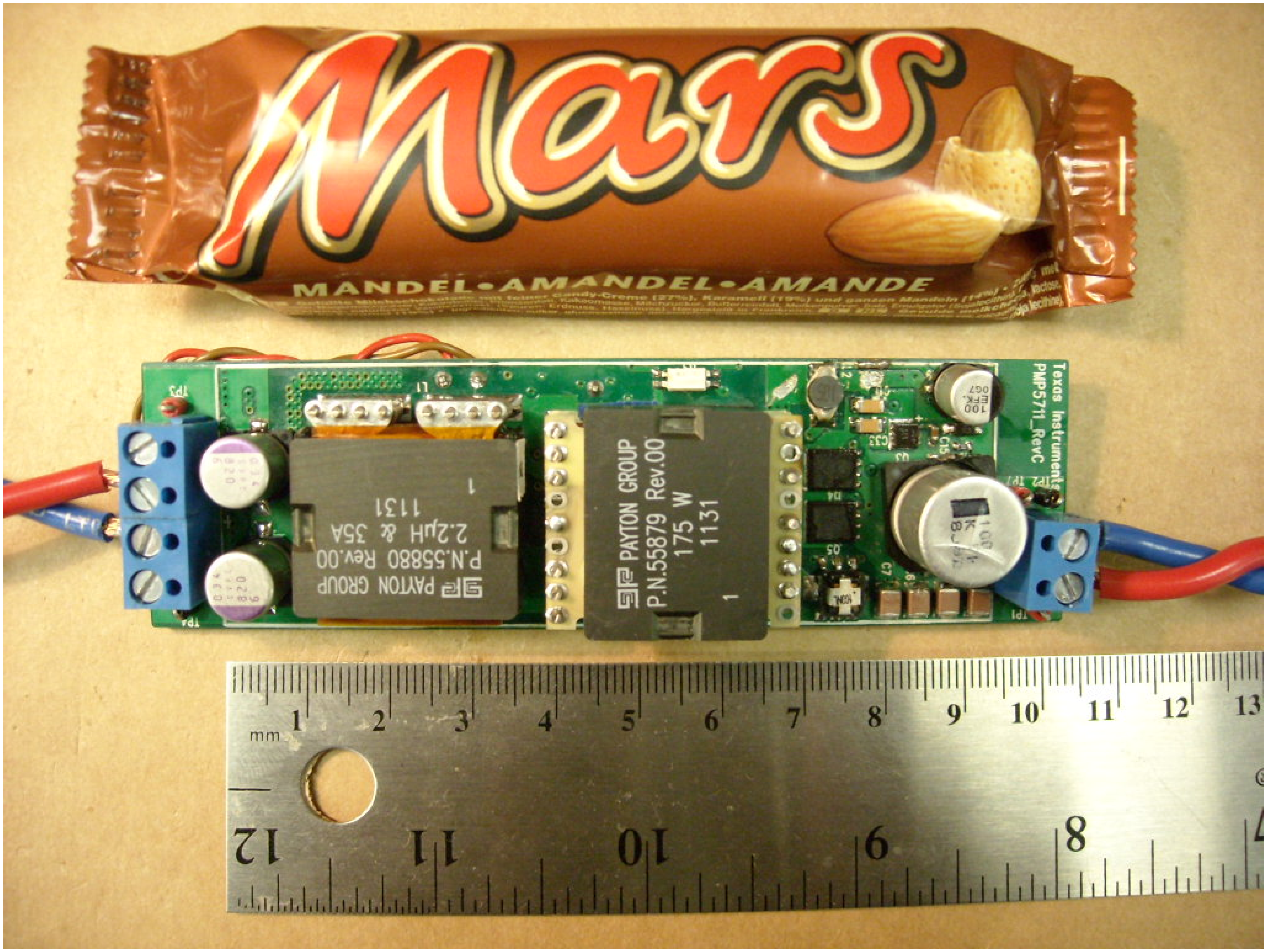
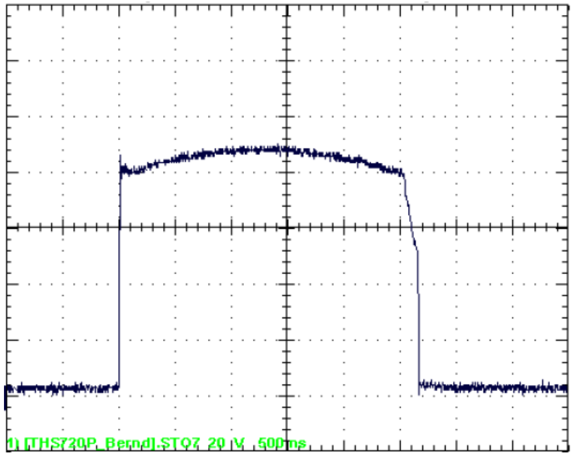
Physical Size – 5.0V/35A Forward Converter

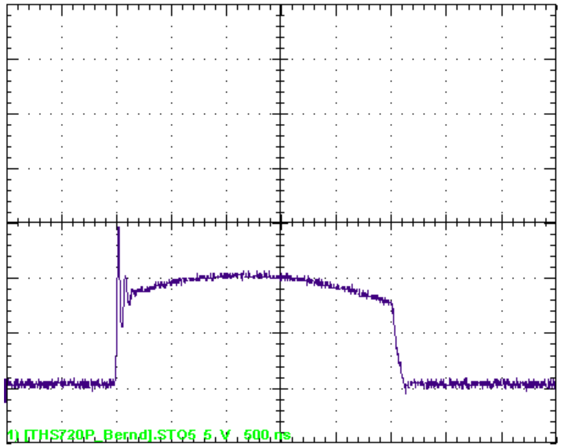


L x W x H = 93mm x 31mm x 19mm

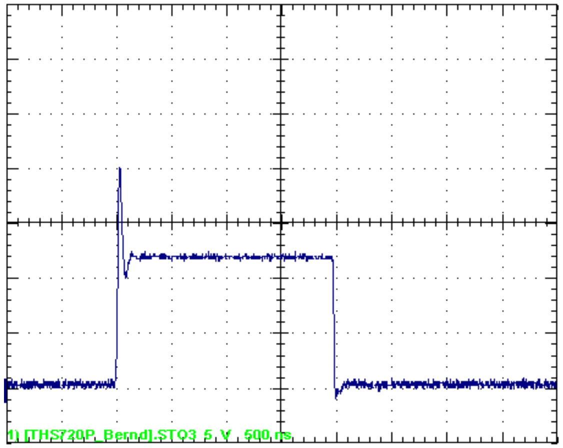
Waveforms – 5.0V/35A Forward Converter



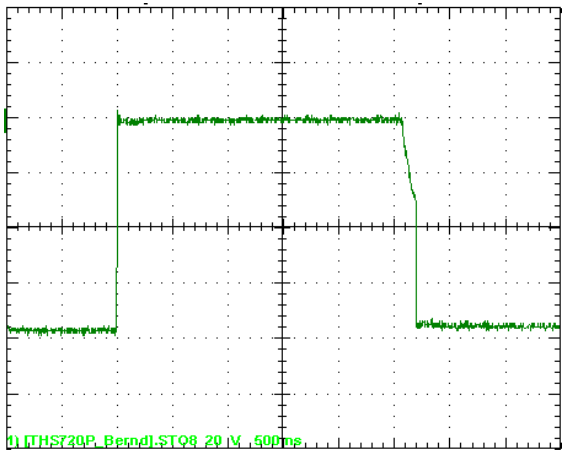
Vds primary NFETs



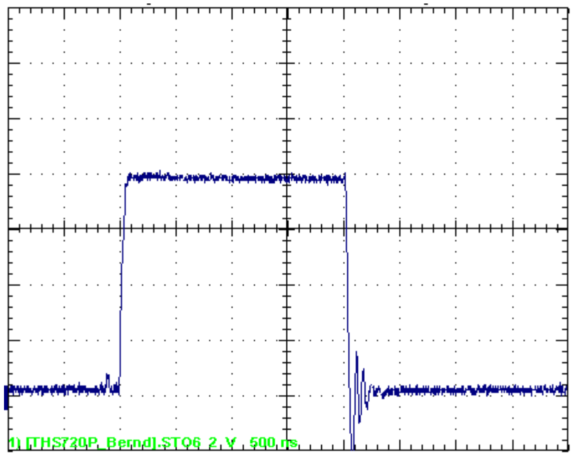
Vds sync. rectifiers



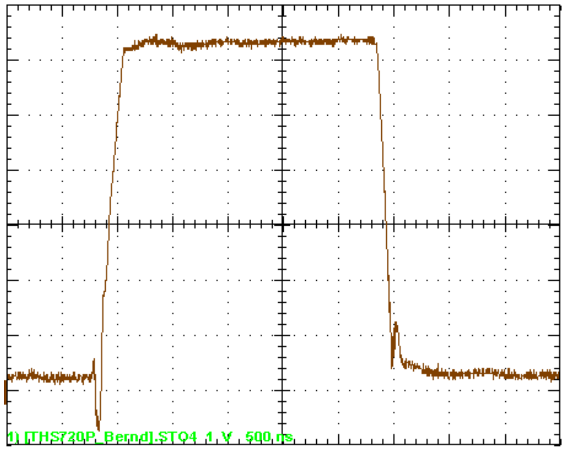
Vds freewheeling FET



Vds clamping PFET

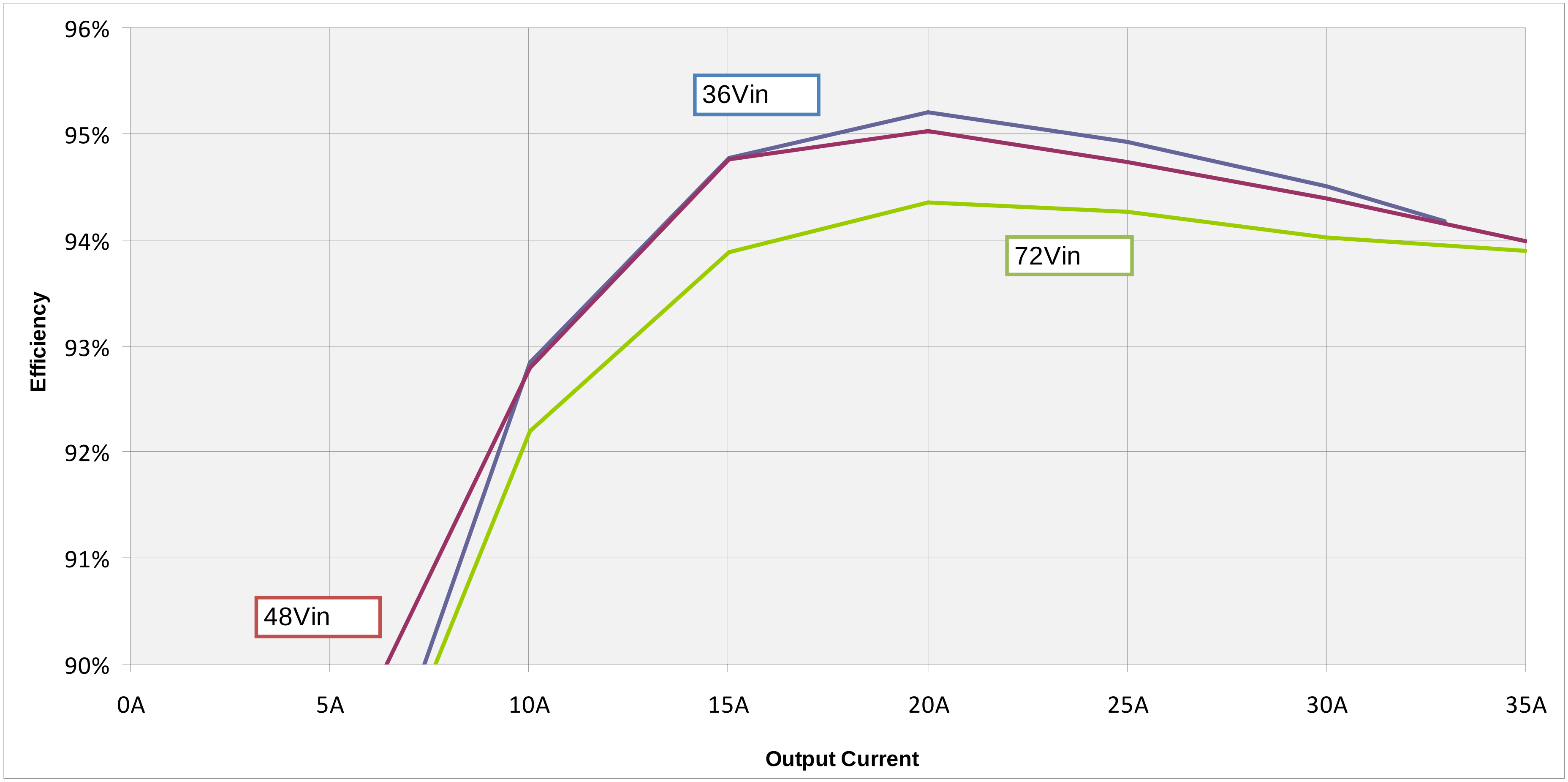


Vgs sync. rectifiers



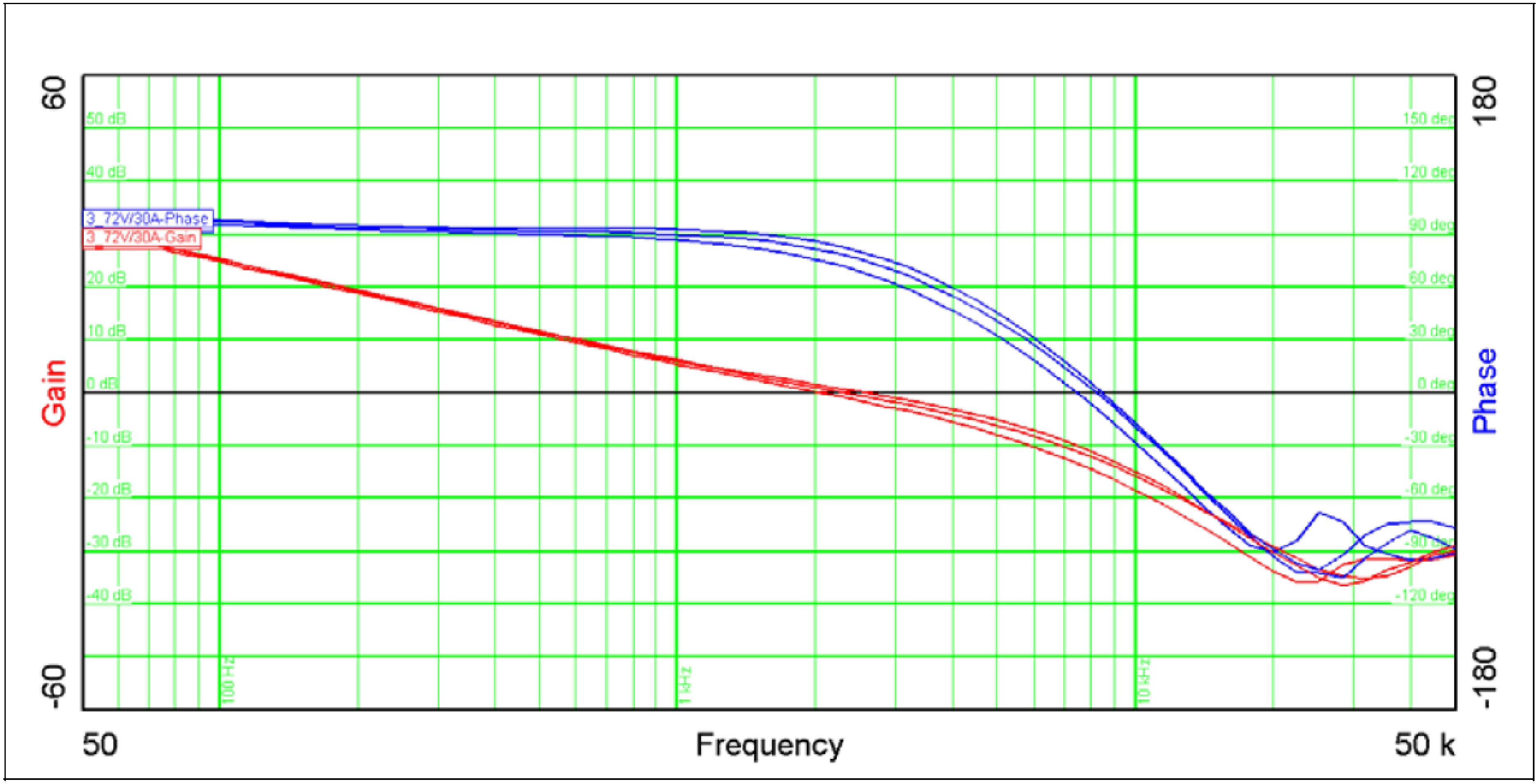
Vgs freewheeling FET

Efficiency – 5.0V/35A Forward Converter



effcy > 94% in a range of 13A to 35A, 95% around 20A

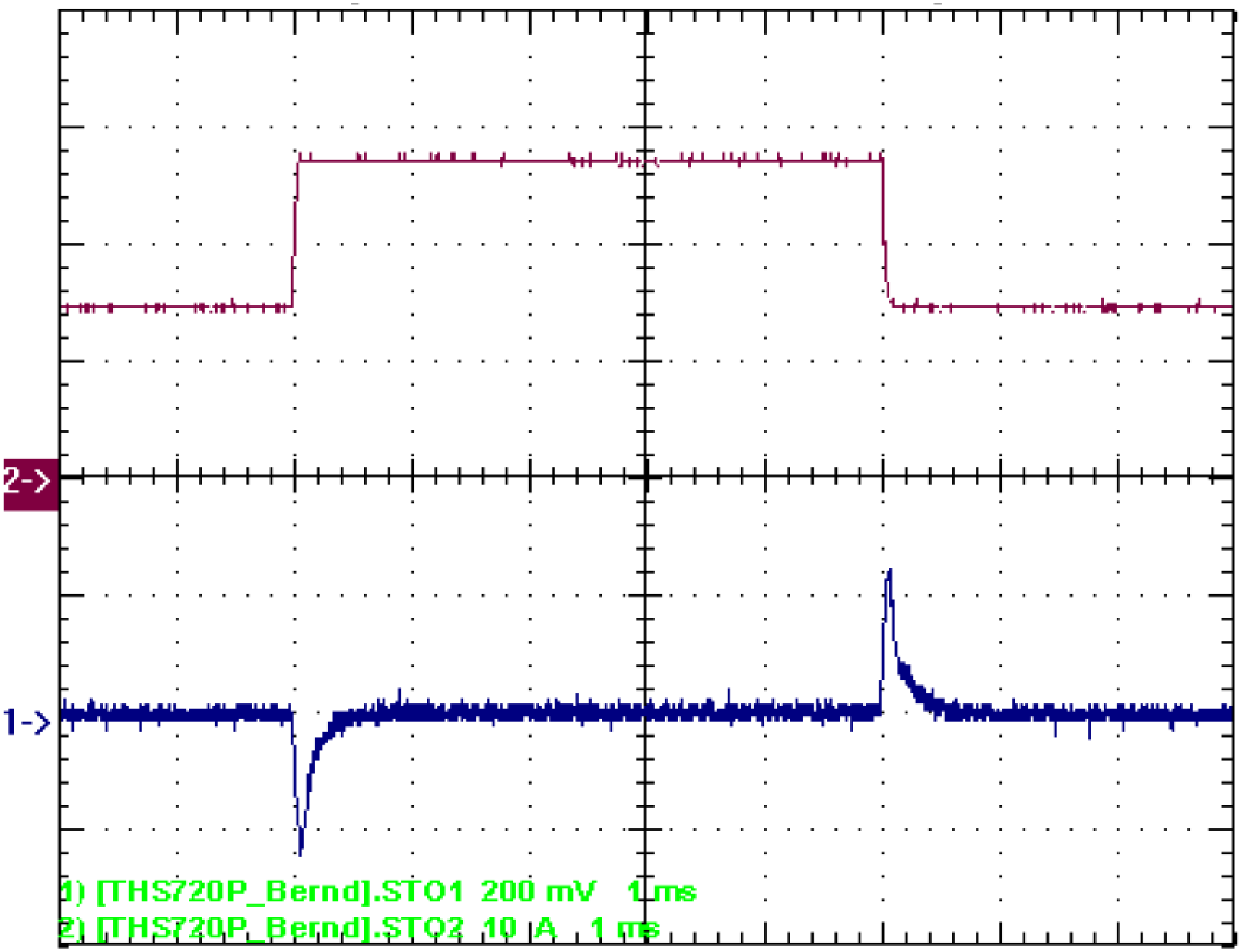
Dynamic Behavior – 5.0V/35A Forward Conv.



small signal analysis of outer loop w/ network analyzer at 30Amps load, results in:

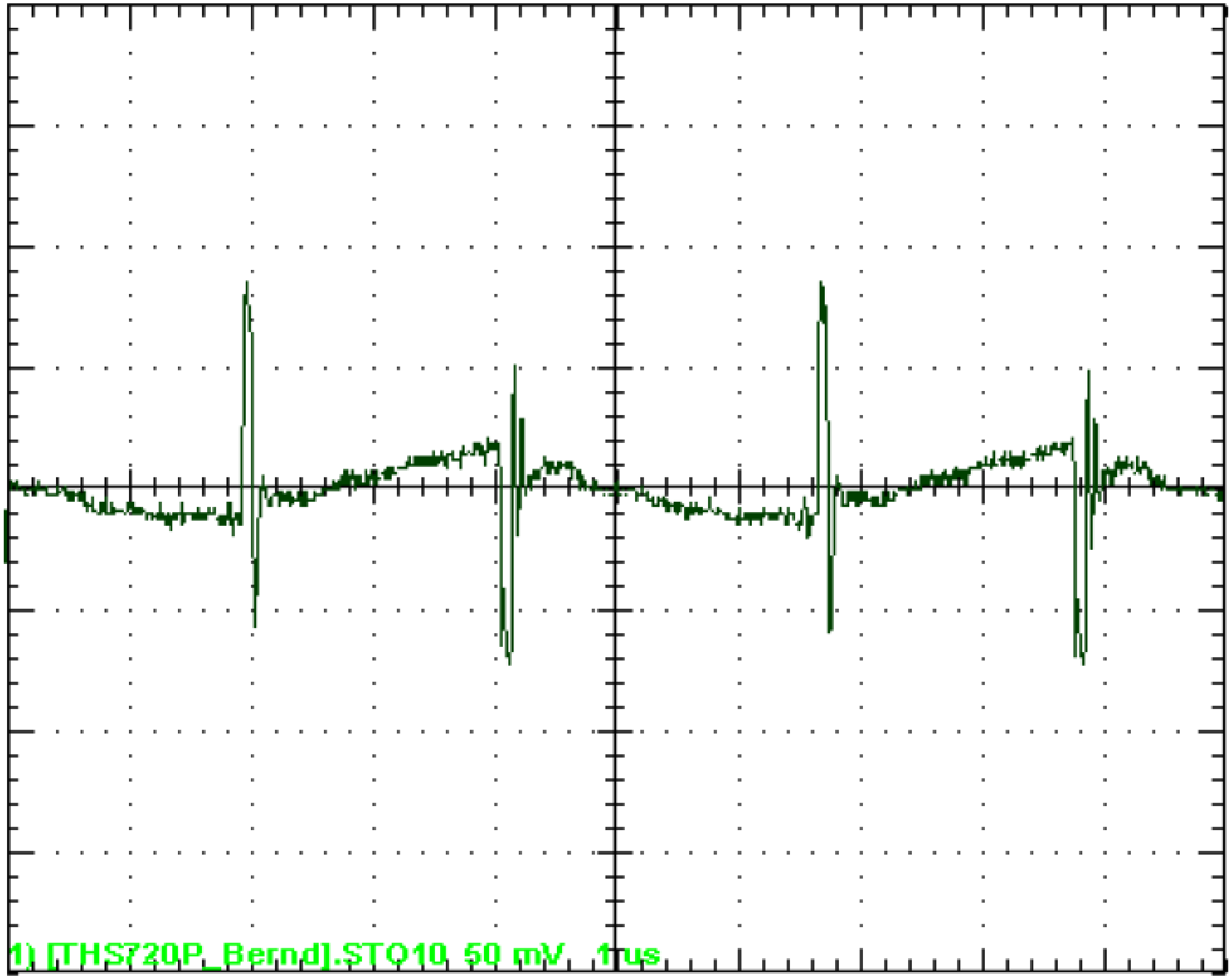
bandwidth > 2kHz, phasemargin >70degs, gain margin <-12dB

Dynamic Behavior – 5.0V/35A Forward Conv.



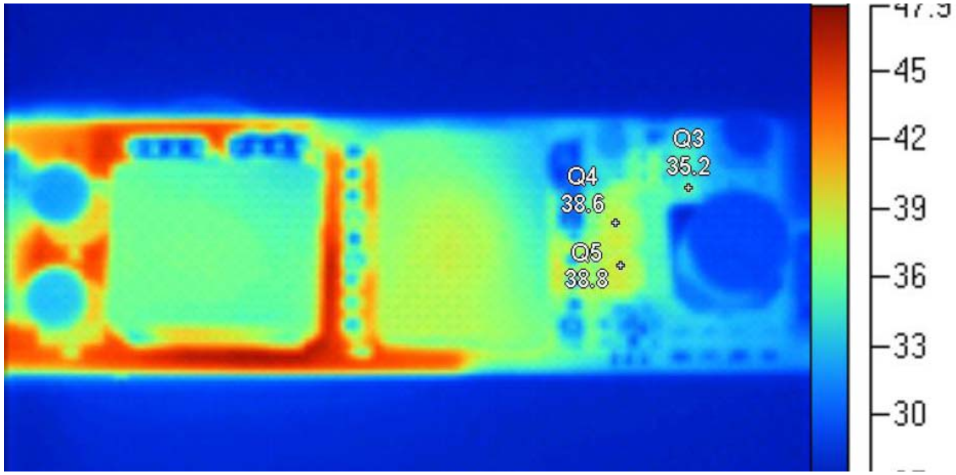
large signal analysis with load step 50%, 15Amps / 30Amps

Ripple & Noise – 5.0V/35A Forward Conv.



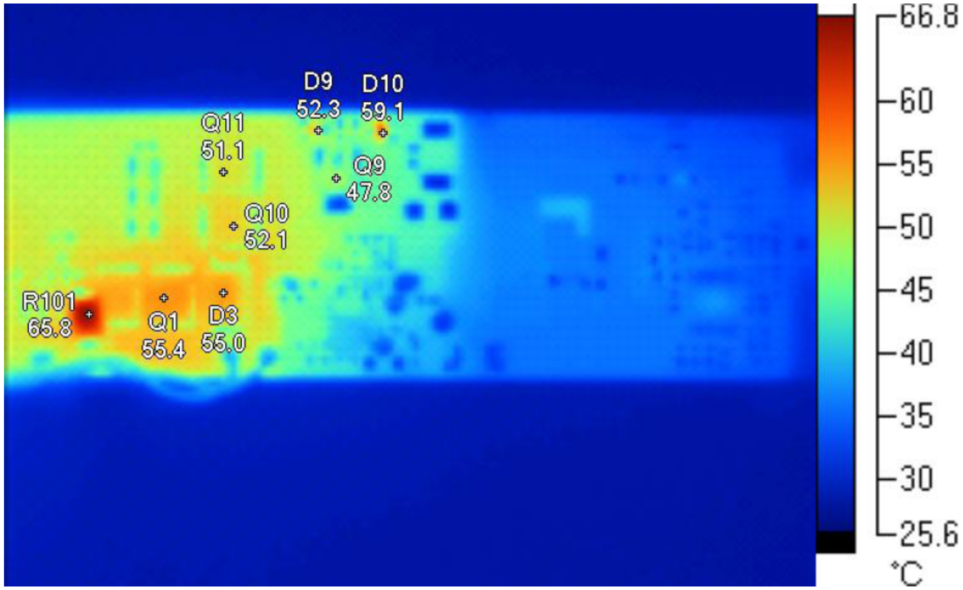
ripple 40mVpp, noise 110mVp at max. load 35Amps

Thermal Behavior – 5.0V/35A Forward Conv.



Name	Temperature
Q5	38.8°C
Q4	38.6°C
Q3	35.2°C

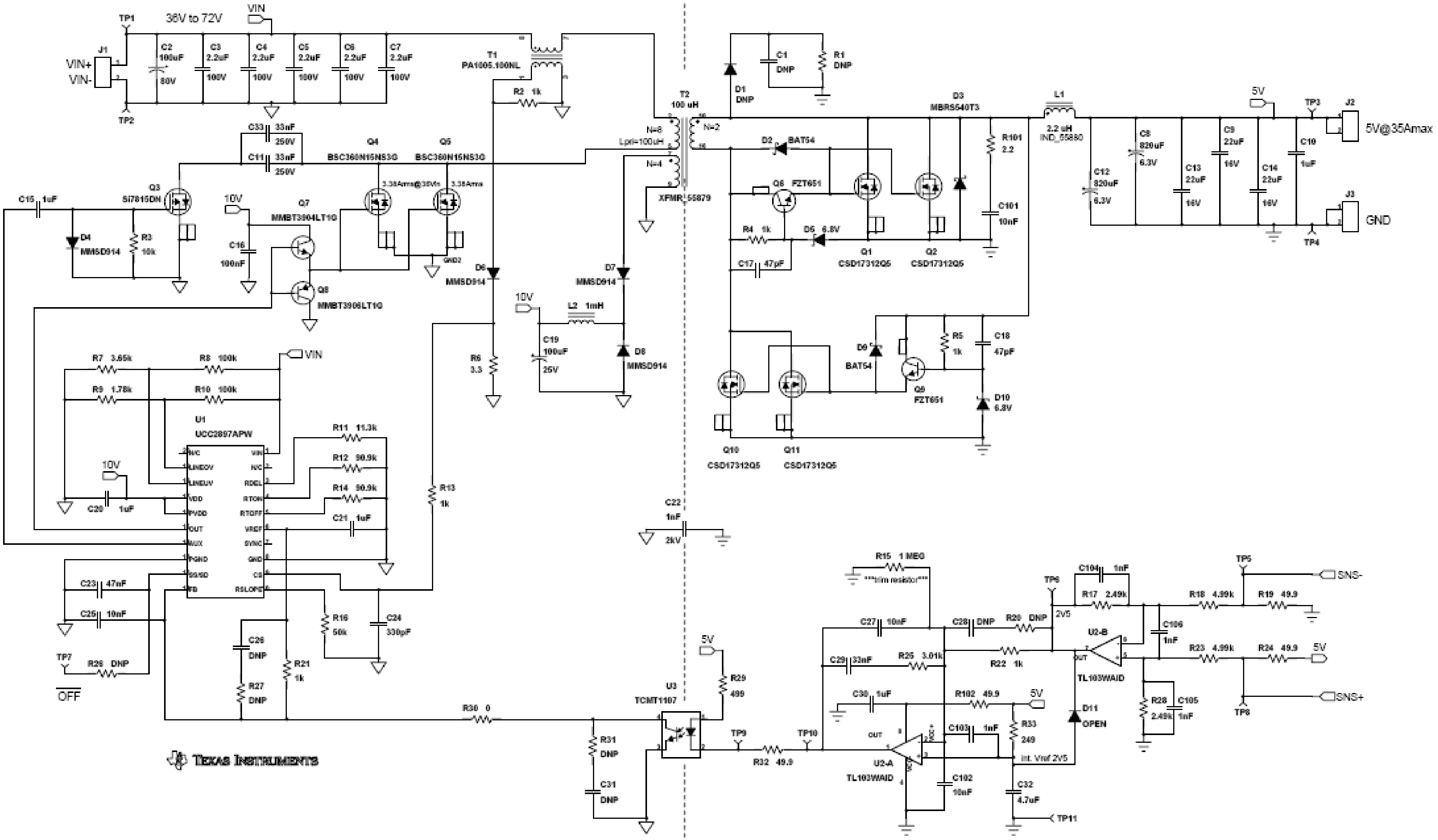
top side at max. load 35A
at forced cooling 400lfm



Name	Temperature
R101	65.8°C
D10	59.1°C
D9	52.3°C
Q1	55.4°C
D3	55.0°C
Q9	47.8°C
Q10	52.1°C
Q11	51.1°C

bottom side at max. load 35A
at forced cooling 400lfm

Active Clamp Forward 5.0V/35A, 175-W Bus Converter Using UCC2897A



Summary

- Adding active clamp and sync rectifiers improves efficiency of forward (and flyback) up to 5% (Efficiencies >90%, here up to 95%)
- Forward provides best efficiency due to lower conduction losses than flyback
- Forward can be scaled to higher output power with similar results
- Flyback for multiple outputs or when cost is most important

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