TMS320C5515/05/VC05 DSP Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)

User's Guide

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About This Manual

This document provides an overview of the Successive Approximation Register (SAR) analog-to-digital Converter (ADC) on the TMS320C5515/05/VC05 digital signal processor (DSP). The SAR is a 10-bit ADC using a switched capacitor architecture that converts an analog input signal to a digital value at a maximum rate of 64 ksps for use by the DSP. This SAR module supports six channels that are connected to four general purpose analog pins (GPAIN [3:0]), which can also be used as general-purpose digital outputs.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320C5515/14/05/04 Digital Signal Processor (DSP) Digital Signal Processor (DSP). Copies of these documents are available on the internet at http://www.ti.com.

SWPU073 — **TMS320C55x 3.0 CPU Reference Guide.** This manual describes the architecture, registers, and operation of the fixed-point TMS320C55x digital signal processor (DSP) CPU.

SPRU652 — **TMS320C55x DSP CPU Programmer's Reference Supplement.** This document describes functional exceptions to the CPU behavior.

SPRUFO0 — **TMS320VC5505/5504 Digital Signal Processor (DSP) Universal Serial Bus 2.0 (USB) User's Guide.** This document describes the universal serial bus 2.0 (USB) in the TMS320VC5505/5504 Digital Signal Processor (DSP) devices. The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices.

SPRUFO1A — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Inter-Integrated Circuit (I2C) Peripheral User's Guide.** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The I2C peripheral provides an interface between the device and other devices compliant with Phillips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. This document assumes the reader is familiar with the I2C-bus specification.

SPRUFO2 — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Timer/Watchdog Timer User's Guide.** This document provides an overview of the three 32-bit timers in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The 32-bit timers of the device are software programmable timers that can be configured as general-purpose (GP) timers. Timer 2 can be configured as a GP, a Watchdog (WD), or both simultaneously.

SPRUFO3 — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Serial Peripheral Interface (SPI) User's Guide.** This document describes the serial peripheral interface (SPI) in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to four SPI slave devices. The SPI can operate as a master device only.

SPRUFO4 — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) General-Purpose Input/Output (GPIO) User's Guide.** This document describes the general-purpose input/output (GPIO) on the TMS320C5515/14/05/04/VC05/VC04 digital signal processor (DSP) devices. The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of an internal register. When configured as an output you can write to an internal register to control the state driven on the output pin.

SPRUFO5 — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Universal Asynchronous Receiver/Transmitter (UART) User's Guide.** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The UART performs serial-to-parallel conversions on data received from a peripheral device and parallel-to-serial conversion on data received from the CPU.

SPRUFO6 — **TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) Multimedia Card (MMC)/Secure Digital (SD) Card Controller User's Guide.** This document describes the Multimedia Card (MMC)/Secure Digital (SD) Card Controller on the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The multimedia card (MMC)/secure digital (SD) card is used in a number of applications to provide removable data storage. The MMC/SD card controller provides an interface to external MMC and SD cards.

SPRUF07 — **TMS320VC5505/5504 Digital Signal Processor (DSP) Real-Time Clock (RTC) User's Guide.** This document describes the operation of the Real-Time Clock (RTC) module in the TMS320VC5505/5504 Digital Signal Processor (DSP) devices. The RTC also has the capability to wake-up the power management and apply power to the rest of the device through an alarm, periodic interrupt, or external WAKEUP signal.

SPRUFO8A — **TMS320VC5505/5504 Digital Signal Processor (DSP) External Memory Interface (EMIF) User's Guide.** This document describes the operation of the external memory interface (EMIF) in the TMS320VC5505/5504 Digital Signal Processor (DSP) devices. The purpose of the EMIF is to provide a means to connect to a variety of external devices.

SPRUFO9 — **TMS320VC5505/5504 Digital Signal Processor (DSP) Direct Memory Access (DMA) Controller User's Guide.** This document describes the features and operation of the DMA controller that is available on the TMS320VC5505/5504 Digital Signal Processor (DSP) devices. The DMA controller is used to move data among internal memory, external memory, and peripherals without intervention from the CPU and in the background of CPU operation.

SPRUFP0 — **TMS320VC5505 Digital Signal Processor (DSP) System User's Guide.** This document describes various aspects of the TMS320VC5505/5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

SPRUGL6 — **TMS320VC5504 Digital Signal Processor (DSP) System User's Guide.** This document describes various aspects of the TMS320VC5505/5504 digital signal processor (DSP) including: system memory, device clocking options and operation of the DSP clock generator, power management features, interrupts, and system control.

SPRUFP1 — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Successive Approximation (SAR) Analog to Digital Converter (ADC) User's Guide. This document provides an overview of the Successive Approximation (SAR) Analog to Digital Converter (ADC) on the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The SAR is a 10-bit ADC using a switched capacitor architecture which converts an analog input signal to a digital value.

SPRUFP3 — TMS320C5515/05/VC05 Digital Signal Processor (DSP) Liquid Crystal Display Controller (LCDC) User's Guide. This document describes the liquid crystal display controller (LCDC) in the TMS320C5515/14/05/04/VC05/VC04 Digital Signal Processor (DSP) devices. The LCD controller includes a LCD Interface Display Driver (LIDD) controller.

SPRUFP4 — TMS320VC5505/5504 Digital Signal Processor (DSP) Inter-IC Sound (I2S) Bus User's Guide. This document describes the features and operation of Inter-IC Sound (I2S) Bus in the TMS320VC5505/5504 Digital Signal Processor (DSP) devices. This peripheral allows serial transfer of full duplex streaming data, usually streaming audio, between DSP and an external I2S peripheral device such as an audio codec.

Successive Approximation (SAR) Analog-to-Digital Converter (ADC)

1 Introduction

This following sections provide an overview of the successive approximation (SAR) analog-to-digital converter (ADC) on the digital signal processor (DSP).

1.1 Purpose of the 10-bit SAR

The SAR in the device is a 10-bit ADC using a switched capacitor architecture that converts an analog input signal to a digital value at a maximum rate of 64 kilo samples per second (ksps) for use by the DSP. This SAR module supports six channels that are connected to four general-purpose analog pins (GPAIN [3:0]) that can be used as general-purpose outputs.

1.2 Features

- Up to 64 ksps
- Single conversion and continuous back-to-back conversion modes
- Interrupt driven or polling conversion or DMA event generation
- Internal configurable reference voltages of: V_{DD_ANA} or bandgap_1.0V or bandgap_0.8V
- Software controlled power down
- Individually configurable general-purpose digital outputs

1.3 Supported Use Case Statement

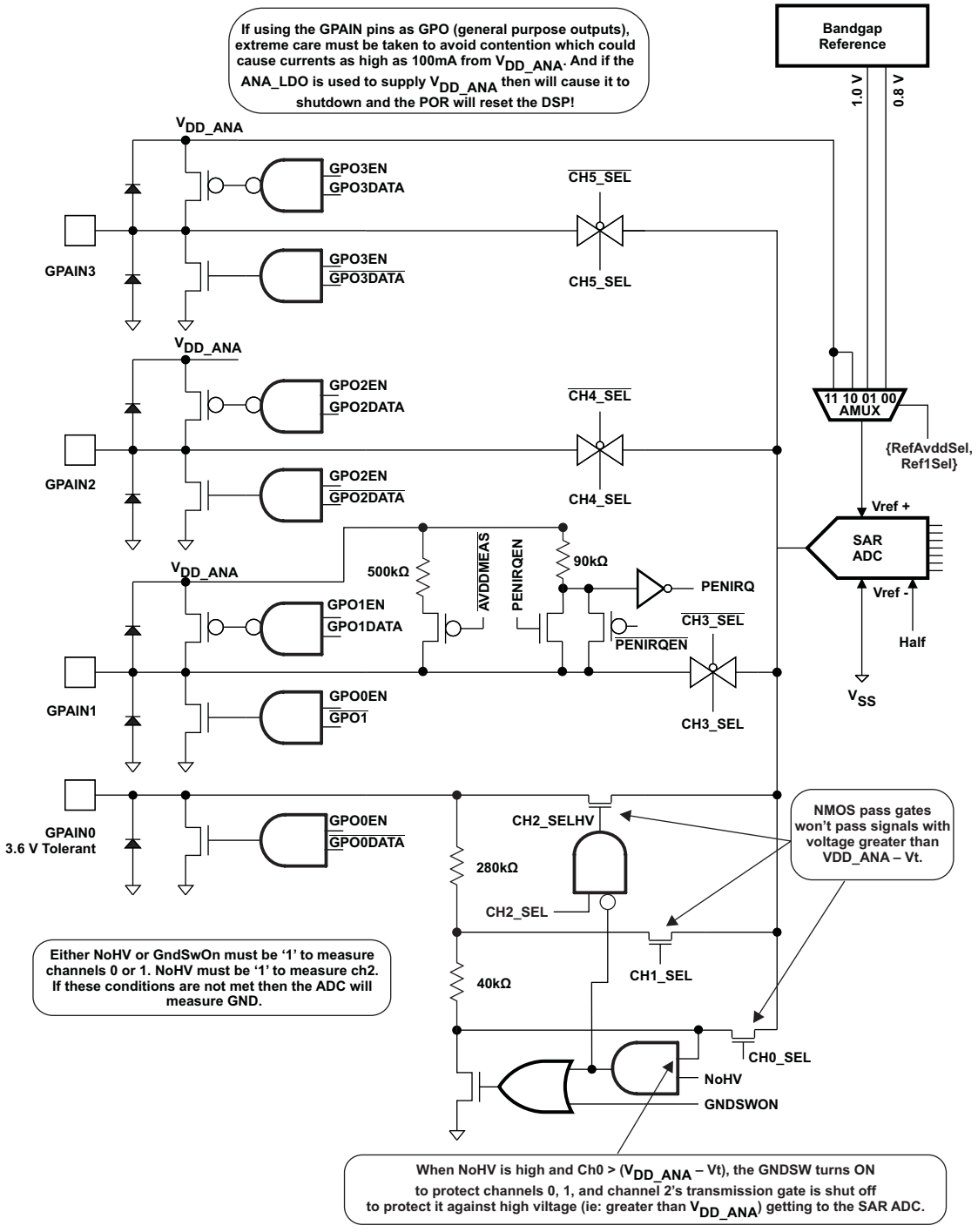
- Measure battery voltage, internal analog voltage (V_{DDA_ANA}), and volume control by measuring across a potentiometer
- 4-wire resistive touch screen coordinate pair measurement and pen down interrupt
- General-purpose outputs that can be driven high or low (except for GPAIN0, which only drives low)
- General-purpose voltage measurement

1.4 Industry Standard(s) Compliance Statement

This peripheral is not intended to conform to any specific industry standard.

1.5 Functional Block Diagram

Figure 1. SAR Converter



2 SAR Architecture

The 10-bit successive approximation analog-to-digital module in the device converts an analog input signal to a digital value for use by the DSP. The SAR module supports six channels, VIN[5:0]. These channels are connected to four general purpose analog pins, GPAIN[3:0]. (See Figure 1.) All general purpose analog pins can be used as general-purpose outputs by setting the corresponding GPIO bits in the SAR A/D Pin Control Register.

Once a conversion is initiated, the programmer must wait until the conversion completes before selecting another channel or initiating a new conversion. To indicate that a conversion is in progress, the ADCBUSY bit field is set. After the conversion completes, the ADCBUSY bit field changes from 1 to 0, indicating that the conversion data is available. The DSP can then read the data from the ADCDAT bits in the SAR A/D Data Register (SARDATA). The value of the CHSEL bit in SAR A/D Control Register (SARCTRL) is reproduced in the CHAN bit of the SARDATA register, so that the DSP can identify which samples were acquired from which channel.

A DMA event is also generated at the end of every conversion.

2.1 SAR Clock Control

The SAR A/D module can operate at a maximum clock rate of 2 MHz (500 ns) and takes 32 clocks cycles to convert a value. This results in a maximum sample rate of 64 ksps. The following equations describe the relationship between the A/D programmable control registers:

SAR A/D Clock Frequency = (System Clock Frequency) / (SystemClkDivisor + 1) ≤ 2 MHz

SAR A/D Conversion Time = (SAR A/D Clock Period * 32)

2.2 Memory Map

Table 1. SAR Memory Map

Address	Acronym	Description
7012h	SARCTRL	SAR A/D Control Register
7014h	SARDATA	SAR A/D Data Register
7016h	SARCLKCTRL	SAR A/D Clock Control Register
7018h	SARPINCTRL	SAR A/D Reference and Pin Control Register
701Ah	SARGPOCTRL	SAR A/D GPO Control Register

2.3 Signal Descriptions

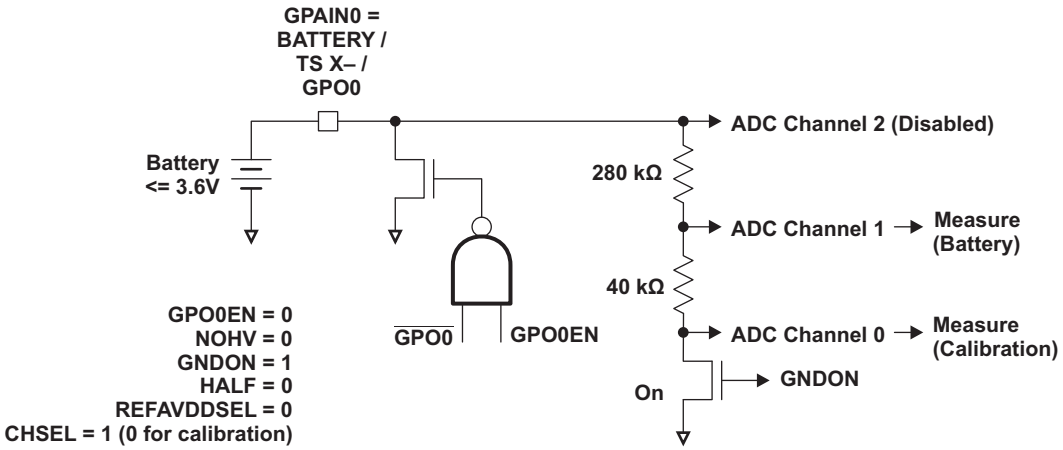
The device's GPAIN[3:0] pins can be configured as inputs to the SAR ADCs or they can be configured as general-purpose outputs that can be driven high or low (excluding GPAIN0 that can only be driven low). The SAR inputs can be used for battery measurement, internal voltage measurement, volume control, and touch screen control. GPAIN[0] is capable of accepting analog input voltage from 0 V up to 3.6 V while GPAIN[1:3] can accept a range of 0 V to V_{DDA_ANA}.

2.4 Battery Measurement

The SAR can be configured to measure a battery using GPAIN0.

To measure a battery that has less than 3.6 V, first connect the battery to GPAIN0 and set the ground switch (GNDON) bit of SAR channel 0. Next, calibrate the measurement by sampling the voltage at SAR Channel 0 (set CHAN to Channel 0). Channel 0 should now be tied to ground with GNDON set to 1. If there is an offset on Channel 0, this needs to be applied to the battery reading that can be obtained by switching to channel 1 and sampling the battery voltage through the voltage divider. The voltage divider divides the value from channel 1 by a factor of 8 (see data manual for limits) before being sampled by the SAR ADC. (See Figure 2.) After measuring the battery, the ground switch transistor should be shut off to eliminate current draw from the battery.

Figure 2. Battery Measurement

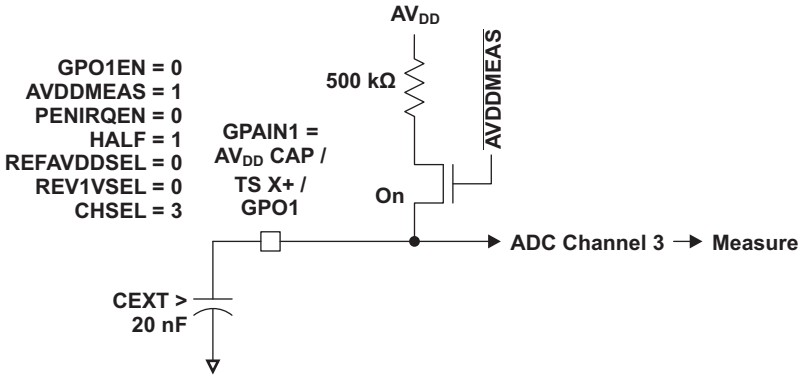


2.5 Internal Voltage Measurement

Using GPAIN1, the SAR can measure the internal voltage of V_{DDA_ANA} on AVDDMEAS channel 3 of the SAR.

To measure the internal AV_{DD}, set the internal voltage reference by setting in SAR A/D Reference and Pin Control Register (SARPINCTRL). A 20 nF cap is recommended to be connected between GPAIN1 and GND to provide low pass filtering and less measurement noise. Next, sample SAR channel 3. Selecting HALF = 1 has the effect of reducing the ADC's input sampled voltage in half. Therefore, with AV_{DD} (i.e., V_{DDA_ANA}) at its max of 1.43 V, divided by two is 0.715 V. Then, with the ADC's VREF set to bandgap_0.8 V, the dynamic range is optimum. See Figure 3.

Figure 3. Voltage Measurement

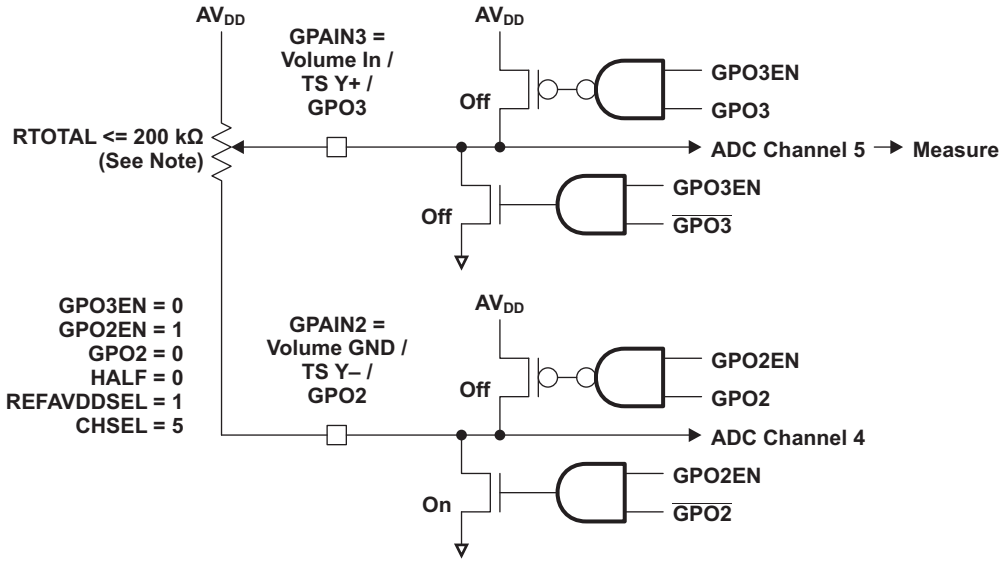


2.6 Volume Control

The SAR can be used to sample a volume control potentiometer connected across GPAIN2 and GPAIN3. Note that other combinations of the GPAIN[3:0] could be used to perform this function. We have chosen GPAIN2 and GPAIN3 for this example.

To use the SAR for volume control, place a potentiometer across GPAIN3 and GPAIN2, then ground GPAIN2 by clearing GPO2 and sample SAR channel 5 voltage. Use the settings in Figure 4.

Figure 4. Voltage Control



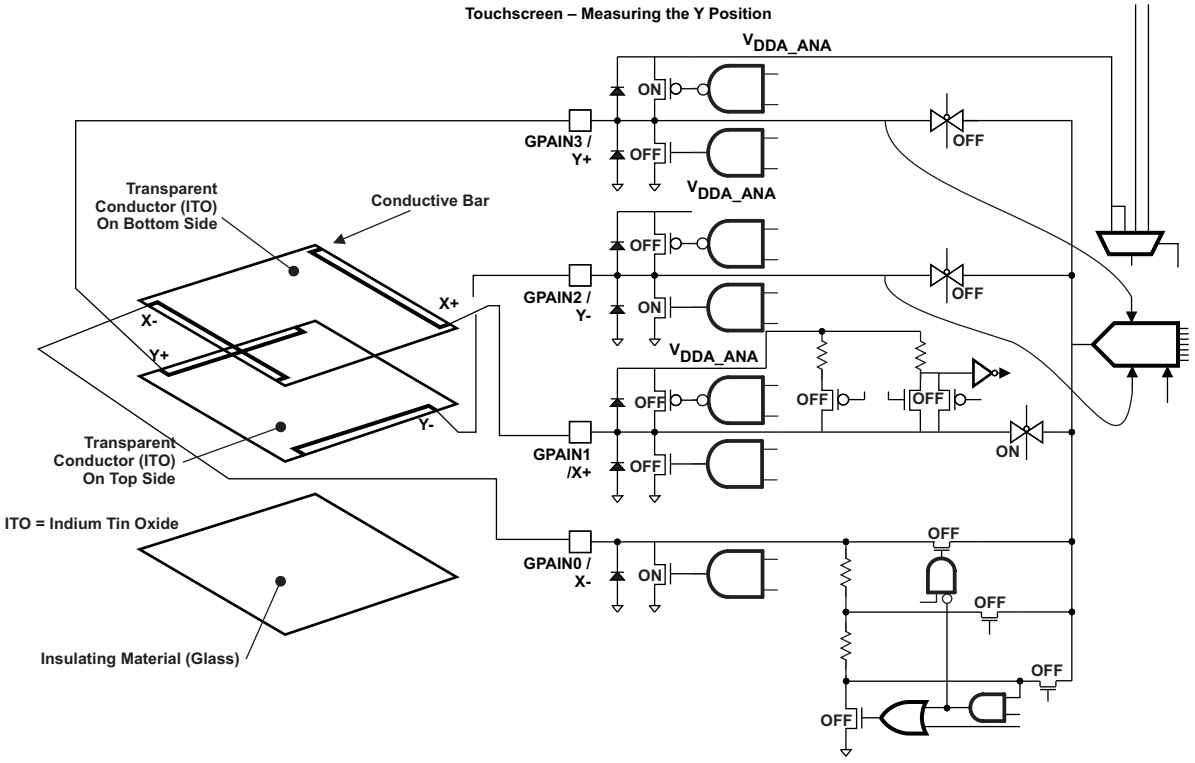
2.7 Touch Screen Digitizing

Using all 4 GPAIN pins, the SAR can be used for digitizing touch screen coordinates. With GPAIN3 as Y+, GPAIN2 as Y-, GPAIN1 as X+, and GPAIN0 as X-.

To measure Y position, enable GPAIN3 and GPAIN2 as general-purpose outputs using GPO3EN=1 and GPO2EN=1. Then, ground GPAIN2 by clearing GPO2 and drive GPAIN3 high by setting GPO3. Let the touch panel settle (duration depends on the bypass caps you have at the X+, X-, Y+, Y- terminals of the touch screen) and measure the voltage at GPAIN1 using SAR channel 3.

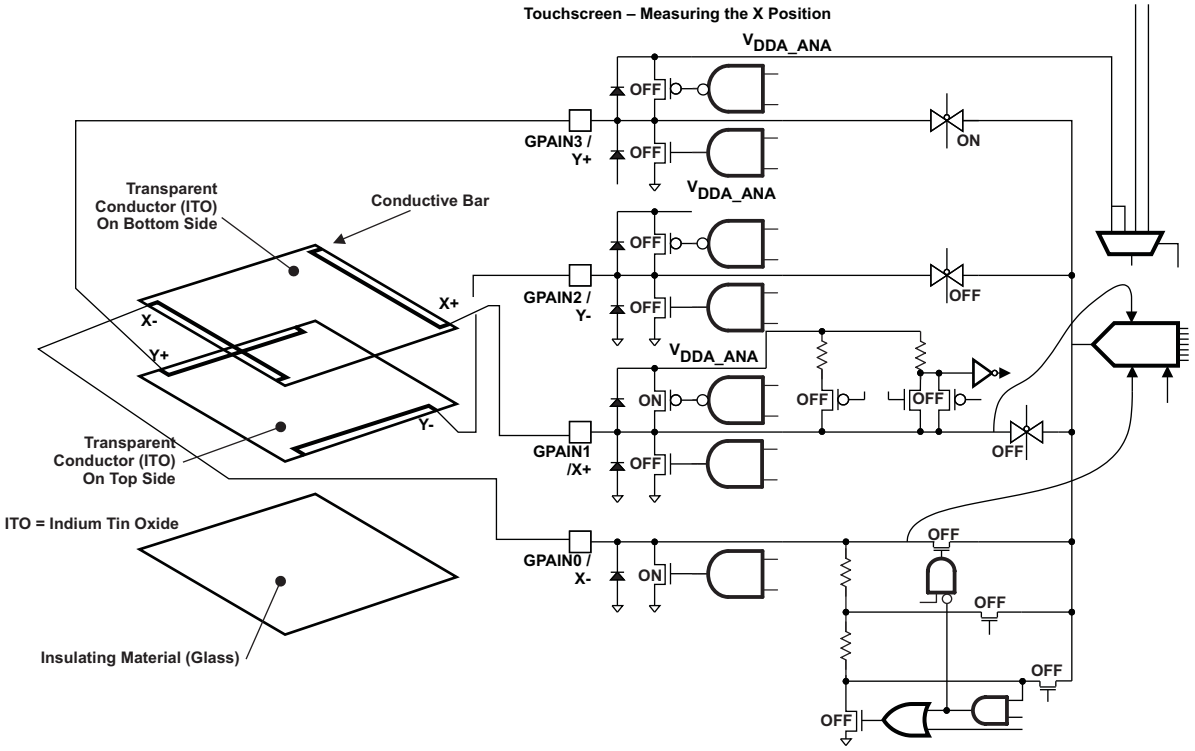
NOTE: It is recommended that an external LDO be used to supply power to V_{DDA_ANA} rather than using ANA_LDO. When ANA_LDO is used to supply power to V_{DDA_ANA}, the pins GPAIN[3:1] cannot be used as general-purpose outputs (driving high) since the maximum current capability of the ANA_LDO can be exceeded. The ISD parameter of the ANA_LDO is too low to drive any realistic load on the GPAIN[3:1] pins while also supplying the PLL through V_{DDA_PLL} and the SAR through V_{DDA_ANA}. Using AVA_LDO to supply power to V_{DDA_ANA} in such a case may result in the on-chip power-on reset (POR) resetting the chip.

Figure 5. Y Position



To measure X position, enable GPAIN1 and GPAIN0 using GPO1EN=1 and GPO0EN=1. Then, ground GPAIN0 by clearing GPO0 and drive GPAIN1 high by setting GPO1. Let the touch panel settle, then measure the voltage at GPAIN3 using SAR channel 5.

Figure 6. X Position

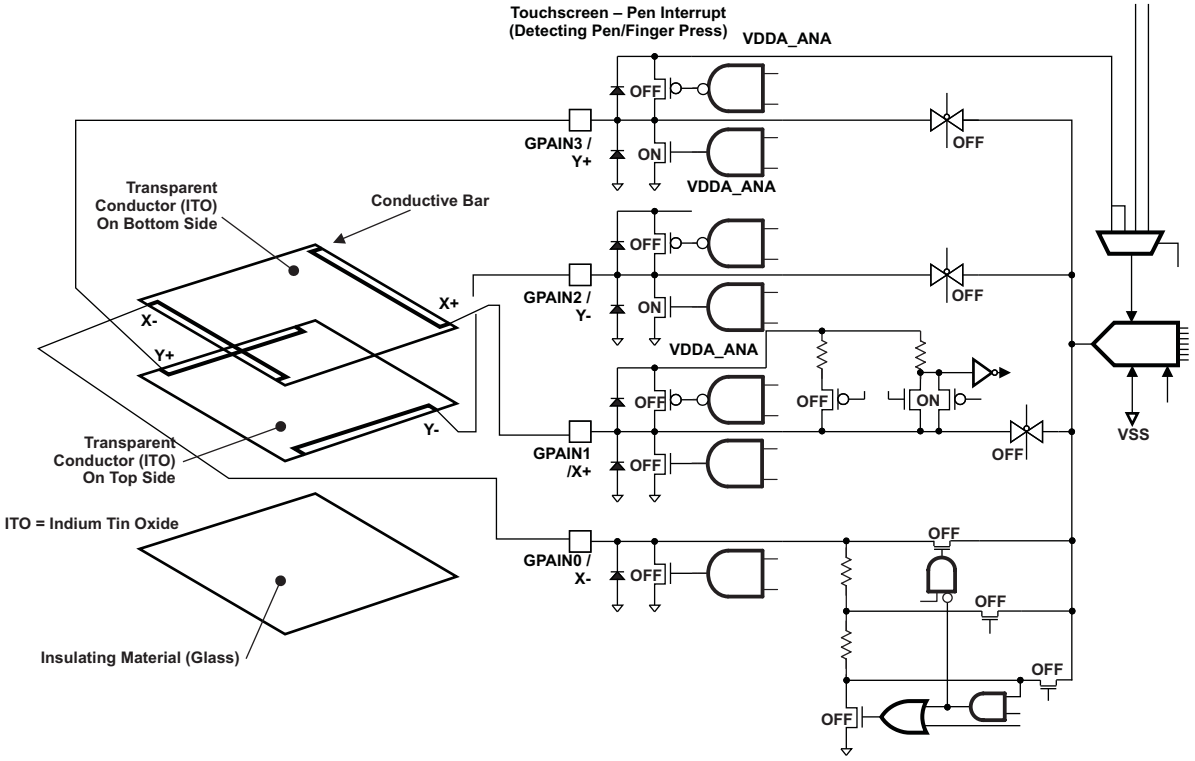


2.8 Touch Screen : Pen Press Interrupts

To detect when the touch screen is touched, the SAR peripheral has a PENIRQ feature. This feature makes it possible to detect touch events without continuous ADC polling.

The SAR should be configured as shown in Figure 7.

Figure 7. Pen Interrupt



The DSP should be configured to allow SAR interrupts. When the touch screen is not pressed, a pullup resistor biases the PENIRQ buffer high so that an interrupt is not generated. When the touch screen is pressed it creates a path to ground that is lower impedance than the pullup resistor. Therefore, the PENIRQ buffer generates an interrupt and the DSP can then take the steps necessary to digitize the X & Y coordinates.

2.9 General-Purpose Output

GPAIN[3:0] can be configured as general-purpose outputs. This is accomplished by enabling the GPAIN pin as an output in the SAR A/D GPO Control Register (SARGPOCTRL). After enabling the GPO you can set the output as grounded or driven high. In the case where V_{DDA_ANA} is supplied by the ANA_LDOO, care must be taken to avoid shorting GPAIN pins to ground as this will cause the maximum current of the ANA_LDOO to be exceeded and the POR circuit to reset the DSP. The total current from all GPAIN[3:0] pins to ground should never exceed Imax of the ANA_LDOO. For more information, see the device-specific data manual. In the case where V_{DDA_ANA} is supplied by some source other than the on-chip ANA_LDO, this is not an issue.

2.10 Reset Considerations

The SAR can only be reset by a hardware reset.

2.10.1 Software Reset Considerations

A software reset (such as a reset generated by the emulator) will not cause the SAR controller registers to be altered. After a software reset, the SAR controller continues to operate as it was configured prior to the reset.

There is no peripheral reset for the SAR.

2.10.2 Hardware Reset Considerations

A hardware reset of the processor causes the SAR controller registers to return to their default values after reset.

2.11 A/D Conversion

To start an analog to digital conversion the following steps must be executed:

1. Set SAR clock to be less than or equal to 2 MHz in the SAR A/D clock Control Register (SARCLKCTRL) for fastest conversion rate and operation of the A/D module.
   A/D function clock = (Sys Clk)/(ADCCLKDIV+1)
2. Write to the SARPINCTRL register (7018h) to power up the SAR circuits and select the SAR reference voltage.
3. Write a 1 to the ADCSTRT bit in the SARCTRL register and the desired channel for the conversion in the CHSEL bit field.
4. Read the ADCBUSY bit in the SARDATA register to ensure it is set to 1 to indicate the start of conversion. Due to delays between the CPU write instruction and the actual write to the SAR A/D registers the ADCBUSY bit must be set before proceeding.
5. ADCSTRT in the SARCTRL register and ADCBUSY bit in the SARDATA register are set to 0 to indicate the end of the conversion sequence.
6. Once ADCBUSY bit in the SARDATA register is set to 0, the SAR A/D Data Register contains the channel converted in the CHSEL bit field and the actual converted value in the ADCDAT bit field.

2.12 Interrupt Support

2.12.1 Interrupt Events and Requests

The SAR peripheral generates DSP interrupts every time an ADC conversion is completed and data is available to be read by the DSP. Additionally, when connected to a touch screen device, the SAR can be configured to detect when the touch screen is pressed and generate an interrupt without having to perform continuous conversion to poll the touch screen.

2.13 Emulation Considerations

The SAR controller is not affected by emulation halt events (such as breakpoints).

3 Registers

Table 2 list the memory mapped registers associated with the successive approximation (SAR) analog-to-digital converter (ADC).

Table 2. SAR A/D Memory Mapped Registers

CPU Word Address	Acronym	Register Description	Section
7012h	SARCTRL	SAR A/D Control Register	Section 3.1
7014h	SARDATA	SAR A/D Data Register	Section 3.2
7016h	SARCLKCTRL	SAR A/D Clock Control Register	Section 3.3
7018h	SARPINCTRL	SAR A/D Reference and Pin Control Register	Section 3.4
701Ah	SARGPOCTRL	SAR A/D GPO Control Register	Section 3.5

3.1 SAR A/D Control Register (SARCTRL)

The SAR A/D control register (SARCTRL) selects the channel number and indicates the start of a conversion.

The SAR A/D control register (SARCTRL) is shown in Figure 8 and described in Table 3.

Figure 8. SAR A/D Control Register (SARCTRL)

15	14 12	11	10	9 0
ADCSTRT	CHSEL	MULTICH	SNGLCONV	Reserved
RW, +0	RW, +000	RW,+0	RW,+0	RW, +0000000000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3. SAR A/D Control Register (SARCTRL) Field Descriptions

Bit	Field	Value	Description
15	ADCSTRT		Start Conversion
		0	No conversion.
		1	Start conversion cycle by setting START signal.
14-12	CHSEL		Channel Select
		0	Channel CH0 is selected.
		1h	Channel CH1 is selected.
		2h	Channel CH2 is selected.
		3h	Channel CH3 is selected.
		4h	Channel CH4 is selected.
		5h	Channel CH5 is selected.
		6h-7h	All channels are off.
11	MULTICH		Multi Channel operation.
		0	Normal Mode.
		1	In this mode, the SAR state machine is optimized to give more time to sampling the analog input. This mode could possibly improve measurements in cases where the ADC input has abrupt voltage changes such as when changing from one input channel to another. The additional time given to sampling does not affect the 32 cycles for conversion, but it does come at the expense of settling time for the ADC's internal comparator. Therefore, this mode should not be used unless the above situation exists and it is determined to improve the measurements.
10	SNGLCONV		Single Conversion mode.
		0	Continuously perform back-to-back conversions, as long as ADCSTRT is set.
		1	Perform one conversion and stop. ADCSTRT must be cleared and then set high to perform another conversion.
9-0	Reserved	0	Reserved.

3.2 SAR A/D Data Register (SARDATA)

The SAR A/D data register (SARDATA) indicates if a conversion is in process, the actual digital data converted from the analog signal, and the channel belonging to this conversion.

The SAR A/D data register (SARDATA) is shown in Figure 9 and described in Table 4.

Figure 9. SAR A/D Data Register (SARDATA)

15	14 12	11 10	9 0
ADCBUSY	CHAN	Reserved	ADCDAT
R, +0	R, +111	R, +00	R, +0000000000

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4. SAR A/D Data Register (SARDATA) Field Descriptions

Bit	Field	Value	Description
15	ADCBUSY		ADC Converter Busy. The ADCBUSY bit will be set three SAR clock cycles after the ADCSTRT bit is set.
		0	ADCDAT available.
		1	ADCBUSY performing a conversion. After ADCSTRT is high, the ADCBUSY becomes high.
			This will always read 0 when STATUSMASK=1.
14-12	CHAN		Channel Select
		0	Channel CH0 is selected.
		1h	Channel CH1 is selected.
		2h	Channel CH2 is selected.
		3h	Channel CH3 is selected.
		4h	Channel CH4 is selected.
		5h	Channel CH5 is selected.
		6h-7h	Reserved
			These bits will always read 000 when STATUSMASK = 1.
11-10	Reserved	0	Reserved.
9-0	ADCDAT	0-3FFh	Converter Data.

3.3 SAR A/D Clock Control Register (SARCLKCTRL)

The SAR A/D clock control register (SARCLKCTRL) sets the clock divider to control the speed of conversion. The clock rate of the SAR module must not exceed 2MHz.

The SAR A/D clock control register (SARCLKCTRL) is shown in Figure 10 and described in Table 5.

Figure 10. SAR A/D Clock Control Register (SARCLKCTRL)

15	14	0
Reserved	ADCCLKDIV	
R, +0	RW, +111111111111111	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5. SAR A/D Clock Control Register (SARCLKCTRL) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14-0	ADCCLKDIV	0-7FFFh	System Clock Divisor This specifies the divider rate of the system clock: $F_{SAR\_Clock} = (F_{System\_Clock}) /(ADCCLKDIV[14:0] + 1)$ Allows for divide-by-1 up to divide-by-32768.

3.4 SAR A/D Reference and Pin Control Register (SARPINCTRL)

The SAR A/D reference and pin control register (SARPINCTRL) controls the SAR's reference voltage and the circuits surrounding the GPAIN pins. The SAR's reference voltage determines the voltage at the ADC input that corresponds to the fullscale output code (ie: 1111111111b). Note, however, that due to the circuitry between the ADC input and the GPAIN[3:0] pins, the voltage at the ADC input isn't necessarily the same as the voltage at the GPAIN[3:0] pins. For example, the voltage divider on GPAIN0/Channel 1 scales the voltage of the signal by a factor of 8 before it arrives at the ADC. It is important to select the best voltage reference according to the voltage range of signal that will be digitized by the ADC so that the best resolution is obtained.

The SAR A/D reference and pin control register (SARPINCTRL) is shown in Figure 11 and described in Table 6.

Figure 11. SAR A/D Reference and Pin Control Register (SARPINCTRL)

15	14	13	12	11	10	9	8
Reserved	STATUSMASK	PWRUPBIAS	SARPWRUP	Reserved	REFBUFFEN	REFLVSEL	REFAVDDSEL
R, +0	Rw,+0	RW,+0	RW,+0	R,+0	RW, +0	RW, +0	RW, +0

7	5	4	3	2	1	0
Reserved		TOUCHSCREENMODE	AVDDMEAS	Reserved	GNDON	HALF
R,+0		RW, +0	RW, +0	RW, +0	RW, +0	RW, +0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6. SAR A/D Reference and Pin Control Register (SARPINCTRL) Field Descriptions

Bit	Field	Value	Description
15	Reserved	0	Reserved.
14	STATUSMASK		Asserting this bit causes bits 12-15 of the SAR_DATA register to be forced to 0000. Those four bits correspond to the ChannelSelected and ADCBusy bits. The purpose for clearing/masing them is so that DMA transfers from the SAR to a memory buffer do not include those status bits and thus post-processing of the memory buffer is not required to strip the status bits out of the sample set. For example, if the SAR & DMA collect a 2k sample set into memory to perform an FFT on the sampled data, you wouldn't want the ChannelSelected status bits to be in the data when the FFT is performed.
		0	The SAR_DATA register includes the status info in bits 12-15.
		1	The SAR_DATA register bits 12-15 are always read as 0000.
13	PWRUPBIAS		Enables or disables the current bias circuit that is needed for the SAR to perform A/D conversions.
		0	Powered Down. Low power setting.
		1	Powered Up. Required setting for performing A/D conversions.
12	SARPWRUP		Enables or disables the analog power to the SAR.
		0	SAR analog Powered down.
		1	SAR analog power present.
11	Reserved	0	Reserved.
10	REFBUFFEN		Reference Buffer enable. The reference buffer can be disabled to save power when the ADC's VREF is set to VDDA_ANA (REFAVDDSEL=1) or when VREF is provided by the TOUCHSCREENMODE pins (TOUCHSCREENMODE=1). The reference buffer must be enabled whenever one of the bandgap reference voltages are used (ie: REFAVDDSEL=0). REFBUFEN can be 0 or 1 when TOUCHSCREENMODE=1.
		0	Reference Buffer is disabled. Low power setting.
		1	Reference Buffer is enabled. Required when using bandgap generated VREF.
9	REFLVSEL		Bandgap-based reference voltage value select. The on-chip bandgap provides two references to the SAR peripheral: 0.8v & 1.0v. This register is used to select which bandgap reference voltage is used when REFAVDDSEL=0. In general, the lowest VREF should be used to get the best resolution from the converter. However, VREF should always be greater than the input signal else clipping will occur.
		0	Bandgap-Based Reference Voltage set to 0.8V.
		1	Bandgap-Based Reference Voltage set to 1V.

Table 6. SAR A/D Reference and Pin Control Register (SARPINCTRL) Field Descriptions (continued)

Bit	Field	Value	Description
8	REFAVDDSEL		ADC Reference Voltage Select. When asserted, this register selects VDDA_ANA as the voltage reference for the SAR ADC. Otherwise, one of the two selectable bandgap references will be used. This register has no effect when TOUCHSCREENMODE=1.
		0	Reference Voltage based on Bandgap. The voltage value of the Bandgap reference is dictated by REFLVSEL.
		1	Reference Voltage set to Analog Voltage (VDD_ANA).
7-6	Reserved	0	Reserved.
5	Reserved	0	Reserved must write 0.
4	TOUCHSCREENMODE		Enables Touch Screen Mode. In this mode, the SAR detects which coordinate, X or Y, is being measured based on the GPOxEN and GPOxDATA settings, and switches the ADC's VREF+ and VREF- to the appropriate GPAIN[3:0] pins to reduce offset and gain errors caused by the dc current flowing thru the touch screen and the drop across the GPO output transistors. See Figure 5 and Figure 6 to see how the VREF+ and VREF- are affected by this mode.
		0	TOUCHSCREENMODE is Disabled.
		1	TOUCHSCREENMODE is Enabled.
3	AVDDMEAS		Enable measurement of internal analog voltage (V_{DD_ANA}) on SAR Channel 3.
		0	PMOS switch on channel 3 is open, thus VDDA_ANA is not connected to channel 3 ADC input.
		1	PMOS switch on channel 3 is closed, thus VDDA_ANA is connected to channel 3 ADC input thru a pullup resistor to enable measuring the internal VDDA_ANA voltage. Note, when measuring VDDA_ANA, an independent voltage reference is needed for the ADC. So one of the two bandgap voltages should be used. Half mode will also be necessary since VDDA_ANA is greater than the two bandgap voltage references.
2	Reserved	0	Reserved.
1	GNDON		Ground SAR Analog Channel 0 and introduce a voltage resistor divider network in SAR Channel 1.
		0	SAR Analog Channel 0 is not grounded.
		1	SAR Analog Channel 0 grounded. Introduces a divider into the SAR Channel 1 input of 1/8 * GPAIN0. See datasheet for tolerance specs on the resistor divider.
0	HALF		Divides the ADC analog input by two before doing the conversion. The attenuation is accomplished by only charging half of the SAR ADC's internal capacitive array during the sample phase, then the whole capacitive array is used for the successive approximation conversion. By sampling with half the capacitance and comparing against VREF with the full capacitance, the input voltage is attenuated by a factor of 2.
		0	A-to-D conversion is based on Vin.
		1	A-to-D conversion is based on Vin / 2.

3.5 SAR A/D GPO Control Register (SARGPOCTRL)

The SAR A/D general-purpose output control register (SARGPOCTRL) sets the corresponding GPAIN pins to general-purpose outputs or analog inputs. In general-purpose output mode, the GPAIN pins can be individually driven high or low.

The SAR A/D GPO control register (SARGPOCTRL) is shown in Figure 12 and described in Table 7.

Figure 12. SAR A/D GPO Control Register (SARGPOCTRL)

15						10	9	8
Reserved							PENIRQ	PENIRQEN
R, +00000							RW, +0	RW, +0
7	6	5	4	3	2	1	0	
GPO3EN	GPO2EN	GPO1EN	GPO0EN	GPO3	GPO2	GPO1	GPO0	
RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	RW, +0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 7. SAR A/D GPO Control Register (SARGPOCTRL) Field Descriptions

Bit	Field	Value	Description
15-10	Reserved	0	Reserved.
9	PENIRQ		Pen Interrupt Request Status.
		0	No pen input detected.
		1	Pen input detected.
8	PENIRQEN		Pen Interrupt Request Enable.
		0	Disable the pen interrupt.
		1	Enable the pen interrupt and route to the CPU's SAR interrupt signal.
7	GPO3EN		Enable General Purpose Output on GPAIN3. Allows using GPAIN3 as a general output.
		0	GPAIN3 output driver disabled.
		1	GPAIN3 used as output.
6	GPO2EN		Enable General Purpose Output on GPAIN2. Allows using GPAIN2 as a general output.
		0	GPAIN2 output driver disabled.
		1	GPAIN2 used as output.
5	GPO1EN		Enable General Purpose Output on GPAIN1. Allows using GPAIN1 as a general output.
		0	GPAIN1 output driver disabled.
		1	GPAIN1 used as output.
4	GPO0EN		Enable General Purpose Output on GPAIN0. Allows using GPAIN0 as a general output
		0	GPAIN0 output driver disabled.
		1	GPAIN0 used as output.
3	GPO3		Drive high or low GPAIN3 when set as General Purpose Output.
		0	GPAIN3 grounded.
		1	GPAIN3 driven high.
2	GPO2		Drive high or low GPAIN2 when set as General Purpose Output.
		0	GPAIN2 grounded.
		1	GPAIN2 driven high.
1	GPO1		Drive high or low GPAIN1 when set as General Purpose Output.
		0	GPAIN1 grounded.
		1	GPAIN1 driven high.
0	GPO0		Ground GPAIN0 when set as General Purpose Output.
		0	GPAIN0 grounded.
		1	GPAIN0 driven high.

3.6 Conversion Example

To request a conversion the CPU must execute the following sequence of events:

1. Set SAR clock to be less than or equal to 2MHz in SAR Clock Control Register for fastest conversion rate and operation of the A/D module.
2. Write a “1” to the ADCSTRT bit of the SARCTRL register and the desired channel for conversion in the CHAN bit field in the SARDATA register.
3. ADCBUSY bit of the SARDATA register is set to “1” to indicate the start of A/D conversion.
4. Due to delays between the CPU write instruction and the actual write to the SAR A/D Registers, it is recommended to read the SARDATA register and verify the ADCBUSY bit is set to “1” before proceeding with step 6.
5. ADCSTRT and ADCBUSY bits are set to “0” to indicate the end of the conversion sequence. The SAR A/D module enters stand-by mode to conserve power until event 2 occurs over again.
6. Once ADCBUSY bit is set to “0”, the SARDATA register contains the channel converted in the CHAN bit field and the actual converted value in the ADCDAT bit field

Appendix A Revision History

This revision history reflects the changes made to this document from its original version.

Table 8. Revision History

See	Revision
Figure 1	Updated SAR Converter figure.
Figure 2	Updated Battery Measurement figure.
Figure 3	Updated Voltage Measurement figure.
Figure 4	Updated Voltage Control figure.
Figure 5	Updated Y Position figure.
Figure 6	Updated X Position figure.
Figure 7	Updated Pen Interrupt figure.
Section 3	Updated descriptions for SARCTRL and SARDATA registers.

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