Application Report
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Creating a Universal Car Charger for USB Devices From the TPS54240 and TPS2540A

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ABSTRACT

This application report describes how to design an iPhone™ or Universal Car Charger for USB devices. The design meets the Battery Charging Specification BC1.2 for DCP and CDP, Chinese Telecommunications Industry Standard YD/T 1591-2009, and is compatible with USB2.0 and 3.0 power switch requirements. The form factor of the design complies to the UL standard 2089 and ANSI/SAE J563 specification and can be easily adapted to meet other form factors.

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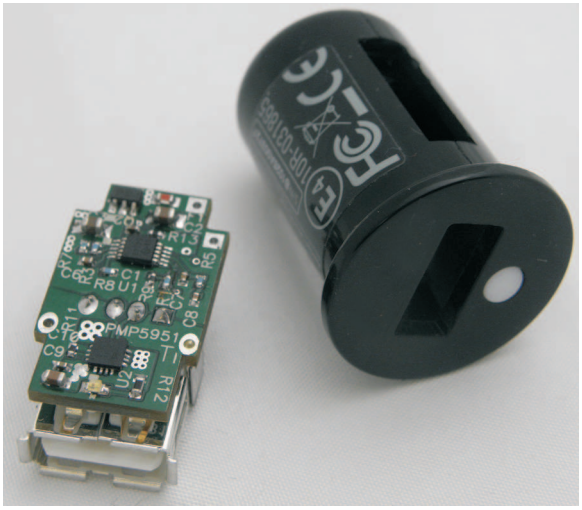

Figure 1. Universal Car Charger

The input voltage supply for a car charger is typically 12 V, but can range from 6 V to 14.5 V with input surges of up to 40 V for multiple 16-ms durations. The power supply must be able to tolerate these surges, and regulate the output to a nominal 5 V with a tolerance of 4.75 V to 5.25 V. Short-circuit protection is required in case of a fault with the USB port. The average current consumption depends on the device connected to the USB port, but can be as high as 2.1 A continuous.

The form factor of the design is an important consideration, allowing for the car charger to be inserted and removed easily, with little material extending beyond the socket. The form factor must be small enough to meet UL standard 2089 and ANSI/SAE J563 specification.

Additionally, to charge devices quickly, the car charger must support the data handshaking protocol required to support USB 2.0 BC1.2 and Divider Mode devices such as iPod™ and iPhone™ to allow charging currents as much as four times greater than USB 2.0 allows. Without this handshaking protocol, many handsets and smartphones on the market fail to charge.

The report goes through step-by-step procedure to design the car charger power supply with the help of a reference design implemented using TPS54240 and TPS2540.

The TPS54240 SWIFT™ converter has the following features:

- Current mode control: Provides simple external compensation and flexible component selection.
- Pulse skip mode: Reduces no load supply current.
- 200-mΩ, high-side MOSFET (FET) provides a cost-effective power supply for 1-A to 2-A transient load with a minimum current limit of 3.5 A.
- Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin.
- Slow Start controls the output voltage start-up ramp and can also be configured for sequencing/tracking.
- An open-drain, power-good signal indicates the output is within 93% to 107% of its nominal voltage.
- A wide switching frequency range allows efficiency and external component size to be optimized.
- Frequency foldback and thermal shutdown protects the part during an overload condition

The TPS2540 USB Charging Port Power Switch and Controller has the following features:

- Meets Battery Charging Specification BC1.2 for DCP and CDP.
- Support Sleep-Mode Charging for most available Apple devices.
- Compatible with USB 2.0 and 3.0 Power Switch requirements.
- 73-mΩ, high-side MOSFET for low power dissipation

2 Input Protection Circuitry

Several different options are available for protecting the car charger from large voltage swings during normal operation, double battery jump start, or load dump when the battery is disconnected. The solution chosen for this example is a simple Zener diode and FET to regulate the voltage to 39 V. This allows the use of the TPS54240 (42-V converter), which is cost effective and efficient. If a wider input voltage is expected, a higher voltage FET can be used to extend the range as high as necessary. Care needs to be taken that the safe operating area of the FET is not exceeded under transient conditions. The diode D1 provides protection against reverse polarity connection of the input. F1 is a 2-A fuse used to protect against catastrophic failures.

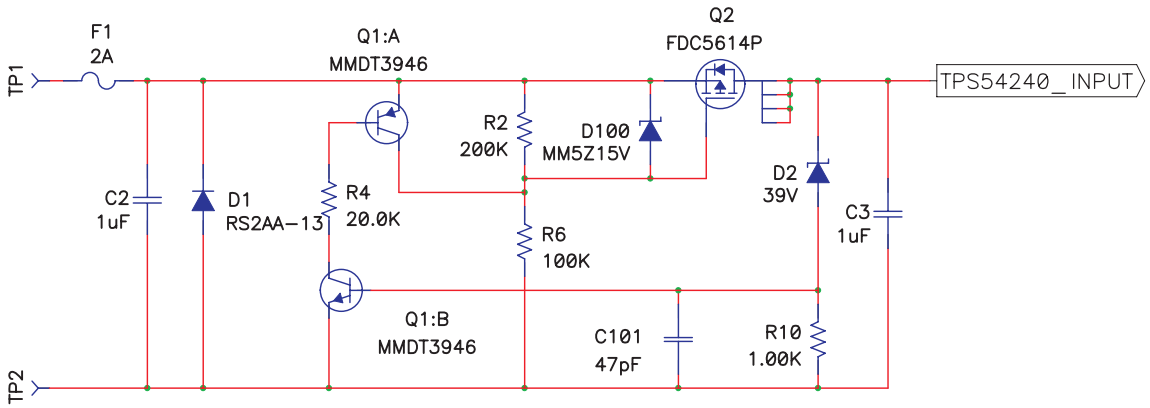

Figure 2. USB iPhone Car Charger Input Protection Circuit Schematic

2.1 Design Example with FET and Linear Regulator Zener Selection

The maximum voltage for the TPS54240 is 42 V, therefore the input voltage to the converter is limited to 39 V. Q2 and D2 form a linear regulator that clamps the voltage at 39 V if the input goes higher. To be able to handle 40-V surges, a 60-V, P-Channel FET is chosen. This provides some margin on the input voltage spikes and not exceed the VDS of the FET. Care must also be taken to ensure that the SOA of the FET is not exceeded. For this case, a FDC5614P from Fairchild is used. The Zener diode D2 sets the regulation voltage point, so a 39-V part is used. The other components (Q1, D100, R2, R4, R6, R10, and C101) provide the bias and control for the gate of the FET.

3 Switching Power Supply Specifications Using the TPS54240

Consider the following system parameters:

- Output Voltage 5 V
- Transient Response 1-A to 2-A load step Vout between 4.75 V and 5.25 V (5%)
- Output Current 500 mA for USB, 700 mA for iPhone, 2.1 A for iPhone™ (DC)
- Input Voltage 12 V nom. 8 V to 40 V
- Output Voltage Ripple 1% of Vout
- Start Input Voltage (rising VIN) 8 V
- Stop Input Voltage (falling VIN) 6 V

NOTE: All the equations given in the following design examples come from TPS54240 (SLVSAA6) data sheet. For detailed variable names and assumptions refer to the data sheet.

3.1 Switching Frequency

Higher switching frequencies enable the use of smaller (and cheaper) output filter components whereas lower switching frequencies tend to have higher efficiencies. To meet both the size requirements as well as thermal requirements, a suitable switching frequency must be a compromise. The TPS54240 can be operated at switching frequencies from 100 kHz to 2500 kHz.

The following equations impose limits over the maximum switching frequency:

1. **To avoid pulse-skipping:** As the frequency is increased, the on time for a given duty cycle is decreased (D = T ON × f sw). For consistent switching action without pulse skipping, the on time must be greater than the minimum controllable on time. For the TPS54240, this minimum controllable on time is typically 135 ns.
2. **Frequency Foldback:** During overcurrent conditions, the output voltage decreases as the overcurrent protection is activated. As the foldback voltage at VSENSE decreases below 0.6 V, the switching frequency is reduced by 50% of the nominal value. At a VSENSE voltage of 0.4 V, the switching frequency is reduced to 25%, and finally when the VSENSE voltage falls below 0.2 V, the switching frequency is reduced to 12.5% of the nominal set frequency. This is done so that in any individual switching cycle, sufficient time is available for the inductor current to ramp below the overcurrent threshold. This feature is known as Frequency Foldback.

$$f_{SW(max\,skip)} = \left(\frac{1}{t_{ON}}\right) \times \left(\frac{(I_L \times Rdc + V_{OUT} + Vd)}{(V_{IN} - I_L \times Rhs + Vd)}\right) \quad (1)$$

$$f_{SW(shift)} = \frac{fdiv}{t_{ON}} \times \left(\frac{(I_L \times Rdc + V_{OUTSC} + Vd)}{(V_{IN} - I_L \times Rhs + Vd)}\right) \quad (2)$$

Where:

I_L = inductor current
R_{DC} = inductor resistance
V_{INMAX} = maximum input voltage
V_{OUT} = output voltage
V_{OUTSC} = output voltage during short
I_{OUTS} = output short circuit current Vd = diode voltage drop
$R_{DS(on)}$ = switch on resistance
t_{ONmin} = minimum controllable on time
$f$div = frequency division factor (1, 2, 4, or 8)

Using Equation 1 and Equation 2, the maximum skip and shift frequencies are 3.38 MHz and 5.5 MHz, thus the switching frequency is less than 2.5 MHz (the lesser value of maximum skip and shift frequencies or 2.5 MHz).

This design uses a nominal switching frequency of 500 kHz to allow for high efficiency and good thermal performance. The switching frequency is set by placing a resistor, R5, from the RT/CLK pin to ground.

The value of the R5 is calculated by Equation 3:

$$RT\ (kOhm) = \frac{206033}{f\,sw\ (kHz)^{1.0888}} \quad (3)$$

For 500 kHz – switching frequency, R5 must be 237 kΩ.

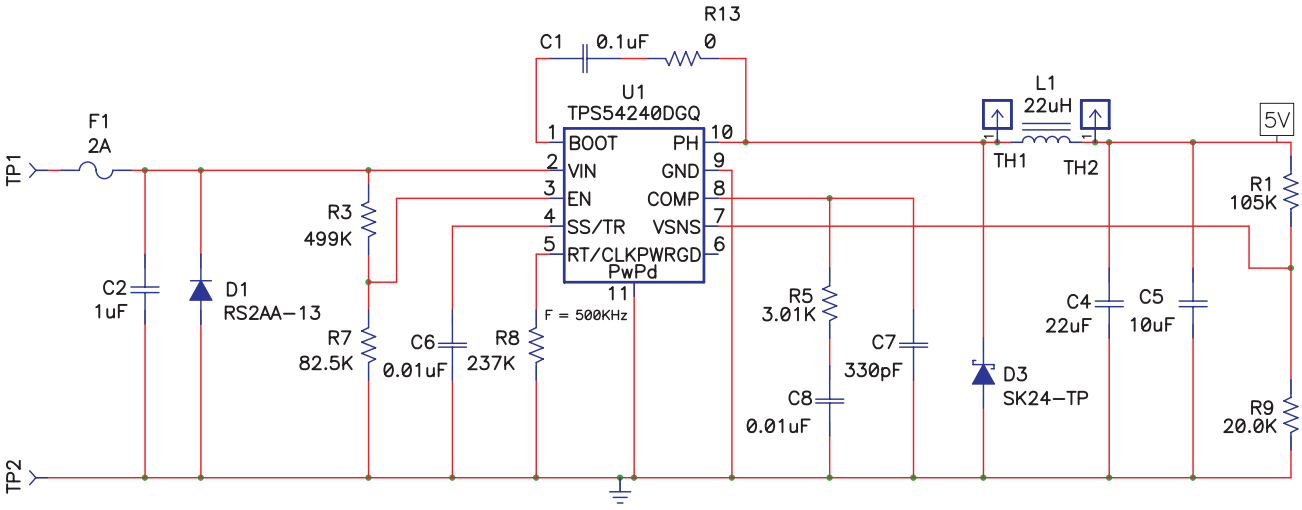

Figure 3. 5-V Output TPS54240 Design Example

3.2 Output Inductor Selection

The output inductor is typically selected so that the peak-to-peak ripple current is 30% of the output current. Verify that the RMS and saturation current ratings for the inductor exceed application specifications.

Once the inductor is chosen, the peak-to-peak inductor current can be calculated using Equation 5.

$$\text{Lo min} = \frac{\text{Vinmax} - \text{Vout}}{\text{Io} \times K_{IND}} \times \frac{\text{Vout}}{\text{Vinmax} \times \text{fsw}} \tag{4}$$

$$I_{RIPPLE} = \frac{V_{OUT} \times (\text{Vinmax} - V_{OUT})}{\text{Vinmax} \times L_O \times f_{SW}} \tag{5}$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from:

$$I_{L(rms)} = \sqrt{(I_O)^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (\text{Vinmax} - V_{OUT})}{\text{Vinmax} \times L_O \times f_{SW}} \right)^2} \tag{6}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{7}$$

Using a Kind of 2, the required minimum inductor is calculated to be 20.8 µH. The nearest standard value inductor is 22 µH. The rms current rating is 3.5 A, and the saturation current rating is 3.6 A before a 20% drop in inductance. The calculated peak-to-peak ripple current, rms current, and peak currents are 390 mA, 2.1 A, and 2.3 A.

3.3 Output Capacitor

The output capacitor determines the modulator pole, the output voltage ripple, and response of the regulator to a large change in load current. It needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor (Cout = C4 || C5) needs to supply the load with current when the regulator can not.

$$\text{Cout} > \frac{2 \times \Delta\text{Iout}}{\text{fsw} \times \Delta\text{Vout}} \tag{8}$$

For this example, the transient load response is specified as a 5% change in Vout for a load step from 1 A to 2 A. Thus, ΔIout = 1 A and ΔVout = 0.05 × 5 = 0.250 V. Using these numbers gives a minimum capacitance of 9 µF.

When the load current rapidly decreases, the stored energy in the inductor produces an output voltage overshoot. To absorb this energy, the output capacitor needs to be sized properly, thereby maintaining the desired output voltage during these transient periods. Equation 9 is used to calculate the minimum capacitance required to keep the output voltage overshoot to a desired value.

$$\text{Cout} > \text{Lo} \times \frac{\left(\text{Ioh}^2 - \text{Iol}^2\right)}{\left(\text{Vf}^2 - \text{Vi}^2\right)} \tag{9}$$

Where L is the value of the inductor, I_{OH} is the output current under heavy load, I OL is the output under light load, Vf is the final peak output voltage, and Vi is the initial capacitor voltage. For this example, the worst-case load step is from 2 A to 0.1 A. The output voltage increases during this load transition and the stated maximum in our specification is 5% of the output voltage. This makes Vf = 1.05 × 5 = 5.25.

Vi is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 9 yields a minimum capacitance of 26 µF.

Equation 10 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, $V_{ORIPPLE}$ is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. The maximum ESR an output capacitor can have to meet the output voltage ripple specification is calculated using following:

$$\text{Cout} > \frac{1}{8 \times f\text{sw}} \times \frac{1}{\frac{V_{ORIPPLE}}{I_{RIPPLE}}} \tag{10}$$

Equation 11 indicates the ESR is less than 75 mΩ. The most stringent criterion for the output capacitor is found to be 26 µF of capacitance to keep the output voltage in regulation during a load transient.

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} \tag{11}$$

Additional capacitance de-ratings for aging, temperature, and dc bias must be factored, which increases this minimum value. For this example, a 22-µF and 10-µF, 10-V ceramic capacitors with 3 mΩ of ESR are used.

Using Equation 12 the total rms current in the output capacitors is calculated. For this application, following equation yields 115 mA.

$$\text{Icorms} = \frac{\text{Vout} \times (\text{Vin max} - \text{Vout})}{\sqrt{12} \times \text{Vin max} \times \text{Lo} \times f\text{sw}} \tag{12}$$

The ceramic capacitor used has an rms current rating of 2 A.

3.4 Catch Diode

The selected diode must have a reverse voltage rating equal to or greater than Vinmax. The peak current rating of the diode must be greater than the maximum inductor current. The diode must also have a low forward voltage.

For the example design, the SK24-TP Schottky diode with 40V reverse voltage is selected for its lower forward voltage and it comes in a smaller package size which has good thermal characteristics. The typical forward voltage of the SK24-TP is 0.55 V.

During the converter on time, the output current is provided by the internal switching FET. During the off time, the output current flows through the catch diode. The average power in the diode is given by Equation 13:

$$\text{Pd} = \frac{(\text{Vin max} - \text{Vout}) \times \text{Iout} \times \text{Vfd}}{\text{Vin max}} + \frac{\text{Cj} \times f\text{sw} \times (\text{Vin} + \text{Vfd})^2}{2} \tag{13}$$

The SK24-TP has a junction capacitance of 50 pF. The selected diode dissipates up to 0.75 W, as the package is rated at 20°C/W.

3.5 Input Capacitor

The TPS54240 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54240. The input ripple current can be calculated using Equation 14:

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{\text{Vout}}{\text{Vin min}} \times \frac{(\text{Vin min} - \text{Vout})}{\text{Vin min}}} \tag{14}$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15:

$$\Delta\text{Vin} = \frac{\text{Iout max} \times 0.25}{\text{Cin} \times f\text{sw}} \tag{15}$$

3.6 Slow Start Capacitor

The slow start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Using the slow-start time as 3.5 ms, the value of slow-start capacitor is computed with the help of Equation 16 to be 8.75 nF. For this design, the next larger standard value of 10 nF is used.

$$\text{Tss} > \frac{\text{Cout} \times \text{Vout} \times 0.8}{\text{Issavg}} \tag{16}$$

Where:

Issavg = Average slow start current
Tss = Minimum slow start time

3.7 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. The capacitor must have a 10V or higher voltage rating.

3.8 Undervoltage Lockout Set Point

The programmable UVLO and enable voltages are set using the resistor divider of R1 and R4 between Vin and ground to the EN pin. Equation 17 and Equation 18 can be used to calculate the necessary resistance values.

For the example application, a 200 kΩ between Vin and EN (R3) and a 34.8 kΩ between EN and ground (R7) are required to produce the 8 V and 6 V start and stop voltages.

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS}} \tag{17}$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1} \tag{18}$$

Where I_{HYS} = 2.9 µA and I_1 = 0.9 µA.

3.9 Output Voltage and Feedback Resistors Selection

For the example design, 20 kΩ was selected for R9 and R1 was calculated to be 105 kΩ using Equation 19:

$$R1 = R2 \times \left(\frac{Vout - 0.8V}{0.8\ V} \right) \quad (19)$$

3.10 Compensation

To stabilize the closed-loop circuit, a compensation network is required. The compensation components are connected from the COMP pin to GND. For this example, some simplifying assumptions are made so as to ease the design procedure.

To properly compensate the closed-loop circuit, the gain characteristics of the power stage must be determined. In general, the power stage pole, and the power stage zero frequency must be known. These terms are defined as follows:

$$fp\ mod = \frac{Ioutmax}{2 \times \pi \times Vout \times Cout} \quad (20)$$

$$fz\ mod = \frac{1}{2 \times \pi \times Resr \times Cout} \quad (21)$$

For Cout, a de-rated value of 19 µF is used.

Use Equation 22 and Equation 23, to estimate a starting point for the crossover frequency, fco, to design the compensation.

For the example design:

fpmod is 3.52 kHz {V OUT = 5 V, I OUT = 2.1 A, C_{OUT} = 19 µF bias de-rated}

fzmod is 5584 kHz {Resr = 3 mΩ / 2 = 1.5 mΩ , C_{OUT} = 19 µF bias de-rated}

Equation 22 is the geometric mean of the modulator pole and the ESR zero and Equation 23 is the mean of modulator pole and the switching frequency.

$$f_{co} = \sqrt{f_p mod \times f_z mod} \quad (22)$$

$$f_{co} = \sqrt{f_p mod \times \frac{f_{sw}}{2}} \quad (23)$$

Equation 22 yields 140 kHz and Equation 23 gives 29.7 kHz. Using the lower value of Equation 22 or Equation 23 as the upper limit for an initial crossover frequency, the target cross-over frequency(f_{CO}) is 15 kHz.

Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

To determine the compensation resistor, R5, use Equation 24.

$$R5 = \left(\frac{2 \times \pi \times f_{CO} \times C_{OUT}}{gmps} \right) x \left(\frac{V_{OUT}}{V_{REF} \times gmea} \right) \quad (24)$$

Assume the power stage transconductance, gmps, is 10.5 A/V. The output voltage, V_O, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 5 V, 0.8V and 310 mA/V, respectively.

R5 is calculated to be 2.94 kΩ, use the nearest standard value of 3.01 kΩ. Use Equation 25 to set the compensation zero to the modulator pole frequency. Equation 25 yields 0.016 µF for compensating capacitor C8, a 0.01 µF is used for this design.

$$C8 = \frac{1}{2 \times \pi \times R4 \times f_p mod} \quad (25)$$

A compensation pole can be implemented if desired using an additional capacitor C7 in parallel with the series combination of R5 and C8. Use the larger value of Equation 26 and Equation 27 to calculate C7 to set the compensation pole. 330 pF is selected for C7.

$$C7 = \frac{C_O \text{ x } Resr}{R4} \quad (26)$$

$$C7 = \frac{1}{R4 \times f_{sw} \times \pi} \quad (27)$$

4 Current Limit Switch Specifications Using the TPS2540

The TPS2540 is operated as a dedicated charging port. Two modes are used, divider mode and BC1.2 mode. Divider mode is used to charge Apple devices. BC1.2 mode is used to charge any BC1.2 mode device that can include Android phones, Blackberry phones, and other compliant devices. As an optional feature, a LED (D4) provides a status indicator.

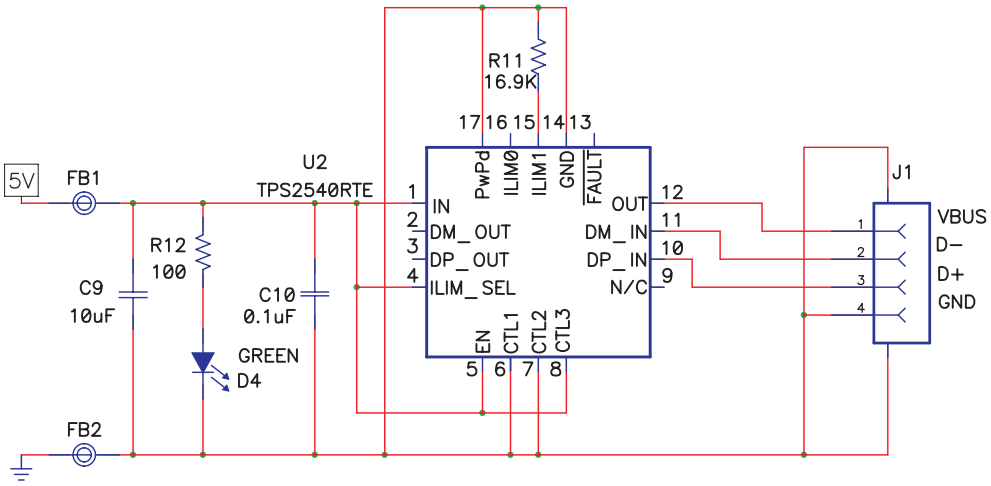

Figure 4. 5-V Output TPS2540 Design Example

4.1 Selecting the Current Limit Resistor

R11 is used to set the current limit for the switch. The current limit is set to the maximum value to ensure that the device is able to provide the full 2.1 A for charging. Equation 28 is used to calculate the nominal short-circuit protection level. Equation 29 and Equation 30 calculate the minimum and maximum protection levels

$$I_{SHORT} = \frac{48000}{R_{ILIMx}} \quad (28)$$

$$I_{SHORT\_min} = \frac{48000}{R_{ILIMx}^{1.037}} \quad (29)$$

$$I_{SHORT\_max} = \frac{48000}{R_{ILIMx}^{0.962}} \quad (30)$$

4.2 Connecting the D+/D- Data Lines

Because the TPS2540 is used to emulate a wall adapter, it is configured as a Dedicated Charging Port (DCP). The D+/D- lines are not used to transmit data. Inside the iPhone the charging circuit looks for a specific voltage on the D+ and D– lines to ensure that it can pull the full amount of current. If it does not see these voltages it only pulls 100 mA. The iPhone charger puts 2 V on the D+ line and 2.7 V on the D– line. If an Apple device is not connected to the DCP, the TPS2540 uses an auto detect feature that then shorts the data lines together to provide maximum charge current for other devices.

5 Experimental Results

Figure 4 to Figure 22 show the experimental test results of the Figure 3 design. The input current draw at no load at 12-V input voltage is 10 mA (most of which is powering the optional LED).

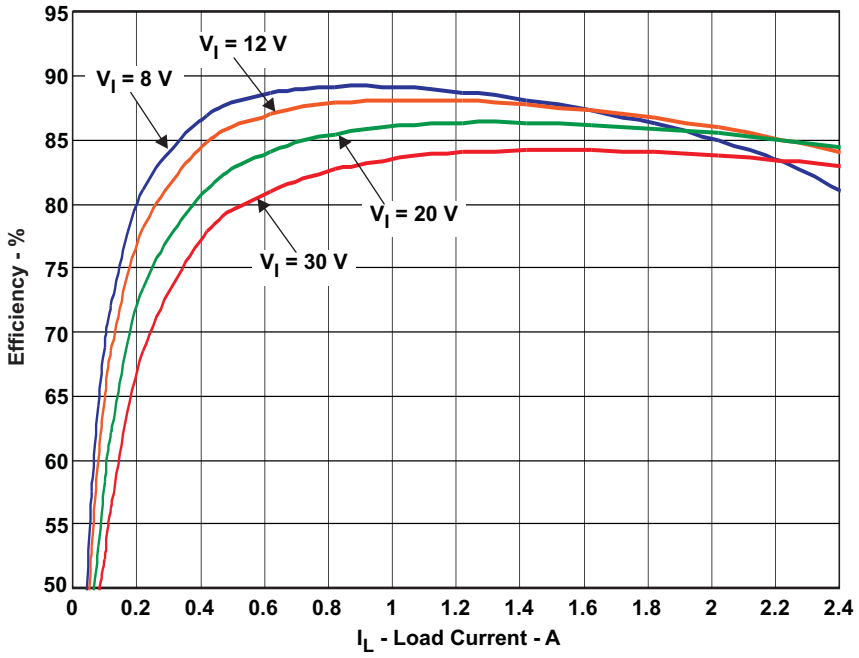

Figure 5. Efficiency vs Load Current Prior to the Load Switch

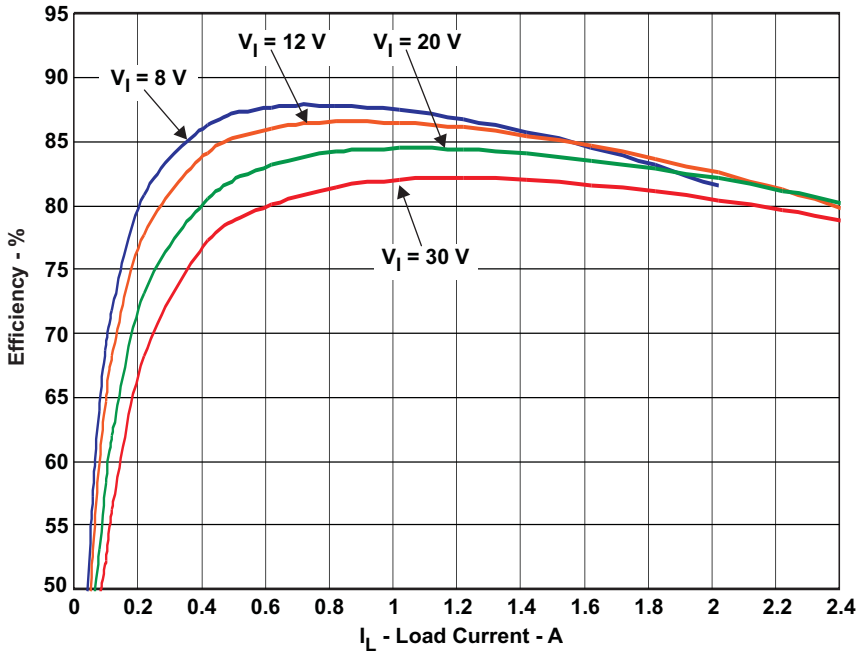

Figure 6. Efficiency vs Load Current After the Load Switch

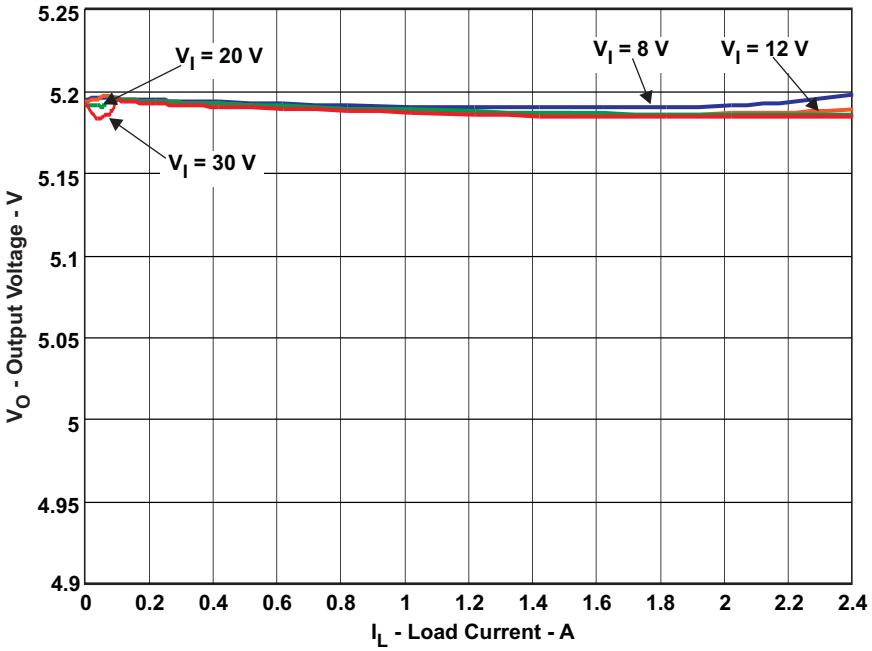

Figure 7. Output Voltage vs Load Current Before the Switch

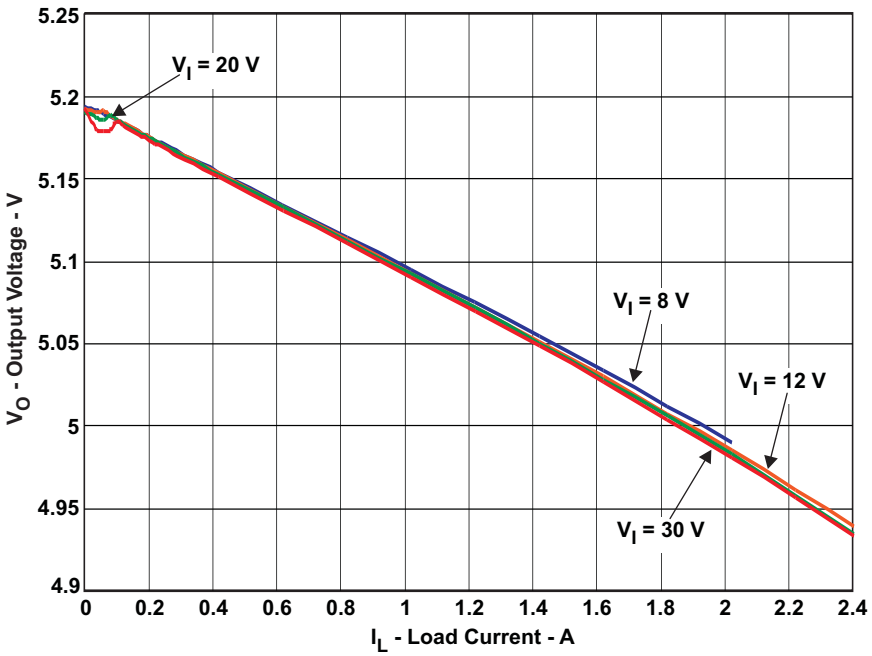

Figure 8. Output Voltage vs Load Current After the Switch

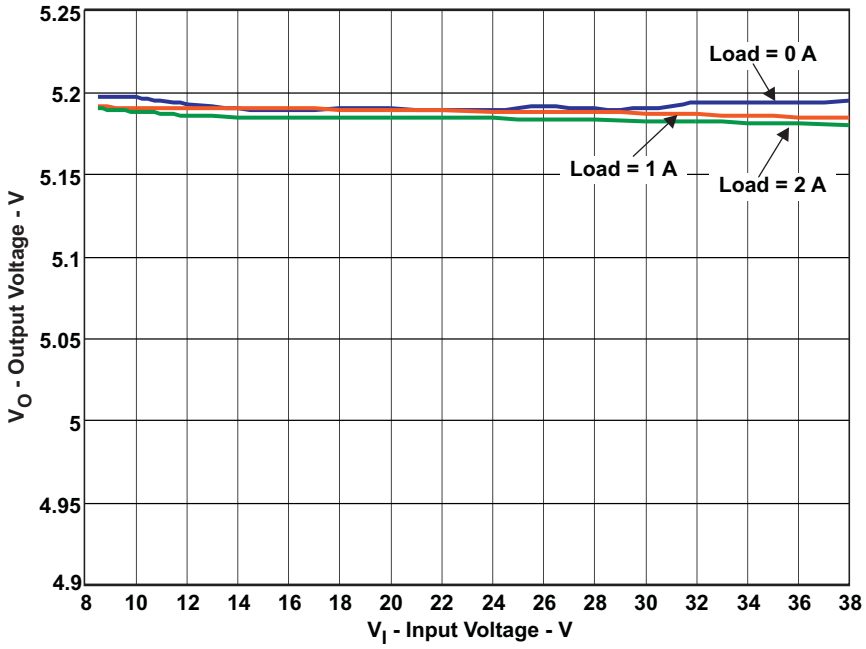

Figure 9. Output Voltage vs Input Voltage

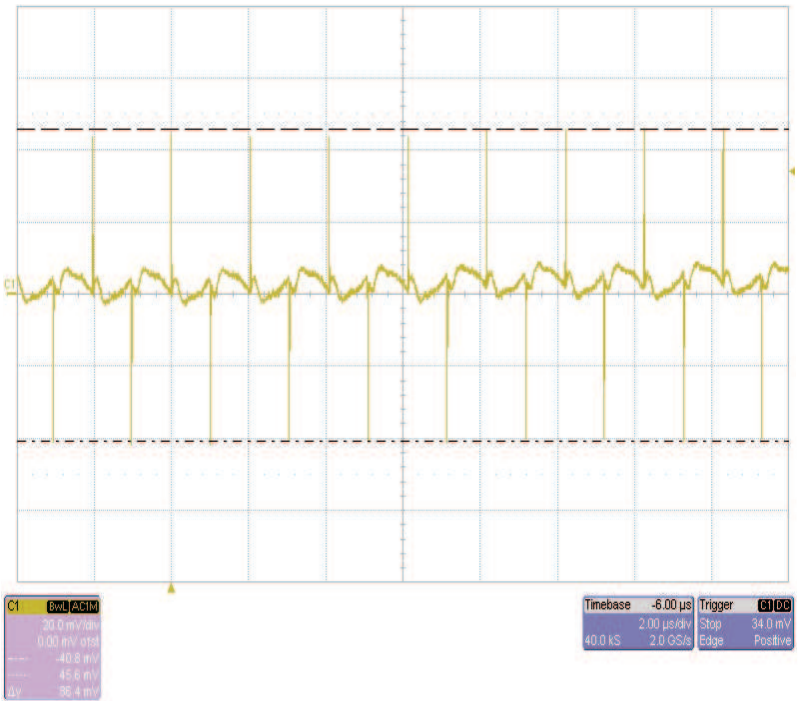

Figure 10. Output Voltage Ripple Before the Switch, Iout = 2

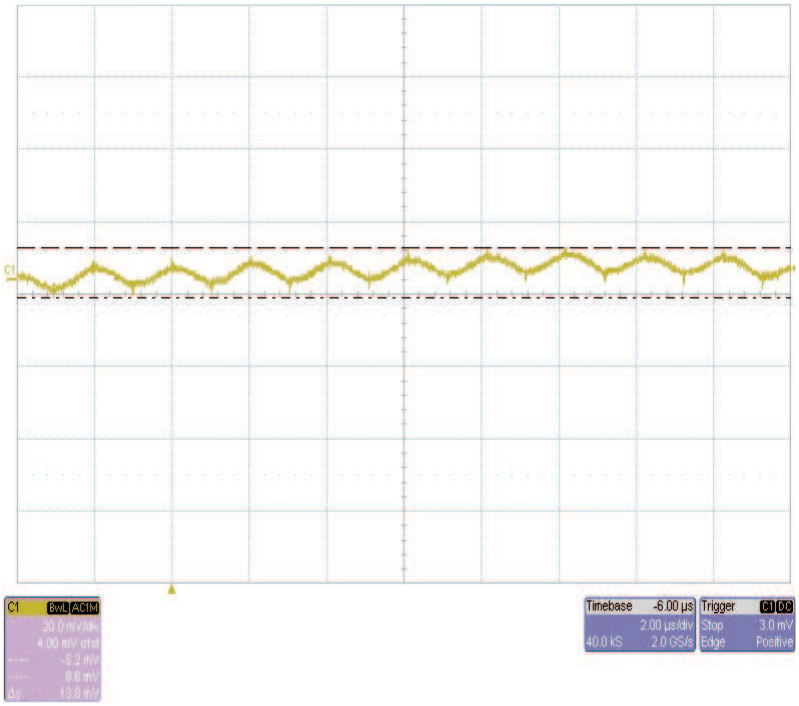

Figure 11. Output Voltage Ripple After the Switch, Iout = 2 A

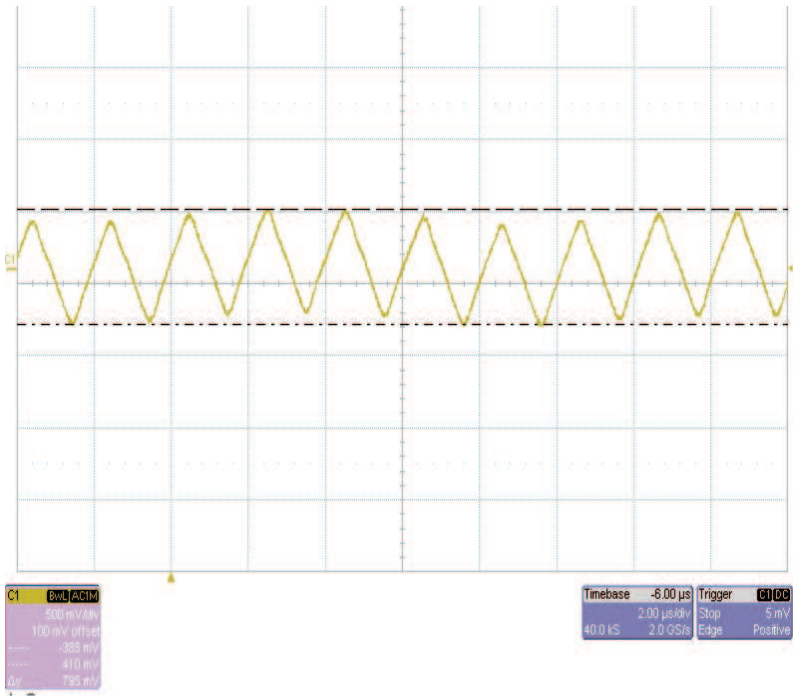

Figure 12. Input Voltage Ripple, Iout = 2 A

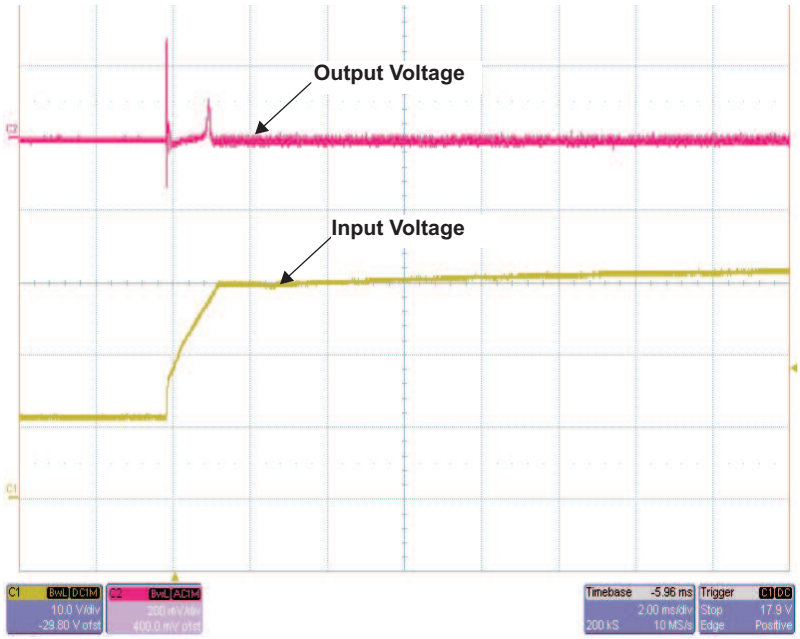

Figure 13. Line Transient, Vin 12-V to 30-V Step

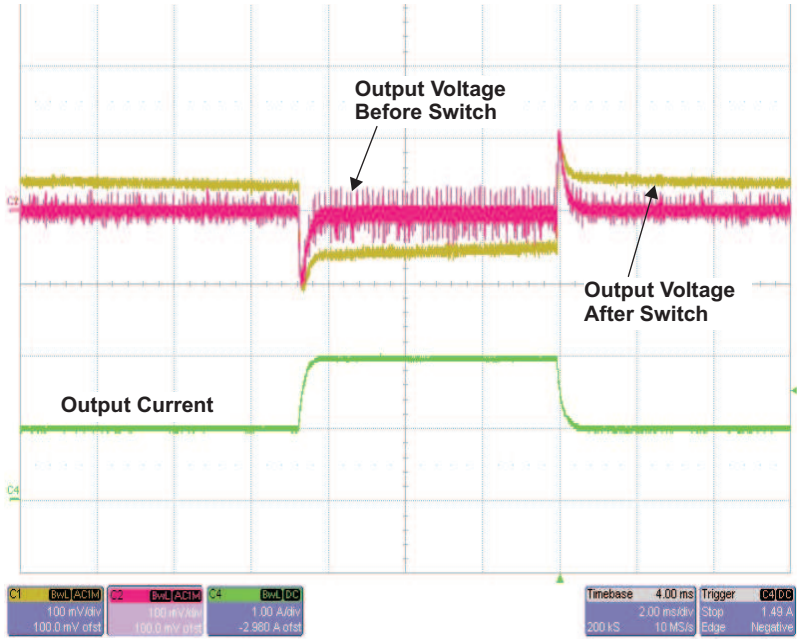

Figure 14. Load Transient 1-A to 2-A Step

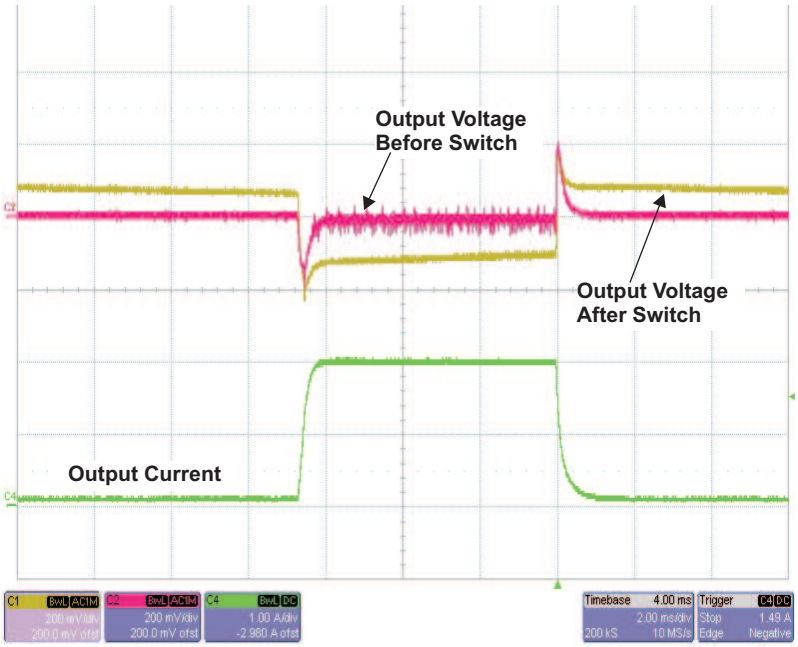

Figure 15. Load Transient 0.1-A to 2-A Step

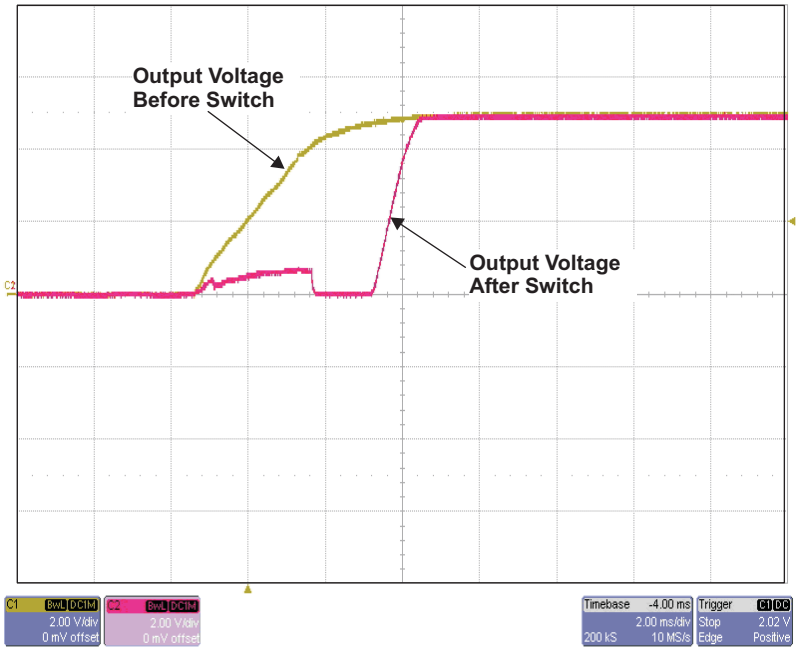

Figure 16. Start-Up Relative to VIn

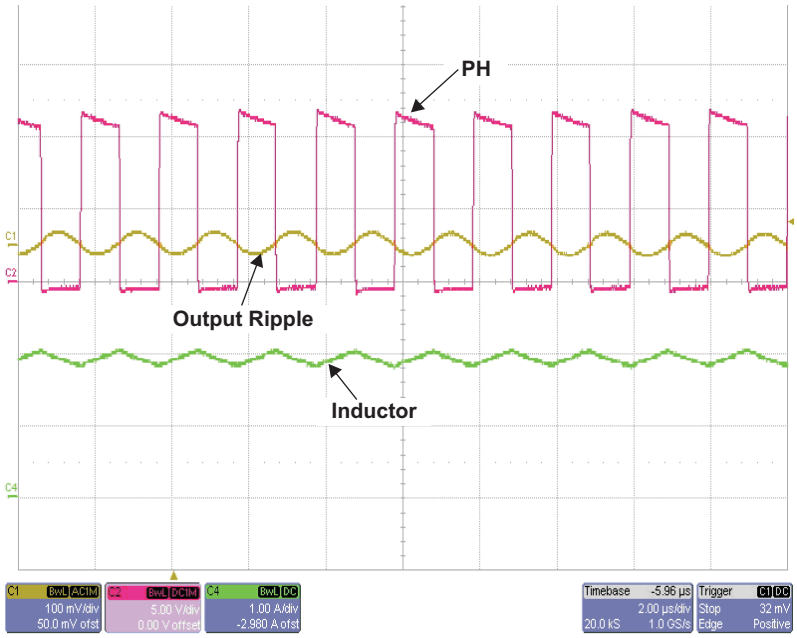

Figure 17. Vout, Inductor Current and PH, CCM

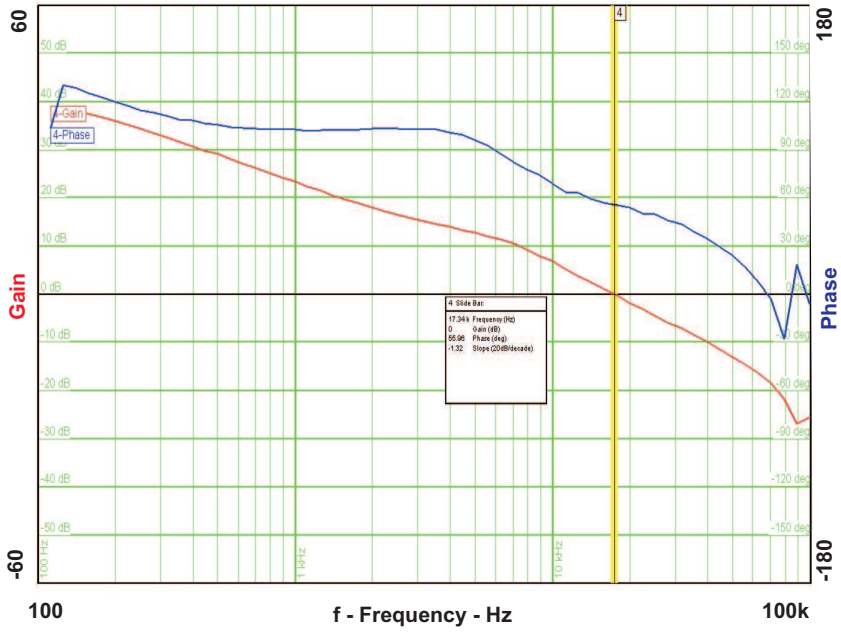

Figure 18. Overall Loop Frequency Response, Iout = 2 A

6 Board Layout

This section provides a description of the board layout and layer illustrations. The board layout for the reference designs is shown in Figure 19 through Figure 22. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for VIN, VOUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54240 and a large area filled with ground. The bottom layer contains ground and a signal route for the BOOT capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including six vias directly under the TPS54260

device to provide a thermal path from the top-side ground area to the bottom-side ground plane. The input decoupling capacitor (C3) and bootstrap capacitor (C1) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper VOUT trace past the output capacitors.

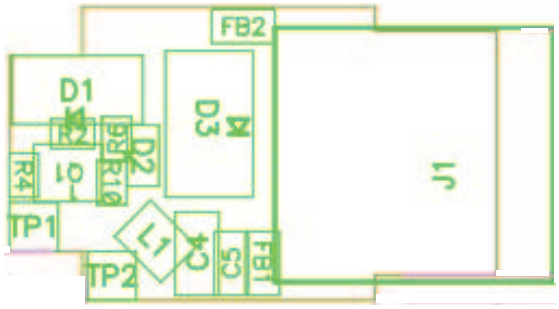

Figure 19. PMP5951 Top-Side Assembly

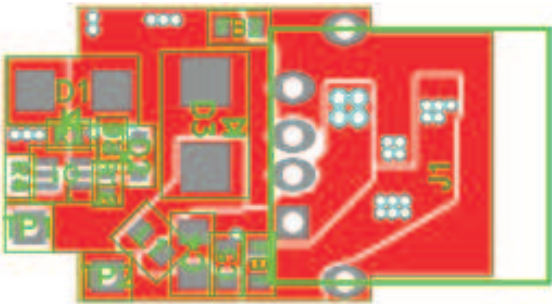

Figure 20. PMP5951 Top-Side Layout

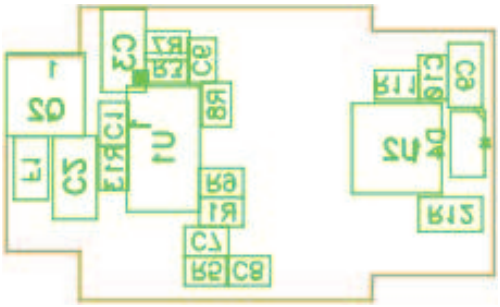

Figure 21. PMP5951 Bottom-Side Assembly

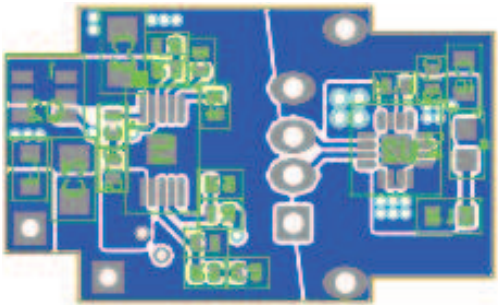

Figure 22. PMP5951 Bottom-Side Layout

Table 1. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	Mfr
2	C1, C10	0.1 µF	Capacitor, Ceramic, 16V, X7R, 10%	0402	Std	Std
1	C101	47 pF	Capacitor, Ceramic, 16V, X7R, 10%	0402	Std	Std
2	C2, C3	1 µF	Capacitor, Ceramic, 50V, X7R, 10%	0805	Std	Std
1	C4	22 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	Std	Std
2	C5, C9	10 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	Std	Std
2	C6, C8	0.01 µF	Capacitor, Ceramic, 16V, X7R, 10%	0402	Std	Std
1	C7	330 pF	Capacitor, Ceramic, 16V, X7R, 10%	0402	Std	Std
1	D1	RS2AA-13	Diode, Rectifier, 1.5-A, 50-V	SMA	Std	Std
1	D100	15 V	Diode, Zener, 15V, 100-mA, 200mW	SOD-523	MM5Z15VT1	On Semi
1	D2	39 V	Diode, Zener, 39V, 100-mA, 200mW	SOD-523	MM5Z39VT1	On Semi
1	D3	SK24-TP	Diode, Schottky, 2-A, 40-V	SMB	SK24-TP	Std
1	D4	GREEN	Diode, LED, Green, 2-V, 20-mA	0603	LTST-C190KGKT	Lite On
1	F1	2A	Fuse, Axial, Fast Acting, 2A	0603	F0603E3R00FSTR	AVX
2	FB1, FB2	26ohms	Bead, SMD Ferrite, 26ohms @ 100MHz, 10mohm DC, 6A	0603	BLM18KG260TN1D	Murata
1	J1	C-292303-x	Connector, USB TH	14.0 x 14.0 mm	C-292303-x	Tyco
1	L1	22 µH	Inductor, Torroid 8mm, 25 turns #24AWG	8 x 3 mm	T38-52 Core	MicroMetals
1	Q1	MMDT3946	Transistor, Dual NPN, 60V, 200mA, 200mW	SC-70[SOT-363]	MMDT3946	Diodes
1	Q2	FDC5614P	MOSFET, Pch, -60V, 3.4A , 105-milliOhms	TSOP-6	FDC5614P	Fairchild
1	R1	105K	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R10	1.00K	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R11	16.9K	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R12	100	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R13	0	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R2	200K	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R3	499K	Resistor, Chip, 1/16W, 1%	0402	Std	Std
2	R4, R9	20.0K	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R5	3.01K	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R6	100K	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R7	82.5K	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	R8	237K	Resistor, Chip, 1/16W, 1%	0402	Std	Std
1	U1	TPS54240DGQ	IC, 3.5V-42V Stepdown SWIFT™, DC-DC Converter With ECO-Mode	MSOP-10	TPS54240DGQ	TI
1	U2	TPS2540RTE	IC, USB CHARGING PORT POWER SWITCH & CONTROLLER	QFN-16	TPS2540RTE	TI

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