

1 Operations

The Power supply system has been tested in all his functionalities, according to the specifications on Rev.1.0 dated 10th July 2007 and their update dated 1st November 2007.

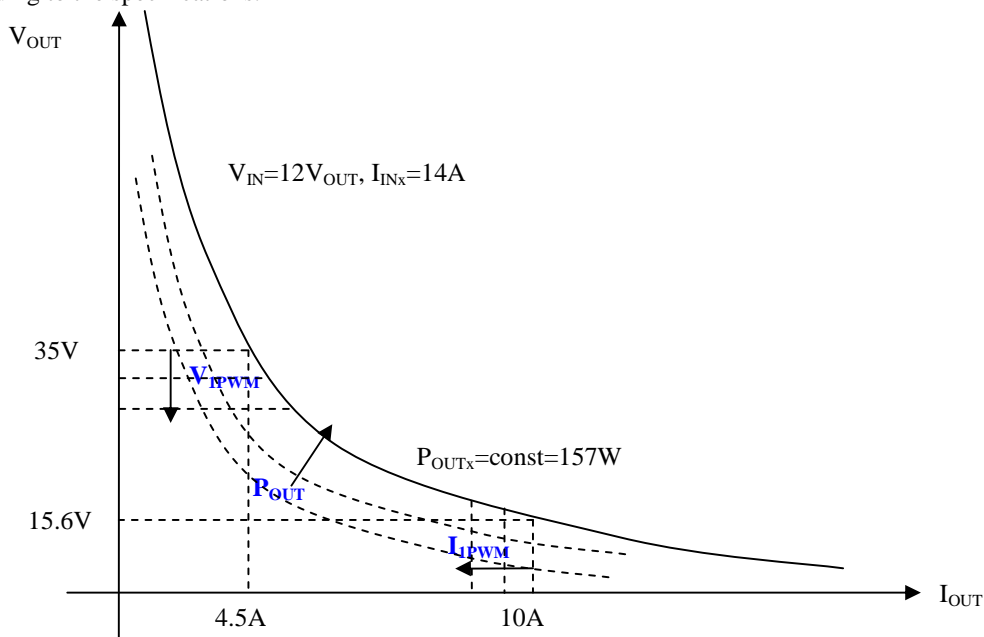
The schematic and layout of the tested board including all the introduced modifications are in Rev.D.

Fixed Outputs (Specs Par.3.2) with current limitation, have been tested with the following results:

Vin[V]	Vout[V]	Iout[mA]	Pout[W]	$\eta\%$
3.3	3.078	3	9.23	93.27
3.3	3.012	3.69	11.11	
3.3	3.007	3.77	11.34	
3.3	2.994	3.82	11.44	
3.3	2.985	3.91	11.67	
3.3	1.7	2.4	4.08	
3.3	0.41	2.05	0.84	
Vin[V]	Vout[V]	Iout[mA]	Pout[W]	$\eta\%$
5.17	5.03	3.04	15.29	97.29
5.17	4.89	3.36	16.43	
5.17	4.77	3.82	18.22	
5.17	4.66	3.95	18.41	
5.17	3.28	2.96	9.71	
5.17	3.07	2.72	8.35	
5.17	1.143	2.347	2.68	

The second value for each output voltage gives the start of output current limitation, which follows a fold-back characteristic with tested possibility of OC reset form the micro (on the board also with manual switch).

For Variable Outputs (specs Par.3.1) the power stages test results are the object of the following paragraphs. They have been designed to satisfy the following summary operational characteristic curves, according to the specifications.



For simplicity and time reason in the following, all the results reported have been tested just on one Power stage (Sheet 1 of SCH, left side of PCB, left side of the board top side), because the two Power stages are symmetrical and identical. Complete characterization is performed at $V_{out}=25V$, while main eventual differences with other output voltage are reported.

The CV mode (Specs Par.5) has been tested with an external 0-5V 1kHz **20-80% duty cycle**, obtaining the V_{out} range from-to **8.53V - 34.40V** (not to the nominal 35V).

The CI mode has been tested with an external 0-5V 1kHz **20-80% duty cycle**, obtaining the range for reduced output current limitation from-to **2.1 A - 8.4A**, (not to the maximum 10A).

The circuit implements two types of current limitation, input (**14A**) and output (**10A**) current.

The measured input current limitation takes place at **14.1A**.

A set of measured results useful in the next paragraphs, for Output Voltage and Output Current limitation as a function of V_{IPWM} , of I_{IPWM} are the following:

V_{out}	V_{IPWM}	I_{out}	I_{IPWM}
8.5	20%	2.1	20%
14.5	35%	5.4	50%
25	60%	6.5	60%
34.5	80%	8.4	80%

Latch protection (cut-off) on Output current is implemented selecting manual switch S1 on the board, and it works with reset (switch S1 off) after its activation (overcurrent) when selected (switch S1 on).

1.2 Thermal considerations

All the Thermal measurement have been performed at $T_{amb}=25^{\circ}C$, with a forced ventilation of 40CFM imposed through the entire section of the board. Further, some extra heatsinks have been applied to the board close to the primary mosfets to simulate the use of a thicker PCB with multiple layers.

According to the specifications, T_{amb} up to $85^{\circ}C$, achieved results on Rev.D (details in the following, last paragraph) evidence the need of reduce the power losses per input mosfet.

The proposed solution is to duplicate both input mosfets than their relative drives.

Details are shown in the schematic Rev.E.

Thermal resistance junction to amb for each mosfet has to be less than $40^{\circ}C$.

To achieve this performance, we propose the following points:

- 1) realize the new board with $70\mu m$ (2OZ) copper thickness, four layers (mandatory), maximizing the input traces
- 2) to devote to primary mosfet drain a PCB area of at least 2.5 square inches, for all the four layers, introducing an adequate number of thermal vias of proper section, among the layers (mandatory).
- 3) to maintain a forced ventilation of 40CFM on the board (eventual according to reduced maximum ambient temperature).
- 4) The PCB layout can be simply derived form the actual one, just increasing the mosfet area, both on drains according to point 2. that sources, after duplicating their number and drives. The input traces of the power stage has to be also maximized to allow power dissipation.

To allow maximum ambient temperature operations, the actual board built on Rev.D has been limited in input at output current, to guarantee an acceptable maximum operating temperature on the overall range.

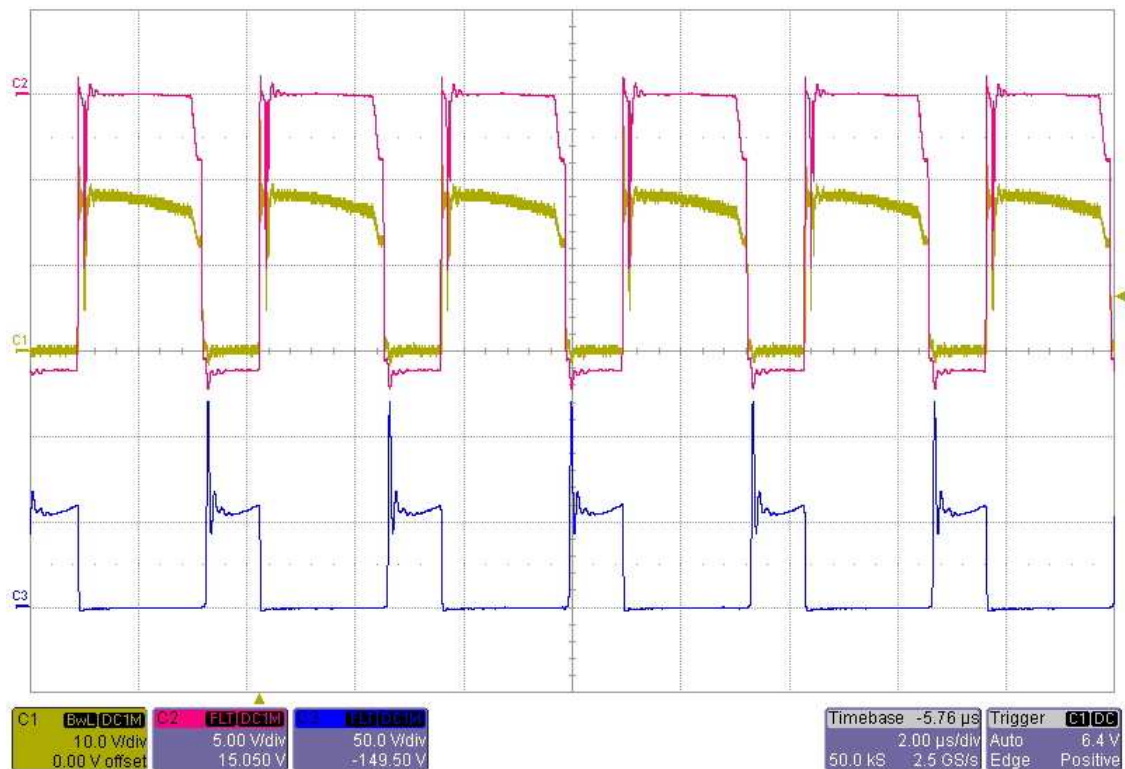
In particular, the output limitation has been set to **6.6A** ($I_{IPWM}=80\%$, $V_{IPWM}=60\%$, $V_{out}=25V$) (that's equivalent to 4.8A ($I_{IPWM}=80\%$, $V_{IPWM}=35\%$, $V_{out}=14.5V$)). This has been implemented with the following changes of components values on the board:

- $R_{58}=R_{63}=24\text{ k}\Omega$,
- $R_{17}=R_{16}=20\text{ k}\Omega$.

This variation compared to the schematic in Rev.D has been implemented just before delivering the board, while the test report has been realized with the board fully in line with Rev.D.

2 Main Waveforms

The converter is operating in Continuous Mode in most of its range of operation. At $V_{out}=25V$, the minimum current for Discontinuous current is $I_{out}=0.3A$. Switching frequency is $f_s=303kHz$. Waveforms for the main switches in CCM are in the following picture.

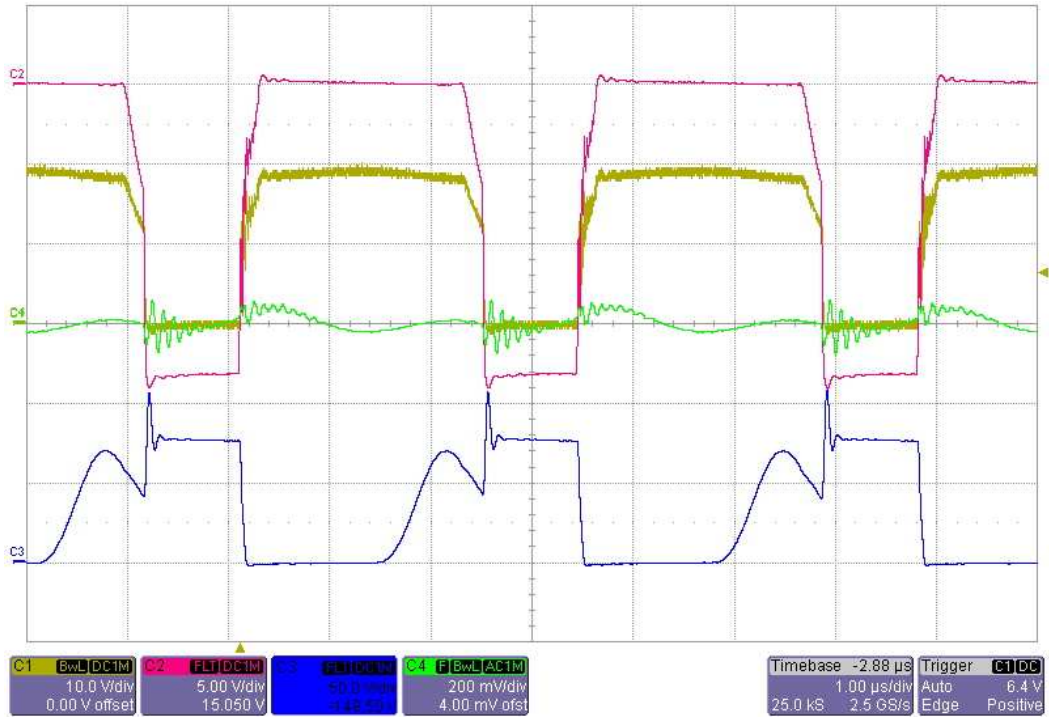


C1: Primary Mosfets Drain Voltage @ $V_{out}=25V$, $P_{out}=156W$

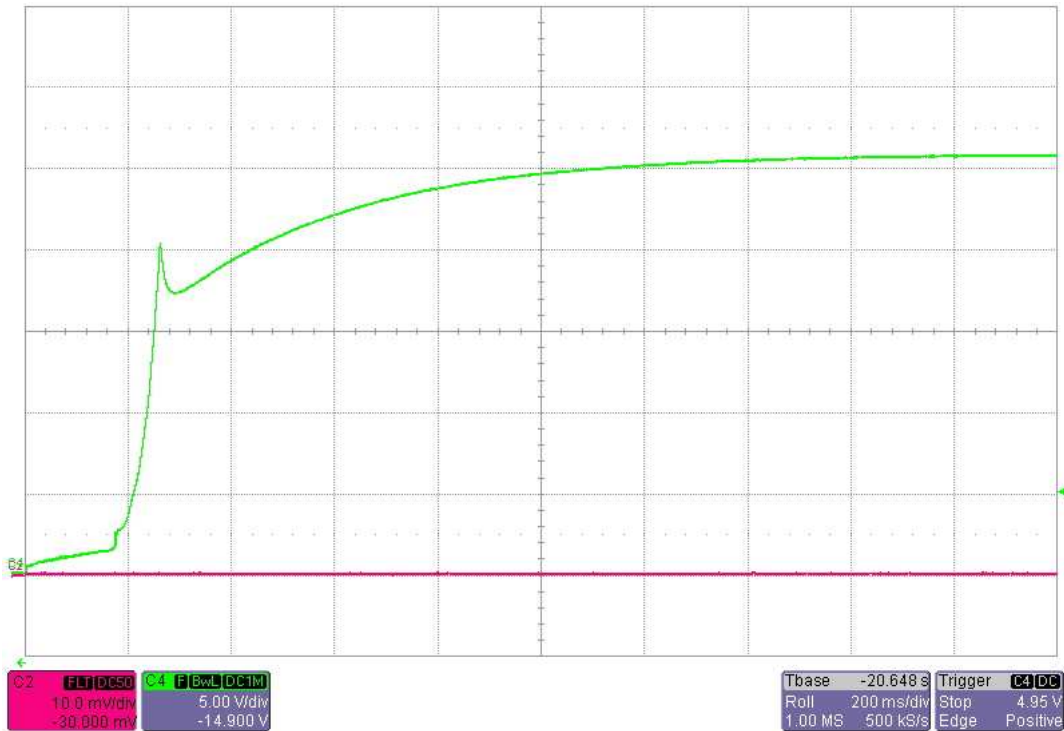
C2: Auxiliary (active clamp) Primary Mosfet Drain Voltage

C3: Output Diode Cathode Voltage

Same waveforms for the main switches in DCM are in the following picture.



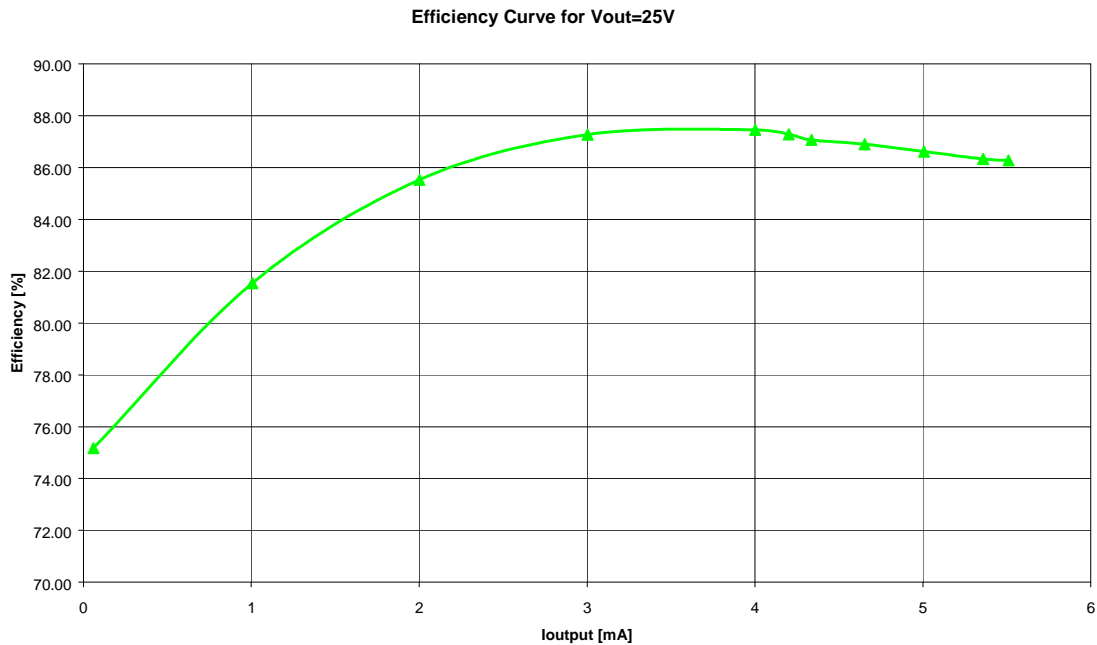
C1: Primary Mosfets Drain Voltage @ $V_{out}=25V$, $P_{out}=156W$
 C2: Auxiliary (active clamp) Primary Mosfet Drain Voltage
 C3: Output Diode Cathode Voltage



Start-up waveforms of the circuit, with Output full loads @ $V_{out} 25V$.

3 Efficiency

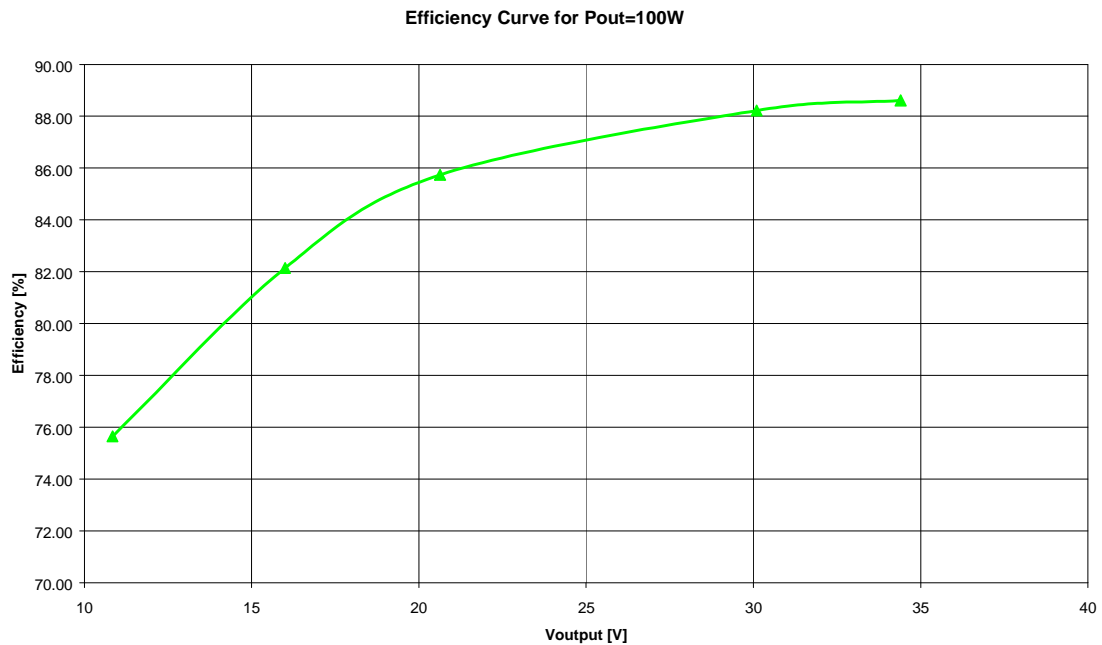
The efficiency diagram below as a function of the Output current is derived for $V_{out}=25V$ ($V_{IPWM}=60\%$).



The following table shows the measured values for $V_{in}=12V$, $V_{out}=25V$:

$V_{in}[V]$	$I_{in}[A]$	$V_{out}[V]$	$I_{out}[A]$	$P_{in}[W]$	$P_{out}[W]$	$\eta\%$
12.97	0.16	26	0.06	2.08	1.56	75.17
12.82	2.47	25.64	1.007	31.67	25.82	81.54
12.68	4.75	25.73	2.002	60.23	51.51	85.52
12.53	7.08	25.78	3.003	88.71	77.42	87.27
12.37	9.52	25.74	4.001	117.76	102.99	87.45
12.33	10.04	25.72	4.201	123.79	108.05	87.28
12.32	10.21	25.25	4.337	125.79	109.51	87.06
12.26	11.05	25.3	4.653	135.47	117.72	86.90
12.18	12.02	25.33	5.006	146.40	126.80	86.61
12.11	13	25.36	5.359	157.43	135.90	86.33
12.03	13.92	26.22	5.51	167.46	144.47	86.27

The efficiency diagram below as a function of the Output Voltage, is derived for a constant Output Power of about 100W, evidencing the different performances of the system with the different output voltages.

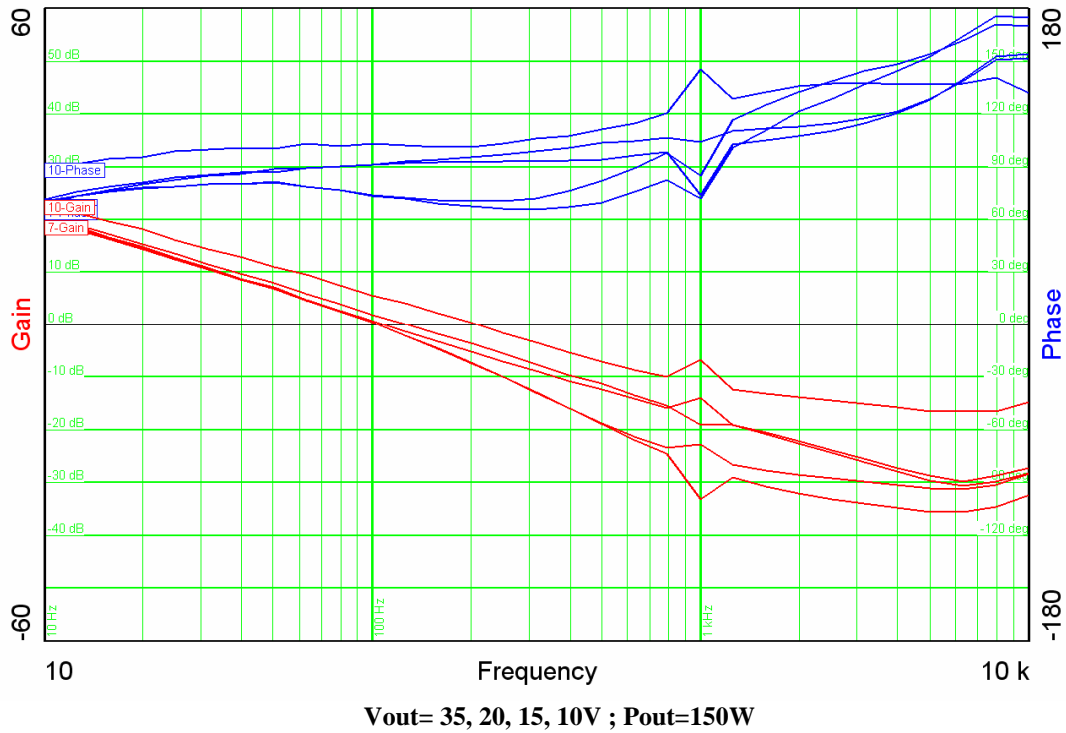
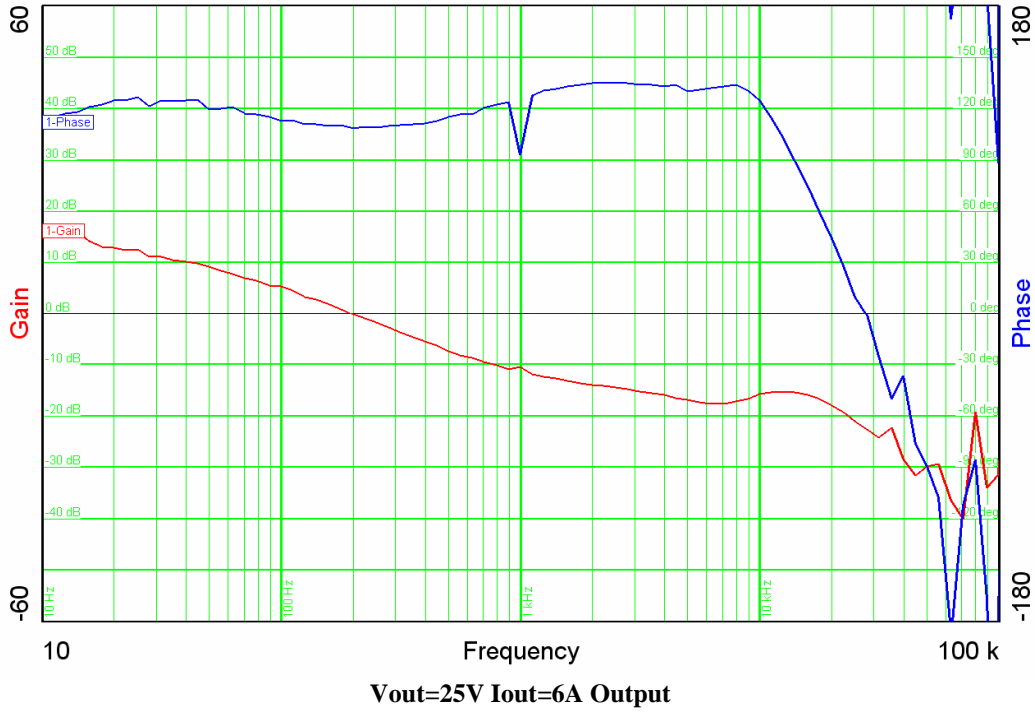


The following table shows the measured values for **Vin=12V, Pout=100W**:

Vin[V]	Iin[A]	Vout[V]	Iout[A]	Pin[W]	Pout[W]	η %
12.32	10.11	10.84	8.692	124.56	94.22	75.65
12.31	10.28	16	6.497	126.55	103.95	82.15
12.35	9.74	20.63	4.999	120.29	103.13	85.73
12.33	10.1	30.1	3.65	124.53	109.87	88.22
12.32	10.09	34.4	3.202	124.31	110.15	88.61

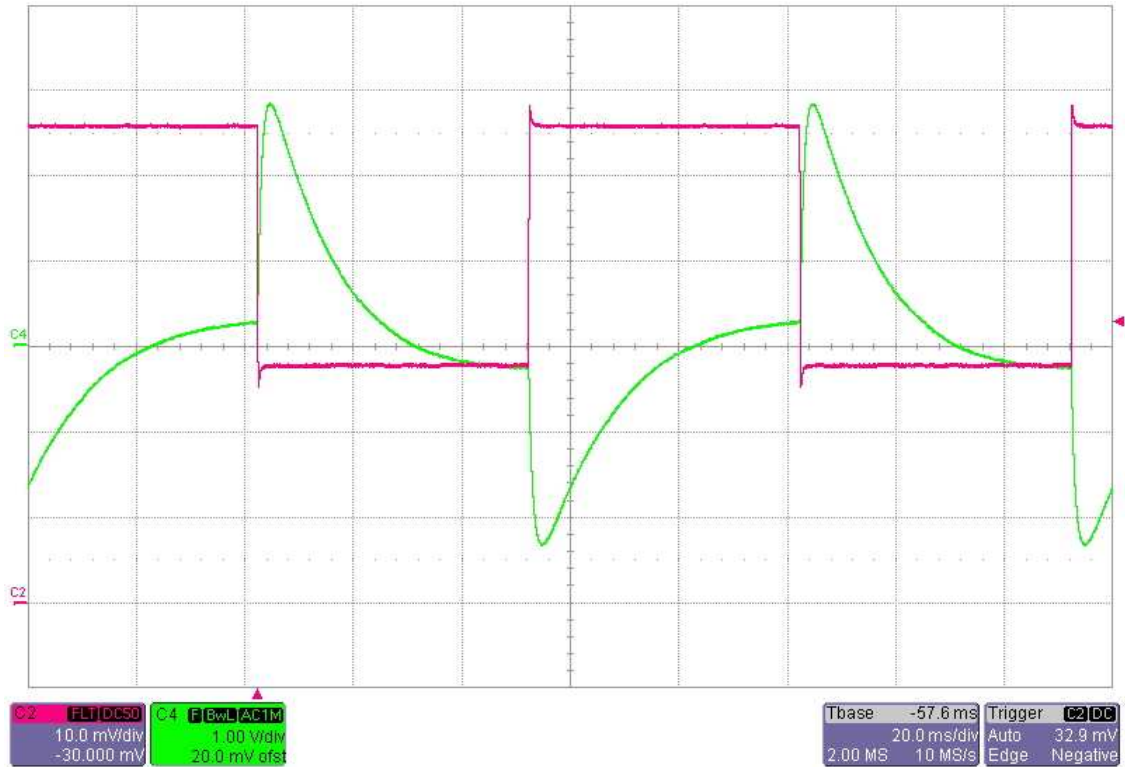
4 Control Loop Frequency Response

The figures below show the open loop response at full load on Output with different Output Voltage



5 Load Transients

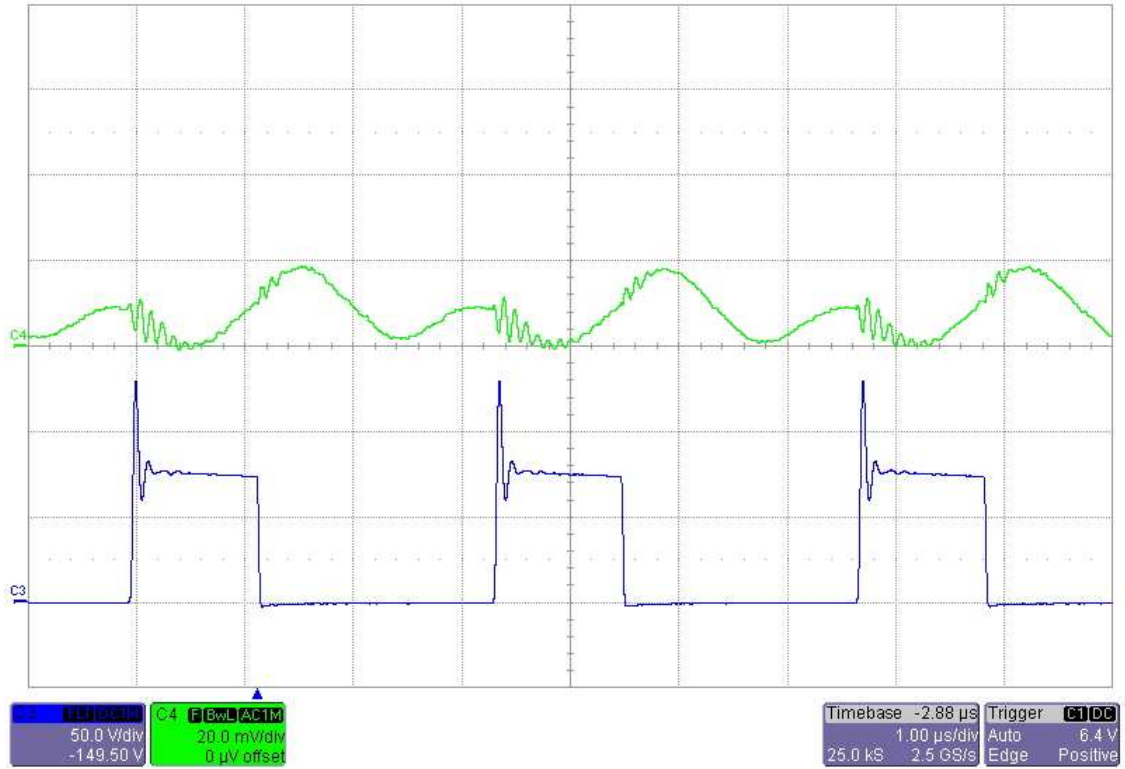
The figures below show the response to load transients. $V_{out}=25V$ The current on Output is stepping from 3 to 6A output load and viceversa.



CH2 Output Current Step load (10mV/1A), CH4 Output Voltage Changes (AC)

6 Output Ripple Voltage

The output ripple voltage is shown in the figure below, for the 25V Output Voltage at full load.



CH4: Output Voltage Ripple @ $V_{out}=25V$, $I_{out}=6A$

5 Thermal Images

The thermal images of the board (top) are shown in particular for the left side of the board where the first power stage is located.

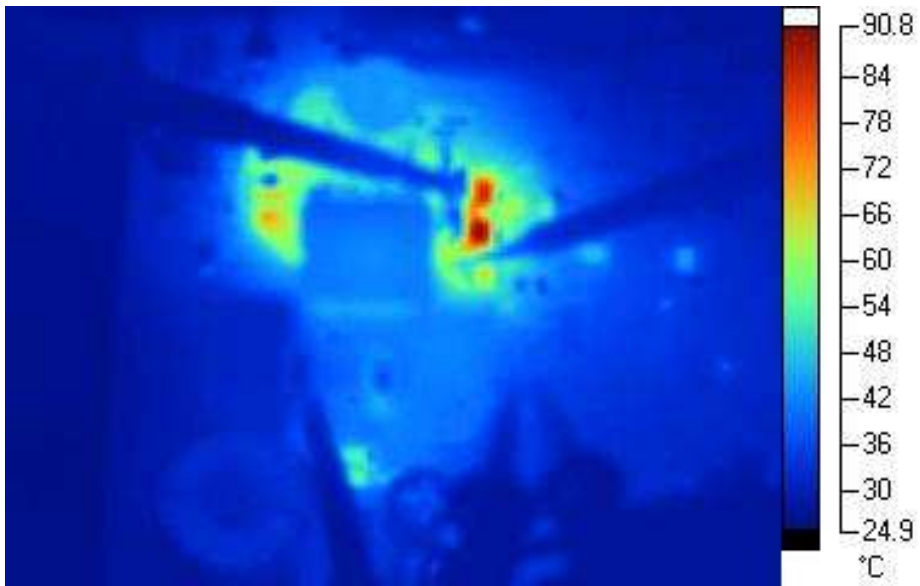
In the pictures, the two Fixed Outputs are turned off, because their thermal interaction is neglectable while their maximum reached temperature is lower than 60°C at full load, at $T_{amb}=25^{\circ}\text{C}$. The different pictures show different performances with increasing output power to full power at $V_{out}=25\text{V}$, at $T_{amb}=25^{\circ}\text{C}$, and the most stressful condition at lowest output voltage and increasing output current.



TOP Side Left side Power stage $P_{out}=115\text{W}$ @ $V_{out}=25\text{V}$ ($V_{IPWM}=60\%$)



TOP Side Left side Power stage $P_{out}=150\text{W}$ @ $V_{out}=25\text{V}$



TOP Side Left side Power stage Pout=100W @ Vout=14.5V ($V_{IPWM}=35\%$), Iout=7A

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