TI Designs：TIDA-01550
具有隔离 AFE 的多相分流计量参考设计

说明

此参考设计通过使用计量模拟前端 (AFE) 实现了具有隔离式分流传感器的 0.5% 级三相电能计量系统。计量 AFE 检测每个相位的电压和电流，计算相位的计量参数，然后通过一个数字隔离式 UART 端口将计算的参数发送到主机微控制器。该设计采用了用于隔离 UART 引脚的电容隔离技术和用于为计量 AFE 提供电源的电容压降电源，从而使得该无变压器设计能够抗磁篡改干扰。而且，由于计量参数是在计量 AFE 本地进行计算，而不是在主机微控制器上进行计算，因此计算计量值时占用的主机 CPU 带宽更低。

资源

TIDA-01550	设计文件夹
ISO7731	产品文件夹
MSP430i2041	产品文件夹
TLV704	产品文件夹
MSP432P4111	产品文件夹
TRS3232E-Q1	产品文件夹
ISO7721	产品文件夹
TPS709	产品文件夹

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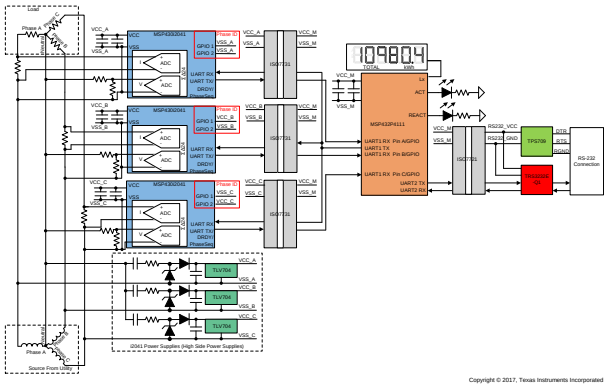
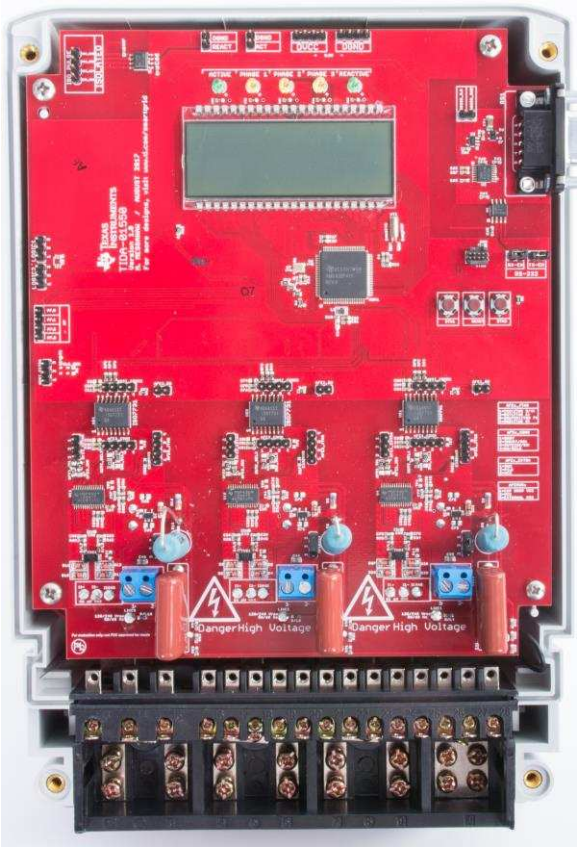


特性

- 使用隔离式、低成本电流和电压测量 AFE 实现的具有电隔离分流的 0.5% 级三相计量
- 分布式计算：计量参数在每个相位本地计算并发送到主机微控制器
- $5kV_{RMS}$ 和 8kV 峰值的增强型隔离
- 抗磁干扰的电容压降高侧电源
- 相位序列检测
- 计量 AFE 无需使用外部晶振或时钟

应用

- 电表
- 电能质量监测仪



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1 System Description

Three-phase electricity meters measure the energy consumption at a business or industrial site. To properly sense energy consumption, voltage and current sensors translate mains voltage and current to a voltage range that an analog-to-digital converter (ADC) can sense. For three-phase electricity meters, it is necessary for the current sensors to be isolated so they can properly sense the energy consumption of multiple phases without damaging the ADC. As a result, current transformers, which inherently have isolation, have historically been used for the current sensors for three-phase electricity meters. One disadvantage of current transformers (and many transformers in general) is that they can be paralyzed by applying a strong enough magnetic field so that the sensed energy consumption would be less than the actual energy consumption. Due to this weakness of current transformers against magnetic fields, it is common for people to try to tamper with a meter by placing a strong magnet outside the electricity meter to try to paralyze the current transformers to steal electricity. This reference design prevents magnet tampering by using isolated shunts as current sensors instead of current transformers.

This reference design implements a class 0.5 three-phase energy measurement system with isolated shunt sensors by using programmable metrology analog front-end (AFE) microcontrollers. The metrology AFEs sense the voltage and current for each phase, calculates the metrology parameters for the phase, and then sends out the calculated parameters to a host microcontroller using a UART port. The key parameters calculated by the metrology AFE include:

- RMS current and voltage
- Active power, reactive power, and apparent power factor
- Frequency
- Number of sag and swell occurrences
- Total number of sag and swell cycles

External digital isolators capacitively isolate the UART communication between the host microcontroller and the metrology AFE, which allows the host microcontroller to communicate to different metrology AFEs that are referenced with respect to different phases. Because the metrology AFEs measure both voltage and current and have their UART pins externally isolated, voltage sensing is isolated in addition to the required current sensing isolation necessary for implementing shunts in poly-phase systems. As a result, the host microcontroller is completely isolated from mains voltage. Also, because metrology parameters are calculated locally at the metrology AFEs instead of at the host microcontroller, less CPU bandwidth is needed from the host to calculate metrology parameters.

In this reference design, the host microcontroller determines phase sequence, drives the board's liquid crystal display (LCD), and communicates to a PC GUI through the board's isolated RS-232 circuitry. The host microcontroller also takes the metrology readings from the different metrology AFEs and aggregates these results. In addition, the host microcontroller accumulates the average active power readings sent by the metrology AFEs to calculate the total consumed active energy. Using the host microcontroller to accumulate the energy readings instead of the metrology AFEs enables the use of the metrology AFE's internal clock to calculate metrology parameters for many applications. Using the internal clock of the metrology AFE eliminates the need for external crystals or clocks for each metrology AFE, thereby

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reducing system cost. By having the metrology AFEs run off their own clock instead of feeding a clock through the isolation boundary, the data rate of the signals sent through the isolation boundary are greatly reduced because only the actual metrology parameter values, which have a relatively low data rate, need to be sent to the host microcontroller. This low data rate reduces the current consumption of the digital isolators as well as reduces emissions.

Each metrology AFE is powered by a cap-drop supply that is also transformerless. Because a transformer is not used in this reference design (whether a power supply transformer or current transformer), this design is inherently magnetically immune, thereby preventing electricity theft due to magnetic tampering. Moreover, the high-side cap-drop power supply reduces the entire system cost, has inherent low conducted and radiated emissions, and reduces the current consumption drawn from the low-side power supply because the high-side is separately powered from mains instead of being derived from the low-side power supply.

Another advantage of using shunts is that it does not share the same degradation in metrology results that current transformers show when harmonics are present in a system. As a result, these isolated shunt current sensors can also be used for equipment that performs harmonic analysis such as power quality meters.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	SPECIFICATIONS	DETAILS
Number of phases	Three	2.1 节
Accuracy class	Class 0.5	节 3.2.3
Current sensor	Shunt	节 2.3.1.3
Voltage ADC type	Sigma delta (integrated within MSP430i2041 metrology AFE)	节 2.3.1.3
Sigma delta modulator clock	1,024,000 Hz	节 2.3.2.1.2
Sigma delta oversampling ratio (OSR)	256	节 2.3.2.1.2
Ratio of skipped samples to total samples	0/5	节 2.3.2.1.2
Effective sample rate	4000 samples per second	节 2.3.2.1.2
Phase compensation implementation	Hardware (sigma delta module feature)	节 2.3.2.3.2
Metrology AFE clock speed	16.384 MHz	节 2.3.2.1.1
System nominal frequency	50 Hz	节 2.3.2.3.1
Measured parameters (updated every 50 cycles)	Active power, reactive power, apparent power; root mean square (RMS) current and voltage; power factor; line frequency; sag and swell duration; sag and swell number of occurrences	节 2.3.2.2.1
Isolation channels necessary	Two or three	2.1 节
Host MCU clock speed	48 MHz	节 2.3.2.1.4
Utilized LEDs	Total active energy and total reactive energy	节 2.3.2.4.3.2.1
Metrology AFE power	Option 1: Power derived from mains using cap-drop supply; Option 2: External power	节 2.3.1.1

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2 System Overview

2.1 Block Diagram

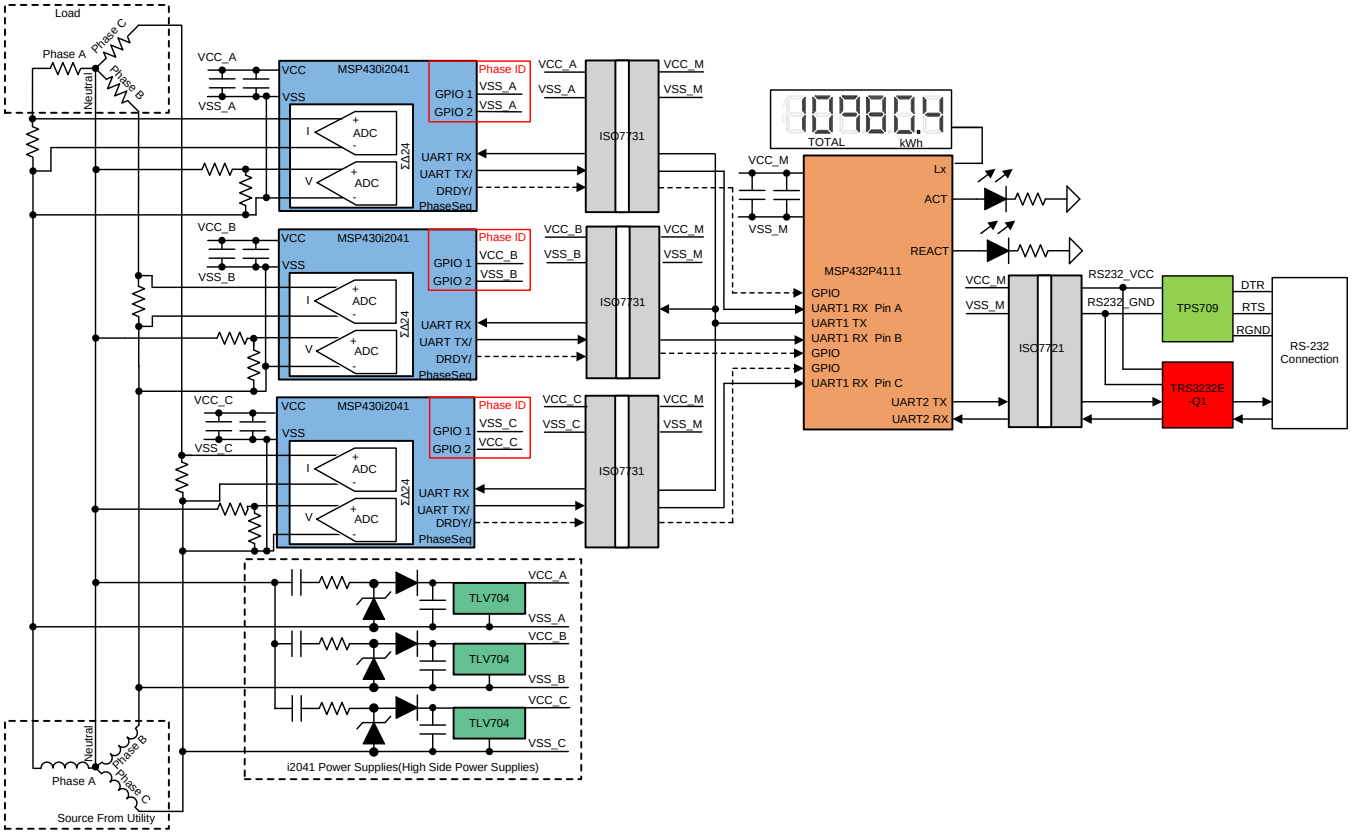

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图 1. TIDA-01550 Block Diagram, Three Isolated Channels

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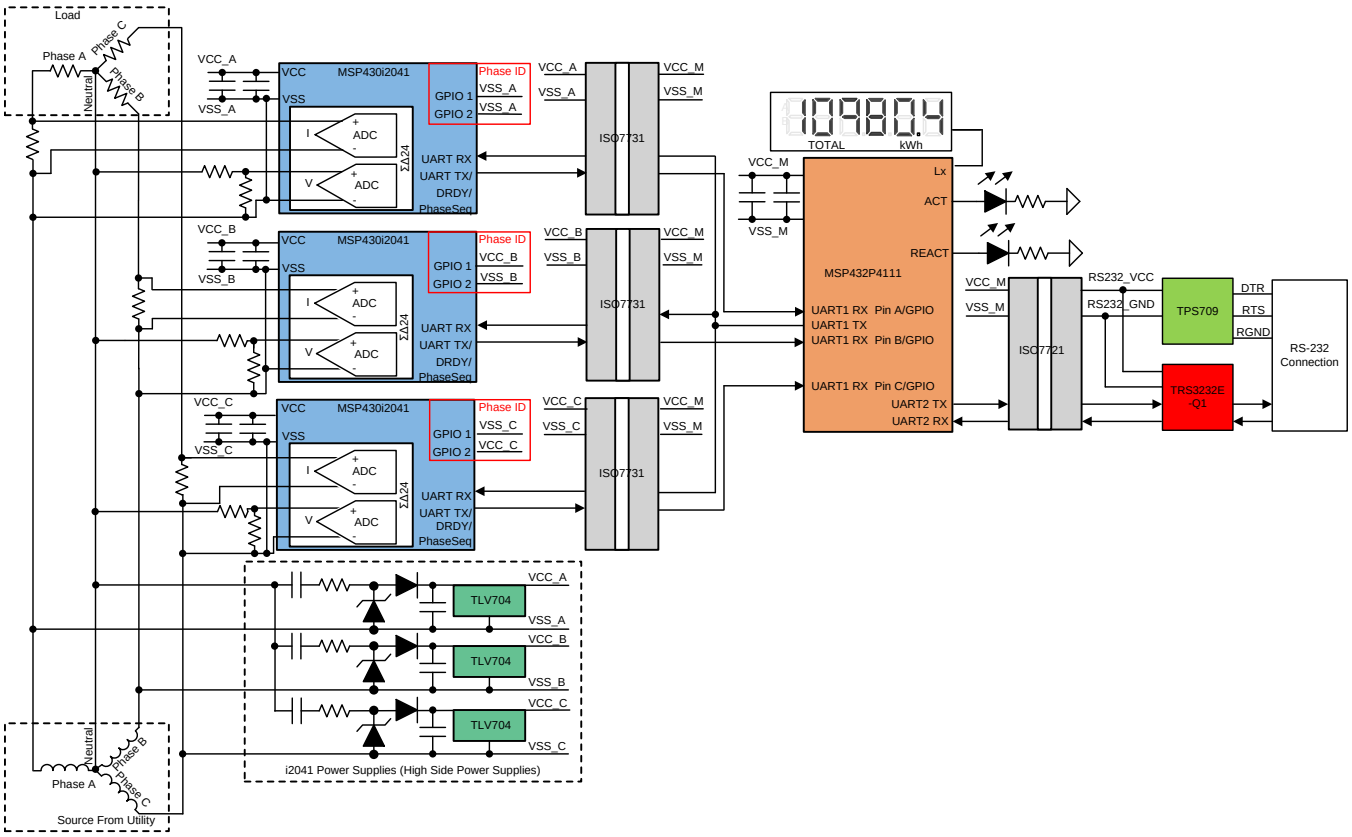

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图 **2. TIDA-01550 Block Diagram, Two Isolated Channels**

图 1 and 图 2 depict a block diagram that shows the high-level interface used for a MSP430i20xx three-phase energy measurement application with isolated shunts. These figures show a three-phase, four-wire star connection to the AC mains. In this reference design, each phase has a shunt current sensor and a MSP430i20xx device. The MSP430i20xx device in this design is responsible for sensing the mains voltage, sensing the current by measuring the voltage drop across the shunt, calculating the metrology parameters (except energy), and sending it to the MSP432™ host microcontroller in this design. The resistance of the shunt is selected based on the current range required for energy measurements and also the minimization of the maximum power dissipation of the shunt. The MSP430i20xx senses the mains voltage by using resistor dividers as the voltage sensor to ensure that the input voltage to the ADC fits within the ADC's input voltage range. Because the MSP430i20xx can accept negative voltages, level shifting the voltage from the resistor divider is not necessary. In this reference design, the superset four-channel MSP430i2041 device variant is used; however, to minimize cost, the two-channel MSP430i2020 variant can also be used. To measure temperature in addition to voltage and current, the three-channel MSP430i2030 device can be used instead.

Only one UART module on the MSP432 communicates with the three MSP430i2041 devices. Multiplexing one MSP432's UART module to communicate with the different MSP430i2041 devices is done by using an addressing scheme where the MSP432 provides the address of the MSP430i2041 device that it is talking to in the commands that the MSP432 sends. Whenever a command is sent by the MSP432 device, the MSP432 MCU sends it to all the MSP430i2041 devices, but only the addressed MSP430i2041 device responds. The address of the different MSP430i2041 devices is configured by providing the proper combination of voltages (VSS or VCC) on two designated phase identification GPIO pins of the

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MSP430i2041 devices. Each device would have its own combination of voltages to ensure that each device has a unique Phase ID. Using the phase identification addressing scheme allows the different MSP430i2041 devices to communicate with the same MSP432 UART module without feeding in any external chip select lines either through the isolation boundary or to the isolator output enable pins. In addition, the phase identification addressing scheme allows the same firmware to be programmed onto the MSP430i2041 devices at the same time, thereby reducing programming time.

Each MSP430i2041 device updates its metrology readings after 50 mains cycles of data has been received. After new metrology readings have been received, a normally high data ready (DRDY) GPIO pin on the MSP430i2041 is asserted low to alert the MSP432 that new metrology parameters are ready. Because this GPIO pin assertion is done a fixed amount of time after the last zero crossing, the phase sequence can be detected by the MSP432 when the MSP430i2041 devices are synchronized by observing the order at which this GPIO pins are asserted. To synchronize the different MSP430i2041 devices, a sync command can be sent by the MSP432 device to make sure that the assertion of the different MSP430i2041 DRDY GPIO pins are synchronized from the same starting point. In this reference design, there is an option to have the DRDY functionality implemented on a dedicated pin as shown in 图 1 or to have it multiplexed with the UART TX pin as shown in 图 2. The two-channel configuration is only valid when the shared UART TX/DRDY pin on the MSP430i2041 is connected to a GPIO pin on the host microcontroller that has the ability to dynamically switch between being a UART RX pin to being an interruptible GPIO input pin. For two-channel mode, the pins on the host microcontroller that are connected to the DRDY pins of the different MSP430i2041 devices must also be able to be configured as the same UART module port through the use of port mapping.

Because each MSP430i2041 device is referenced with respect to a different phase, it is necessary to isolate the communication from the MSP430i2041 to the MSP432. In this design, this isolation is done by the ISO7731 devices; however, for the two channel configuration shown in 图 2 , an ISO7721 device can be used instead to reduce cost. The low power consumption of these isolators enable power supplies with limited maximum current specifications such as cap-drop supplies to be used to power each phase. For proper operation of the isolators, the output channels of different isolators must not be connected to each other; however, the input channels can be directly connected to each other. As a result, although only one UART module is used, the isolated UART TX signal output from the different MSP430i2041 devices must not be physically connected to each other and fed into one RX pin for the MSP432 MCU. Instead of physically connecting together the different isolated UART TX signals from the MSP430i2041 devices, in this design each of these signals is fed into a different port mappable GPIO pin that has the ability to be configured as the RX functionality of the same UART module. An alternative approach, which is not used in this reference design, is to connect the different isolated UART TX signals to inputs of an OR/AND logic gate and to connect the output of this logic gate to one UART RX pin of the MSP432 MCU.

To power the MSP430i2041 devices and the high-side of the isolators, each phase has an external power supply. Because each MSP430i2041 and the high-side of its corresponding isolator must be referenced from a different line voltage, three different cap-drop supplies are used. Each implemented power supply provides power to the associated MSP430i2041 and isolator by using a half-bridge cap-drop power supply between the line of that phase and neutral.

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This reference design uses the MSP432P4111 as the host microcontroller. The MSP432P4111 aggregates the data from the different MSP430i2041 devices. The MSP432P4111 also accumulates the power readings into energy, which allows the MSP430i2031 device to use its own internal clock so that external clock components such as clock generators are not necessary. The MSP432 MCU is responsible for outputting the active and reactive energy pulses used for accuracy measurement and calibration. In addition to isolated pulses, the design also supports isolated RS-232 communication through the use of the TPS70933, ISO7721, and TRS3232E-Q1 devices. For more information on the isolated RS-232 portion of the design, see the *Self-Powered Isolated RS-232 to UART Interface Reference Design*.

2.2 Highlighted Products

2.2.1 ISO7731

The ISO7731 device is a high-performance, triple-channel digital isolator with 5000-V_{RMS} (DW package) and 3000-V_{RMS} (DBQ package) isolation ratings per UL 1577. The ISO7731 device provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. This device comes with enable pins that can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO7731 device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

2.2.2 MSP430i2041

The MSP430i2041 metrology AFE device finds its application in power and energy measurement and has the necessary architecture to support it. The MSP430i2041 device1 has an internal 16.384-MHz DCO, which generates system clocks without an external crystal. The MSP430i2041 has four independent, 24-bit, ΣΔ ADCs based on a second-order sigma-delta architecture that supports differential inputs. The sigma-delta module (referred to as SD24) operate independently, are capable of 24-bit results, and can be grouped together for simultaneous sampling of voltages and currents on the same trigger. In addition, each converter also has an integrated gain stage for amplification of low-output current sensors. The MSP430i2041 device also has a 16-bit × 16-bit hardware multiplier that can be used to further accelerate math intensive operations during metrology computations. 图 3 shows these features as well as additional ones for the MSP430i2041 metrology AFE. The key parameters calculated during measurements by the MSP430i2041 are as follows:

- RMS current and voltage
- Active and reactive power
- Power factor
- Frequency
- Sag duration
- Number of sag occurrences
- Swell duration
- Number of swell occurrences

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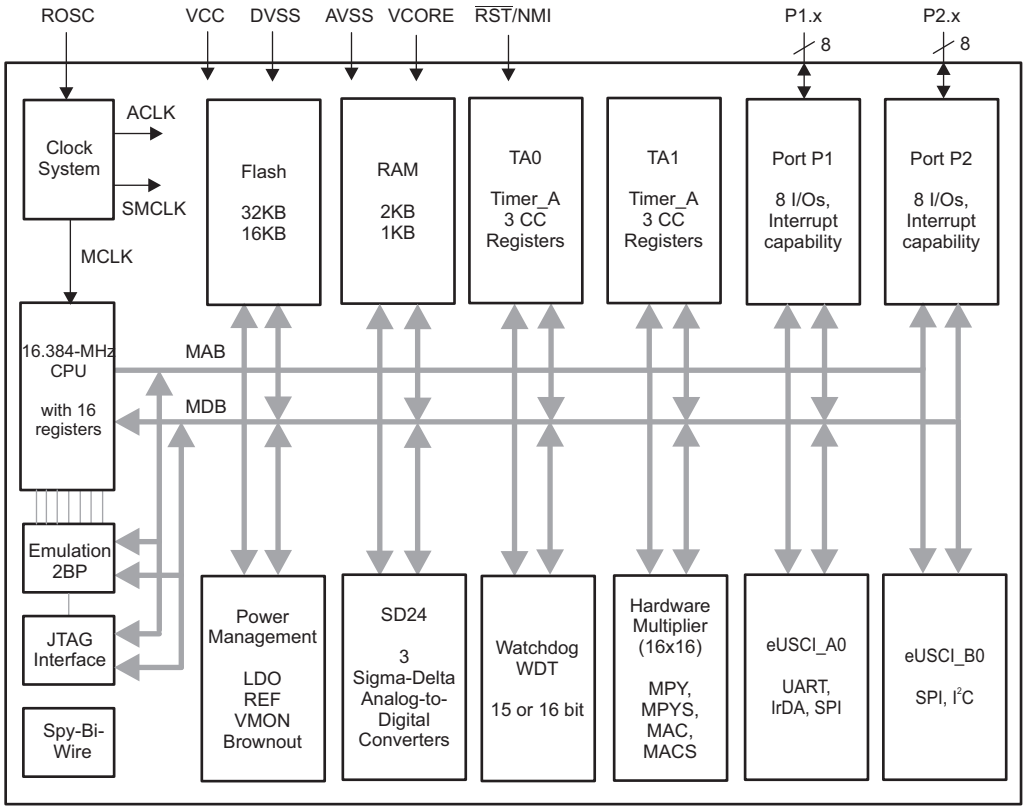

图 **3. Functional Block Diagram of MSP430i2041**

2.2.3 TLV704

The TLV70433 low-dropout (LDO) regulator is an ultra-low quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power-management attachment to low-power microcontrollers such as the MSP430™. The TLV70433 operates over a wide operating input voltage of 2.5 V to 24 V. Thus, the device is an excellent choice for both battery-powered systems as well as industrial applications that undergo large line transients.

2.2.4 MSP432P4111

The SimpleLink™ MSP432P4111 MCUs are optimized MCUs that deliver ultra-low-power performance with FPU and DSP extensions. This device has an Arm® 32-Bit Cortex®-M4F CPU with Floating-Point Unit and Memory Protection Unit, a real-time clock, LCD driver, port mappable GPIOs, an AES encryption and decryption accelerator, and multiple serial communication options. The MSP432P4111 device is part of the SimpleLink MCU platform, which consists of Wi-Fi®, *Bluetooth*® low energy, Sub-1 GHz, and host MCUs. All of these devices share a common, easy-to-use development environment with a single-core software development kit (SDK) and rich tool set.

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2.2.5 TRS3232E-Q1

To properly interface with the RS-232 standard, a voltage translation system is required to convert between the 3.3-V domain on the board and from the 12 V on the port itself. To facilitate the translation, the design uses a TRS3232E-Q1 device. The TRS3232E-Q1 device is capable of driving the higher voltage signals on the RS-232 port from only the 3.3-V DVCC through a charge pump system.

The TRS3232E-Q1 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV electrostatic discharge (ESD) protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of the Telecommunications Industry Association and Electronic Industries Alliance TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

2.2.6 ISO7721

To add isolation to the RS-232 connection to a PC, the isolated RS-232 portion of this reference design uses capacitive galvanic isolation, which has an inherent lifespan advantage over an opto-isolator. In particular, industrial devices are usually pressed into service for much longer periods of time than consumer electronics; therefore, maintenance of effective isolation over a period of 15 years or longer is important.

The variant of the ISO7721 used in the RS-232 circuitry of this reference design provides galvanic isolation up to 3.0 kV_{RMS} for one minute per UL. This digital isolator has two isolated channels where one is a forward channel and the other is a reverse channel. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. This chip supports a signaling rate of 100 Mbps. The chips can operate from a 3.3-V and 5-V supply and logic levels.

2.2.7 TPS709

To power the data terminal equipment (DTE) side of the isolation boundary and the RS-232 charge pump, there are two choices. The interface can either implement an isolated power supply or harvest power from the RS-232 line. Integrating a power supply adds cost and complexity to the system, which is difficult to justify in low-cost sensing applications.

To implement the second option of harvesting power from the RS-232 port itself, this reference design uses the flow control lines that are ignored in most embedded applications. The RS-232 specification (when properly implemented on a host computer or adapter cable), keeps the request to send (RTS) and data terminal ready (DTR) lines high when the port is active. As long as the host has the COM port open, these two lines retain voltage on them. This voltage can vary from 5 V to 12 V, depending on the driver implementation. The 5 V to 12 V is sufficient for the use requirements in this design.

The voltage is put through a diode arrangement to block signals from entering back into the pins. The voltage charges a capacitor to store energy. The capacitor releases this energy when the barrier and charge pump pull more current than what is instantaneously allowed. The TPS70933 is used to bring the line voltage down to a working voltage for the charge pump and isolation device.

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The TPS70933 linear regulator is an ultra-low quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. A quiescent current of only 1 µA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety. These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA (typical).

2.3 System Design Theory

2.3.1 Design Hardware Implementation

2.3.1.1 High-Side Power Supply

To properly sense, calculate, and send metrology parameters, it is necessary for the MSP430i2041 and the high-side of the corresponding isolation device to be powered. Because each MSP430i2041 device and corresponding isolator are referenced from a different line voltage, a different high-side power supply is required for each power supply. In this reference design, there are two high-side power supply options: an onboard half-bridge cap-drop power supply or an off-board, custom power supply.

There are multiple advantages to using the onboard cap-drop high-side power supply. First, this cap-drop power supply does not have any magnetic components, so the power supply would be magnetically immune to magnetic fields instead of only being magnetically tolerant to a certain limit. Additionally, cap-drop supplies are relatively inexpensive compared to alternative power supply options. Also, LDO-based cap-drop power supplies inherently have low conducted and radiated emissions compared to SMPS power supplies. Finally, because the high-side power is derived directly from mains instead of from the host MCU's power supply, less current is drawn from the host MCU's power supply, thereby allowing the specifications on that power supply's maximum current drive to be relaxed.

图 4 shows the design's implementation of the high-side power supply. In this implementation, a TLV70433-based, half-bridge, cap-drop power supply translates the mains voltage to the necessary 3.3 V needed to power the MSP430i2041 and the high-side of the ISO7731. As an alternative to using the onboard cap-drop power supply, the design has the option to instead power the MSP430i2041 and ISO7731 by providing the necessary 3.3 V from an external isolated voltage supply to the associated terminal block (U$13 in 图 4).

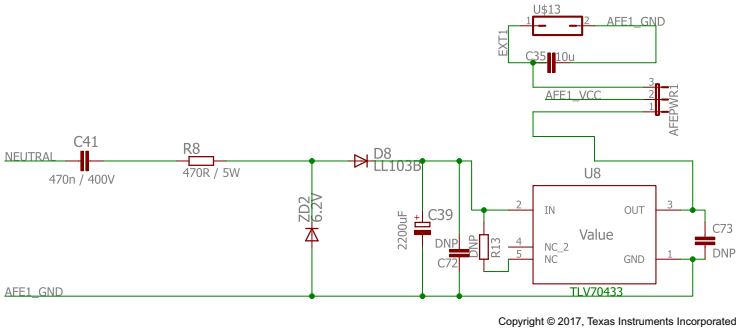

图 4. High-Side Power Supply

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Cap-drop power supplies have a limited maximum current so it is important that their load be low-power. 表 2 shows a typical current consumption of 4.5 mA when the MSP430i2041 device is running in active mode at 16.384 MHz. Based on 表 3, there is also a maximum additional current consumption of 250 µA per ADC converter turned on, resulting in an additional 500 µA of current drawn from the power supply to properly sense voltage and current.

表 2. MSP430i2041 Active Mode Current Consumption(1) (2) (3)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,\ 1.024MHz}$	Active mode current at 1.024 MHz	f_{DCO} = 16.384 MHz, f_{MCLK} = f_{SMCLK} = 1.024 MHz, f_{ACLK} = 32 kHz, Program executes from flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	3 V		1.6		mA
$I_{AM,\ 8.192MHz}$	Active mode current at 8.192 MHz	f_{DCO} = 16.384 MHz, f_{MCLK} = f_{SMCLK} = 8.192 MHz, f_{ACLK} = 32 kHz, Program executes from flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	3 V		3.0		mA
$I_{AM,\ 16.384MHz}$	Active mode current at 16.384 MHz	f_{DCO} = f_{MCLK} = f_{SMCLK} = 16.384 MHz, f_{ACLK} = 32 kHz, Program executes from flash, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	3 V		4.5		mA

(1) Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(2) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
(3) All peripherals are inactive.

表 3. MSP430i2041 SD24 Current Consumption

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	AVSS = DVSS = 0 V			2.2		3.6	V
I_{SD24}	Analog plus digital supply current per converter (reference current not included)	SD24OSRx = 256	GAIN: 1, 2, 4, 8, 16	3 V		190		µA
			GAIN: 1, 16	3 V			250	

This reference design uses a baud rate of 57600 baud. The current consumption of the isolators decreases as frequency decreases, which indicates that the maximum current consumption of the ISO7731 is less than the 3.4-mA maximum current consumption at 1 Mbps mentioned in 图 5. The cap-drop in this implementation is designed to provide more than the 8.4 mA needed to power the MSP430i2041 core, the MSP430i2041 converters, and the digital isolators.

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7731							
Supply current - disable	EN1 = EN2 = 0 V; V_I = V_{CCI}(1) (ISO7731); V_I = 0 V (ISO7731 with F suffix)		I_{CC1}		0.8	1.2	mA
			I_{CC2}		0.7	1	mA
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7731); V_I = V_{CCI} (ISO7731 with F suffix)		I_{CC1}		3	4.3	mA
			I_{CC2}		1.8	2.6	mA
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7731); V_I = 0 V (ISO7731 with F suffix)		I_{CC1}		1.3	1.7	mA
			I_{CC2}		1.6	2.2	mA
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7731); V_I = V_{CCI} (ISO7731 with F suffix)		I_{CC1}		3.5	5	mA
			I_{CC2}		2.8	4.1	mA
		1 Mbps	I_{CC1}		2.4	3.4	mA
			I_{CC2}		2.2	3.3	mA

图 5. ISO7731 Current Consumption

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2.3.1.2 External Resistor and Oscillator For Metrology AFE Clock

The MSP430i2041 internal DCO supports two modes of operation. This device can operate with an internal resistor or an external resistor that is connected to ROSC pin of the device. The internal resistor option is the lowest cost option because it does not require any external components while the external resistor option provides the most accurate clock. When selecting the external resistor option, a recommended 20-kΩ, ±50-ppm resistor with 0.1% tolerance is recommended. This resistor is populated on this reference design in case it is desired to use external resistor mode for other applications; however, the software is configured by default not to use this external resistor option because the energy accumulation from power is done by the MSP432 host MCU and using the internal resistor option is the lowest cost option. For applications that require an accurate clock for precise measurement of other time dependent calculations besides energy (such as line frequency), the external resistor option can be used by modifying the metrology AFE firmware to select the external resistor option instead of the internal resistor option.

2.3.1.3 Analog Inputs

The MSP430i2041's AFE circuitry, which consists of the ΣΔ ADC within the MSP430i2041's SD24 module, is differential and requires that the input voltages at the pins do not exceed ±928 mV when a gain of 1 is used and ±58 mV when a gain of 16 is used. To meet this specification, the current and voltage inputs need to be scaled down. In addition, the SD24 ADCs allows a maximum negative voltage of –1 V. Therefore, the AC current signal from mains can be directly interfaced without the need for level shifters. This section describes the AFE circuitry used for the voltage and current channels.

2.3.1.3.1 Voltage Front End Circuitry

The voltage from the mains is usually 230 V or 120 V and must be scaled down within 928 mV. The AFE circuitry for voltage consists of spike protection varistors followed by a voltage divider network, and a RC low-pass filter that acts like an antialiasing filter. For this design, footprints for suppressant inductors are also available. These inductor footprints are shown in 图 6 as R/L3 and R/L4, and by default are populated with 0-Ω resistors.

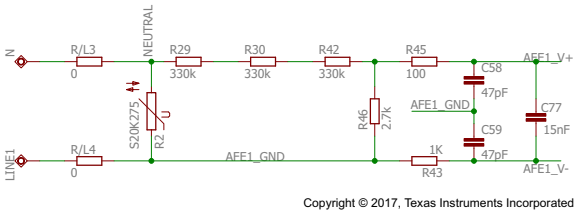

图 6. MSP430i2041 Voltage Front-End Circuitry

图 6 shows the AFE circuitry for the voltage inputs for a mains voltage of 230 V. In this circuitry, the voltage is brought down to approximately 626-mV RMS, which is a 885-mV peak, and fed to the positive input of the convertor. The antialiasing resistors on the positive and negative sides are different because the input impedance to the positive terminal is much higher; therefore, a lower value resistor is used for the antialiasing filter. If this is not maintained, a relatively large phase shift appears between voltage and current samples.

2.3.1.3.2 Current Front-End Circuitry

The AFE circuitry for current inputs is slightly different from the AFE circuitry for the voltage inputs. 图 7 shows the AFE circuitry used for a current channel.

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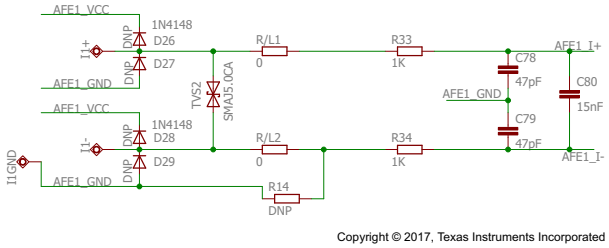

图 7. MSP430i2041 Current Front-End Circuitry

The AFE circuitry for current consists of diodes and transorbs for any additional transient voltage suppression, footprints (R/L1 and R/L2) that could be replaced with inductors for EMI suppression (these footprints are populated with 0-Ω resistors by default), and an antialiasing filter.

图 7 shows the three-terminal shunt used for current measurement to be connected at I1+, I1−, and I1GND. The value of this shunt is selected based on balancing maximizing the peak analog voltage input into the MSP430i2041 with minimizing the power dissipation of the shunt. In particular, for optimal accuracy, the peak DC voltage fed into the MSP430i2041 must be as close as possible to 58 mV without surpassing this voltage. This peak voltage is dependent on the rated maximum current of the system and the resistance of the selected shunt. For example, this reference design uses 400-µΩ shunts (for more information on the shunts used, see http://www.vishay.com/docs/30173/wsms3124.pdf). With these 400-µΩ shunts and a maximum RMS current of 90 A, the maximum DC voltage fed into the MSP430i2041 SD24 ADC is $90 \times \sqrt{2} \times (400 \times 10^{-6}) = 51$ mV. To minimize the power dissipation in the shunt, a smaller value shunt can also be used. This reference design also uses 220-µΩ shunts; however, by using smaller value shunts, the voltage fed into the MSP430i2041 ADC is also reduced. As a result, there is a tradeoff in accuracy. Based on the requirements of the system, the tradeoff in accuracy from using a shunt with a small resistance and the reduced power dissipation from choosing the smaller shunt must be taken into account when selecting the proper shunt value.

2.3.2 Design Software Implementation

This section discusses the software for this reference design. 节 2.3.2.1 discusses the setup of various peripherals of the metrology and host processors. 节 2.3.2.2 and 节 2.3.2.3 describe the metrology software as two major processes: the foreground process and background process. 节 2.3.2.4 describes the application software. 节 2.3.2.5 describes the MSP430i2041 to MSP432 communication process.

2.3.2.1 Peripheral Setup

2.3.2.1.1 MSP430i2041 Start-up Code

The INFO memory of each MSP430i2041 device stores device-specific calibration values. These values affect items such as clock accuracy, SD24 operation, and reference voltage operation. For proper functionality of this device, these values need to be loaded into the proper calibration and trim registers, as mentioned in the TLV and Start-Up Code section of the *MSP430i2xx Family User's Guide* . In addition, a decision whether to secure or unsecure the MSP430i2041 must be made in the first 64 MCLK cycles after RESET. Both of these functions are accomplished in the low_level_init function (in low_level_init.c), which runs before even the main function is called.

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Because the device-specific peripheral calibration is stored in INFO memory, do not change the project settings to erase INFO memory as that erases these values. Also note that meter calibration data is stored in the same segment as the peripheral calibration information. As a result, do not delete the peripheral calibration values if performing meter calibration. This reference design stores the device-specific peripheral calibration data before erasing the INFO memory, and then rewrites INFO memory with this peripheral calibration factors as well as any new meter accuracy calibration factors.

2.3.2.1.2 MSP430i2041 SD24 Setup

The MSP430i2041 has four sigma-delta data converters, which are used to measure the voltage and currents in the system. This reference design only uses two of the four sigma-delta converters. For the MSP430i2041, the clock to the SD24 ADCs (f_M) is fixed at 1.024000 MHz. In the software, an OSR of 256 is chosen, which results in a sampling frequency of 4.000 ksps for the converters. At every sampling instance, the ADCs are configured to generate regular interrupts.

In the software, the following channel associations are used:

- A0.0+ and A0.0- → Current
- A1.0+ and A1.0- → Voltage

2.3.2.1.3 MSP430i2041 AFE UART Setup

The MSP430i2041 is configured to communicate to the MSP432P4111 using a UART module configured for 8N1 at 57,600 baud. When the device is configured in two-channel mode, the UART TX pin is switched between UART TX functionality and DRDY GPIO functionality.

2.3.2.1.4 MSP432P4111 Clock Setup

The MSP432 is configured to have its CPU clock (MCLK) set at 48 MHz and its subsystem master clock (SMCLK) set to 12 MHz. The clock source for MCLK and SMCLK is an external 48-MHz crystal. An external 32.768-kHz crystal is used as the clock source for the device's auxiliary clock (ACLK). This ACLK clock is set to a frequency of 32.768 kHz. The clock is configured using MSP432 driverlib functions.

2.3.2.1.5 MSP432P4111 LCD Controller

The LCD controller on the MSP432P4111 can support up to 8-mux displays and 320 segments or 4-mux displays and 176 segment displays. In the current design, the LCD controller is configured to work in 4-mux mode using 144 segments. The eight segment lines not used in this design's 4-mux mode are used for the port mapping functionality that allows multiplexing multiple TX signals from the MSP430i2041 to the RX signal of only one UART module. To use the full 176 segments in 4-mux mode, the port mapping functionality might not be able to be used to multiplex the different TX signals. Instead, external logic gates may need to be used to OR/AND the multiple TX signals to only one pin on the MSP432P4111. In this reference design, the LCD is configured for a refresh rate set to ACLK/64, which is 512 Hz. For contrast control, external resistors are added between the R23, R13, R03 pins and GND, as shown in 图 8. The LCD is configured primarily using MSP432 driverlib functions.

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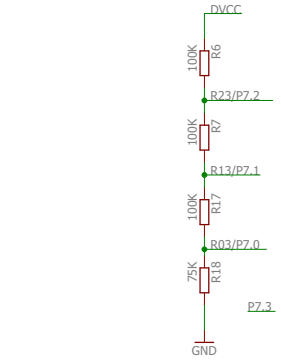

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图 **8. LCD External Resistors**

2.3.2.1.6 MSP432P4111 Real Time Clock (RTC)

The MSP432's real-time clock module is configured to give precise one second interrupts. Based off of these one second interrupts, the time and date are updated in software, as necessary. The RTC is configured using MSP432 driverlib functions.

2.3.2.1.7 MSP432P4111 UART Setup for GUI Communication

The MSP432 MCU is configured to communicate to the PC GUI through the RS-232 connection on this reference design. The MSP432 MCU communicates to the PC GUI using a UART module configured for 8N1 at 9600 baud. The UART is configured using MSP432 driverlib functions.

2.3.2.1.8 MSP432P4111 Timer Setup

In this reference design, the MSP432 MCU uses Timer_A1 to create interrupts at a rate of 4000 Hz. This timer accumulates active power readings into active energy and to keep track of necessary timeouts. In addition, the timer is used to space out requesting metrology parameters for different phases to ensure that there is enough time to receive metrology parameters of a phase before the next phase's metrology parameters are requested. The timer ensures that there is a fixed time delay from when a phase's new metrology readings are ready to when they are requested. The timer is configured using the MSP432 timer driver.

2.3.2.1.9 MSP432P4111 Port Mapping

The MSP432 MCU has a port mapping controller that allows a flexible mapping of digital functions to port pins. The set of digital functions that can be ported to other pins is dependent on the device. For the MSP432 device in particular, the EUSCIA1 UART module's TX and RX functionality are available to ports P2, P3, and P7. In this reference design, this port mapping feature provides flexibility in the PCB layout as well as multiplexing the three TX signals from the different MSP430i2041 devices to the RX signal of the same EUSCIA1 UART port. In this reference design, the three different TX signals are connected to different port mappable GPIO pins. Each of these pins have their port mapping functionality changed switched between "PMAP_NONE" functionality, which disables mapping a digital function to a particular

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pin, and "PMAP_UCA1RXD", which enables communication to a corresponding metrology AFE. The design's software ensures that only one port mapping pin at a time is configured to PMAP_UCA1RXD functionality. Whenever the MSP432 device requests data from a particular metrology AFE, the MCU sends the command to all the metrology AFEs and enables only the PMAP_UCA1RXD functionality on the MSP432's port mapping GPIO pin that is connected to the desired MSP430i2041's UART TX pin.

When the host is configured for two-channel mode, the port mapping pins are also switched from port mapping functionality to interruptible GPIO pins. Because only the P2 and P3 ports of the MSP432 have both port mappable and interruptible GPIO input pins, this two-channel mode only works with ports P2 and P3 on the MSP432. In two-channel mode, the port mapping pins are configured as interruptible input pins majority of the time. The only time the port mapping pins are configured for the PMAP_UCA1RXD functionality is when the MSP432 has sent a command to a specific MSP430i2041 device and it is expecting a response back. Once the requested data has been correctly received by the MSP432P4111 or there has been a timeout, the corresponding port mapping pin is configured back to be an interruptible GPIO pin.

Using the port mapping controller, the following mappings are used:

- PMAP_UCA1TXD (EUSCIA1 UART TX) → Port P2.6
- PMAP_UCA1RXD (EUSCIA1 UART RX) → Port P2.5 (Connected to the isolated UART Tx signal from Phase A's MSP430i2041)
- PMAP_UCA1RXD (EUSCIA1 UART RX) → Port P2.3 (Connected to the isolated UART Tx signal from Phase B's MSP430i2041)
- PMAP_UCA1RXD (EUSCIA1 UART RX) → Port P2.1 (Connected to the isolated UART Tx signal from Phase C's MSP430i2041)

The port mapping functionality is configured using the driverlib; however, the majority of the other GPIO pins are configured using the MSP432 GPIO driver.

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2.3.2.1.10 MSP432P4111 Direct Memory Access (DMA)

The direct memory access (DMA) module transfers packets from the MSP430i2041 to the MSP432P4111 with minimal bandwidth requirements from the MSP432's CPU. Only the third channel of the DMA is used. The DMA transfers each byte received from the MSP432's EUSCIA1 UART module's RX signal to memory until an entire packet of data has been received. Once an entire packet of data has been obtained, the DMA module triggers an interrupt to immediately parse any critical data.

2.3.2.1.11 MSP432P4111 Interrupt Priorities

The software has five interrupts that are priorities. 表 4 lists these interrupt priorities, with the smaller priority codes having higher interrupt priorities.

表 4. MSP432P4111 Interrupt Priorities

INTERRUPT	SIGNIFICANCE	PRIORITY CODE
TA1_0	Update energy accumulation registers and timeout state	0x20
PORT2	New metrology readings are now available for a particular MSP430i2041 device	0x40
DMA1	Received response packet from a MSP430i2041 device	0x60
EUSCIA0	UART transmit buffer empty for sending a packet to the PC GUI or new UART character has been received from the PC GUI	0x80
RTC	A new second has elapsed every time this interrupt is triggered. Every two seconds, update the LCD.	0x80

2.3.2.2 MSP430i2041 Metrology Foreground Process

The foreground process includes the initial setup of the MSP430i2041 hardware and software immediately after a device RESET. 图 9 shows the flowchart for this process.

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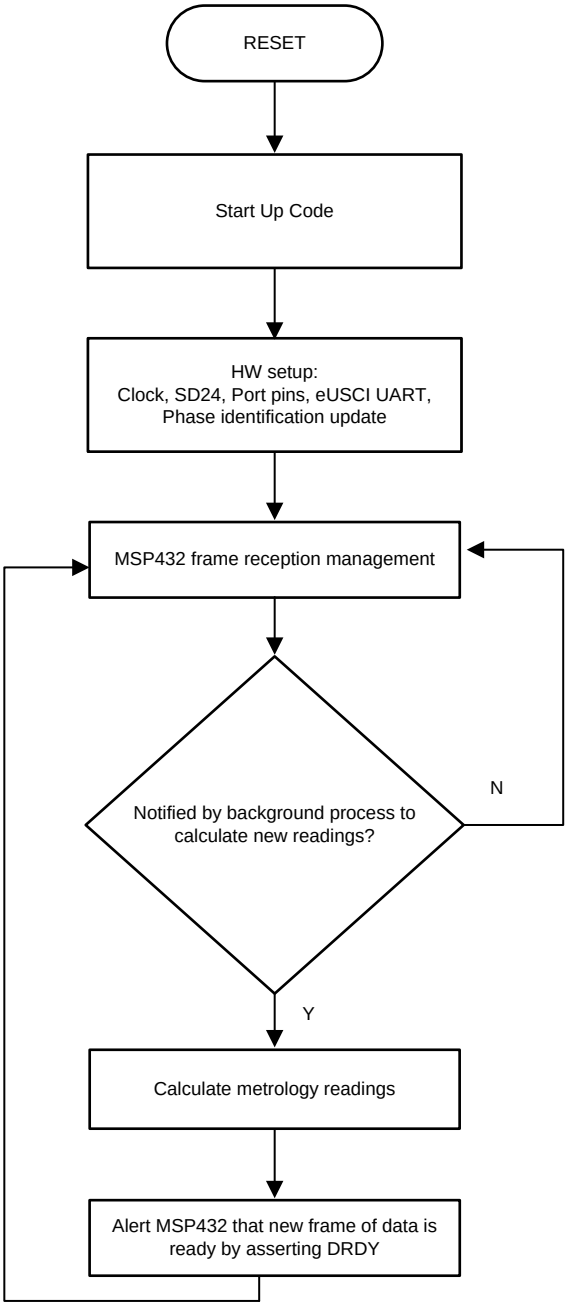

图 9. Metrology Foreground Process

The initialization routines involve the setup of the ADC, clock system, general purpose input/output (port) pins, phase identification (whether a particular device is set to be Phase A, Phase B, or Phase C), and the USCI_A0 for UART functionality. After the hardware is set up, any received frames from the MSP432P4111 are processed. Subsequently, the foreground process checks whether the background process has notified it to calculate new metering parameters. This notification is done through the assertion of the "PHASE_STATUS_NEW_LOG" status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for 50 cycles in the background process.

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The processed dot products include the V_{RMS}, I_{RMS}, active power, and reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real world units. Processed voltage dot products are accumulated in 48-bit registers. In contrast, processed current dot products, active energy dot products, and reactive energy dot products are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the foreground's calculated values of active and reactive power, the apparent power is calculated. The frequency (in Hertz) and power factor are also calculated using parameters calculated by the background process using the formulas in 节 2.3.2.2.1. Once new metrology readings have been calculated, the DRDY pin is asserted low for a duration of approximately 5 ms, thereby alerting the MSP432 MCU that new metrology parameters are ready.

2.3.2.2.1 MSP430i2041 Metrology Formulas

This section briefly describes the formulas used for the voltage, current, and power calculations. As previously described, voltage and current samples are obtained at a sampling rate of 4000 Hz. All of the samples that are taken in 50 cycles are kept and used to obtain the RMS values for voltage and current for each phase. The RMS values are obtained by the following formulas:

$$V_{RMS,ph} = K_{v,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} v_{ph}(n) \times v_{ph}(n)}{\text{Sample count}}} - v_{offset,ph} \quad (1)$$

$$I_{RMS,ph} = K_{i,ph} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} i_{ph}(n) \times i_{ph}(n)}{\text{Sample count}}} - i_{offset,ph} \quad (2)$$

where:

- ph = Phase parameters that are being calculated [that is, Phase A (= 1), B (= 2), or C (= 3)],
- $V_{ph}(n)$ = Voltage sample at a sample instant n,
- $V_{offset,ph}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter,
- $I_{ph}(n)$ = Each current sample at a sample instant n,
- $I_{offset,ph}$= Offset used to subtract effects of the additive white Gaussian noise from the current converter,
- Sample count = Number of samples in 50 cycles,
- $K_{v,ph}$ = Scaling factor for voltage,
- $K_{i,ph}$ = Scaling factor for current.

Power and energy are calculated for a frame's worth of active and reactive energy samples. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

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$$P_{ACT,ph} = K_{ACT,ph} \frac{\sum_{n=1}^{\text{Sample Count}} v(n) \times i_{ph}(n)}{\text{Sample Count}} - P_{ACT\_Offset,ph} \quad (3)$$

$$P_{REACT,ph} = K_{REACT,ph} \frac{\sum_{n-1}^{\text{Sample Count}} V_{90,ph}(n) \times i_{ph}(n)}{\text{Sample Count}} - P_{React\_Offset,ph} \quad (4)$$

$$P_{APP,ph}{}^2 = \sqrt{P_{ACT,ph}{}^2 + P_{REACT,ph}{}^2} \quad (5)$$

where:

- $V_{90}(n)$ = Voltage sample at a sample instant 'n' shifted by 90°,
- $K_{ACT,ph}$ = Scaling factor for active power,
- $K_{REACT,ph}$ = Scaling factor for reactive power,
- $P_{ACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the active power measurements from other phases and the neutral,
- $P_{REACT\_offset,ph}$ = Offset used to subtract effects of crosstalk on the reactive power measurements from other phases and the neutral.

Note that for reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents.
2. This approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency calculates the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, first measure the mains frequency accurately to phase shift the voltage samples accordingly.

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90 degrees before the current sample and a voltage sample slightly less than 90 degrees before the current sample are used. The application's phase shift implementation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays.

The background process also calculates the frequency in terms of samples per mains cycle. The foreground process then converts this samples per mains cycle unit to Hertz using 公式 6:

$$\text{Frequency (Hz)} = \frac{\text{Sample Rate (samples / second)}}{\text{Frequency (samples / cycle)}} \quad (6)$$

After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the system's internal representation of power factor, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated using 公式 7:

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$$\text{Internal Representation of Power Factor} = \begin{cases} \dfrac{P_{Act}}{P_{Apparent}}, \text{if capacitive load} \\ -\dfrac{P_{Act}}{P_{Apparent}}, \text{if inductive load} \end{cases} \quad (7)$$

2.3.2.3 MSP430i2041 Metrology Background Process

The background function deals mainly with timing critical events in software. This function uses the SD24 interrupt as a trigger to collect voltage and current samples. The SD24 interrupt is generated when a new voltage sample is ready. Once the voltage sample is obtained, sample processing is done on the previously obtained voltage and current samples. This sample processing is done by the "per_sample_dsp()" function.

2.3.2.3.1 per_sample_dsp

The flowchart for the per_sample_dsp function is shown in 图 10. In this function, the per_sample_dsp function calculates intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. Because 16-bit voltage samples are used, the voltage samples are further processed and accumulated in dedicated 48-bit registers. In contrast, because 24-bit current samples are used, the current samples are processed and accumulated in dedicated 64-bit registers. Per-phase active power and reactive power are also accumulated in 64-bit registers.

After sufficient samples have been accumulated, the foreground function is triggered to calculate the final values of V_{RMS}, I_{RMS}, active, reactive, and apparent powers, active, reactive, and apparent energy, frequency, and power factor. The foreground process is triggered to calculate new parameters every 50 cycles. If mains voltage is not available, a timeout is set to trigger the foreground process to calculate new metrology readings after 4160 samples. To ensure that the assertion of the DRDY GPIO pin is synchronized among all the MSP430i2041 devices, a sync command is sent by the MSP432P4111 to all of the MSP430i2041 devices. This sync command clears the current count of the cycle_count variable used to trigger the foreground process. The MSP432 device sends this sync command whenever a phase's mains voltage becomes available after it was previously unavailable.

In the software, there are two sets of dot products: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products.

Whenever there is a leading-edge zero-crossing (– to + voltage transition) on a voltage channel, the per_sample_dsp function is also responsible for updating the corresponding phase's frequency (in samples/cycle) and voltage sag and swell conditions. For the sag conditions, whenever the RMS voltage is below a certain user-defined threshold percentage, the number of mains cycles where this condition persists is logged as the sag duration. The sag threshold is based on the settings of the SAG_THRESHOLD and MAINS_NOMINAL_VOLTAGE macros within the metrology-template.h file. An event is defined as being a sag when the RMS voltage is below the following value:

$$\left(\frac{(100 - \text{SAG\_THRESHOLD})}{100}\right) \times \text{MAINS\_NOMINAL\_VOLTAGE} \quad (8)$$

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The number of occurrences where there was a sag condition is logged as the sag events count. Note that the sag duration corresponds to the total number of cycles in a sag condition since reset and is therefore not cleared for every sag event. Also, when the RMS voltage is above a certain threshold percentage, swell events and duration are logged in a similar way; except then an event is defined as being a swell event when the calculated RMS voltage is above the following value:

$$\left(\frac{(100 + \text{SAG\_THRESHOLD})}{100}\right) \times \text{MAINS\_NOMINAL\_VOLTAGE} \tag{9}$$

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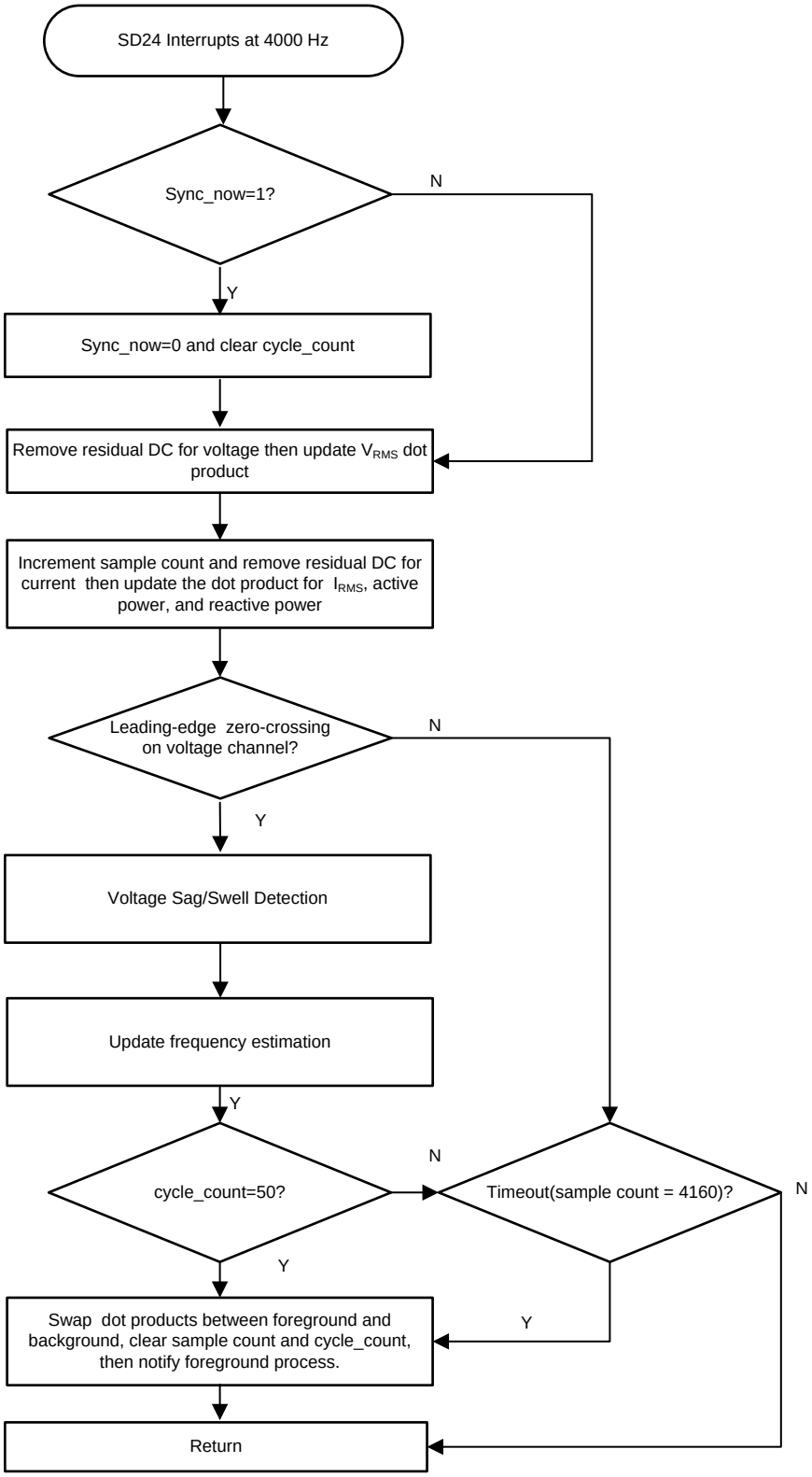

图 10. per_sample_dsp Function

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2.3.2.3.1.1 Voltage and Current Signals

The output of each SD24 converter is a signed integer and any stray DC or offset value on these converters is removed using a DC tracking filter. Separate DC estimates for all voltages and currents are obtained using the filter and voltage and current samples, respectively. These estimates are then subtracted from each voltage and current sample.

The resulting instantaneous voltage and current samples are used to generate the following intermediate dot product results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively
- Accumulated energy samples to calculate active powers
- Accumulated energy samples using current and 90° phase shifted voltage to calculate reactive powers

These accumulated values are processed by the foreground process.

2.3.2.3.1.2 Frequency Measurement and Cycle Tracking

The instantaneous voltage of each phase is accumulated in 48-bit registers. In contrast, the instantaneous current, active power, and reactive power are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When approximately 50 cycles worth of samples have been accumulated, the background process switches the foreground and background then notifies the foreground process to produce the average results such as RMS and power values.

For frequency measurements, a straight line interpolation is used between the zero crossing voltage samples. 图 11 shows the samples near a zero cross and the process of linear interpolation.

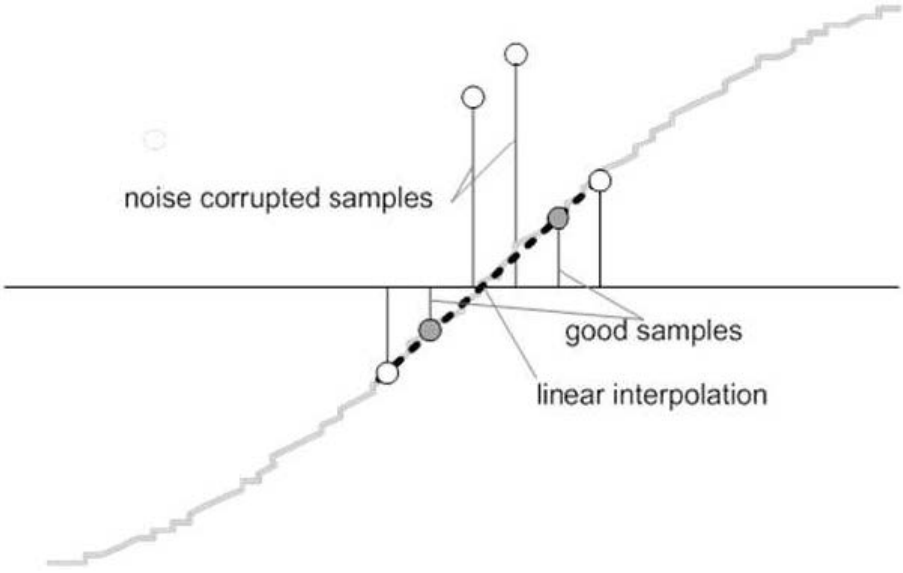

图 11. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate of change check to filter out the possible erroneous signals and makes sure that the two points are interpolated from are genuine zero crossing points. For example, with two negative samples, a noise spike can make one of them positive and therefore make the negative and positive pair looks as if there is a zero crossing.

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The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out cycle-to-cycle variations. This results in a stable and accurate frequency measurement that is tolerant of noise.

2.3.2.3.2 Phase Compensation

To ensure accurate measurements, the relative phase shift between voltage and current samples must be compensated. This phase shift can be caused by the passive components of the voltage and current input circuit. The SD24 converters have programmable delay registers (SD24PREx) that can be applied to any current or voltage channel. This built-in feature (PRELOAD) is used to provide the phase compensation required.

The fractional delay resolution of the preload register is a function of input frequency (f_{IN}), OSR, and the sampling frequency (f_S):

$$\text{Delay resolution}_{Deg} = \frac{360° \times f_{IN}}{OSR \times f_s} = \frac{360° \times f_{IN}}{f_M} \quad (10)$$

In this application, for an input frequency of 50 Hz, OSR of 256, and sampling frequency of 4000, the resolution for every bit in the preload register is approximately 0.02° with a maximum of 4.48° (maximum of 255 steps).

2.3.2.4 MSP432P4111 Host Software

2.3.2.4.1 Peripheral Setup and Idle Tasks

After the MSP432 MCU resets, the device initializes its peripherals. The initialization routines involve the setup of the GPIO port pins and associated port map controller; clock system; eUSCI_A0 UART module for communication to a PC GUI using RS-232; eUSCI_A1 UART module for communication to the different MSP430i2041 metrology AFEs; timer; RTC for keeping track of time; LCD; and DMA for streamlining communication from the metrology AFEs.

Once the MSP432P4111 has completed setup of its peripherals, the device enters a loop where it performs low-priority tasks until it is interrupted by hardware interrupts. 图 12 shows a flowchart of the peripheral setup and the idle tasks performed.

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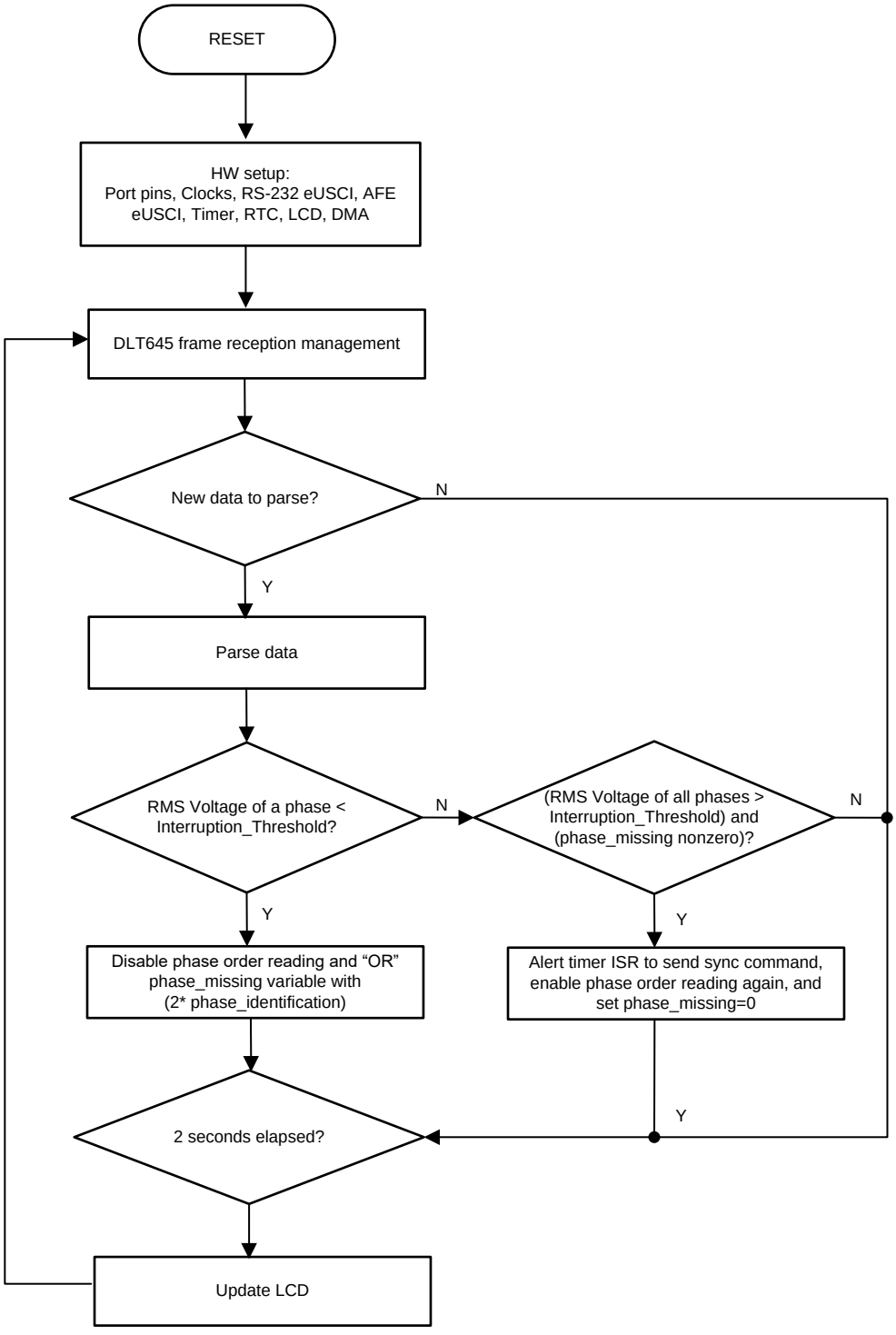

图 **12. Peripheral Setup and Idle Tasks**

The first task performed in the loop is to process any received frames from the GUI. Next, the application checks to see if there is new, noncritical data from any of the MSP430i2041 devices that need to be parsed (any critical data is parsed in the DMA interrupt service routine itself instead of in this loop). If there is new data available to parse, the data is parsed and used to update the MSP432P4111's internal variables if necessary. When there are new metrology parameters to parse and the RMS voltage is

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parsed, a check is made to determine if the RMS voltage reading of the phase is sufficiently larger than a defined interruption threshold. If the RMS voltage for the phase is below this threshold, then the phase is determined to be missing so the phase order calculations are disabled. If the RMS voltage for all phases is above the interruption threshold after one or more phases were previously declared as missing, a sync command is sent to all the MSP430i2041 devices and the phase order calculations are enabled again. Finally, the application checks to see if a new 2-second interval has elapsed since the last time the LCD has been updated. The RTC keeps track of when a new 2-second interval has occurred and alerts this LCD idle task of this new 2-second interval so that the LCD can be updated to display a new metrology parameter.

2.3.2.4.2 Port 2 ISR

Whenever any of the MSP430i2041 devices has just calculated new metrology parameters, the MSP430i2041 asserts a DRDY GPIO pin low to alert the MSP432 MCU that new parameters are now ready. The assertion of this MSP430i2041 GPIO pin specifically triggers the MSP432 Port 2 ISR. In this ISR, the application keeps track of the relative order of when the different DRDY pins are asserted. When each phase's line voltage is available, this order of when the different DRDY pins are asserted determine the phase sequence. In addition, the timer's count when a particular MSP430i2041's DRDY pin was asserted is logged. This timer count is used by the timer ISR to determine the intentional delay that must be added before the MSP432 actually requests a phase's metrology parameters. In this reference design, the intentional delay from DRDY assertion to request of metrology parameters is 0 ms for phase A, 20 ms for phase B, and 40 ms for phase C. This delay ensures that there is enough time to get the metrology parameters from a phase. In addition to using the timer count for adding intentional delays for metrology parameters, this timer count also determines when a particular phase times out.

2.3.2.4.3 Timer ISR

The timer ISR is triggered at a rate of 4000 Hz. Every time this ISR is called, the timer_count_update and energy_processing functions are called. The following two sections go over these functions.

2.3.2.4.3.1 timer_count_update

The timer_count_update function serves two purposes. The first purpose is to send commands to the MSP430i2041 devices at the proper point in time. Whenever there is a request to send a sync command to all the MSP430i2041 devices for ensuring correct phase sequence measurements, the timer_count_update function is where this actual sync command is sent to the MSP430i2041 devices. In addition, this function is where the MSP432P4111 sends the commands to request metrology parameters from any MSP430i2041 device that has indicated through its DRDY GPIO pin that a new frame of data has been calculated. To ensure that there is enough time to transfer the data packets from each MSP430i2041 device, there is an intentional delay added from when the DRDY GPIO pin was asserted to when the timer_count_update function requests the metrology parameters for a phase. The intentional delay from DRDY assertion to request of metrology parameters is 0 ms for phase A, 20 ms for phase B, and 40 ms for phase C. Whenever there is a request to get the calibration factors from a MSP430i2041 device, the timer_count_update function is also where the actual request command for the calibration factor is sent to the MSP430i2041.

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The second purpose of the timer_count_update function is to keep track of timeouts and to take the appropriate action when there is a timeout. The first set of timeouts managed by this function are triggered when the previous set of metrology readings for a phase has been received more than approximately 1.05 seconds ago. This timeout considers the scenario where the DRDY pin has been asserted by the MSP430i2041 and the MSP432 device has made a request for the new metrology parameters but it has not received a valid response from the MSP430i2041. In addition, this timeout also considers the scenario where the DRDY pin has not been asserted at all. This reference design has a separate timeout for each individual phase. Whenever a timeout occurs for a particular phase, the metrology parameters for that associated phase are set to 0 and a flag is asserted to let the application know that phase is missing. The second set of timeouts managed by the timer_count_update function determine if a request has been sent to an MSP430i2041 device but a response has not been received within 0.25 seconds from when the request was sent to specified MSP430i2041 device.

When a request for metrology readings or calibration factors has been sent to a specified MSP430i2041, any other requests for metrology readings or calibration factors are not made until the specified MSP430i2041 either gets the requested data or the specified command timeout for that phase occurs. Each time the MSP432P4111 requests a parameter from a specified MSP430i2041 device, the corresponding MSP432 UART RX pin that is connected to that MSP430i2041 device is enabled by modifying the port mapping controller to output the UART RX functionality on this pin. Simultaneously, the UART RX functionality is disabled from the UART RX pins for the other MSP430i2041 devices. If the two-channel mode is selected in this design, there is an additional step of also enabling the UART RX pin from GPIO mode to peripheral mode. If the system is in two-channel mode and the MSP432P4111 gets a requested response from a specified MSP430i2041 device or there is a timeout for the request sent to the MSP430i2041, the shared DRDY/UART RX pin of the specified MSP430i2041 is set from UART RX pin mode to GPIO mode. Switching to GPIO mode enables the MSP432 MCU to detect the next time the MSP430i2041 has calculated new metrology parameters.

2.3.2.4.3.2 energy_processing

2.3.2.4.3.2.1 Pulse Generation

In electricity meters, the active energy consumed is normally measured in fraction of kilowatt-hour (kWh) pulses. This information can be used to calibrate any meter for accurate measurement. The meter is responsible for generating pulses proportional to the energy consumed.

This application uses average power to generate these energy pulses. If the absolute value of the average power is greater than the residual power cutoff value set in software, the average power is accumulated during every timer interrupt, thereby spreading the accumulated energy from the previous frame of data evenly for each interrupt in the current 50 cycles frame. This is equivalent to converting it to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and new energy value is added on top of it in the next interrupt cycle.

The residual power cutoff value is used to set the cutoff power reading at which the meter must not register power readings. If the absolute value of a power reading is below this cutoff value, then the power is not accumulated for the energy pulses. Additionally, if any phase's power reading is below this power cutoff value, then the corresponding cumulative energy reading used for pulse generation does not accumulate that phase's power reading.

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The threshold determines the energy "tick" specified by meter manufacturers and is a constant. A tick is usually defined in pulses per kWh or just in kWh. One pulse is generated for every energy tick. For example, in this application, the number of pulses generated per kWh is set to 6400 for active and reactive energies. The energy tick in this case is 1 kWh/6400. Energy pulses are generated and available on a header and also through LEDs on the board. General-purpose I/O (port) pins are used to produce the pulses.

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In the reference design, the LEDs that are labeled "Active" and "Reactive" correspond to the aggregate active energy consumption and aggregate reactive energy consumption, respectively. The number of pulses per kWh and each pulse duration can be configured in software. 图 13 shows the flow diagram for pulse generation. This flow diagram is valid for active and reactive energy.

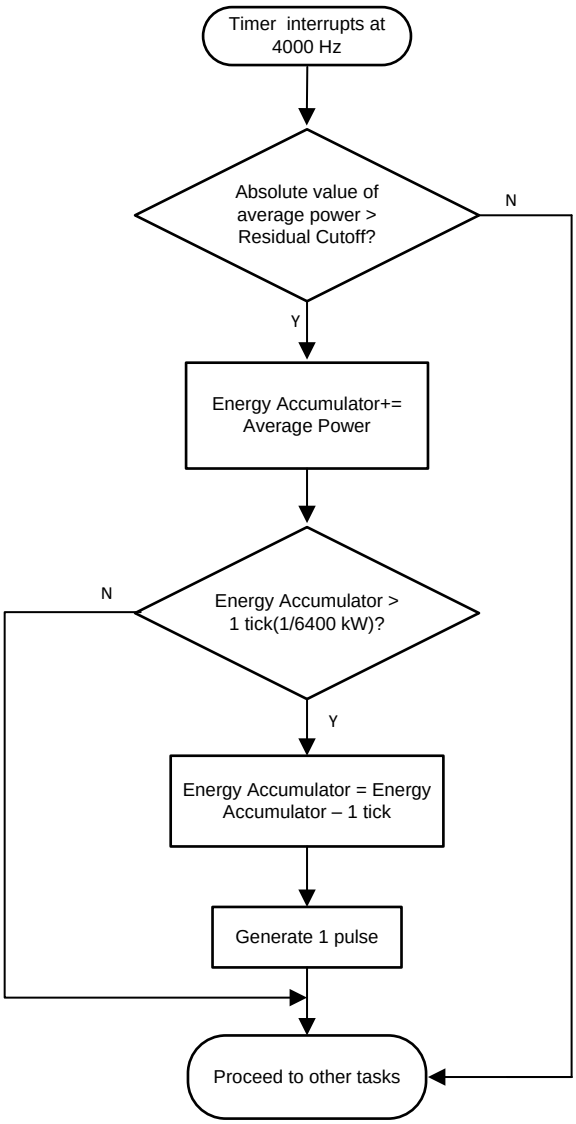

图 13. Pulse Generation

The average power is in units of 0.001 W and the 1 kWh threshold is defined as:
1-kWh threshold = (1 / 0.001) × 1 kW × (number of interrupts per second) × (number of seconds in one hour) = 1000000 × 4000 × 3600 = D18C2E28000

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2.3.2.4.3.2.2 Energy Buffers

In addition to outputting energy pulses to indicate energy consumption, this reference design also stores the total consumed energy readings into separate buffers, which can be seen from the PC GUI. These buffers store the total amount of energy consumed since a system reset. The energy stored in these energy buffers are accumulated in a similar method as the energy used for pulse generation except a different energy tick is used. Instead of each tick corresponding to 1 kWh/6400 as is the case for pulse generation, the internal tick value corresponds to 0.1 Wh. This value means that the energy buffers in the MSP432P4111 software is in units of 0.1 Wh.

Similar to the energy used for pulse generation, the residual power cutoff value is used to set the cutoff power reading at which the meter must not register power readings. If the absolute value of a power reading is below this cutoff value, then the power is not accumulated into the energy buffers. Additionally, if any phase's power reading is below this power cutoff value, then the corresponding cumulative energy buffers does not accumulate that phase's power reading.

In this reference design, there are four sets of buffers that are available: one for each phase and one for the cumulative of the phases. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active energy ≥ 0)
2. Active export energy (active energy when active energy < 0)
3. React. Quad I energy (reactive energy when reactive energy ≥ 0 and active power ≥ 0; inductive load)
4. React. Quad II energy (reactive energy when reactive energy ≥ 0 and active power < 0; capacitive generator)
5. React. Quad III energy (reactive energy when reactive energy < 0 and active power < 0; inductive generator)
6. React. Quad IV energy (reactive energy when reactive energy < 0 and active power ≥ 0; capacitive load)
7. App. import energy (apparent energy when active energy ≥ 0)
8. App. export energy (apparent energy when active energy < 0)

2.3.2.4.4 DMA1 ISR

When the MSP432P4111 sends a request for metrology parameters or calibration factors to an MSP430i2041 device, the DMA module is used to place the packet response from the MSP430i2041 in memory without CPU intervention. Once an entire packet is received, the DMA1 interrupt is triggered. 图 14 shows the flowchart of the DMA1 ISR. In this ISR, the application calculates a checksum and compares it to the checksum value in the packet sent. The checksum is calculated by adding each element in the packet except the final byte, which is the checksum, and then taking a logical OR of the calculated checksum with 0xFF. If the checksum passes, any critical portions of the packet are parsed in the ISR, an alert is made to the idle task to parse other portions of the packet, the DRDY/UART RX pin is configured back to a GPIO pin when in two-channel mode, and transmission of other commands to the MSP430i2041 devices is enabled again.

When a request for metrology parameters is sent to an MSP430i2041 device and the received packet does not pass the checksum check, the MSP432 MCU sends a duplicate request for the packet. If the packet received does not pass the checksum check for a second consecutive time, no further requests are sent for metrology parameters until the MSP430i2041 alerts the MSP432P4111 of new metrology parameters being ready through its DRDY GPIO pin.

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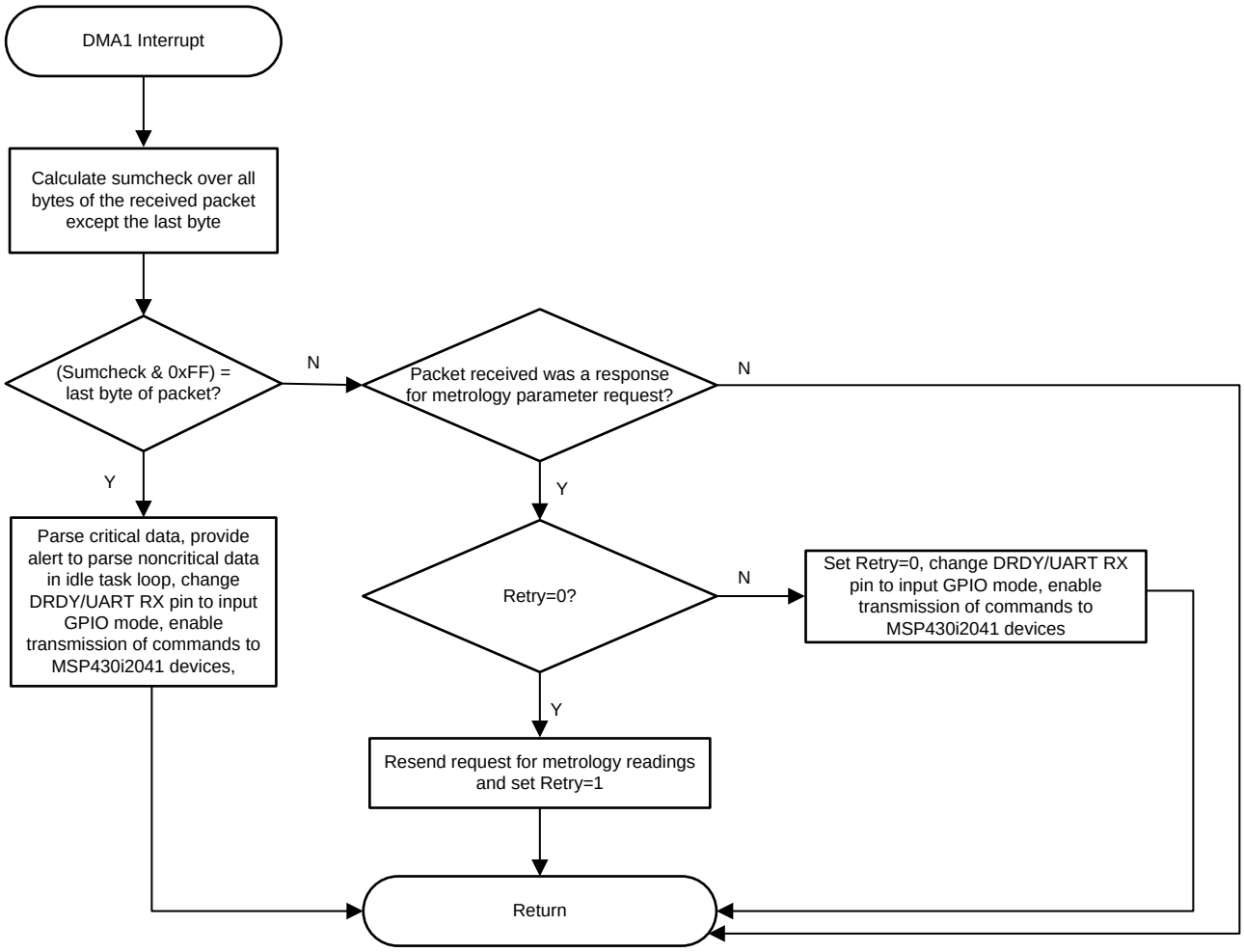

图 **14. DMA1 ISR**

2.3.2.5 MSP430i2041-to-MSP432P4111 Communication

The MSP432P4111 can send five primary commands to the MSP430i2041 devices. These commands obtain metrology readings for a phase, perform metrology calibration, and synchronize the different MSP430i2041 devices for phase sequence detection. When the MSP430i2041 receives a command from the MSP432 device and is in two-channel mode, the MSP430i2041 configures its shared DRDY/UART TX pin from GPIO mode to UART mode. Based on the received command from the MSP432 MCU, the MSP430i2041 device performs any required actions and, if necessary, sends a response packet back to the MSP432P4111.

For specifically receiving a phase's metrology parameters from a particular MSP430i2041 device, the HOST_CMD_GET_READINGS_n command is sent by the MSP432 MCU, where the n value corresponds to the phase and has a value of either 1 (for phase A), 2 (for phase B) or 3 (for phase C). The n value is used by the MSP432 device to request the parameters for a specific phase by having the different HOST_CMD_GET_READINGS_n commands have different command byte values. For example, if the

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MSP432 device wants the metrology parameters for Phase A, the MSP432 device sends the HOST_CMD_GET_READINGS_1 command to all the MSP430i2041 devices. The device that has a phase ID (as configured by the voltages present on the two phase-identification GPIO pins) that corresponds to Phase A then responds with its metrology parameters while the other phases ignore the request.

表 5 shows an example command sent by the MSP432P4111 and the MSP430i2041's response. The command byte that is sent by the MSP432 MCU is shown in yellow and the MSP430i2041's response packet is shown in green. For the command byte shown in the figure, the value of 0x60+n is shown, which means HOST_CMD_GET_READINGS_PHASE_1 (Phase A) has a command byte of 0x61, HOST_CMD_GET_READINGS_PHASE_2 (Phase B) has a command byte of 0x62, and HOST_CMD_GET_READINGS_PHASE_3 (Phase C) has a command byte of 0x63. In 表 5, the "LEN" row indicates the packet length of the command packet sent by the MSP432P4111 and the response packet sent back from the specified MSP430i2041 device. The Data column mentions the contents of the different bytes in the packets and the Offset (bytes) columns mentions where the data is placed with respect to the first byte in the packet. The data fields that are listed as "Don't Care" are fields that are not used by the MSP432 and MSP430i2041 devices. The width column mentions the data type for the field, where U8 corresponds to unsigned 8-bit integers, U16 corresponds to unsigned 16-bit integers, U32 corresponds to unsigned 32-bit integers, S16 corresponds to signed 16-bit integers, and S32 corresponds to signed 32-bit integers. For some packets sent by the MSP430i2041 and MSP432 MCU, there is also a checksum byte that is used to verify that a sent packet has been properly received. When this checksum value is added in a packet, it is calculated by summing each byte in a packet and storing the result as an unsigned 8-bit integer that is placed as the last byte in a packet.

2.3.2.5.1 Obtaining Metrology Readings From MSP430i2041

Each MSP430i2041 device calculates a frame of new metrology readings every 50 cycles. After a new set of metrology parameters have just been calculated, the MSP430i2041 device asserts its DRDY pin low to alert the MSP432 device that new metrology parameters are ready. The assertion of this MSP430i2041 GPIO pin specifically triggers the MSP432 Port 2 ISR, which is used to determine phase sequence and update the phase-specific timer count as mentioned in 节 2.3.2.4.2. After the Port 2 ISR has been triggered, the MSP432P4111 sends a packet requesting metrology parameters for a specific phase. There is an intentional delay added from when the Port 2 ISR is triggered to when the MSP432 MCU actually requests a phase's metrology parameters. In this reference design, the intentional delay from DRDY assertion to request of metrology parameters is approximately 0 ms for phase A, 20 ms for phase B, and 40 ms for phase C. After the intentional delay has elapsed from when a phase's DRDY pin is asserted, the request for the metrology parameters for that phase is done within the timer_count_update function (节 2.3.2.4.3.1) in the MSP432's Timer ISR. 表 5 shows the metrology reading request command sent by the MSP432 MCU to the MSP430i2041 devices and the response back from the specified MSP430i2041.

表 5. HOST_CMD_GET_READINGS_PHASE_n Command

COMMAND (MSP432)			RESPONSE (i2041)		
LEN: 1			LEN: 47		
OFFSET (BYTES)	WIDTH	DATA	OFFSET (BYTES)	WIDTH	DATA
0	U8	0x60 + n (n = 1, 2, 3)	0	U8	0x60 + n (n = 1, 2, 3)

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表 5. HOST_CMD_GET_READINGS_PHASE_n Command (continued)

COMMAND (MSP432)	RESPONSE (i2041)		
LEN: 1	LEN: 47		
	1	U8	Don't care
	2	S32	Voltage in mV
	6	S32	Current in µA
	10	S32	Active power in mW
	14	S32	Reactive power in mW
	18	S32	Apparent power in mW
	22	S16	Power factor in 0.001 units
	24	U16	Frequency in 0.01 Hz
	26	S32	Voltage channel DC offset
	30	S32	Current channel DC offset
	34	U16	Number of sag events
	36	U32	Sag duration in cycles
	40	U16	Number of swell events
	42	U32	Swell duration in cycles
	46	U8	Checksum

The MSP430i2041's response provides results based on real world units. As an example, the active power reading sent in the response packet is in units of mW so an active power value of 2300134 in this packet would correspond to 2300.123 W.

In this application, after the MSP432P4111 sends the HOST_CMD_GET_READINGS_PHASE_n command, the MCU configures its DMA to read the 47 byte response from the MSP430i2041 without requiring CPU intervention. After the 47-byte response has been received by the MSP432P4111, the DMA1 ISR is triggered and the critical portions of the packet are parsed as described in 节 2.3.2.4.4. The noncritical portions of the packet are parsed in the idle task loop mentioned in 节 2.3.2.4.1.

2.3.2.5.2 Metrology Calibration

Metrology calibration is performed by changing calibration factors that are stored on the MSP430i2041 devices. In this reference design, the PC GUI calibrates the metrology. When performing calibration, the PC GUI first sends commands to the MSP432P4111 to request the calibration factors of the different phases until the calibration factors of all the phases have been received. 图 15 summarizes the process used for the GUI to obtain the calibration factors for all the phases.

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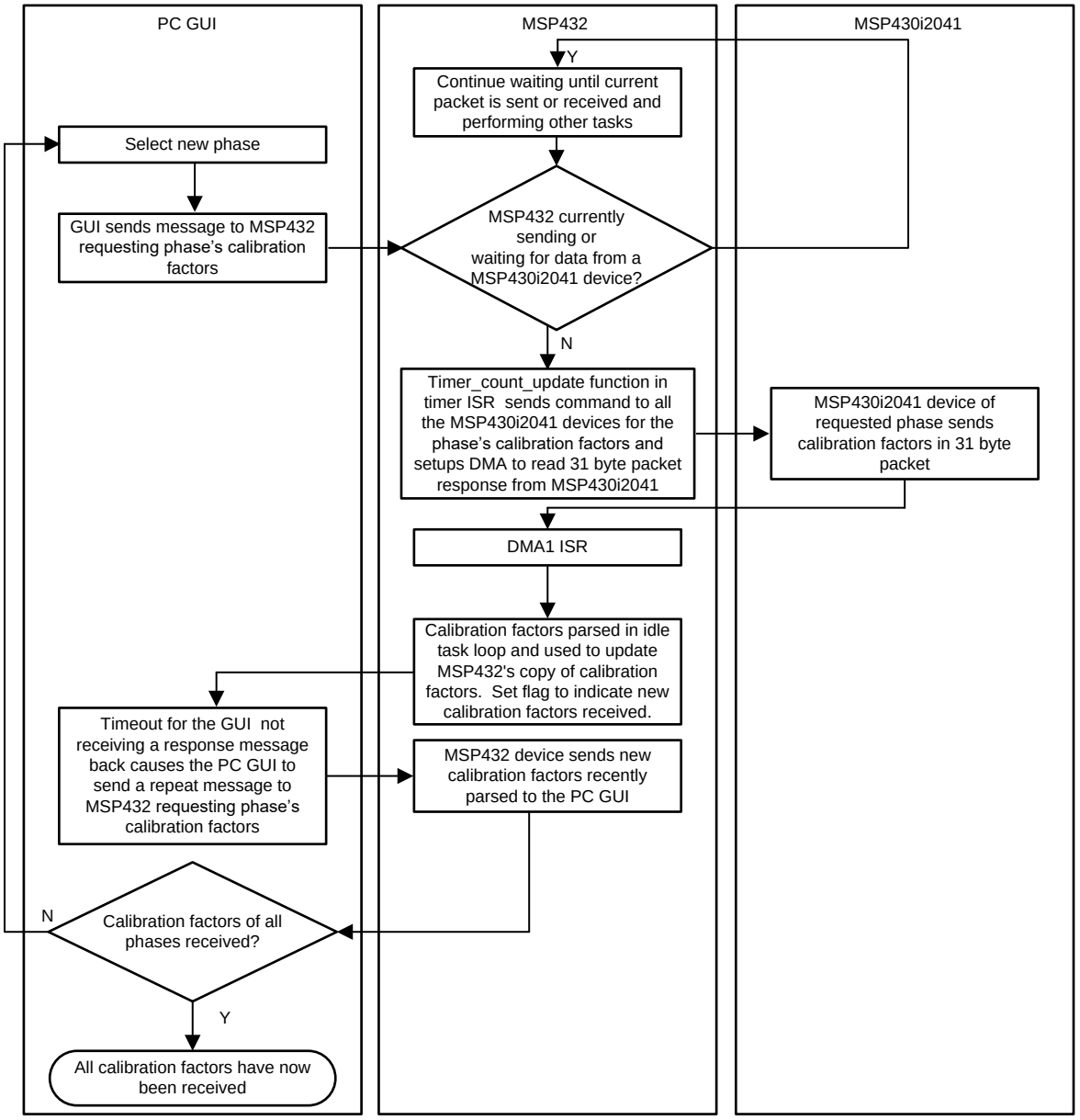

图 **15. Process for Obtaining All Calibration Factors**

When the MSP432 MCU receives a command from the GUI for a phase's calibration factors, the MSP432 MCU sends a command to the MSP430i2041 devices, where it requests the MSP430i2041 device that corresponds to the specified phase to send its metrology factors. Similar to sending commands for obtaining metrology parameters, sending the calibration request command is actually done in the timer_count_update function (节 2.3.2.4.3.1) in the MSP432's Timer ISR. The calibration factor request command is sent in the Timer ISR at the next moment the device is not sending or expecting data from the MSP430i2041. 表 6 shows the calibration factor request command sent by the MSP432P4111 to the MSP430i2041 devices and the response back from the specified MSP430i2041.

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表 6. HOST_CMD_GET_CALIBRATION_PHASE_n Command

COMMAND (MSP432)			RESPONSE (i2041)		
LEN: 1			LEN: 31		
OFFSET (BYTES)	WIDTH	DATA	OFFSET (BYTES)	WIDTH	DATA
0	U8	0xD5 + n (n = 1, 2, 3)	0	U8	0xD5 + n (n = 1, 2, 3)
			1	U8	Don't care
			2	S16	Voltage channel DC offset
			4	S16	Don't care
			6	S16	Current channel DC offset
			8	S16	Don't care
			10	S32	Active power offset
			14	S32	Reactive power offset
			18	S16	Phase correction factor × 8
			20	U16	V_{RMS} scaling factor
			22	S16	Don't care
			24	U16	I_{RMS} scaling factor
			26	U16	Don't care
			28	U16	Power scaling factor
			30	U8	Checksum

Except for the phase compensation calibration factor, the GUI displays and operates on all the other calibration factors mentioned in 表 6 directly without having to do any conversions to other units. This means the value passed to the MSP432P4111 and GUI is the actual calibration value used internally by the MSP430i2041 for calculating metrology parameters. The phase compensation calibration factor is the only calibration factor that is displayed on the GUI in different units than are actually used internally. The MSP430i2041 uses a phase compensation value that is in units of modulation clock cycles. For this reference design, a modulation clock frequency of 1,024,000 Hz is used so the phase compensation factor is in units of 0.9765625 µs. In the MSP430i2041's response to the MSP432P4111, the MSP430i2041 multiplies the phase compensation factor by 8, which results in the phase compensation factor sent by the MSP40i2041 to the MSP432 MCU being in units of 0.1220703 µs. The MSP432P4111 sends this parameter directly to the GUI, which then converts this parameter to units of µs. The phase compensation parameter is displayed on the GUI in µs and phase calibration input is performed in units of µs as well.

In this application, after the MSP432P4111 sends the HOST_CMD_GET_CALIBRATION_PHASE_n command, it configures its DMA to read the 31-byte response from the MSP430i2041 without requiring CPU intervention. After the 31-byte response has been received by the MSP432 MCU, the DMA1 ISR is triggered, which alerts the idle task loop to parse the calibration packet received from the MSP430i2041 as mentioned in 节 2.3.2.4.1 and for it to update its local copy of the requested phase's calibration factors with the new factors from the corresponding MSP430i2041. The timeout for the GUI not receiving a response message back to the original GUI request for calibration factors causes the GUI to send a second request for the calibration parameters of the requested phase. The timing of the timeout occurs so that the MSP432P4111 has received a phase's calibration factors before the second-phase calibration parameter request is made. When the MSP432 MCU gets this second request for calibration parameters from the GUI, the MSP432P4111 sends the GUI its recently updated calibration factors for the requested phase.

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After all the calibration factors have been received from all the MSP430i2041 devices, the GUI uses the error inputted into the GUI to calculate new calibration parameters for all the phases. The calibration factors for each phase are then sent one by one to the MSP432P4111 until the calibration factors of all the phases have been sent. The process of setting the new calibration factors is summarized in 图 16.

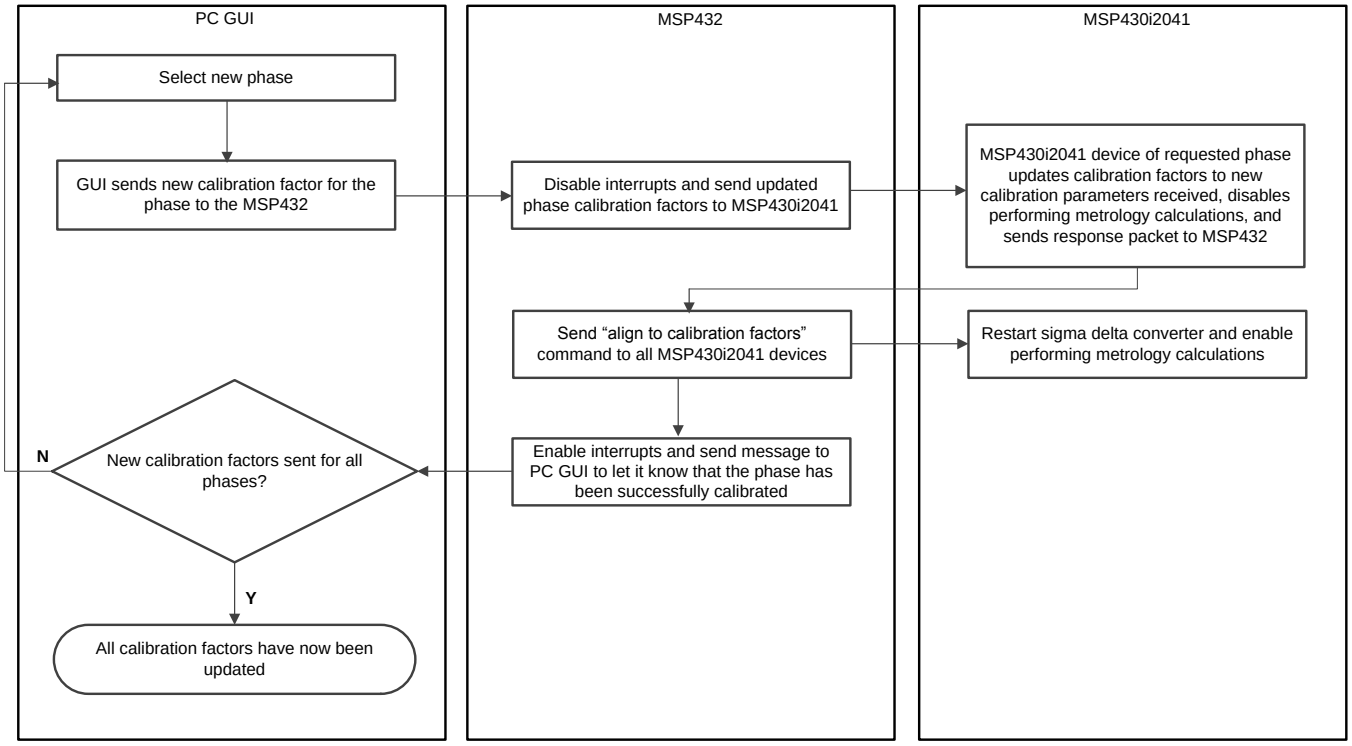

图 16. Process for Setting New Calibration Factors

When the MSP432P4111 receives a phase's new calibration factors, it disables interrupts then sends out the HOST_CMD_SET_CALIBRATION_PHASE_n packet to the MSP430i2041 devices so that the specified MSP430i2041 device could update its calibration factors accordingly. Then waits for an expected response from the MSP430i2041 device to let it know that the MSP430i2041 device has finished updating its calibration factors. Once the MSP430i2041 device receives the new calibration factors, it disables performing metrology calculations, updates its metrology calibration factors, and sends a response back to the MSP432 device.

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表 7 shows the HOST_CMD_SET_CALIBRATION_PHASE_n packet sent to the MSP430i2041 and its response packet. In the packet sent to the MSP430i2041 device, the phase compensation factor is in units 8 times smaller than the internal phase compensation value used by the MSP430i2041 device so the phase compensation value in the packet is divided by 8 before being set as the MSP430i2041's new phase compensation value.

表 7. HOST_CMD_SET_CALIBRATION_PHASE_n Command

COMMAND (MSP432)			RESPONSE (i2041)		
LEN: 31			LEN: 2		
OFFSET (BYTES)	WIDTH	DATA	OFFSET (BYTES)	WIDTH	DATA
0	U8	0xD0 + n (n = 1, 2, 3)	0	U8	0xD0 + n (n = 1, 2, 3)
1	U8	Don't care	1	U8	0xD0 + n (n = 1, 2, 3)
2	S16	Voltage channel DC offset			
4	S16	Don't care			
6	S16	Current channel DC offset			
8	S16	Don't care			
10	S32	Active power offset			
14	S32	Reactive power offset			
18	S16	Phase correction factor × 8			
20	U16	V_{RMS} scaling factor			
22	S16	Don't care			
24	U16	I_{RMS} scaling factor			
26	U16	Don't care			
28	U16	Power scaling factor			
30	U8	Checksum			

When the MSP432 device has received a valid response from the MSP430i2041 device that it sent calibration factors to, the MSP432 MCU sends a HOST_CMD_ALIGN_WITH_CALIBRATION_FACTORS command to all the MSP430i2041 devices. 表 8 shows the HOST_CMD_ALIGN_WITH_CALIBRATION_FACTORS packet sent to the MSP430i2041 devices. This command is used to enable performing metrology calculations after any MSP430i2041 device has received a HOST_CMD_SET_CALIBRATION_PHASE_n command addressed to it. The HOST_CMD_ALIGN_WITH_CALIBRATION_FACTORS differs from the other calibration factors in that it is intended to be sent to all the MSP430i2041 devices so there are not different variations of this command for different phases. When each device receives this command, they all perform the same actions. In addition, the MSP430i2041 devices do not send a response packet when they receive this command. After the MSP432 device has sent the HOST_CMD_ALIGN_WITH_CALIBRATION_FACTORS command, the MSP432P4111 enables interrupts again and sends a message to the GUI to let it know that calibration has been successfully completed on the phase it sent calibration factors for and the GUI can send the updated parameter for the next phase until all of the phase calibration factors have been sent.

表 8. HOST_CMD_ALIGN_WITH_CALIBRATION_FACTORS Command

COMMAND (MSP432)			RESPONSE (i2041)		
LEN: 1			LEN: 0		
OFFSET (BYTES)	WIDTH	DATA	OFFSET (BYTES)	WIDTH	DATA
0	U8	0x5A			

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2.3.2.5.3 Synchronizing MSP430i2041 Devices for Phase Sequence Detection

Every 50 mains cycles, each MSP430i2041 outputs a pulse on the DRDY pin to indicate that new metrology parameters are ready. The delay from the last leading zero crossing to the assertion of the DRDY pin is fixed and does not vary significantly across MSP43i2041 devices, which allows the user to determine the phase sequence by noting the order at which the DRDY pin is asserted when the devices are synchronized to start from the same starting point. To synchronize the different MSP430i2041 devices to start from the same starting point, the HOST_CMD_SEND_SYNC command is sent to all the MSP430i2041 devices at the same time. 表 9 shows the HOST_CMD_SEND_SYNC packet sent to the MSP430i2041 devices. Similar to the HOST_CMD_ALIGN_WITH_CALIBRATION_FACTORS command, the MSP430i2041 devices do not send a response back after they receive the HOST_CMD_SEND_SYNC command.

表 **9. HOST_CMD_SEND_SYNC Command**

COMMAND (MSP432)			RESPONSE (i2041)		
LEN: 1			LEN: 0		
OFFSET (BYTES)	WIDTH	DATA	OFFSET (BYTES)	WIDTH	DATA
0	U8	0xDB			

As mentioned in 节 2.3.2.3.1, when a MSP430i2041 device receives a sync command, the device clears the current count of the cycle_count variable used to trigger the foreground process so that all the different MSP430i2041 devices would start counting cycles from the same mains cycle at the next time the DRDY pins are asserted.

The HOST_CMD_SEND_SYNC is sent by the MSP432P4111 each time one of the phases has gone missing and then returns so that all of the phases are available again. A phase is determined as being missing whenever the parsed RMS voltage is below an interruption threshold (as mentioned in 节 2.3.2.4.1) or whenever a DRDY pulse has not been received from the phase in the last 1.05 seconds. Similar to sending commands for obtaining calibration parameters, sending the HOST_CMD_SEND_SYNC command is actually done in the timer_count_update function(节 2.3.2.4.3.1) in the MSP432's Timer ISR. The calibration factor request command is sent in the Timer ISR at the next moment the device is not sending or expecting data from the MSP430i2041 device.

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3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Cautions and Warnings

At high currents, the terminal block can get warm. In addition, note that the MSP430i2041 devices are referenced with respect to the different phase voltages, so take the proper precautions.

WARNING

Hot Surface! Contact can cause burns. Do not touch. Take the proper precautions when operating.

CAUTION

High Voltage! Electric shocks are possible when connecting the board to live wires. The board must be handled with care by a professional. For safety, use of isolated test equipment with overvoltage or overcurrent protection is highly recommended.

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3.1.2 Hardware

The following figures of the EVM best describe the hardware: 图 17 is the top view of the energy measurement system, and 图 18 shows the location of various pieces of the design based on functionality.

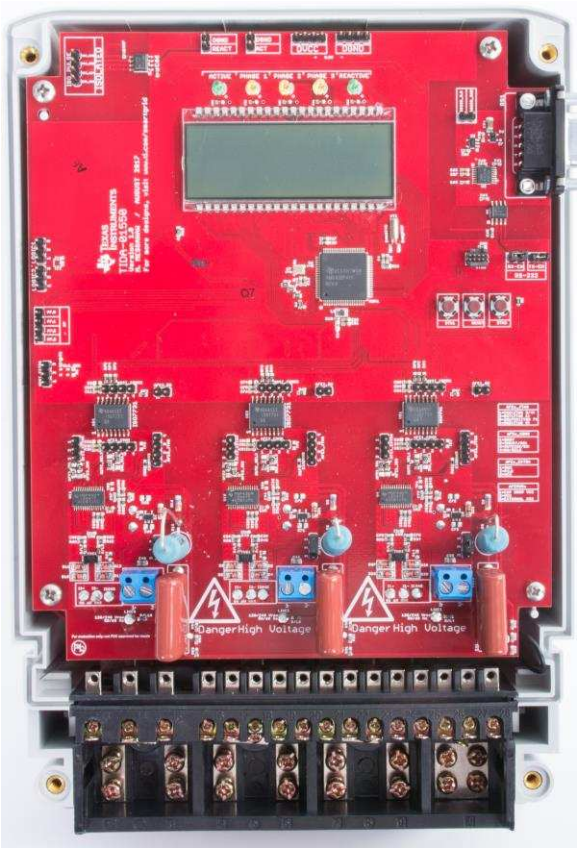

图 17. Top View of Reference Design

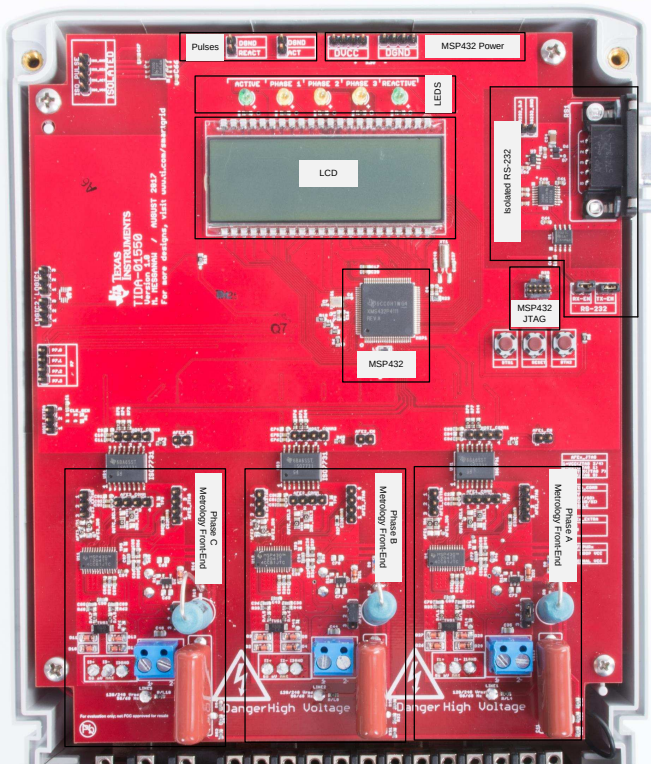

图 18. Top View of Reference Design With Components Highlighted

3.1.2.1 *Connections to the Test Setup for AC Voltages*

AC voltages can be applied to the board for testing purposes at these points:

- Pad "LINE1" corresponds to the line connection for phase A.
- Pad "LINE2" corresponds to the line connection for phase B.
- Pad "LINE3" corresponds to the line connection for phase C.
- Pad "N" corresponds to the neutral voltage. The voltage between any of the three line connections to the neutral connection must not exceed 230-V AC at 50 and 60 Hz.
- I1+, I1−, and I1Live are connected to the output terminals of the shunt that is used for measuring the current for Phase A. When a shunt is selected, the differential voltage that is output across I1+ and I1− must not exceed 58 mV.
- I2+, I2−, and I2Live are connected to the output terminals of the shunt that is used for measuring the current for Phase B. When a shunt is selected, the differential voltage that is output across I2+ and I2− must not exceed 58 mV.
- I3+, I3−, and I3Live are connected to the output terminals of the shunt that is used for measuring the

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current for Phase C. When a shunt is selected, the differential voltage that is output across I3+ and I3− must not exceed 58 mV.

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图 19 shows a mapping between shunt terminals and I1 (Phase A) current pads. A similar mapping is done between the other shunts and corresponding phases.

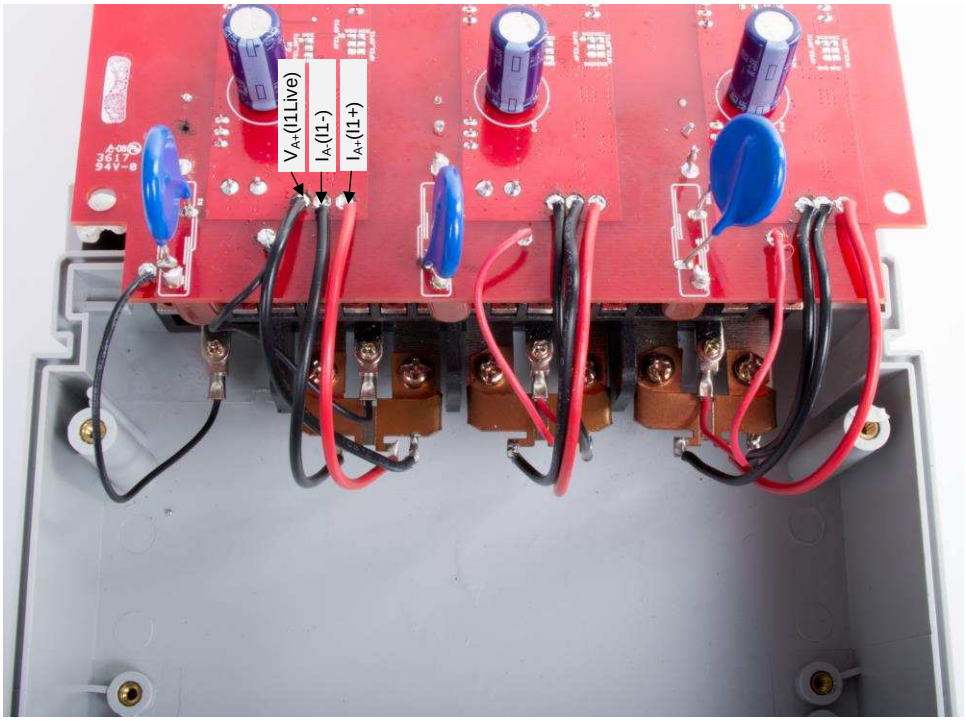

图 **19. Mapping Between Shunt Terminals and Ix Current Pads**

图 20 and 图 21 show the various connections that must be made to the test setup for proper functionality of the EVM. When a test AC source must be connected, the connections have to be made according to the EVM design. When a test AC source must be connected, the links on the board must be connected as shown in 图 20.

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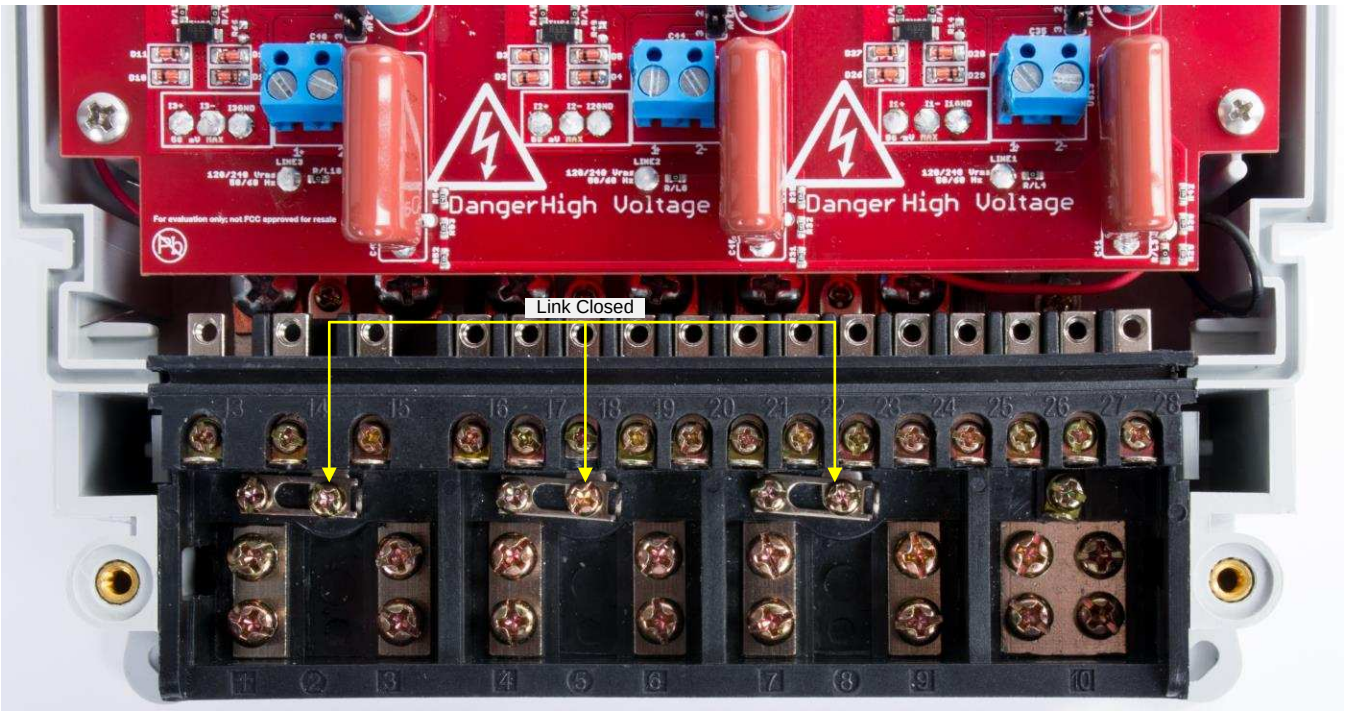

图 **20. Top View of EVM With Links Closed**

图 21 shows the connections from the front view. V_A+, V_B+, and V_C+ correspond to the line voltages for phases A, B, and C, respectively. V_N corresponds to the neutral voltage from the test AC source. I_A+ and I_A− correspond to the current inputs for phase A, I_B+, and I_B− correspond to the current inputs for phase B; I_C+ and I_C− correspond to the current inputs for phase C. V_N corresponds to the neutral voltage from the test setup.

图 **21. Front View of EVM With Test Setup Connections**

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3.1.2.2 Power Supply Options and Jumper Settings

The MSP430i2041 and the high-side of each ISO7731 are powered from mains. The MSP432 side of the board is powered by a single DC voltage rail (DVCC), which must be derived from external power. Various jumper headers and jumper settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for the board to correctly function. 表 10 indicates the functionality of each jumper on the board.

表 10. Header Names and Jumper Settings

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
ACT	1-pin header	Active energy pulses	Probe between here and ground for cumulative three-phase active energy pulses.	
AFEx_COMM (where x = 1, 2, or 3; not isolated, do not probe)	4-pin header	Communication header for MSP430i2401	This contains the UART and GPIO signals that are used to communicate with the MSP432 MCU.	These headers are on the MSP430i2041's side of the isolation barrier and it is referenced with respect to mains so do not probe here unless isolators external to the board are used. Instead of probing this header, it is recommended to probe the corresponding HOST_COMM header because this header is an isolated version oft he AFEx_COMM header. The AFE1_COMM header corresponds to phase A, the AFE2_COMM header corresponds to Phase B, and the AFE3_COMM header corresponds to phase C headers.
AFEx_EN (where x = 1, 2, or 3)	2-pin header	Output enable	Place a jumper here to disable communication from the corresponding phase to the MSP432 MCU.	This header can be used to access the EN2 pin of the ISO7731, which is used to disable the output from the MSP430i2041 to the MSP432. Driving the EN2 pin can be used to implement an alternative method(not supported in this design) to multiplex communication to the different MSP430i2041 devices. Note that this alternative implementation would only work with the ISO7731 devices and not the ISO7721 devices. Alternatively, placing a jumper at this header can be used to disable communication from the corresponding phase to the MSP432. The AFE1_EN header corresponds to phase A, the AFE2_EN header corresponds to Phase B, and the AFE3_EN header corresponds to phase C headers.

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表 **10. Header Names and Jumper Settings (continued)**

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
AFEx_EXTRA (where x = 1, 2, or 3; not isolated, do not probe)	3-pin header	MSP430i2041 P2.0 port pin	Place a jumper between pins 1 and 2 to connect P2.0 to GND. Place a jumper between pins 3 and 2 to connect P2.0 to VCC.	The P2.0 GPIO pin is not used in this design but may be used to add additional functionality. This header has VCC and GND, which can be connected to P2.0 when in input GPIO mode. This can be used for selecting different configuration options in hardware based on whether P2.0 is connected to GND or VCC. When configured in peripheral mode, P2.0 can also be used to feed in an external, isolated 16.384-MHz clock to be used as the system clock for the MSP430i2041. This header is on the MSP430i2041's side of the isolation barrier and it is referenced with respect to mains so do not probe here unless isolators external to the board are used. The AFE1_EXTRA header corresponds to phase A, the AFE2_EXTRA header corresponds to Phase B, and the AFE3_EXTRA header corresponds to phase C headers.
AFEx_IDy (where x = 1, 2, or 3 and y = 0 or 1)	3-pad jumper resistor	Phase identification	Place a 0-Ω resistor between the center pad of AFEx_ID0 and the "1" pad to set the least significant bit of the phase identification to 1. Place a 0-Ω resistor between the center pad of AFEx_ID0 and the "0" pad to set the least significant bit of the phase identification to 0. Place a 0-Ω resistor between the center pad of AFEx_ID1 and the "1" pad to set the most significant bit of the phase identification to 1. Place a 0-Ω resistor between the center pad of AFEx_ID1 and the "0" pad to set the most significant bit of the phase identification to 0.	The AFEx_ID0 and AFEx_ID1 jumper resistor options are used to set how each phase on the board identifies itself in software. The AFEx_ID0 jumper resistor option represents the least significant bit of the identification and the AFEx_ID1 jumper resistor represents the most significant bit of the identification. A phase identification value of 0 corresponds to phase A, a value of 1 corresponds to phase B, and a value of 2 corresponds to phase C. The AFE1_IDy headers correspond to phase A, the AFE2_IDy headers correspond to Phase B, and the AFE3_IDy headers correspond to phase C headers. As a result, AFE1_ID1 is connected to the "0" pad, AFE1_ID0 is connected to the "0" pad, AFE2_ID1 is connected to the "0" pad, AFE2_ID0 is connected to the "1" pad, AFE3_ID1 is connected to the "1" pad, and AFE3_ID0 is connected to the "0" pad.

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表 **10. Header Names and Jumper Settings (continued)**

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
AFEx_JTAG (where x = 1, 2, or 3; not isolated, do not program when connected to Mains)	4-pin header	2-wire JTAG programming option (WARNING)	To program the MSP430i2041 devices, configure AFEPWRx header to the external power option. In addition, connect pin 1 of this header to pin 2 of the MSP-FET tool, pin 2 of this header to pin 1 of the MSP-FET tool, pin 3 of this header to pin 7 of the MSP-FET tool , and pin 4 of this header to pin 9 of the MSP-FET tool.	Do not program the MSP430i2041 devices with the board connected to AC mains. The AFE1_JTAG header corresponds to phase A, the AFE2_JTAG header corresponds to Phase B, and the AFE3_JTAG header corresponds to phase C headers.
AFEx_OPTy (where x = 1, 2, or 3 and y = 1, 2, or 3)	3-pad jumper resistor	Additional GPIO port pins	Place a 0-Ω resistor between the center pad and "GND" pad, to connect the GPIO pin to GND. Place a 0-Ω resistor between the center pad and the "VCC" pad to connect the GPIO pin to VCC.	These GPIO pins are not used in this design but can be used to add additional functionality. These GPIO pins can be connected to VCC or GND by placing a 0 Ohm resistor at the appropriate pads. This can be used for selecting different configuration options in hardware based on whether the GPIO pins are connected to GND or VCC. The AFE1_OPTy headers corresponds to phase A, the AFE2_OPTy headers corresponds to Phase B, and the AFE3_OPTy headers corresponds to phase C headers. AFEx_OPT1 options are connected to the P2.3 GPIO pins, AFEx_OPT2 options are connected to the P1.7 GPIO pins, and AFEx_OPT3 options are connected to the P1.0 GPIO pins
AFEPWRx (where x = 1,2, or 3)	3-pin header	Selection for the high-side power supply for a phase	This header is used to select the power source for the MSP430i2041 and ISO7731 of a phase.	To enable powering the high-side using the onboard cap-drop supply, place a jumper between pins 1 and 2 of this header. To enable powering the high side by external power, place a jumper between pins 2 and 3 of this header. The external power can be applied at any other GND and VCC header option locations for the phase. An example location to connect external power to includes terminal block U$13 for phase A, terminal block U$17 for phase B, and terminal block U$14 for phase C. When programming the MSP430i2041 devices, make sure that the jumper is connected to the external option and mains is not enabled. The AFEPWR1 header corresponds to phase A, the AFEPWR2 header corresponds to Phase B, and the AFEPWR3 header corresponds to phase C headers.

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表 10. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
DGND	Header	Ground voltage header	Not a jumper header, probe here for GND voltage. Connect negative terminal of bench or external power supply when powering the board externally.	
DVCC	Header	VCC voltage header	Not a jumper header, probe here for VCC voltage. Connect positive terminal of bench or external power supply when powering the board externally.	
HOST_COMMx (where x = 1, 2, or 3)	4-pin header	Communication header for MSP432	This contains the UART and GPIO signals that are used to communicate with the MSP430i2041 devices.	These headers are on the MSP432's side of the isolation barrier, which is isolated from mains so they are safe to probe. The HOST_COMM1 header corresponds to the isolated version of the AFE1_COMM header. The HOST_COMM2 header corresponds to the isolated version of the AFE2_COMM header. The HOST_COMM3 header corresponds to the isolated version of the AFE3_COMM header.
HOST_EXTRA	3-pin header	External clock generation output	This design has a footprint that allows placing a clock generator (footprint is labeled CLK_GEN on the PCB) that can be used to generate a clock signal. When using this option, populating the clock generator footprint (not populated by default) and placing a 0-Ω resistor at R1 (also not populated by default) connects the generated clock to this header.	
INB_SELx (where x = 1, 2, or 3 and y = 1, 2, or 3)	3-pad jumper resistor	ISO7731 INB channel selection	Place a 0-Ω resistor between the center pad and "UTSI" pad to configure this design to use UART. Place a 0-Ω resistor between the center pad and "URSO" pad to configure this design to use SPI. Because this design's software uses UART for communication instead of SPI, make sure to place a 0-Ω resistor at the "UTSI" pad, which would connect the MSP430i2041's UART TX signal to the MSP432's corresponding UART RX signal for that phase.	Do not connect an input pin to the INB pin. This jumper resistor ensures this connection does not occur regardless if the hardware supports SPI or UART communication. The INB_SEL1 header corresponds to phase A, the INB_SEL2 header corresponds to Phase B, and the INB_SEL3 header corresponds to phase C headers.

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表 **10. Header Names and Jumper Settings (continued)**

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
JTAG	10-pin 2-row connector	MSP432 programming header	Connect the MSP-FET-432ADPTR adapter to this connector to power the MSP432 MCU	The MSP-FET-432ADPTR is used to allow the MSP-FET tool to program the MSP432 device. One connector of the MSP-FET-432ADPTR adapter connects to the FET tool and the other connector connects to the MSP432's JTAG connector. Note that the MSP432 has to be powered externally to program the MSP432 MCU. The external power can be provided between DVCC and DGND on the board or a cable can be connected from the "DVCC" header on the board to the "VCC Output" header option of the MSP-FET-432ADPTR adapter.
LOGICx	2 3-pin headers	Optional logic header	Probe here for inputs and outputs of two channel gates. To work with three inputs, the output of one gate may be connected to the input of another gate.	An alternative method to share one MSP432 UART Rx function with the multiple MSP430i2041 UART Tx pins is to logically AND or logically OR the different isolated, UART Tx pins and to feed the output of the gate to only one MSP432 UART Rx pin. The U9 footprint (not populated by default) allows adding a logic gate, such as the SN74LVC2G08, to perform this operation. The LOGIC1 and LOGIC2 headers allow accessing the inputs and outputs of these logical gates. The software for this design does not support this alternative implementation for sharing one UART Rx function and instead uses the port mapping controller to multiplex using one UART Rx function.
OUTC_SELx (where x = 1, 2, or 3 and y = 1, 2, or 3)	3-pad jumper resistor	ISO7731 OUTC channel selection	Place a 0-Ω resistor between the center pad and "URSO" pad to configure this design to use UART. Place a 0-Ω resistor between the center pad and "UTSI" pad to configure this design to use SPI. Because this design's software uses UART for communication instead of SPI, make sure to place a 0-Ω resistor at the "URSO" pad, which would connect the MSP430i2041's UART RX signal to the MSP432's UART TX signal.	Do not connect an output pin to the OUTC pin. This jumper resistor ensures this connection does not occur regardless if the hardware supports SPI or UART communication. The OUTC_SEL1 header corresponds to phase A, the OUTC_SEL2 header corresponds to Phase B, and the OUTC_SEL3 header corresponds to phase C headers.

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表 **10. Header Names and Jumper Settings (continued)**

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
P7	4-pin header	MSP432 P7.0, P7.1, P7.2 and P7.3 headers	Probe here for P7.0, P7.1, P7.2, and P7.3 GPIO pins.	The P7.0, P7.1, and P7.2 headers are used for adjusting contrast of the LCD. P7.3 is not used in this design. P7.3 is a port mappable GPIO pin so multiple functions can be brought out to this pin. If more port mappable GPIO pins are needed, P7.0, P7.1, and P7.2 can also be used by disabling the LCD contrast control feature and removing resistors R18, R17, R7, and R6 from the board.
REACT	1-pin header	Reactive energy pulses	Probe between here and ground for cumulative three-phase reactive energy pulses	
RS232_3.3	1-pin header	Voltage source harvested from RS-232 line	Voltage source that is used to power the TRS3232E-Q1 and ISO7321 for isolated RS-232 communication. This voltage source is harvested from the RS-232 line	
RS232_GND	1-pin header	Ground connection for the isolated RS-232	Ground connection for the isolated RS-232 circuitry	
RX_EN	Jumper header	RS-232 receive enable	Place a jumper here to enable receiving characters using RS-232	
TX_EN	Jumper header	RS-232 transmit enable	Place a jumper here to enable RS-232 transmissions	

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3.1.3 Software

The software in this reference design consists of the metrology software that is loaded onto the MSP430i2041 as well as the host software loaded onto the MSP432P4111. The following section discusses how to get started with the software.

3.1.3.1 Loading Metrology Code Onto MSP430i2041 Devices

The MSP430i2041 source code is developed in the IAR™ environment using the IAR compiler version 6.x. Earlier versions of IAR cannot open the project files. When the project is loaded in IAR version 6.x or later, the integrated development environment (IDE) prompts the user to create a backup. Click "YES" to proceed. There are three main parts to the energy metrology software:

- The toolkit that contains a library of mostly mathematics routines
- The metrology code that is used for calculating metrology parameters
- The application code that is used for communication to the MSP432 host

图 22 shows the contents of the *msp430-emeters-i2040* folder, which contains the IAR projects for the MSP430i2041.

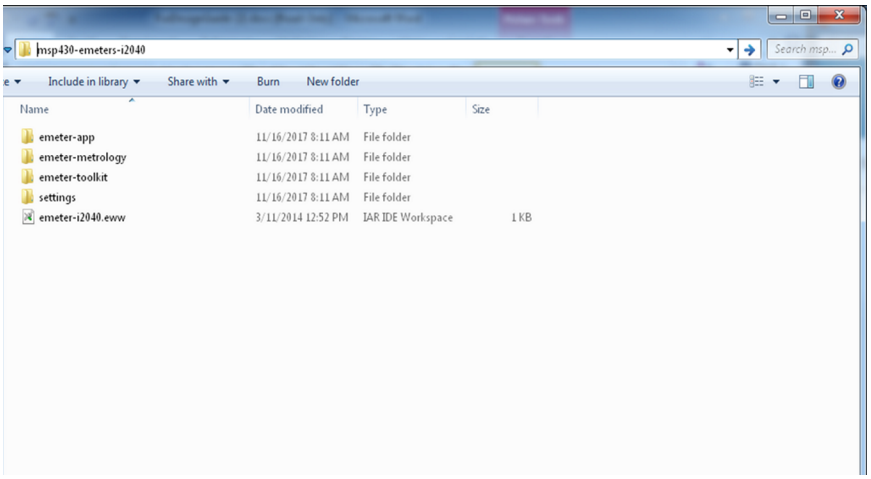

图 22. Source Folder Structure

Within the *emeter-app-i2041* folder in the *emeter-app* folder, the *emeter-app-i2041.ewp* project corresponds to the application code. Similarly, within the *emeter-metrology-i2041* folder in the *emeter-metrology* folder, the *emeter-metrology-i2041.ewp* project corresponds to the portion of the code for metrology. Additionally, the folder *emeter-toolkit-i2041* within the *emeter-toolkit* has the corresponding toolkit project file *emeter-toolkit-i2041.ewp*. For first-time use, TI recommends that all three projects be completely rebuild by performing the following steps:

1. Open the IAR IDE.
2. Open the emeter-i2040 workspace, which is located in the *Source* folder.
3. Within IAR workspace window, click the *Overview* tab to have a list view of all the projects.
4. Right-click the *emeter-toolkit-i2041* option in the workspace window and select *Rebuild All*, as 图 23 shows.
5. Right-click the *emeter-metrology-i2041* option in the workspace window and select *Rebuild All*, as 图 24 shows.
6. Within IARs workspace window, click the *emeter-app-i2041* tab.
7. Within the workspace window, select *emeter-app-i2041*, click *Rebuild All* as 图 25 shows, and then

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download this project onto the MSP430i2041 device.

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Note that if any changes are made to any of the files in the toolkit project and the project is compiled, the metrology project must be recompiled. After recompiling the metrology project, the application project must then be recompiled. Similarly, if any changes are made to any of the files in the metrology project and the project is compiled, the application project must then be recompiled.

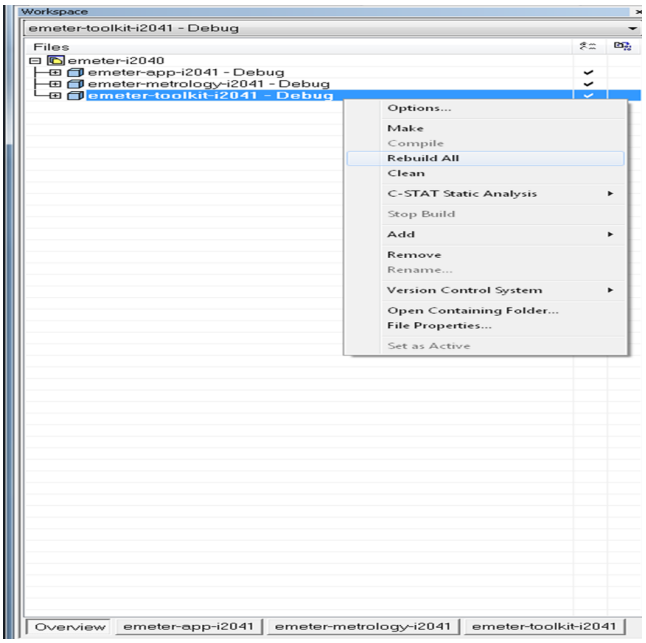

图 **23. Toolkit Project Compilation**

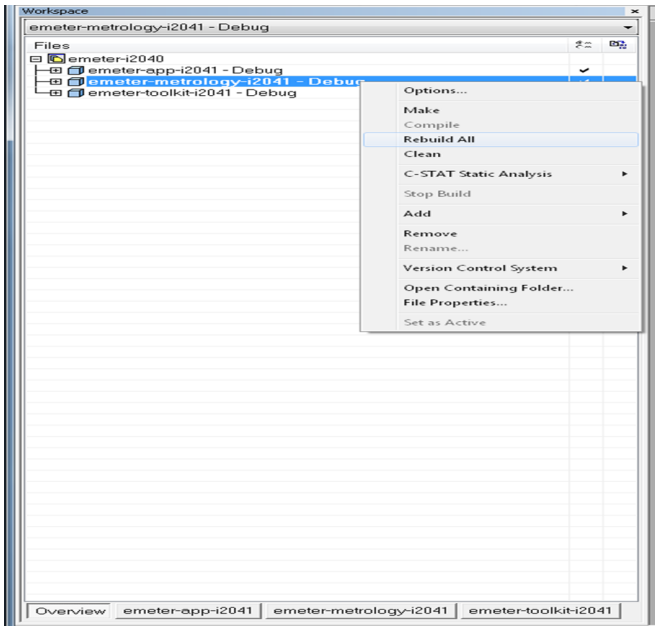

图 **24. Metrology Project Compilation**

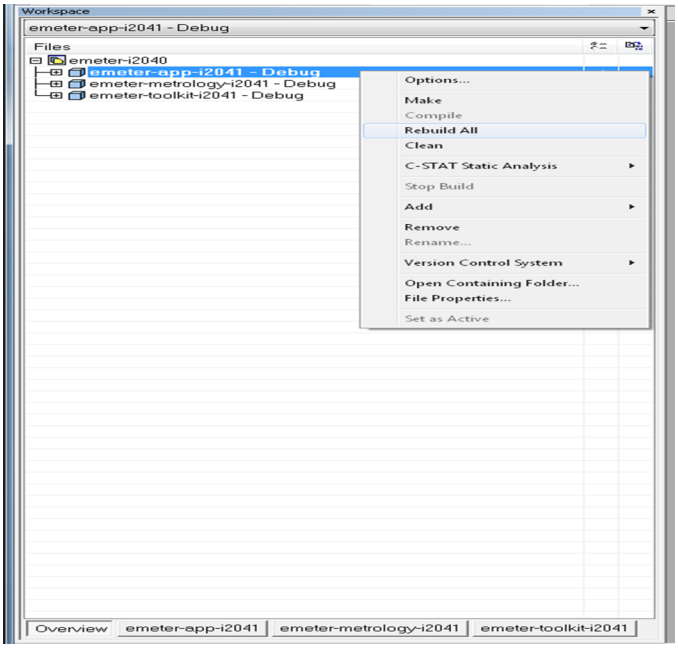

图 **25. Application Project Compilation**

After an executable file has been created, multiple MSP430i2041 devices can also be programmed simultaneously using the MSP-Gang production programmer.

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3.1.3.2 Loading Metrology Code Onto MSP432P4111

The MSP432 code is developed with Code Composer Studio™ (CCS) Version: 7.2.0.00013. To load this firmware onto the MSP432 MCU after installing CCS, follow these instructions:

1. Download the SimpleLink MSP432 SDK available at http://www.ti.com/tool/simplelink-msp432-sdk.
2. Open CCS.
3. From the CCS menu bar, click *File* and select *Import*.
4. From the import dialog box, expand the *Code Composer Studio* folder, select *CCS Projects*, then press the *Next* button.
5. Make sure the *Select search-directory* radio button is pressed and then press the *Browse* button next to this button.
6. Navigate and select the directory where the design's firmware is located.
7. Select the discovered projects in the *Discovered projects* region of the window and click *Finish*.
8. Select the design's projects in *Project Explorer*.
9. Compile the projects by clicking *Project* from the menu bar and then clicking *Build Project* for each project.
10. The project settings are configured so that the MSP-FET debugger and MSP-FET-432ADPTR adapter combination are the default options to program the MSP432P4111. If another debugger is used to program the MSP432 device, update the project settings accordingly to use this other debugger.
11. Load the program onto the MSP432 by clicking *Run* from the menu bard and then clicking *Debug*.

3.1.3.3 metrology-settings.h

The metrology-settings.h file contains different options for configuring the MSP432's metrology settings. Some of these options include the following:

- TWO_ISOLATION_CHANNELS: This macro determines whether the MSP432 MCU is configured in two-channel mode or three-channel mode. In two-channel mode, the MSP432's UART RX functionality for a phase is shared with the DRDY functionality of that phase so that only two isolation channels are used. In three-channel mode, the DRDY functionality and UART RX functionality are done on different pins so there are three channels that are necessary. By defining this macro, the MSP432P4111 is configured in two channel mode. By not defining this macro, the MSP432 device is configured in three channel mode. Both the MSP430i2041 devices and MSP432 MCU must have the same settings on whether this macro is defined. If TWO_ISOLATION_CHANNELS is defined in the MSP432's metrology-settings.h, then TWO_ISOLATION_CHANNELS must also be defined in the emeter-template.h file in the MSP430i2041 project. If TWO_ISOLATION_CHANNELS is not defined in the MSP432's metrology-settings.h, then TWO_ISOLATION_CHANNELS must also not be defined in the emeter-template.h file in the MSP430i2041 project.
- RESIDUAL_POWER_CUTOFF: Tiny power levels must not record energy at all, as they can just be rounding errors, noise, or the consumption of the meter itself. This value is the cutoff level in milliwatts (this is the cutoff per phase). If the absolute value of power for a phase is below this threshold, then the phase would not output energy pulses and the energy buffers also will not be updated. In addition, that phase will not contribute to the cumulative active energy reading used to output energy pulses and update the energy buffers. Note that even if the absolute value of a phase's power is smaller than RESIDUAL_POWER_CUTOFF, the active power readings would not get zeroed out. This macro only operates on the energy readings.
- TOTAL_RESIDUAL_POWER_CUTOFF: Tiny power levels must not record energy at all, as they can just be rounding errors, noise, or the consumption of the meter itself. This value is the cutoff level in milliwatts (this is the cutoff per phase). If the absolute value of the cumulative power is below this

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threshold, then cumulative energy pulses will not be output and the energy buffers also will not be updated. Note that even if the absolute value of cumulative power is smaller than TOTAL_RESIDUAL_POWER_CUTOFF, the active power readings would not get zeroed out. This macro only operates on the energy readings.

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- INTERRUPTION_THRESHOLD: A voltage interruption state is defined when a voltage that is 1 V smaller than this macro value divided by 1000 (that is, if the voltage in volts is smaller than ((INTERRUPTION_THRESHOLD/1000)-1). The state exits the voltage interruption state when the voltage is greater than 1 V larger than this macro divided by 1000 (that is, the voltage in volts is larger than ((INTERRUPTION_THRESHOLD/1000)+1). This macro is used to determine when to sync again to find the new phase sequence after there is a voltage interruption.
- ACTIVE_ENERGY_PULSES_PER_KW_HOUR: This macro defines the total number of pulses per 1 kWh of active energy at each phase. In this application, individual phase energy pulse generation is disabled so this macro is disabled.
- REACTIVE_ENERGY_PULSES_PER_KVAR_HOUR: This macro defines the total number of pulses per 1 kilovar of reactive energy at each phase. In this application, individual phase energy pulse generation is disabled so this macro is disabled.
- APPARENT_ENERGY_PULSES_PER_KVA_HOUR: This macro defines the total number of pulses per 1 kVA of apparent energy at each phase. In this application, individual phase energy pulse generation is disabled so this macro is disabled.
- TOTAL_ACTIVE_ENERGY_PULSES_PER_KW_HOUR: This sets the number of pulses per kilo-watt hour the meter will produce at its total active energy pulse. It does not affect the energy accumulation process. The default setting for this macro is 6400.
- TOTAL_REACTIVE_ENERGY_PULSES_PER_KVAR_HOUR: This sets the number of pulses per kilovar hour the meter will produce at its total reactive energy pulse. It does not affect the energy accumulation process. The default setting for this macro is 6400.
- TOTAL_APPARENT_ENERGY_PULSES_PER_KVA_HOUR: This sets the number of pulses per kVA hour the meter will produce at its total apparent energy pulse. It does not affect the energy accumulation process. Apparent energy pulse generation is disabled in the code, so this macro is disabled.
- ENERGY_PULSE_DURATION: The duration of the LED on time for an energy pulse. This is measured in timer interrupts (that is, increments 1/4000 s). The maximum allowed is 255, giving a pulse of approximately 64 ms. The default value for this macro is 20. For higher pulses/kWh constants, the value for this macro may need to be reduced.
- ACTIVE_ENERGY_SUPPORT: This switch selects support for measuring the active energy consumption on a phase by phase basis. This will allow the GUI to display each phase's active energy consumption in kWh.
- REACTIVE_ENERGY_SUPPORT: This switch selects support for measuring the reactive energy consumption on a phase by phase basis. This will allow the GUI to display each phase's reactive energy consumption in kvarh.
- APPARENT_ENERGY_SUPPORT: This switch selects support for measuring the apparent energy consumption on a phase by phase basis. This will allow the GUI to display each phase's apparent energy consumption in kVA.
- TOTAL_ACTIVE_ENERGY_SUPPORT: This switch selects support for measuring the total active energy consumption. This will allow the GUI to display the cumulative phase's active energy consumption in kWh. This is disabled for the neutral-monitoring configuration.
- TOTAL_REACTIVE_ENERGY_SUPPORT: This switch selects support for measuring the total reactive energy consumption. This will allow the GUI to display the cumulative phase's reactive energy consumption in kvarh. This is disabled for the neutral-monitoring configuration.

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- TOTAL_APPARENT_ENERGY_SUPPORT: This switch selects support for measuring the total apparent energy consumption. This will allow the GUI to display the cumulative phase's apparent energy consumption in kVA. This is disabled for the neutral-monitoring configuration.

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3.2 Testing and Results

3.2.1 Test Setup

To test for metrology accuracy, a source generator was used to provide the voltages and currents to the system at the proper locations mentioned in 节 3.1.2.1. Additionally, a nominal voltage of 230 V, calibration current of 10 A, and nominal frequency of 50 Hz are used for each phase.

When the voltages and currents are applied to the system, the system outputs the cumulative active energy pulses and cumulative reactive energy pulses at a rate of 6400 pulses/kWh. This pulse output is fed into a reference meter (in the test equipment for this reference design, this pulse output is integrated in the same equipment used for the source generator) that determines the energy % error based on the actual energy provided to the system and the measured energy as determined by the system's active and reactive energy output pulse. In this reference design, cumulative active energy error testing, cumulative reactive energy error testing, and frequency variation testing are performed after performing energy gain calibration, phase compensation, and energy offset calibration as described in 节 3.2.2.2.2.

For cumulative active energy error and cumulative reactive energy error testing, current is varied from 100 mA to 80 A simultaneously at each phase. For cumulative active energy error testing, a phase shift of 0°, 60°, and −60° is applied between the voltage and current channels. Based on the error from the active energy output pulse, a plot of active energy % error versus current is created for 0°, 60°, and –60° phase shifts. For cumulative reactive energy error testing, a similar process is followed except that 30°, 60°, –30°, and –60° phase shifts are used and cumulative reactive energy error is plotted instead of cumulative active energy error. Another set of tests performed are frequency variation tests. For this test, the frequency is varied by ±2 Hz from its 50-Hz nominal frequency. This test is conducted at 1 A and 10 A at phase shifts of 0°, 60°, and −60°. The resulting active energy error under these conditions are logged.

3.2.2 Viewing Metrology Readings and Calibration

3.2.2.1 Viewing Results from LCD

The LCD scrolls between metering parameters every two seconds. For each metering parameter that is displayed on the LCD, three items are usually displayed on the screen: a symbol used to denote the phase of the parameter, text to denote which parameter is being displayed, and the actual value of the parameter. The phase symbol is displayed at the top of the LCD and denoted by a triangle shape. The orientation of the symbol determines the corresponding phase. 图 26, 图 27, and 图 28 show the mapping between the different orientations of the triangle and the phase descriptor:

图 **26. Symbol for Phase A**

图 **27. Symbol for Phase B**

图 **28. Symbol for Phase C**

Aggregate results (such as cumulative active and reactive power) and parameters that are independent of phase (such as time and date) are denoted by clearing all of the phase symbols on the LCD.

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The bottom line of the LCD is used to denote the value of the parameter being displayed. The text to denote the parameter being shown displays on the top line of the LCD. 表 11 shows the different metering parameters that are displayed on the LCD and the associated units in which they are displayed. The designation column shows which characters correspond to which metering parameter.

表 **11. Displayed Parameters**

PARAMETER NAME	DESIGNATION	UNITS	COMMENTS
Active power	AcPo	Watt (W)	This parameter is displayed for each phase. The aggregate active power is also displayed.
Reactive power	rEPo	Volt-Ampere Reactive (var)	This parameter is displayed for each phase. The aggregate reactive power is also displayed.
Apparent power	APPo	Volt-Ampere (VA)	This parameter is displayed for each phase.
Power factor	PF	Constant between 0 and 1	This parameter is displayed for each phase.
Voltage	Vrms	Volts (V)	This parameter is displayed for each phase.
Current	Irms	Amps (A)	This parameter is displayed for each phase.
Frequency	Fr2q	Hertz (Hz)	This parameter is displayed for each phase.
Total consumed active energy	AcEn	kWh	This parameter is displayed for each phase.
Total consumed reactive energy	rEEn	kVarh	This parameter is displayed for each phase. This displays the sum of the reactive energy in quadrant 1 and quadrant 4.
Time	t inE	Hour:minute:second	This parameter is only displayed when the sequence of aggregate readings are displayed. This parameter is not displayed once per phase.
Date	dAtE	Year:month:day	This parameter is only displayed when the aggregate readings are displayed. This parameter is not displayed once per phase.

图 29 shows an example of phase B's measured frequency of 49.99 Hz displayed on the LCD.

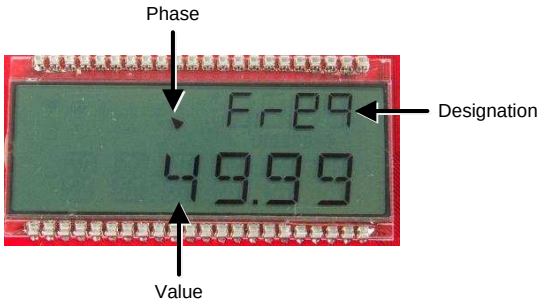

图 **29. LCD**

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3.2.2.2 Calibrating and Viewing Results From PC

3.2.2.2.1 Viewing Results

To view the metrology parameter values from the GUI, perform the following steps:

1. Connect the EVM to a PC using an RS-232 cable.
2. Open the GUI folder and open *calibration-config.xml* in a text editor.
3. Change the *port name* field within the *meter* tag to the COM port connected to the system. As 图 30 shows, this field is changed to *COM7*.

```
260        </correction>
261      </phase>
262      <temperature/>
263      <rtc/>
264    </cal-defaults>
265    <meter position="1">
266      <port name="com7" speed="9600"/>
267    </meter>
268    <reference-meter>
269      <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270      <type id="chroma-66202"/>
271      <log requests="on" responses="on"/>
272      <scaling voltage="1.0" current="1.0"/>
273    </reference-meter>
```

图 30. GUI Configuration File Changed to Communicate With Energy Measurement System

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4. Run the *calibrator.exe* file, which is located in the GUI folder. If the COM port in the *calibration-config.xml* was changed in the previous step to the COM port connected to the EVM, the GUI opens (see 图 31). If the GUI connects properly to the design, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

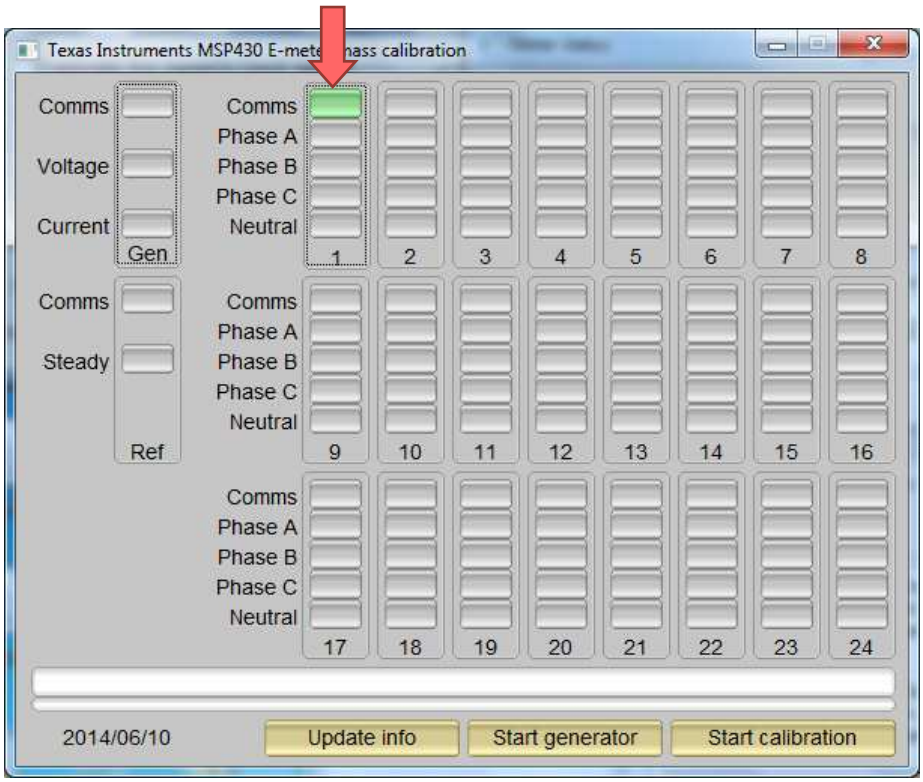

图 31. GUI Startup Window

Upon clicking on the green button, the results window opens (see 图 32). In the figure, there is a trailing "L" or "C" on the *Power factor* values to indicate an inductive or capacitive load, respectively. In order to get the Phase to Phase Sequence to work with the current version of the GUI, there were some changes made that cause a couple misleading values to appear on the GUI. In the GUI, it displays a fundamental active power of 0; however, note that the fundamental active power reading is not actually taken despite it being enabled in the GUI. In addition, the phase sequence is determined by looking at the order of the "Phase to Phase" fields in the GUI for the different phases. The following combinations for the different phase's "Phase to Phase" value corresponds to a phase ABC rotation, where Phase A is at 0°, Phase B is at 120°, and Phase C is at 240°:

- 0.04° for Phase A, 0.00° for Phase B, 0.02° for Phase C (as shown in 图 32)
- 0.00° for Phase A, 0.02° for Phase B, 0.04° for Phase C
- 0.02° for Phase A, 0.04° for Phase B, 0.00° for Phase C

When there is a CBA rotation, where Phase A is at 0°, Phase B is at 240°, and Phase C is at 120°, the GUI displays one of the three possible combinations for "Phase to Phase" readings:

- 0.04° for Phase A, 0.02° for Phase B, 0.00° for Phase C
- 0.00° for Phase A, 0.04° for Phase B, 0.02° for Phase C
- 0.02° for Phase A, 0.00° for Phase B, 0.04° for Phase C

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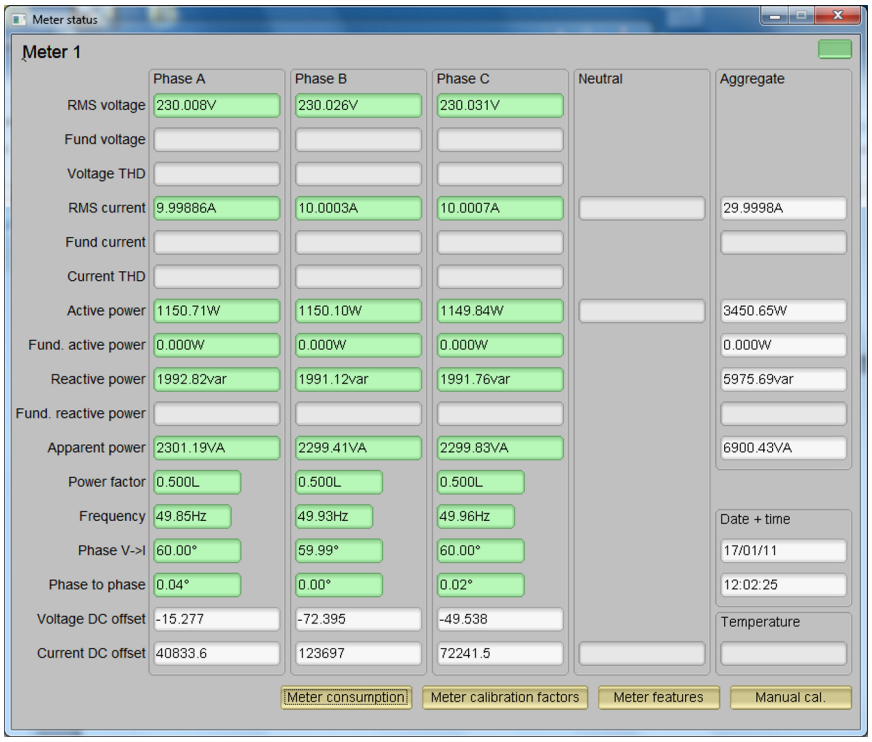

图 **32. GUI Results Window**

From the results window, the total-energy consumption readings and sag or swell logs can be viewed by clicking the *Meter Consumption* button. After the user clicks this button, the *Meter events and consumption* window pops up, as 图 33 shows.

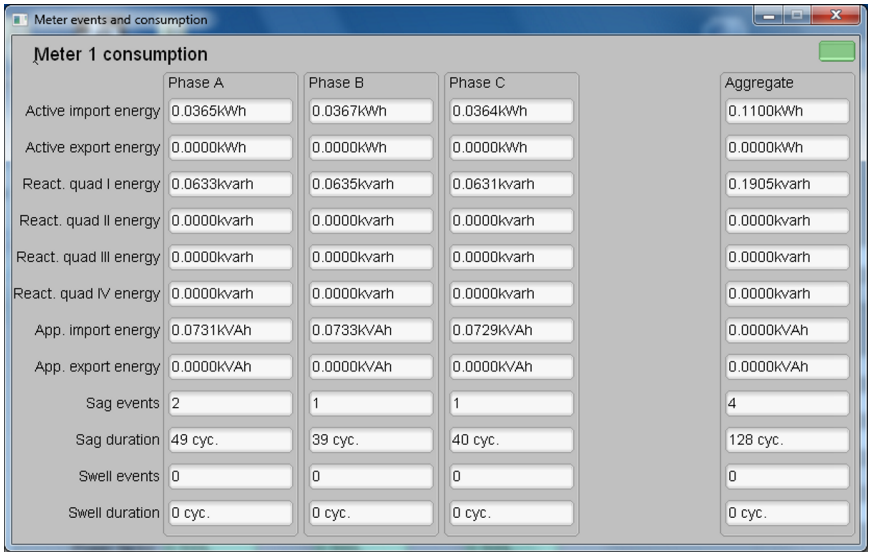

图 **33. Meter Events and Consumption Window**

From this *Meter events and consumption* window, the user can view the meter settings by clicking the *Meter features* button, view the system calibration factors by clicking the *Meter calibration factors* button, or open the window used for calibrating the system by clicking the *Manual cal.* button.

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3.2.2.2.2 Calibration

Calibration is key to any meter performance, and it is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify their effects, every meter must be calibrated. To perform calibration accurately, there must be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this three-phase design.

The GUI used for viewing results can easily be used to calibrate the design. During calibration, parameters called calibration factors are modified in software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, active power offset (erroneously called voltage AC offset in the GUI), current scaling factor, reactive power offset (erroneously called voltage AC offset in the GUI), power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the meter SW is flashed on the MSP430i2041 devices for the first time (available in the **.zip* file), default calibration factors are loaded into these calibration factors. These values are to be modified through the GUI during calibration. The calibration factors are stored in INFO_MEM, and therefore, remain the same if the meter is restarted.

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with 节 3.1.2.1, and the energy pulses connected to the reference meter.

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3.2.2.2.2.1 Gain Calibration

Usually, gain correction for voltage and current can be done simultaneously for all phases. However, energy accuracy (%) from the reference meter for each individual phase is required for gain correction for active power. Also, when performing active power calibration for any given phase, the other two phases must be turned OFF by turning off the current but leaving the other voltages still enabled.

3.2.2.2.2.1.1 Voltage and Current Gain Calibration

To calibrate the voltage and current readings, perform the following steps:

1. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
2. Configure the test source to supply desired voltage and current for all phases. Ensure that these are the voltage and current calibration points with a zero-degree phase shift between each phase voltage and current. For example, for 230 V, 10 A, 0º (PF = 1). Typically, these values are the same for every phase.
3. Click on the *Manual cal.* button that 图 32 shows. The following screen pops up from 图 34:

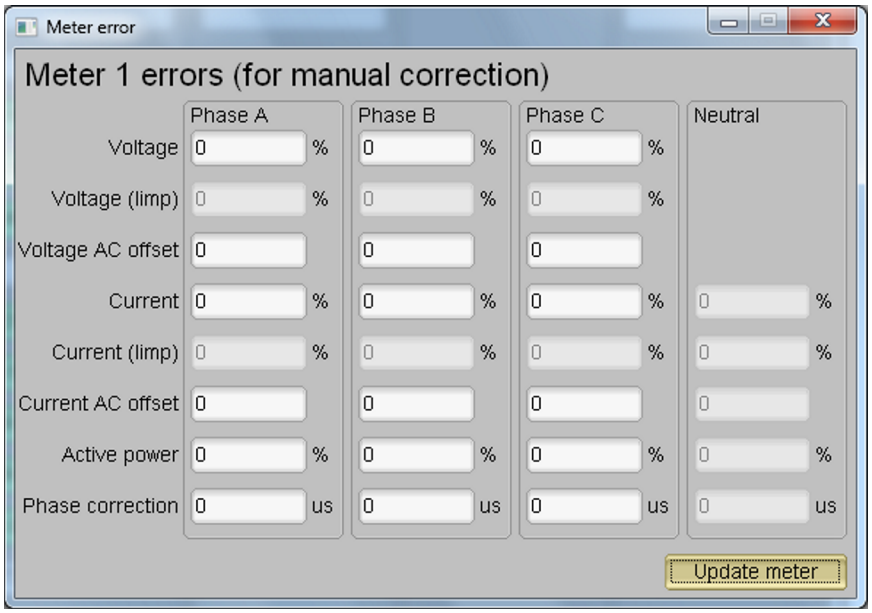

图 **34. Manual Calibration Window**

4. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated using 公式 11:

$$\text{Correction (\%)} = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \tag{11}$$

where:

- $\text{value}_{\text{observed}}$ is the value measured by the TI meter
- $\text{value}_{\text{desired}}$ is the calibration point configured in the AC test source

5. After calculating for all voltages and currents, input these values as is (±) for the fields *Voltage and Current* for the corresponding phases.
6. Click on the *Update meter* button and the observed values for the voltages and currents on the GUI settle immediately to the desired voltages and currents.

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3.2.2.2.2.1.2 Active Power Gain Calibration

注: This section is an example for one phase. Repeat these steps for other phases.

After performing gain correction for voltage and current, gain correction for active power must be done. Gain correction for active power is done differently in comparison to voltage and current. Although, conceptually, calculating using Step 4 with active power readings (displayed on the AC test source) can be done, this method is not the most accurate and should be avoided.

The best option to get the *Correction (%)* is directly from the reference meters measurement error of the active power. This error is obtained by feeding energy pulses to the reference meter. To perform active power calibration, perform the following steps:

1. Turn off the system and connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
2. Turn on the AC test source.
3. Repeat Step 1 to Step 3 from 节 3.2.2.2.2.1.1 with the identical voltages, currents, and 0º phase shift that were used in the same section.
4. Obtain the % error in measurement from the reference meter. Note that this value may be negative.
5. Enter the error obtained in Step 4 into the *Active Power* field under the corresponding phase in the GUI window. This error is already the value and does not require calculation.
6. Click the *Update meter* button and the error values on the reference meter immediately settle to a value close to zero.

3.2.2.2.2.2 Phase Calibration

After performing power gain correction, phase calibration must be performed. Similar to active power gain calibration, to perform phase correction on one phase, the other phases must be disabled. To perform phase correction calibration, perform the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform Step 1 through Step 3 from 节 3.2.2.2.2.1.1 using the identical voltages and currents used in that section.
2. Disable all other phases that are not currently being calibrated by setting the current of these phases to 0 A.
3. Modify only the phase-shift to a non-zero value; typically, +60º is chosen. The reference meter now displays a different % error for active power measurement. Note that this value may be negative.
4. If the error from Step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
   a. Enter a value as an update for the *Phase Correction* field for the phase that is being calibrated. Usually, a small ± integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: +60º), a positive (negative) error requires a positive (negative) number as correction.
   b. Click on the *Update meter* button and monitor the error values on the reference meter.
   c. If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on Step 4a and Step 4b. Note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
   d. Change the phase now to −60° and check if this error is still acceptable. Ideally, errors must be symmetric for same phase shift on lag and lead conditions.

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3.2.2.2.2.3 Offset Calibration

After performing phase correction, if the accuracy at low currents is not acceptable, offset calibration must be performed. Offset calibration removes any crosstalk such as the crosstalk to a phase's current channels from the line voltages of other phases and the neutral.

To perform active power offset calibration for a phase, simply add the offset to be subtracted from the active power reading (in units of mW) to the current value of the active power offset (labeled "voltage AC off" in the meter calibration factors window) and then enter this new value in the *Voltage AC offset* field in the Manual Calibration window. As an example, if the "voltage AC off" has a value of 200(0.2W) in the meter calibration window, and it is desired to subtract an additional 0.300 mW, then enter a value of 500 in the *Voltage AC offset* field in the Manual Calibration window. After entering the value in the *Voltage AC offset* field in the Manual Calibration window, press "Update meter".

To perform reactive power offset calibration for a phase, a similar process is followed as the process used to perform active power offset calibration. Add the offset to be subtracted from the reactive power reading (in units of mvar) to the current value of the reactive power offset (labeled "Current AC offset" in the meter calibration factors window) and then enter the value in the *Current AC offset* field in the Manual Calibration window. After entering the value in the *Current AC offset* field in the Manual Calibration window, press "Update meter".

After performing offset correction, calibration is complete for one phase. Gain calibration, phase calibration, and offset calibration must be performed for the other phases.

This completes calibration of voltage, current, and power for all three phases. View the new calibration factors (see 图 35) by clicking the *Meter calibration factors* button of the GUI metering results window in 图 32. For these displayed calibration factors, note that the "Voltage AC off" parameter actually represents the active power offset (in units of mW) subtracted from each measurement and the "Current AC offset" parameter actually represents the reactive power offset subtracted (in units of mvar) from reactive power readings.

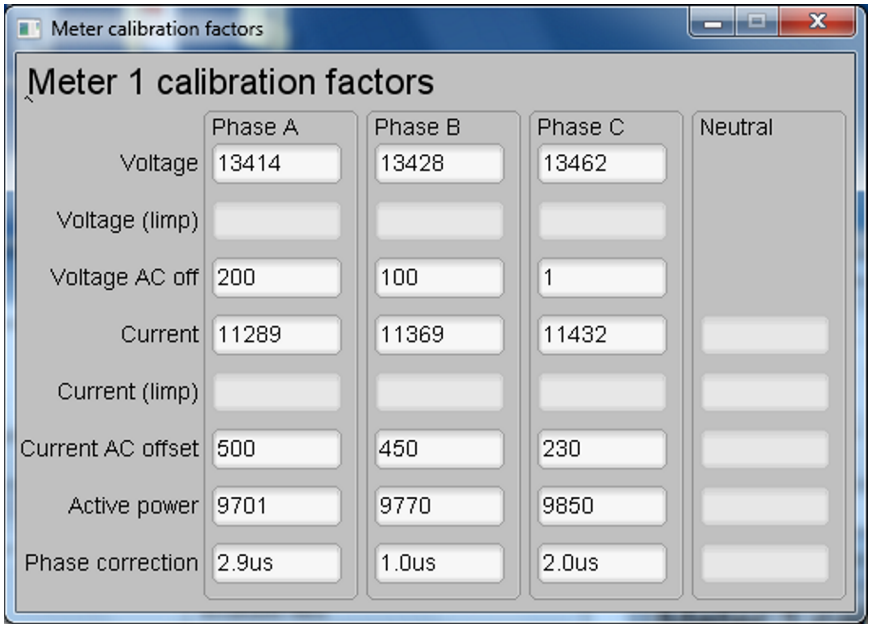

图 35. Calibration Factors Window

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Also view the configuration of the system by clicking on the *Meter features* button in 图 32 to get to the window that 图 36 shows.

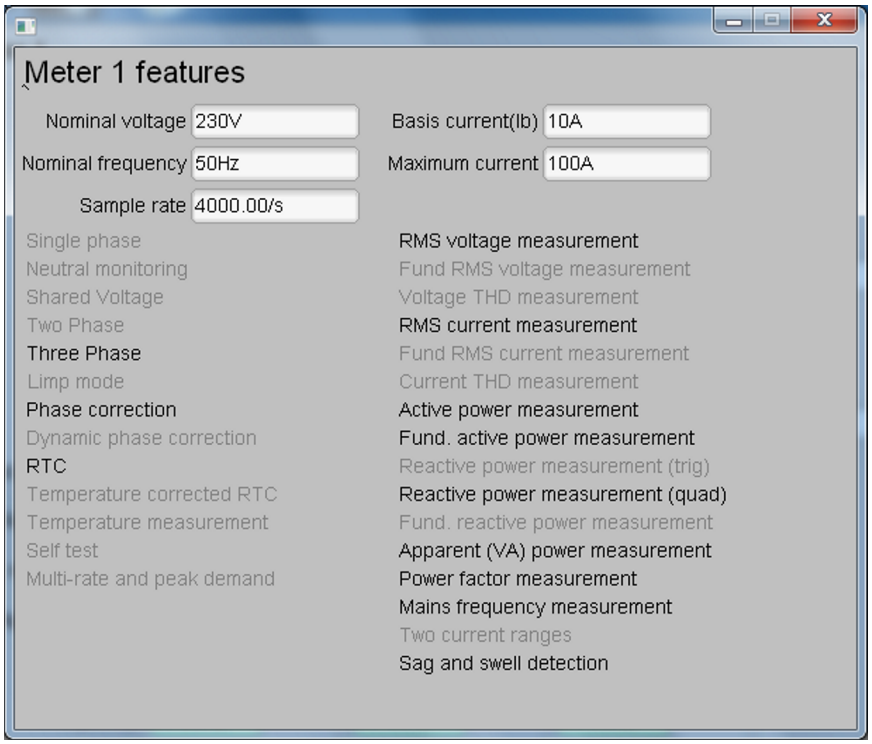

图 36. Meter Features Window

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3.2.3 Test Results

For the following test results, gain, phase, and offset calibration are applied to the meter. At higher currents, the % error shown is dominated by shunt resistance drift caused by the increased heat generated at high currents.

表 12. Cumulative Active Energy % Error Versus Current, 400-µΩ Shunts

CURRENT (A)	0°	60°	–60°
0.1	–0.0095	0.1495	0.13
0.25	0.0027	0.025	0.0245
0.5	0.0115	–0.004	0.063
1	0.007	–0.031	–0.002
2	–0.013	–0.024	–0.002
5	–0.02	–0.023	0.003
10	–0.017	–0.032	–0.002
20	–0.026	–0.049	–0.039
30	–0.032	–0.06	–0.067
40	–0.057	–0.097	–0.099
50	–0.096	–0.149	–0.109
60	–0.147	–0.205	–0.194
70	–0.182	–0.253	–0.251
80	–0.241	–0.3	–0.31

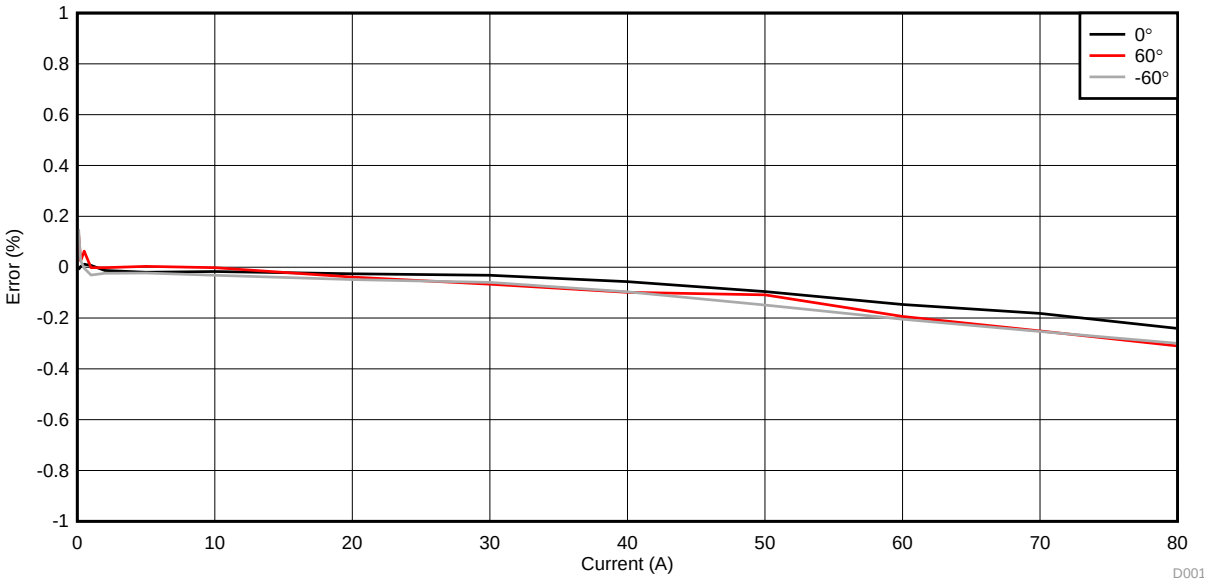

图 37. Cumulative Active Energy % Error Versus Current, 400-µΩ Shunts

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表 13. Cumulative Active Energy % Error Versus Current, 220-µΩ Shunts

CURRENT (A)	0°	60°	–60°
0.1	–0.208	–0.3503	–0.227
0.25	–0.054	–0.1633	–0.0665
0.5	0.001	–0.0933	0.022
1	0.04	–0.034	0.0187
2	0.019	–0.0195	0.034
5	0.028	–0.0185	0.061
10	0.0375	–0.018	0.075
20	0.0243	–0.022	0.05
30	0.028	–0.031	0.051
40	0.019	–0.046	0.025
50	–0.006	–0.082	0.008
60	–0.024	–0.11	–0.016
70	–0.055	–0.149	–0.056
80	–0.1	–0.197	–0.112

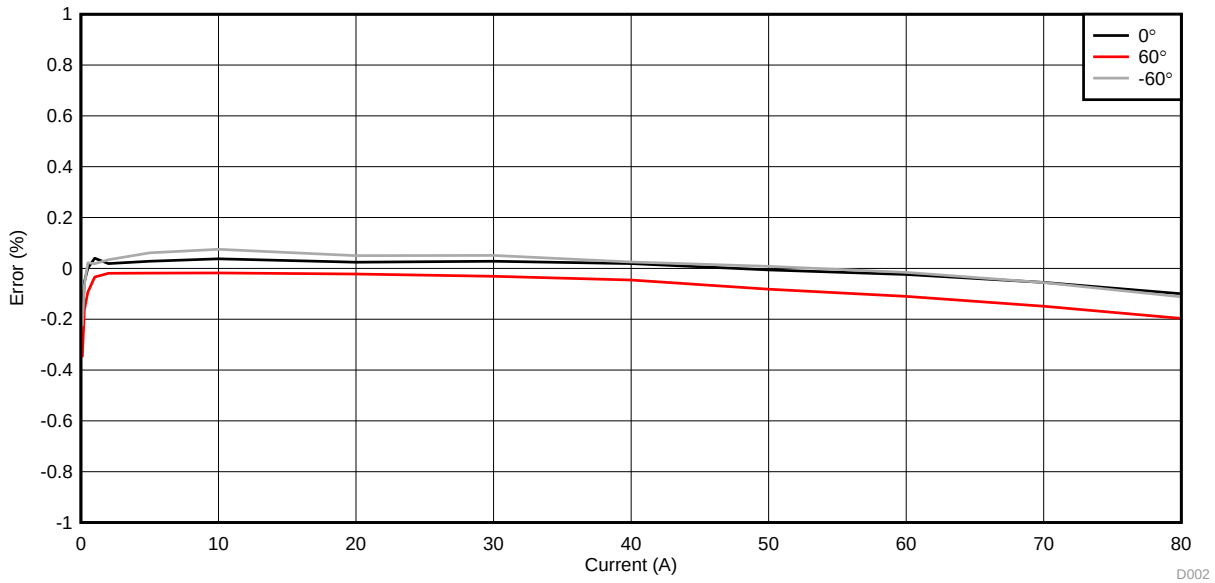

图 38. Cumulative Active Energy % Error Versus Current, 220-µΩ Shunts

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表 14. Cumulative Reactive Energy % Error Versus Current

CURRENT (A)	30°	60°	–30°	–60°
0.1	–0.1395	0.0215	0.023	0.0355
0.25	–0.1895	–0.1443	0.0917	0.0817
1	–0.0853	–0.0567	0.0063	–0.003
5	–0.042	–0.0363	–0.015	–0.027
10	–0.0363	–0.0303	–0.019	–0.016
30	–0.079	–0.07	–0.045	–0.06
50	–0.091	–0.111	–0.099	–0.12
80	–0.139	–0.17	–0.2	–0.22

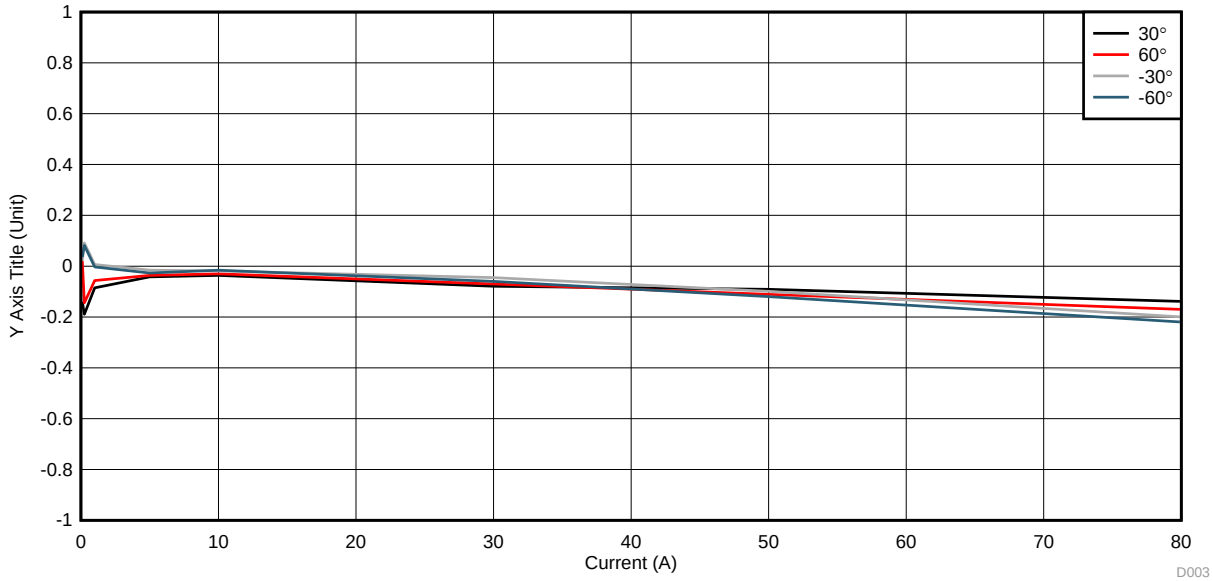

图 39. Cumulative Reactive Energy % Error Versus Current

表 15. Cumulative Active Energy Measurement Error Versus Frequency, ±2 Hz From Nominal Frequency

CONDITIONS	48 Hz	50 Hz	52 Hz
1 A, 0°	0.022	0.0075	–0.022
1 A, 60°	0.0057	–0.0173	–0.024
1 A, 300°	0.01	0.006	–0.0183
10 A, 0°	–0.0127	–0.0177	–0.0263
10 A, 60°	–0.038	–0.029	–0.041
10 A, 300°	–0.028	–0.012	–0.02

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01550.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01550.

4.3 PCB Layout Recommendations

For this reference design, follow these general guidelines:

- Place decoupling capacitors close to their associated pins.
- Use ground planes instead of ground traces and minimize the cuts in the ground plane.
- Give each MSP430i2041 device its own set of ground planes. Each of these ground planes is actually referenced from a different line voltage because each MSP430i2041 device must be connected to a different line voltage.
- Be careful to avoid crosstalk on a phase from other phase voltages and the neutral.
- For the MSP432P4111, minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there must be clean ground underneath the crystal and placing any traces underneath the crystal must be avoided. Also, keep high frequency signals away from the crystal.
- Use wide traces for power supply connections.
- Maintain at least an 8.1-mm spacing between the ground planes of the MSP430i2041 device and the MSP432P4111 ground planes. This spacing maintains the recommended clearance for the ISO7731 isolation rating. In addition, ensure that the recommended clearance and creepage spacing for other isolation devices (such as the ISO7720 and ISO7721) is also followed.
- Keep the traces of the analog input pin symmetrical and as close as possible to each other.

4.4 CAD Project

To download the CAD project files, see the design files at TIDA-01550.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01550.

5 Software Files

To download the software files, see the design files at TIDA-01550.

6 Related Documentation

1. Texas Instruments, *TIDA-00163 Self-Powered Isolated RS-232 to UART Interface Reference Design*

6.1 商标

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7 About the Author

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修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (December 2017) to A Revision **Page**

- 已更改 isolation rating of DBQ package from 2500 V_{RMS} to 3000 V_{RMS} 7
- 已更改 limit of galvanic isolation from 2.5 kV_{RMS} to 3.0 kV_{RMS} 9

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