TI Designs：TIDA-01346
适用于抖动小于 40fs（100Hz 至 100MHz）的多个 PLL 组合参考设计

说明

TIDA-01346 设计结合使用两个 LMX2594 合成器，与使用一个合成器相比，产生的噪声和抖动更低。通过结合相位中两个合成器的输出，理论上可以实现 3dB 相位噪声优势，这是因为输出功率高出 6dB，而噪声功率仅高出 3dB。而 LMX2594 具有 SYNC 功能和可编程相位，因此，这款合成器非常适合这一应用。这样可确保两个合成器在加电周期间保持一致相位关系，同时能够精细去除本设计中任何可重复相位误差。

资源

TIDA-01346	设计文件夹
PLLATINUMSIM-SW	PLLatinum 仿真器软件
TICSPRO-SW	TICSPro 软件

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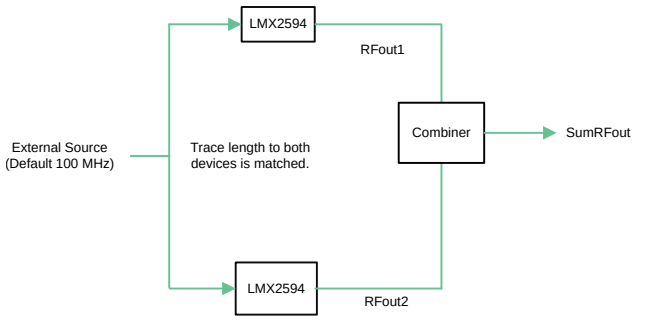
特性

- 输入时钟频率介于 5MHz 至 1400MHz 之间
- 输出频率范围为 1.8MHz 至 12.5GHz
- 抖动低于 40fs

应用

- 无线通信测试仪
- 半导体测试仪
- 信号发生器
- 函数/任意波形发生器
- 示波器
- 频谱分析仪
- 矢量信号分析仪
- 网络分析器
- 雷达
- 军需品和目标应用



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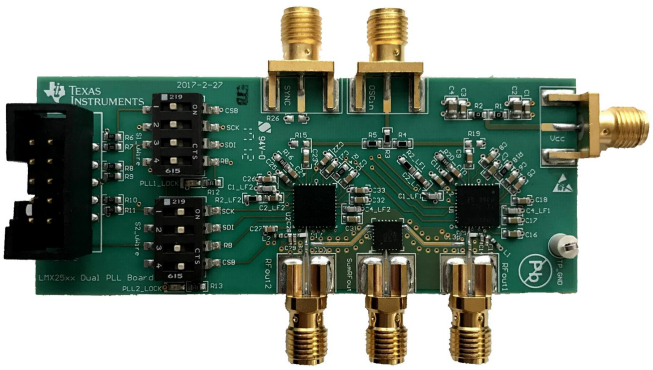

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1 System Description

The TIDA-01346 design uses two LMX2594 synthesizers in combination to produce lower noise than is possible with just one. By combining the output of two synthesizers that are in phase, a theoretical 3-dB phase noise benefit is possible due to the output power being 6-dB higher while the noise power is only 3-dB higher. The LMX2594 is an ideal synthesizer for this application because it has a SYNC feature that allows it to have deterministic and repeatable phase as well as a programmable phase that can be used to correct for any phase error due to trace mismatches or any other factors. The design demonstrates this concept with only two synthesizers, but it can be expanded to use more synthesizers for an even greater benefit.

A low-noise reference is sent through the OSCin pin which is sent to both LMX2594 synthesizers. The outputs of these devices is then with a Mini-Circuits EP2C+ combiner for the final output. The footprints of C13 and C13p should have the capacitor in the C30p footprint, likewise for the C30 and C30p capacitor shared footprint. If the user switches the footprints the other way, this configuration can be used as the SYNC reference design (TIDA-01410). A SYNC connector is included, which necessary where the SYNC is timing critical (as described in the datasheet).

Test equipment often needs an internal signal source to clock data converters, downconvert the input signal, or go generate an output signal. In the case where the signal source is used to clock a data converter, the jitter of the clock can limit the bit resolution, especially at higher clock speeds. When downconverting signals, the noise of this signal source can limit the noise floor of the instrument, and when producing a signal, the noise of this source limits the noise quality of the output signal. In all three, cases, there is a need to produce a clean signal for the test equipment. This therefore makes this reference design useful for wireless testers, semiconductor testers, signal generators, spectrum analyzers, vector signal analyzers, network analyzers, oscilloscopes and function/ arbitrary waveform generators.

There is a very broad class of other applications that can benefit from better phase noise as well. For instance, good close-in phase noise translates to better ability to discern objects that are closer together, which is applicable to RADAR and munitions and targeting.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	VALUE	COMMENTS
Input frequency range	5 MHz to 1400 MHz	100-MHz Wenzel oscillator recommended
Output frequency range	1.8 GHz to 12.5 GHz	9 GHz typical System output frequency range is limited by the combiner: LMX2594 frequency range: 10 MHz to 15 GHz Combiner frequency range: 1.8 to 12.5 GHz
Input voltage range	3.15 V to 3.45 V	3.3 V typical
Jitter	40 fs typical	—

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表 **2. Loop Filter Specifications**

PARAMETER	VALUE	COMMENTS
VCO frequency	7.5 GHz to 15 GHz	The loop filter is optimized for the highest charge pump gain and a 200-MHz phase detector frequency. If the phase detector or charge pump gain is changed significantly, then the loop filter remains stable; however, in an ideal situation the loop filter should be redesigned for optimal performance
Phase detector frequency	200 MHz	
Charge pump gain	15 mA	
Loop bandwidth	250 kHz	
C1_LF	0.39 nF	
C2_LF	68 nF	
C3_LF	1.8 nF	
R2_LF	68 Ω	
R3_LF	18 Ω	

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2 System Overview

2.1 Block Diagram

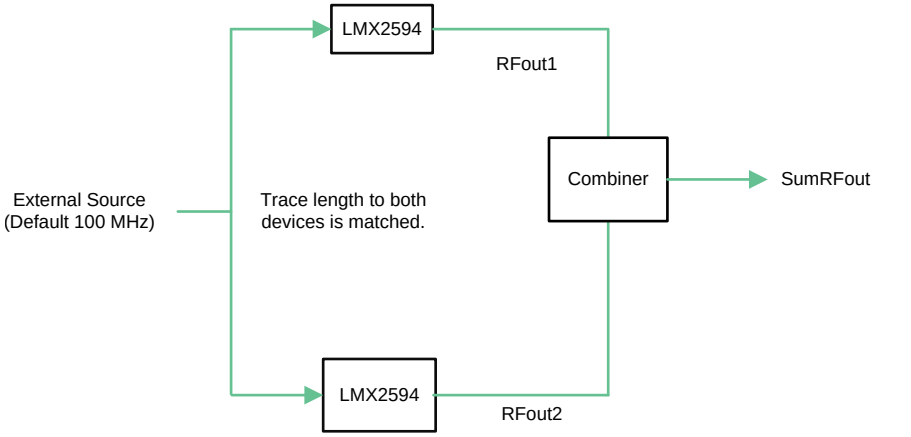

图 **1. Block Diagram**

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2.2 System Design Theory

The TIDA-01346 consists of two LMX2594 devices in a parallel combination. The key concept is that the signal theoretically adds by 6 dB, while the phase noise only adds 3 dB.

Even if the two signals are not perfectly in phase the majority of the phase noise benefit is realized. To illustrate this concept, consider two signals of the same amplitude and frequency but with a phase error of θ. In this case, the designer can determine that the output power is increased by a factor of: $10\times\log[\ 2 + 2\times\cos(\theta)\ ]$. The maximum power is attained when θ is zero degrees; however, even if θ is off by a small value, the increase in output power is still close to the maximum benefit.

As 图 2 shows, a phase error of 30º still reaches within 0.3 dB of the ideal phase noise benefit. The combiner may have losses, but these apply to the noise as well as the intended signal, so they do not impact the phase noise. As the jitter is proportional to the square root of the phase noise, this implies that the combination of the two synthesizers reduces the jitter by a factor of $1/\sqrt{2}$, which corresponds to an approximate 30% reduction.

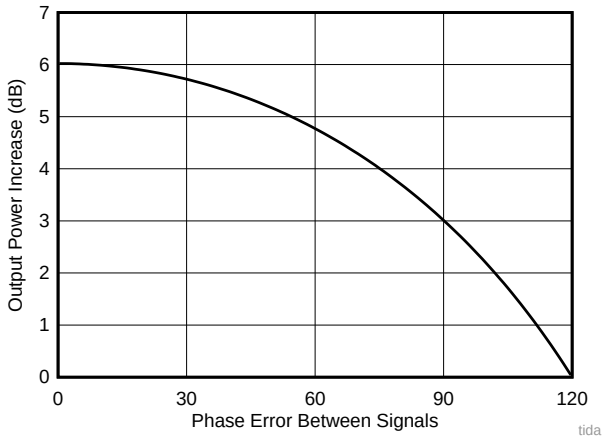

图 2. Theoretical Power Increase by Combining Two Signals

2.3 Design Considerations

Imperfections in board layout, component placement, and components themselves can introduce phase error at the combiner input. This phase error does not have much impact unless it is larger than approximately 30º. At higher frequencies, the MASH_SEED programmable field can be used to optimize the output power and jitter to correct for this phase error. Note that MASH_SEED for the test results in this document.

This design is based on the assumption that the designer is using a very clean input reference. If the noise of the reference is not clean enough, this noise dominates inside the loop bandwidth of the PLL and the full benefit cannot be realized

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2.4 Highlighted Products

2.4.1 LMX2594

The LMX2594 is a high-performance, wideband PLL with integrated VCOs that can generate any frequency from 10 MHz to 15 GHz without using an internal doubler, thus eliminating the need for sub-harmonic filters. The high-performance PLL with figure of merit of –236 dBc/Hz and high phase detector frequency can attain very low in-band noise and integrated jitter. The high-speed N-divider has no pre-divider, thus significantly reducing the amplitude and number of spurs. A programmable input multiplier is also available to mitigate integer boundary spurs. The LMX2594 allows users to synchronize the output of multiple devices and also enables applications that require deterministic delay between input and output. A frequency ramp generator can synthesize up to two segments of ramp in an automatic ramp generation option or a manual option for maximum flexibility. The fast calibration algorithm allows changing frequencies faster than 20 μs. The LMX2594 adds support for generating or repeating SYSREF (compliant to JESD204B standard) making it an ideal low-noise clock source for high-speed data converters. Fine delay adjustment (9-ps resolution) is provided in this configuration to account for delay differences of board traces. The output drivers within LMX2594 delivers output power as high as 7 dBm at a 15-GHz carrier frequency. The device runs from a single 3.3-V supply and has integrated low dropout regulators (LDOs) that eliminate the requirement for onboard LDOs.

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3 Getting Started Hardware and Software

3.1 Hardware Setup

图 3 shows an outline of the hardware setup.

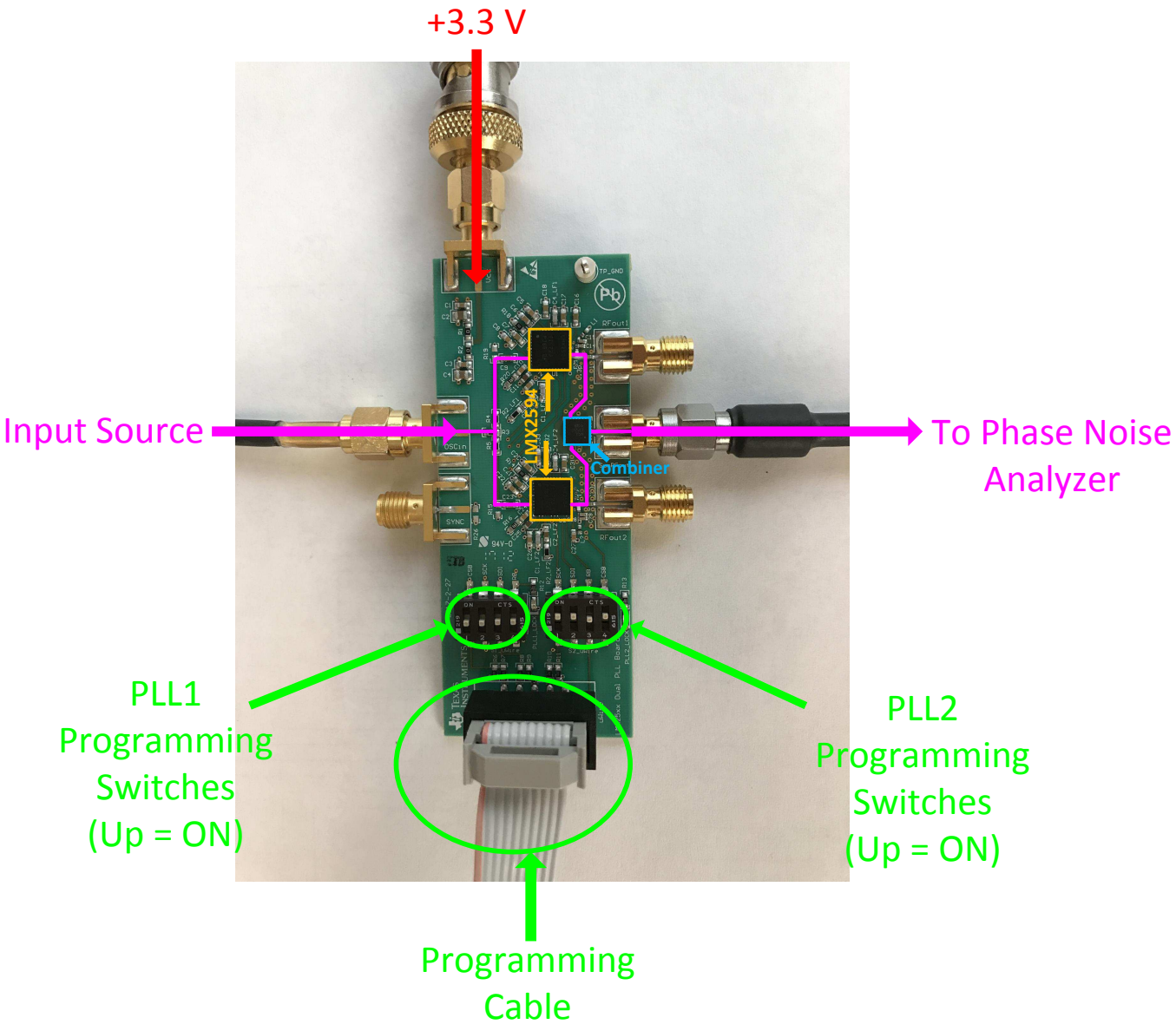

图 3. Hardware Setup

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3.1.1 Power

Set the power supply to 3.3 V and connect this to Vcc. Set the current limit to 1 A.

3.1.2 Input Signal

The input signal is critical and must be low noise, as this noise moves directly to the output. TI recommends the use of a 100-MHz Wenzel oscillator.

注: If using a noisy signal source, such as a signal generator, be aware that this can dominate close-in phase noise.

3.1.3 Output Signal

Connect SumRFout to a phase-noise analyzer. Ensure that C13p and C30p are in place (not C13 and C30).

3.1.4 Programming Interface

3.1.4.1 USB2ANY Interface

Connect the laptop to the board using the USB2ANY or ReferencePro interface. For more details, refer to the *LMX2594 EVM Instructions – 15-GHz Wideband Low Noise PLL With Integrated VCO* user's guide[1]. Note that the reference source from the ReferencePro board is not clean enough to power this reference design.

3.1.4.2 Programming Switches

This reference design has two banks of switches, one for each LMX2594 synthesizer. Each set of switches has four switches for CSB, SCK, SDA, and MUXout and all four switches in the set should be either ON or OFF altogether. If both sets of switches are ON, then both devices are programmed to the same setting. However, if the designer wants to program the synthesizers to different settings, as would be the case when using MASH_SEED, then the switches on one of the devices can be turned OFF so that the other device is not programmed. With this set of instructions using switches, a single programming interface can be used to program both devices.

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3.2 Software

3.2.1 Download Texas Instruments Clock and Synthesizers (TICS) Pro Software

1. Download the TICS Pro software from TI.com: http://www.ti.com/tool/TICSPRO-SW.
2. To start the software, open the *TICS PRO.exe* from the installed directory. 图 4 shows the user interface.

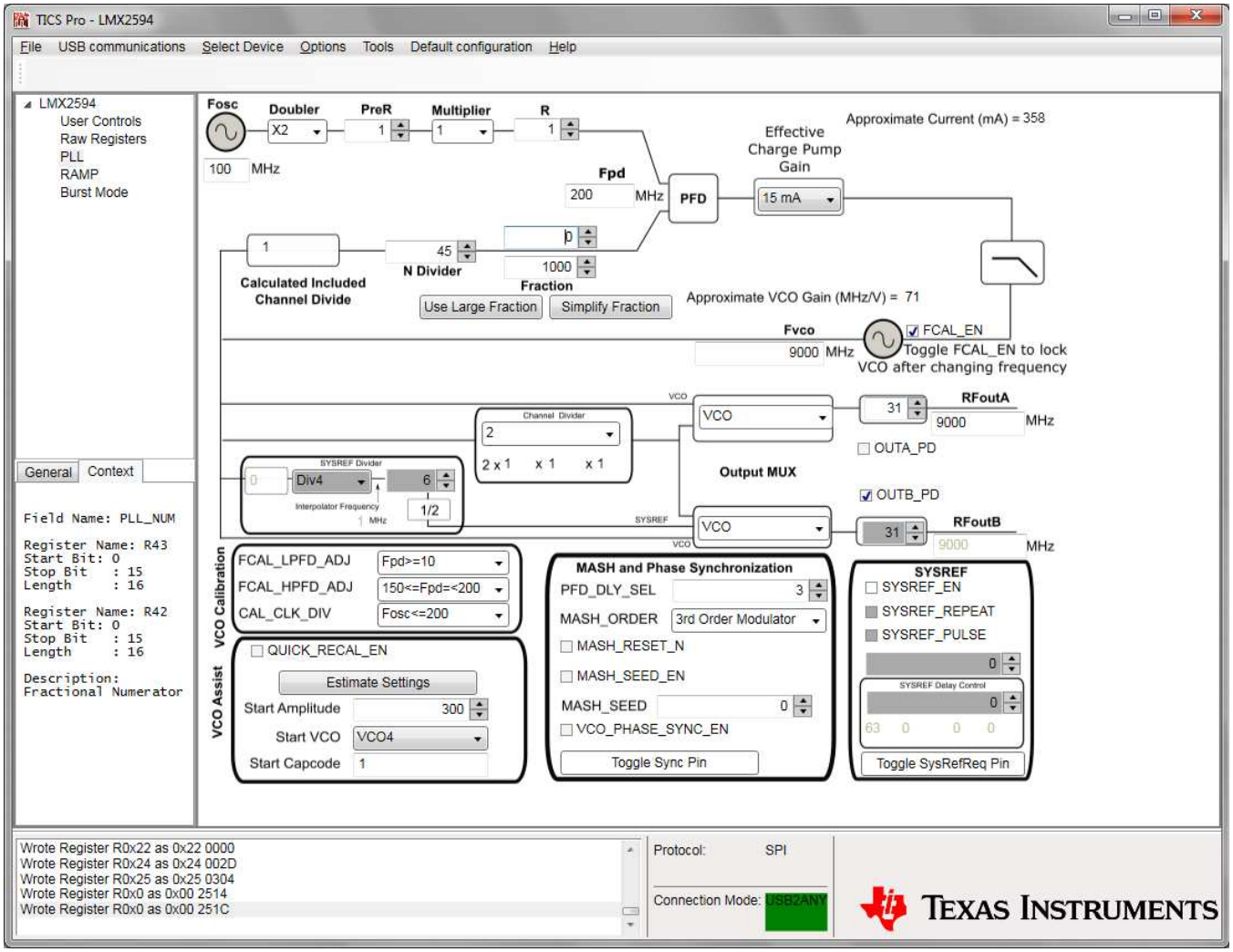

图 4. TICSPro Software Setup

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4 Testing and Results

4.1 Test Setup

The following test setup that 图 5 shows was used to create the measurements for the test data.

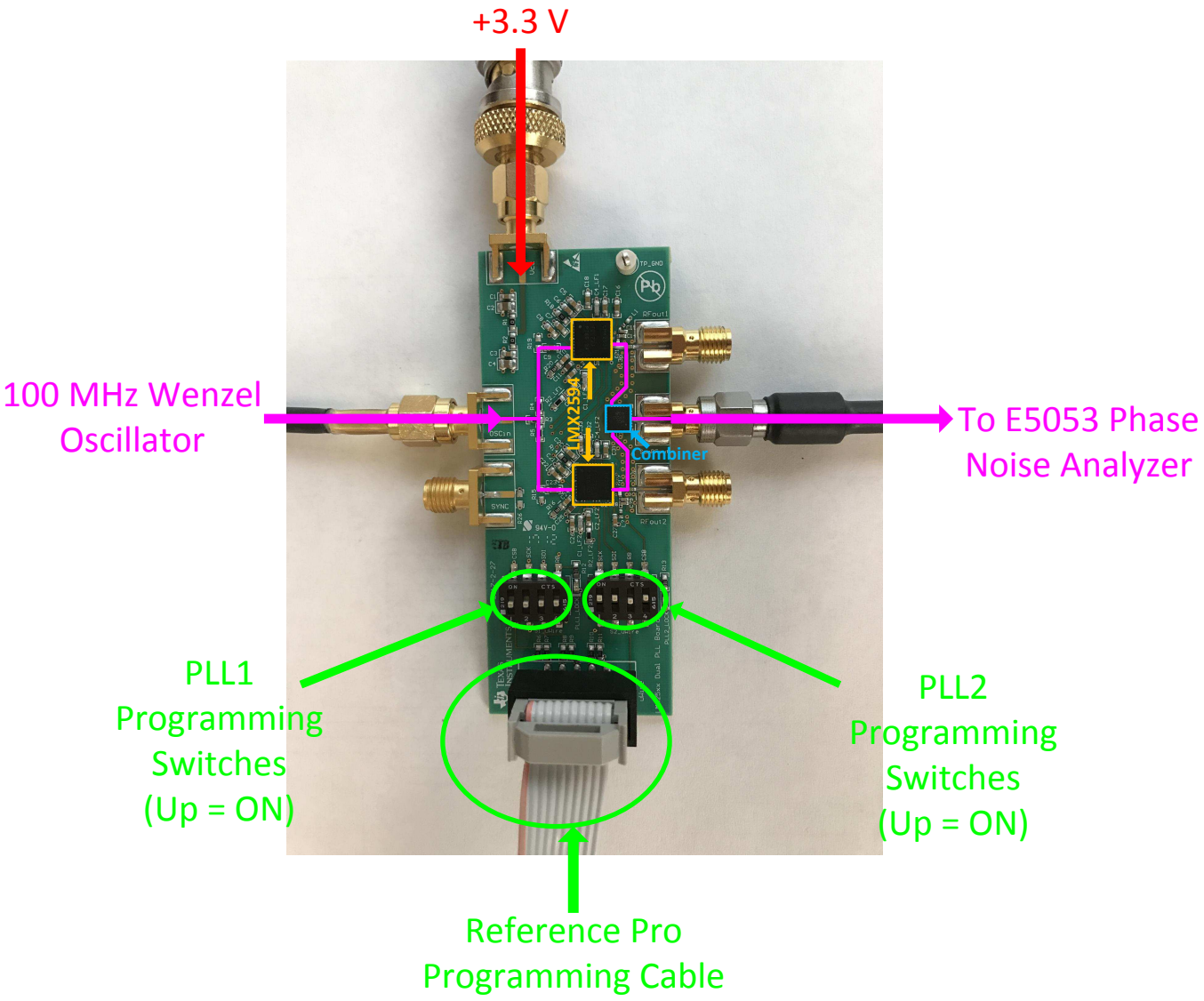

图 5. Test Setup

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4.2 Test Data

Test results were taken using the E5053 phase-noise analyzer. Measuring the phase noise of a single synthesizer required powering down the other synthesizer, but no adjustments were made to the hardware.

4.2.1 Results at 9 GHz

表 3. Reference Design Results at 9 GHz

OFFSET FREQUENCY	COMBINED RESULT	PLL 1 RESULT	PLL2 RESULT
100 Hz	– 90.8 dBc/Hz	– 88.6 dBc/Hz	– 88.0 dBc/Hz
1 kHz	–100.8 dBc/Hz	–98.3 dBc/Hz	–98.1 dBc/Hz
10 kHz	–110.6 dBc/Hz	–107.7 dBc/Hz	–108.2 dBc/Hz
100 kHz	–112.9 dBc/Hz	–110.4 dBc/Hz	–111.0 dBc/Hz
1 MHz	–127.1 dBc/Hz	–123.6 dBc/Hz	–123.0 dBc/Hz
10 MHz	–150.5 dBc/Hz	–147.5 dBc/Hz	–147.3 dBc/Hz
90 MHz	–158.3 dBc/Hz	–156.9 dBc/Hz	–156.9 dBc/Hz
Jitter (100Hz to 100 MHz)	38.3 fs	53.5 fs	53.5 fs

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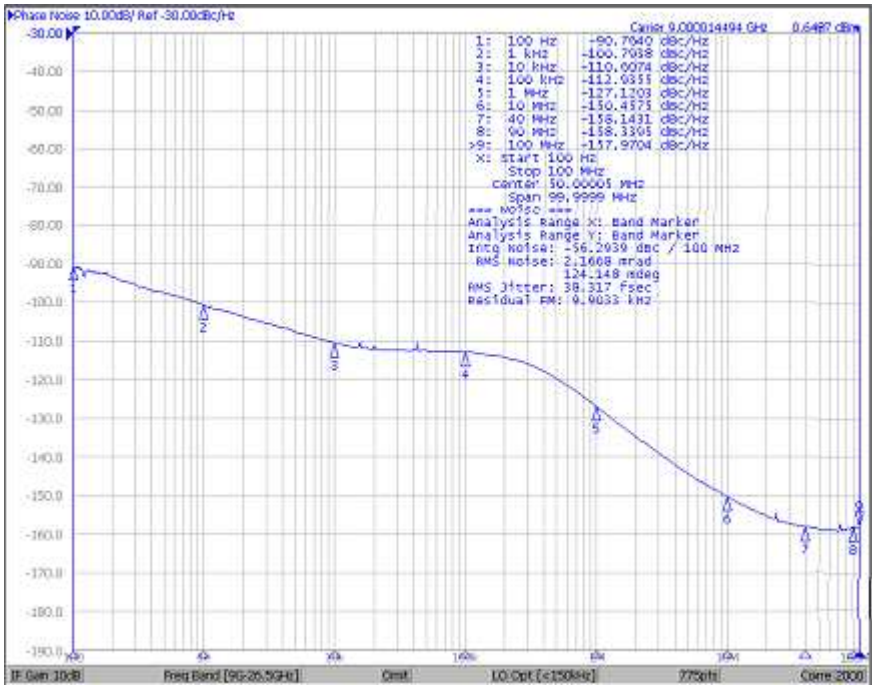

图 6. Combination Board Results at 9 GHz

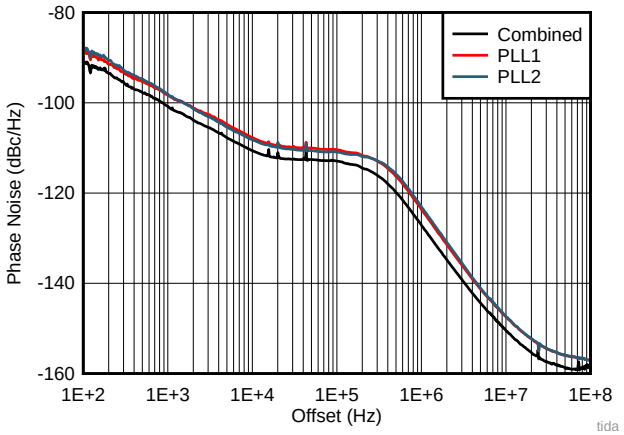

图 7. Phase Noise of Combined and Individual PLLs

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01346.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01346.

5.3 PCB Layout Recommendations

图 8 shows the layer stackup information for the TIDA-01346 design.

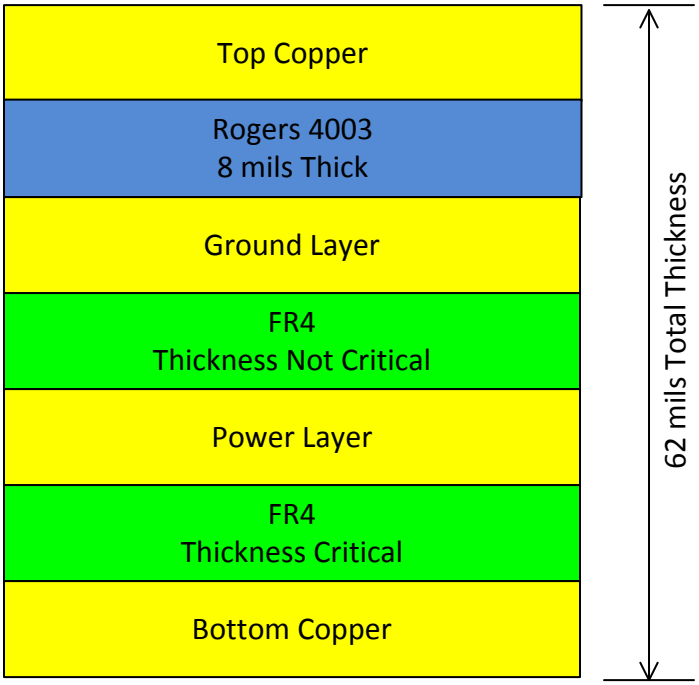

图 8. TIDA-01346 Layer Stackup Information

Rogers 4003 was chosen for high-frequency performance.

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01346.

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5.3.2 Layout Guidelines

The following guidelines list the ideal layout:

- Place capacitors close to the pins.
- Ensure that the input signal trace is well-matched.
- For the routing of the outputs, single-ended is chosen so that trace lengths can be kept short and equal length. Pullup components should be as close to the pin as possible. The unused side was sent to the back side of the board through a via with the loading symmetrical to the used side.

图 9 shows an example layout of the LMX2594 board.

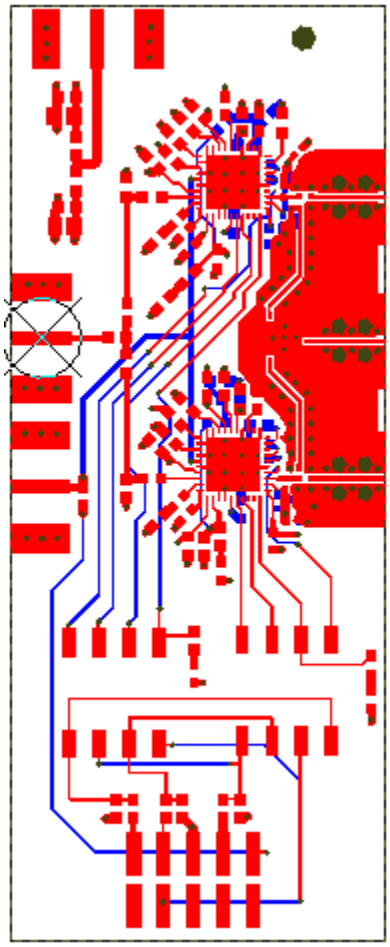

图 **9. LMX2594 Layout Example**

For more information, refer to the LMX2594 datasheet (SNAS696).

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01346.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01346.

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5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01346.

6 Software Files

To download the software files, see the design files at TIDA-01346.

7 Related Documentation

1. Texas Instrument, *LMX2594 EVM Instructions – 15-GHz Wideband Low Noise PLL With Integrated VCO*, LMX2594 User's Guide (SNAU210)
2. Texas Instruments, *LMX2594 15 GHz Wideband PLLatinum™ RF Synthesizer With Phase Synchronization and JESD204B Support*, LMX2594 Datasheet (SNAS696)
3. Texas Instruments, *LMX2594EVM High Performance, Wideband PLLatinum™ RF Synthesizer Evaluation Board Operating Instructions*, User's Guide (SNAU195)

7.1 商标

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8 About the Author

DEAN BANERJEE is an applications engineer with Texas Instruments working with PLL synthesizers and is the author of *PLL Performance, Simulation, and Design*.

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修订历史记录 A

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (April 2017) to A Revision	Page
• 已更改 from "noise theoretically adds by 6 dB" to "signal theoretically adds by 6 dB"	5

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