TPS7B4250-Q1 低压降电压跟踪 LDO

1 特性

- 适用于汽车电子 应用
- 符合 AEC-Q100 标准的下列结果
  - 器件温度等级 1：环境运行温度范围为 -40°C 至 125°C
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 3A
  - 器件带电器件模型 (CDM） ESD 分类等级 C6
- -20V 至 45V 宽范围、最大输入电压范围
- 输出电流，50mA
- 极低输出跟踪容限，5mV（最大值）
- 当 I_{OUT} = 10mA 时，低压降电压为 150mV
- 组合基准和使能输入
- 轻负载时，40µA 的低静态电流
- 极端、宽 ESD 范围。
  - 与 1µF 至 50µF 陶瓷输出电容器，1mΩ 至 20Ω 等效串联电阻 (ESR) 一同使用时保持稳定
- 反极性保护
- 过热保护
- 对接地和电源的输出短路保护
- SOT-23 封装

2 应用

- 电路板外传感器电源
- 高精度电压跟踪

3 说明

TPS7B4250-Q1 器件是一款单片、集成型低压降跟踪器。此器件采用 SOT-23 封装。TPS7B4250-Q1 器件被设计用来为汽车环境中的电路板外传感器供电。此集成电路 (IC) 具有针对过载、过热、反向极性和电池与接地输出短路的集成保护功能。

调节输入引脚 ADJ 上施加的基准电压用于对高达 V_{IN} = 45V 的电源电压进行稳压，负载电流高达 50mA。

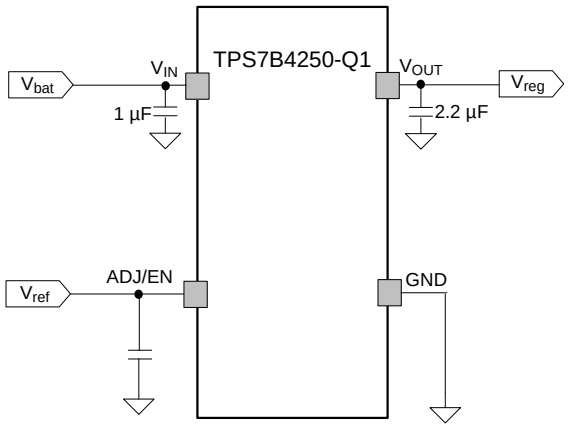
通过将调节/使能输入引脚 (ADJ/EN) 置为低电平，TPS7B4250-Q1 器件可切换至待机模式，从而最大限度地降低静态电流。

器件信息(1)

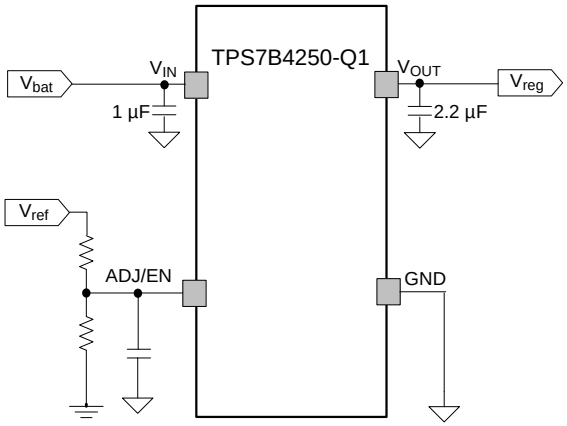
器件型号	封装	封装尺寸（标称值）
TPS7B4250-Q1	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

输出等于基准电压



输出低于基准电压



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

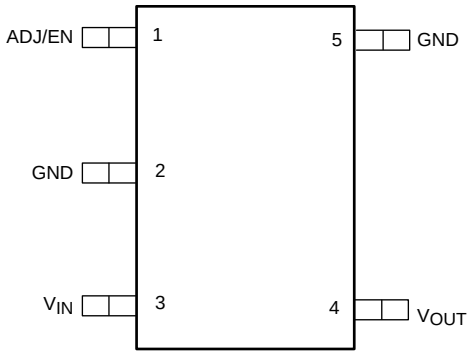
Changes from Revision A (November 2013) to Revision B **Page**

- 已更改 HBM ESD 分类等级，从 2 改为 3A ... 1
- 已更改 CDM ESD 分类等级，从 C4 改为 C6 ... 1
- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Deleted the transient current and 107-pF capacitor for HBM table notes from the *ESD Ratings* table ... 5
- Changed input voltage symbol from V_{IN} to V_I for the $\Delta V_{O(\Delta VI)}$ and $V_{dropout}$ parameters and the output voltage symbol from V_{OUT} to V_O for the I_L parameter in the Electrical Characteristics table ... 6
- Added I_O and C_O to the PSRR test condition in the *Electrical Characteristics* table ... 6
- Changed the max value for $V_{dropout}$ where I_O = 10 mA from 250 to 265 in the *Electrical Characteristics* table ... 6
- Deleted the V_{ADJ} = 5 V condition for the *Ground current vs Temperature* graph and changed the legend ... 7
- Changed the y axis units from mV to mA in the *Current-limit vs Temperature* graph ... 7
- Added the V_{ADJ} condition statement to the *Input Voltage vs Output Voltage* graph and changed the y-axis from I_O to V_O ... 7
- Changed the title of Figure 8 from *Input Voltage vs Output Voltage* to *Reference Voltage vs Output Voltage*, and changed the y-axis from I_O to V_O. Also added the V_I condition statement to the graph ... 7
- Changed the second y axis from I_O to V_I and removed the units in the *Line Transient* ... 7
- Deleted the units from the second y axis in the *Load Transient* ... 7
- Added the V_{ADJ} condition statement to the *Power-supply Rejection Ratio vs Frequency* graph ... 8
- Added resistor-divider values to the *Tracking LDO With Enable Circuit* figure ... 11

Changes from Original (October 2013) to Revision A **Page**

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADJ/EN	1	I	This pin connects to the reference voltage. A low signal disables the IC and a high signal enables the IC. Connected the voltage reference directly or with a voltage divider for lower output voltages. To compensate for line influences, TI recommends to place a capacitor close to the IC pins.
GND	2	G	Internally connected to pin 5
	5		Internally connected to pin 2
V_{IN}	3	I	This pin is the IC supply. To compensate for line influences, TI recommends to place a capacitor close to the IC pins.
V_{OUT}	4	O	V_{OUT} is an external capacitor that is required between V_{OUT} and GND with respect to the capacitance and ESR requirements given in the *Recommended Operating Conditions*.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage, unregulated input, V_{IN}(2)(3)	–20	45	V
Output voltage, regulated output, V_{OUT}	–1	22	V
Adjust input and enable input voltage, ADJ/EN(2)(3)	–0.3	22	V
ADJ Voltage minus input voltage (ADJ–V_{IN}), V_{IN} > 0 V		7	V
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, GND.
(3) Absolute maximum voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Unregulated input	4	40	V
V_{OUT}	regulated output	1.5	18	V
ADJ/EN	Adjust input and enable input voltage	1.5	18	V
ADJ–V_{IN}	ADJ voltage minus input voltage		5	V
C_{OUT}	Output capacitor requirements(2)	1	50	µF
ESR_{COUT}	Output ESR requirements	0.001	20	Ω
T_J	Operating junction temperature	–40	150	°C

(1) Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.
(2) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.

6.4 Thermal Information

THERMAL METRIC(1)(2)		TPS7B4250-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The thermal data is based on the JEDEC standard high K profile, JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

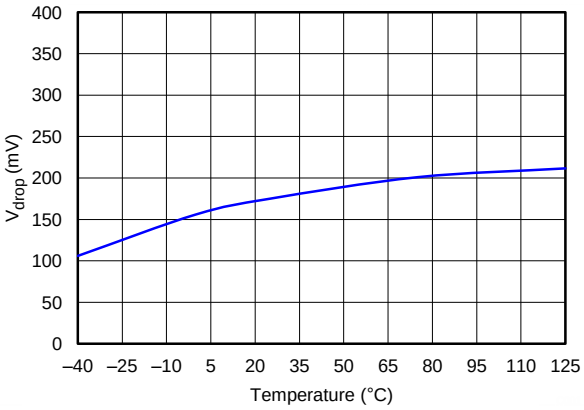
6.5 Electrical Characteristics

V_I = 13.5 V, 18 V ≥ $V_{ADJ/EN}$ ≥ 1.5 V, T_J = –40ºC to 150ºC unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	V_{IN} undervoltage detection	Ramp up V_I until the output turns on, V_{ADJ} = 1.5 V	3.65			V
		Ramp down V_I until the output turns off, V_{ADJ} = 1.5 V			3	
ΔV_O	Output-voltage tracking accuracy	I_O = 100 µA to 1 mA, V_I = 4 V to 40 V, 1.5 V < V_{ADJ} < V_I – 0.3 V	–4		4	mV
		I_O = 1 mA to 50 mA, V_I = 4 V to 40 V, 1.5 V < V_{ADJ} < V_I – 1.5 V	–5		5	
$\Delta V_{O(\Delta IL)}$	Load regulation steady-state	I_O = 1 mA to 30 mA			4	mV
$\Delta V_{O(\Delta VI)}$	Line regulation steady-state	I_O = 10 mA, V_I = 6 V to 40 V			3	mV
PSRR	Power-supply ripple rejection	Frequency = 100 Hz, V_{rip} = 0.5 V_{PP}, I_O = 5 mA, C_O = 2.2 µF		60		dB
$V_{dropout}$	Dropout voltage, $V_{dropout} = V_I - V_Q$	I_O = 10 mA, V_I ≥ 4 V (1)		150	265	mV
		I_O = 50 mA, V_I ≥ 4 V (1)		550	1000	
I_L	Output-current limitation	V_O short to GND	100		500	mA
I_R	Reverse current at V_{IN}	V_I = 0 V, V_O = 20 V, V_{ADJ} = 5 V	–5		0	µA
I_{RN1}	Reverse current at negative input voltage	V_I = –20 V, V_O = 0 V, V_{ADJ} = 5 V	–5		0	µA
I_{RN2}		V_I = –20 V, V_O = 20 V, V_{ADJ} = 5 V	–5		0	
T_{SD}	Thermal shutdown temperature	T_J increasing because of power dissipation generated by the IC		175		°C
I_Q	Current consumption	V_{ADJ} < 0.8 V, T_A ≤ 85°C (2)		7.5	15	µA
		V_{ADJ} < 0.8 V, T_A ≤ 125°C			20	
		I_O = 0.5 mA, V_{ADJ} = 5 V		40	90	
		I_O = 30 mA, V_{ADJ} = 5 V		150	350	
I_{ADJ}	Adjust-input and enable-input current	V_{ADJ} = 5 V			1	µA
$V_{ADJ,low}$	Adjust and enable low signal valid	V_O = 0 V			0.8	V
$V_{ADJ,high}$	Adjust and enable high signal valid	$\lvert V_O - V_{ADJ} \rvert$ < 5 mV	1.5		18	V

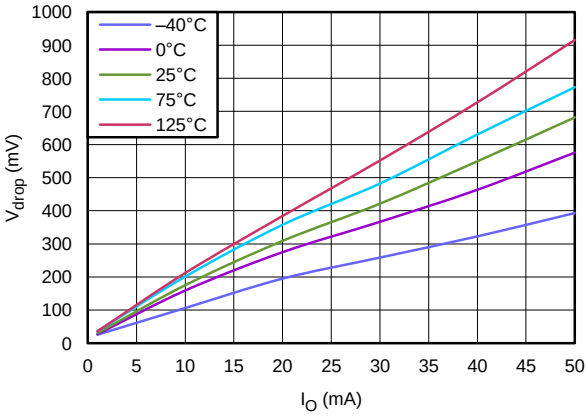
(1) Measured when the output voltage V_Q has dropped 10 mV from the typical value.
(2) Ensured by design.

6.6 Typical Characteristics



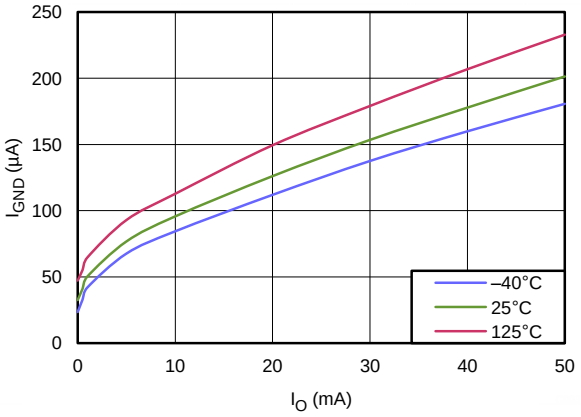
$V_I = V_{ADJ} = 4$ V $I_O = 10$ mA

Figure 1. Dropout Voltage vs Temperature



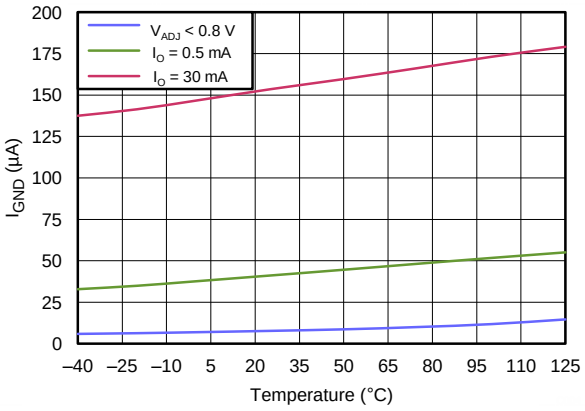
$V_I = V_{ADJ} = 4$ V

Figure 2. Dropout Voltage vs Output Current



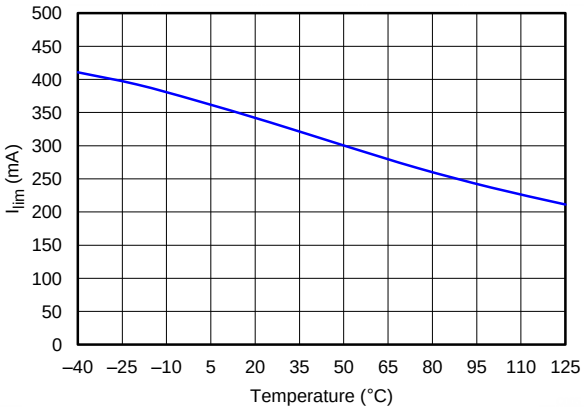
$V_I = 13.5$ V $V_{ADJ} = 5$ V

Figure 3. Ground Current vs Output Current



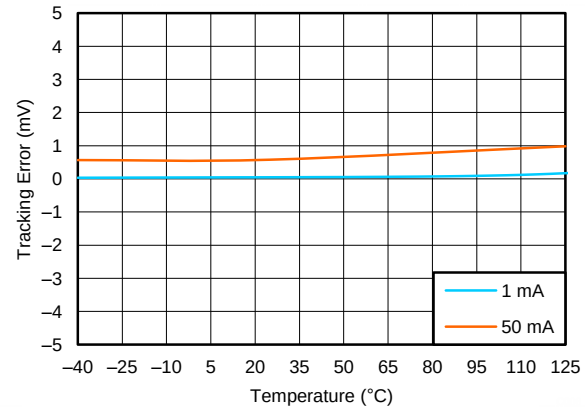
$V_I = 13.5$ V

Figure 4. Ground Current vs Temperature



$V_I = 13.5$ V $V_{ADJ} = 5$ V

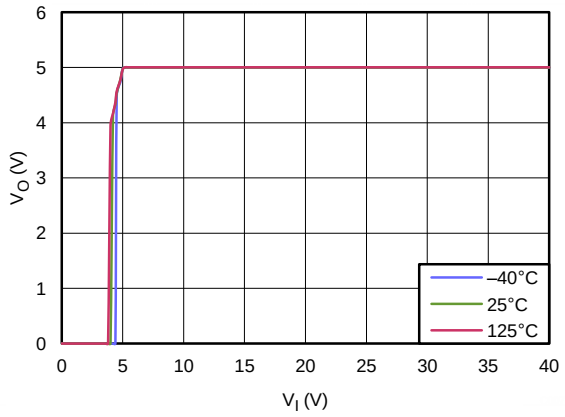
Figure 5. Current-limit vs Temperature



$V_I = 13.5$ V $V_{ADJ} = 5$ V $I_O = 1$ mA, 50 mA

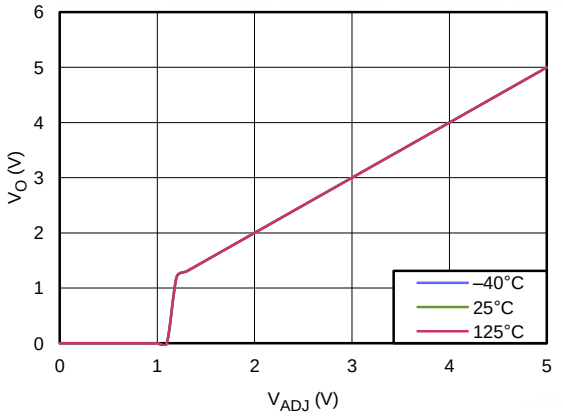
Figure 6. Tracking Error vs Temperature

Typical Characteristics (continued)



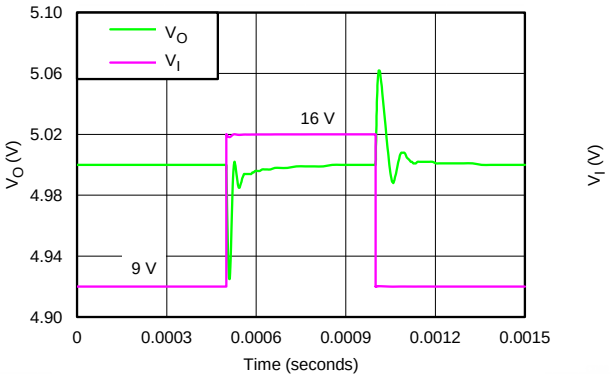
V_{ADJ} = 5 V

Figure 7. Input Voltage vs Output Voltage



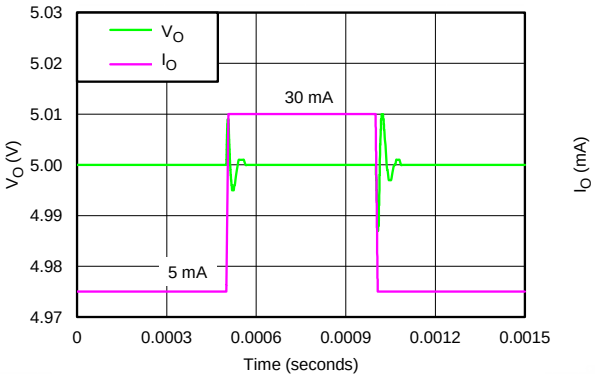
V_I = 13.5 V

Figure 8. Reference Voltage vs Output Voltage



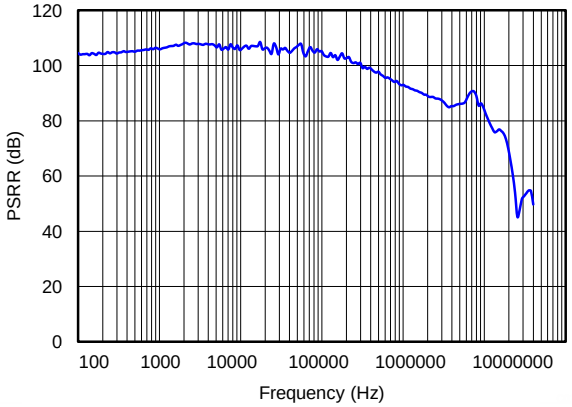
V_I = 9 to 16 V 2.2-µF ceramic output capacitor

Figure 9. Line Transient



I_O = 5 to 30 mA 2.2-µF ceramic output capacitor

Figure 10. Load Transient



V_I = 13.5 V C_O = 2.2 µF I_{LOAD} = 25 mA
V_{ADJ} = 5 V

Figure 11. Power-Supply Rejection Ratio vs Frequency

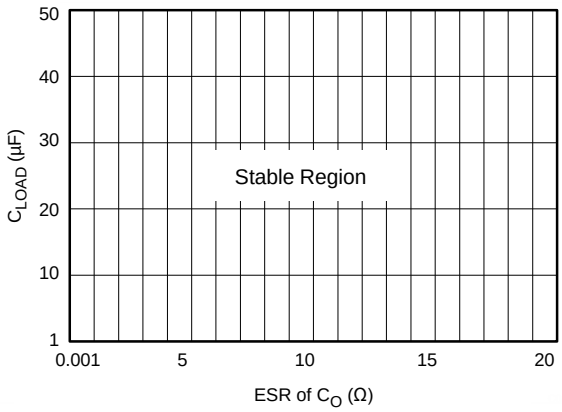


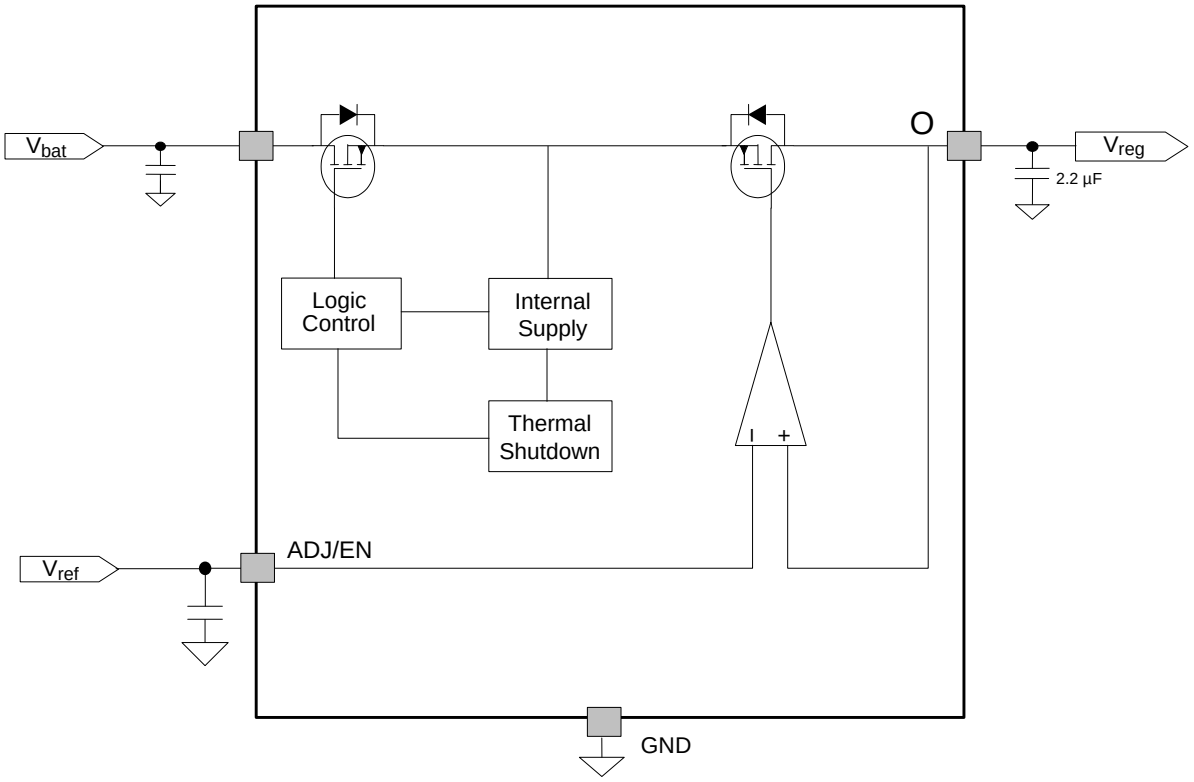
Figure 12. ESR Stability vs Load Capacitance

7 Detailed Description

7.1 Overview

The TPS7B4250-Q1 device is a monolithic integrated low-dropout voltage tracker with ultra-low tracking tolerance. Several types of protection circuits are also integrated in the device such as output current limitation, reverse polarity protection, and thermal shutdown in case of over temperature.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Regulated Output (V_{OUT})

V_{OUT} is the regulated output based on the reference voltage. The output has current limitation. During initial power up, the regulator has an incorporated soft start to control the initial current through the pass element.

7.3.2 Undervoltage Shutdown

The device has an internally-fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on V_{IN} drops below UVLO. This activation ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up similar to a standard power-up sequence when the input voltage is above the required levels.

Feature Description (continued)

7.3.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C which allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The internal protection circuitry of the TPS7B4250-Q1 device has been designed to protect against overload conditions. The circuitry was not intended to replace proper heat-sinking. Continuously running the TPS7B4250-Q1 device into thermal shutdown degrades device reliability.

7.3.4 V_{OUT} Short to Battery

The TPS7B4250-Q1 device survives a short to battery when the output is shorted to the battery as shown in Figure 13. No damage occurs to the device. A short to the battery can also occur when the device is powered by an isolated supply at a lower voltage as shown in Figure 14. In this case the TPS7B4250-Q1 supply input voltage is set at 7 V when a short to battery (14 V typical) occurs on V_{OUT} which typically runs at 5 V. The continuous reverse current flows out through V_{IN} is less than 5 µA.

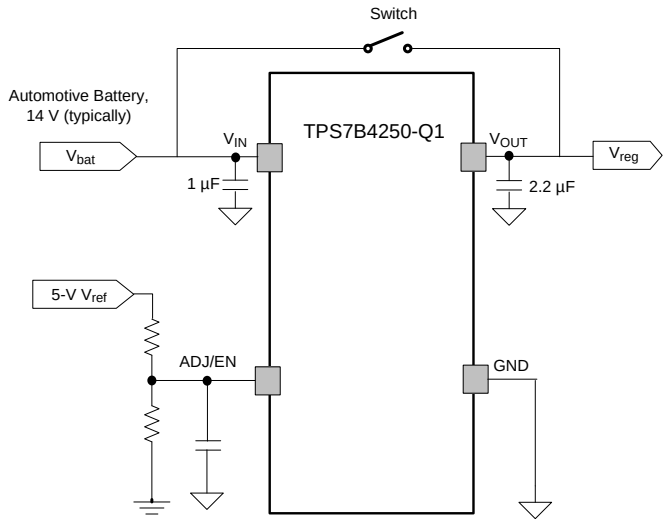


Figure 13. Output-Voltage Short to Battery

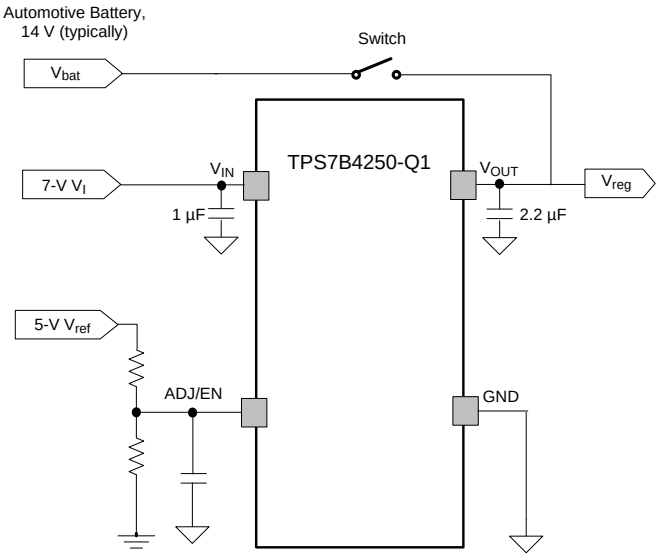


Figure 14. Output Voltage Higher than Input

7.3.5 Tracking Regulator with ENABLE Circuit

By pulling the reference voltage of the device below 0.8 V, the IC disables and enters a sleep state where the device draws 7.5 µA (typical) from the power supply. In a real application, the reference voltage is generally sourced from another LDO voltage rail. A case where the device must be disabled without a shutdown of the reference voltage can occur. In such case, the device can be configured as shown in Figure 15. The TPS7A6650-Q1 device is a 150-mA LDO with ultra-low quiescent current that is used as a reference voltage to the TPS7B4250-Q1 device and also as a power supply to the ADC. In a configuration as shown in Figure 15, the status of the device is controlled by an MCU I/O.

Feature Description (continued)

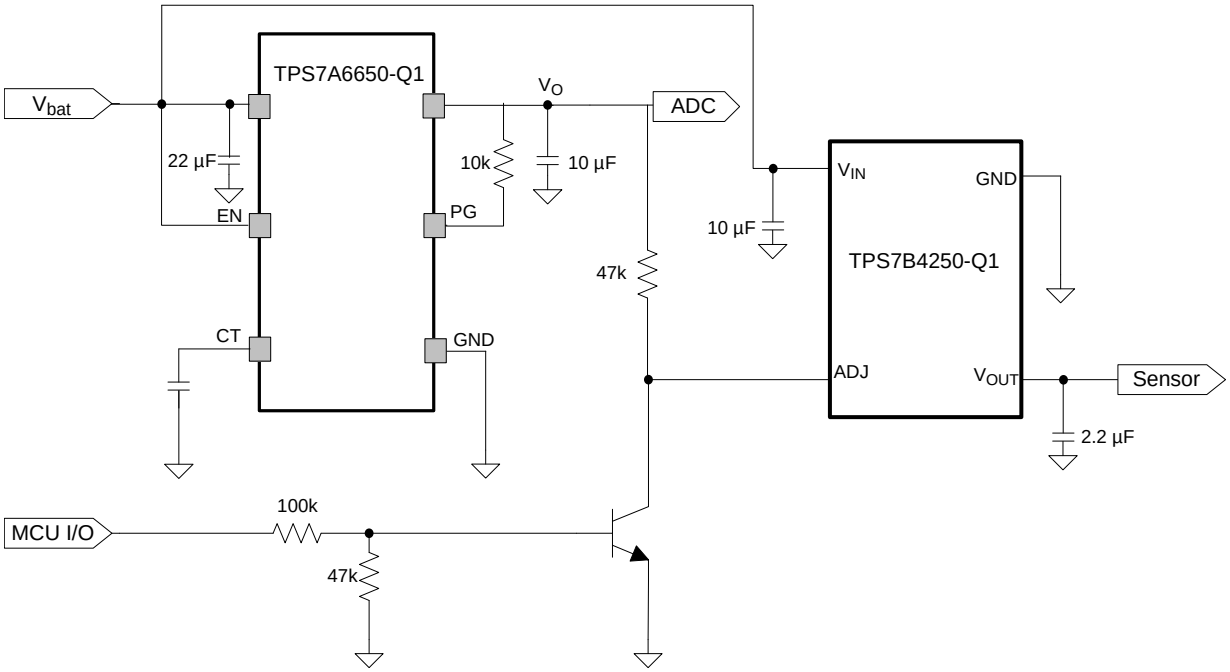


Figure 15. Tracking LDO With Enable Circuit

7.4 Device Functional Modes

7.4.1 Operation With V_I < 4 V

The device operates with input voltages above 4 V. The maximum UVLO voltage is 3 V and operates at input voltage above 4 V. The device can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With ADJ/EN Control

The rising-edge threshold voltage of the ADJ/EN pin is 1.5 V (maximum). When the EN pin is held above that voltage and the input voltage is above the 4 V, the device becomes active. The enable falling edge is 0.8 V (minimum). When the EN pin is held below that voltage the device is disabled, the IC quiescent current is reduced in this state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a reset from occurring. TI recommends a low ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

8.2 Typical Application

Figure 16 show typical application circuit for the TPS7B4250-Q1 device.

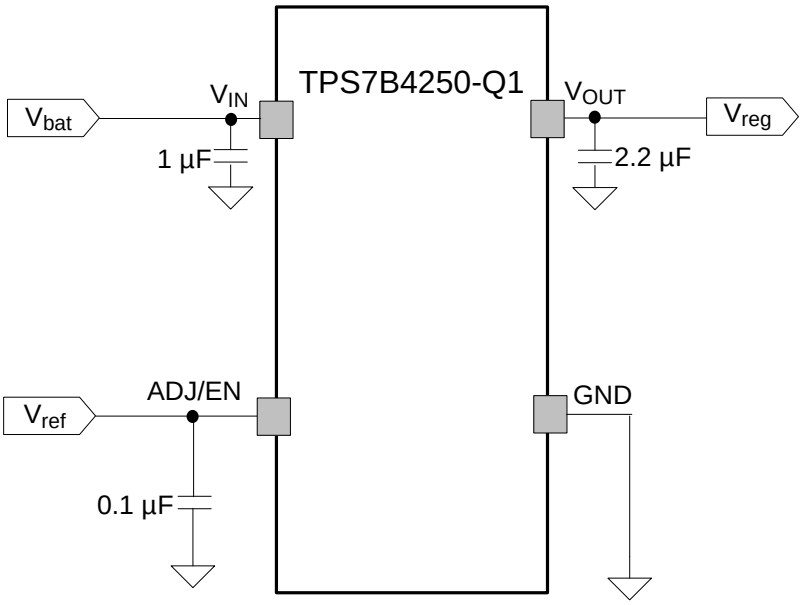


Figure 16. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage	4 to 40 V
ADJ reference voltage	1.5 to 18 V
Output voltage	1.5 to 18 V
Output current rating	50 mA
Output capacitor range	1 µF to 50 µF
Output capacitor ESR range	1 mΩ to 20 Ω

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Reference voltage
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor

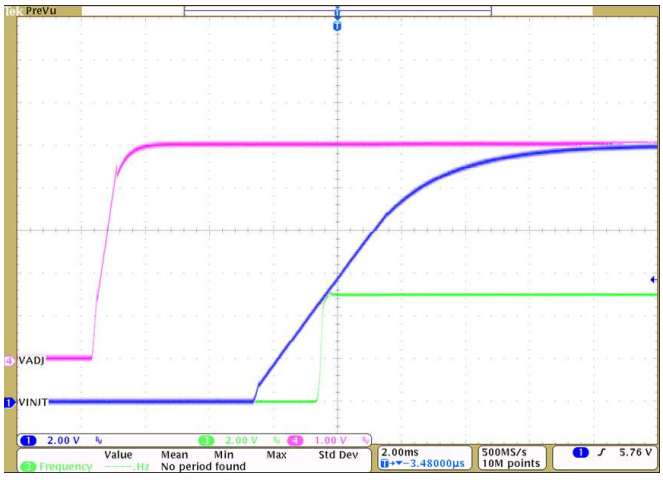
8.2.2.1 External Capacitors

An input capacitor, C_I, is recommended to buffer line influences. Connect the capacitors close to the IC pins.

The output capacitor for the TPS7B4250-Q1 device is required for stability. Without the output capacitor, the regulator oscillates. The actual size and type of the output capacitor can vary based on the application load and temperature range. The effective series resistance (ESR) of the capacitor is also a factor in the IC stability. The worst case is determined at the minimum ambient temperature and maximum load expected. To ensure stability of TPS7B4250-Q1 device, the device requires an output capacitor between 1 µF and 50 µF with an ESR range between 0.001 Ω and 20 Ω that can cover most types of capacitor ESR variation under the recommend operating conditions. As a result, the output capacitor selection is flexible.

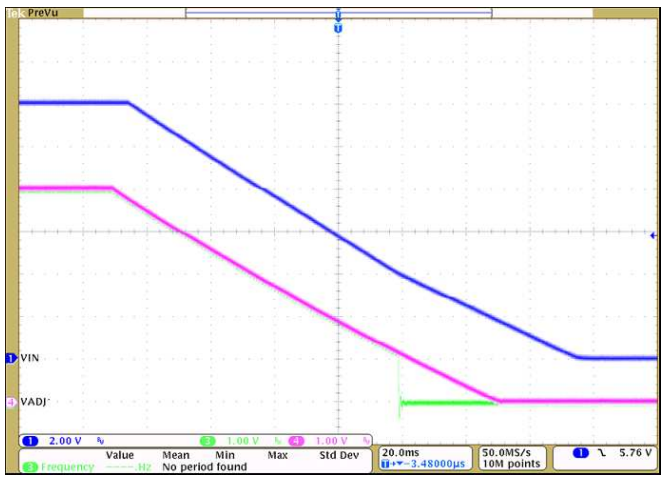
The capacitor must also be rated at all ambient temperature expected in the system. To maintain regulator stability down to –40°C, use a capacitor rated at that temperature.

8.2.3 Application Curves



V_I = 12 V V_{ADJ} = 5 V

Figure 17. Power Up



V_I = 12 V V_{ADJ} = 5 V

Figure 18. Power Down

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B4250-Q1 device, adding an electrolytic capacitor with a value of 10-µF and a ceramic bypass capacitor at the input is recommended.

10 Layout

10.1 Layout Guidelines

10.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4250-Q1 device are available in the *机械、封装和可订购信息* section and at www.ti.com.

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends to design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7B4250 evaluation board, available at www.ti.com.

10.2 Layout Example

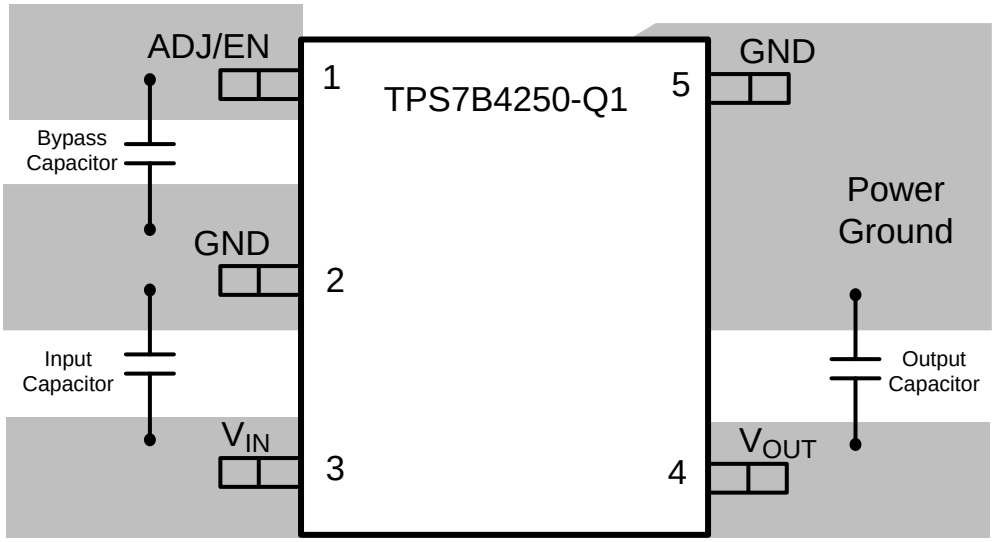


Figure 19. TPS7B4250-Q1 Layout Example

10.3 Power Dissipation and Thermal Considerations

Device power dissipation is calculated with Equation 1.

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I \quad (1)$$

where

- P_D = continuous power dissipation
- I_O = output current
- V_I = input voltage
- V_O = output voltage
- I_Q = quiescent current

As $I_Q \ll I_O$, the term $I_Q \times V_I$ in Equation 1 can be ignored.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) with Equation 2.

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (2)$$

where

- θ_{JA} = junction-to-junction-ambient air thermal impedance

A rise in junction temperature because of power dissipation can be calculated with Equation 3.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (3)$$

For a given maximum junction temperature (T_{JM}), the maximum ambient air temperature (T_{AM}) at which the device can operate can be calculated with Equation 4.

$$T_{AM} = T_{JM} - (\theta_{JA} \times P_D) \quad (4)$$

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档请参见以下部分：

《*TPS7B4250 评估模块*》，SLVU975

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B4250QDBVQ1	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7B4250QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	PA3Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

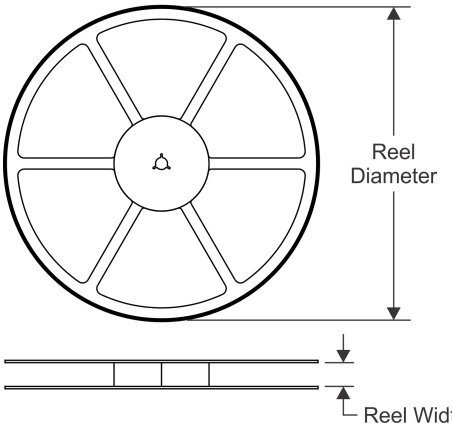
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

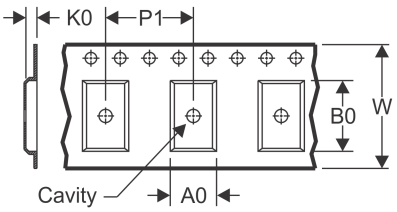
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

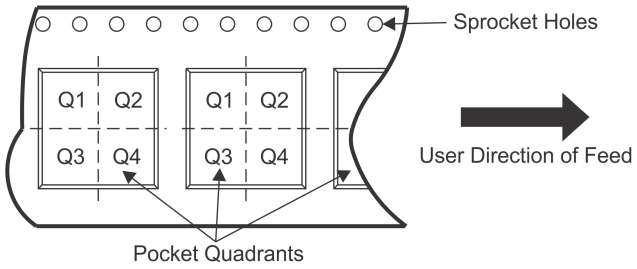


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

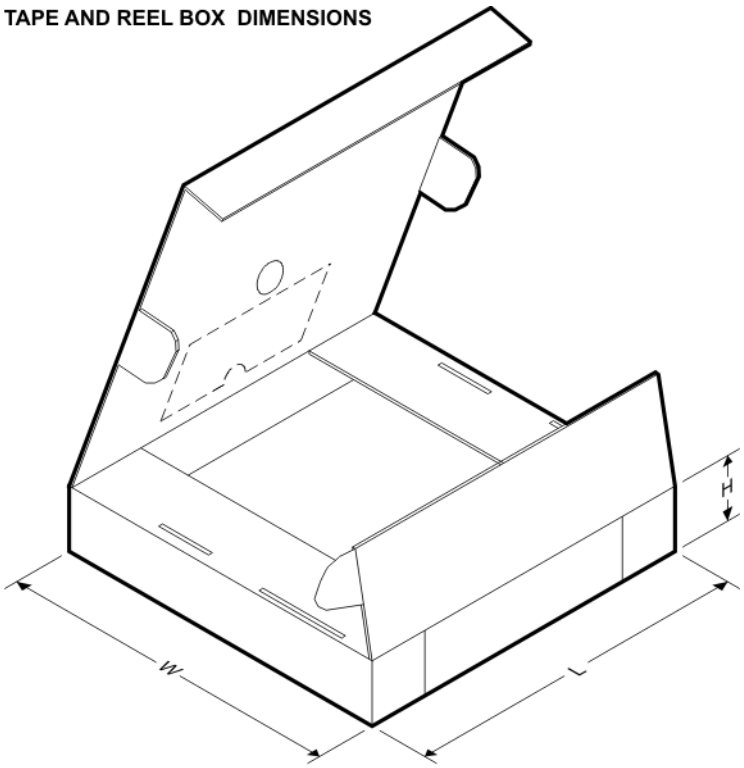
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B4250QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

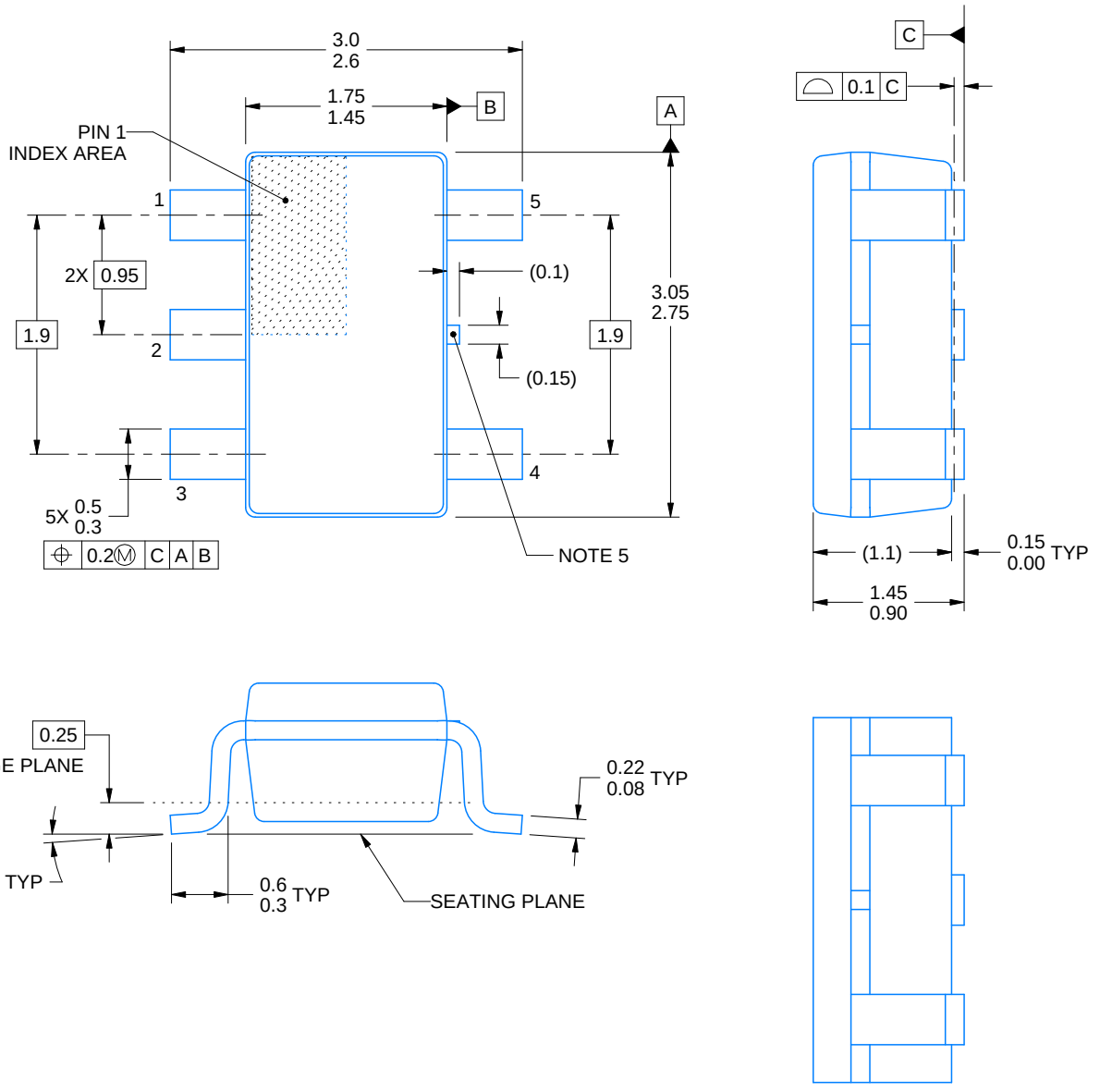
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B4250QDBVRQ1	SOT-23	DBV	5	3000	190.0	190.0	30.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

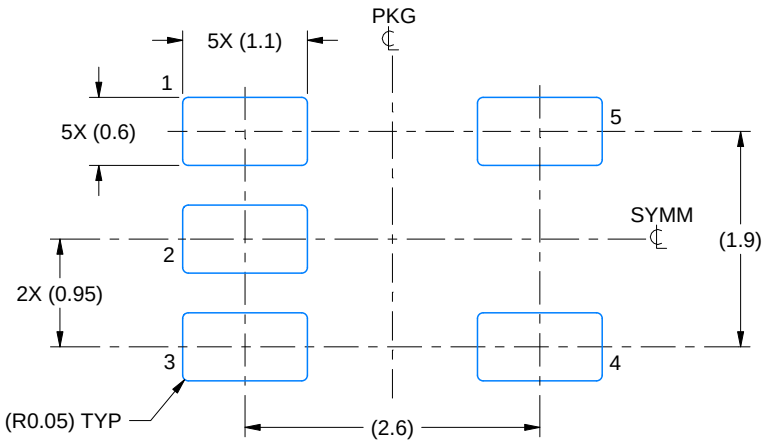


ALTERNATIVE PACKAGE SINGULATION VIEW

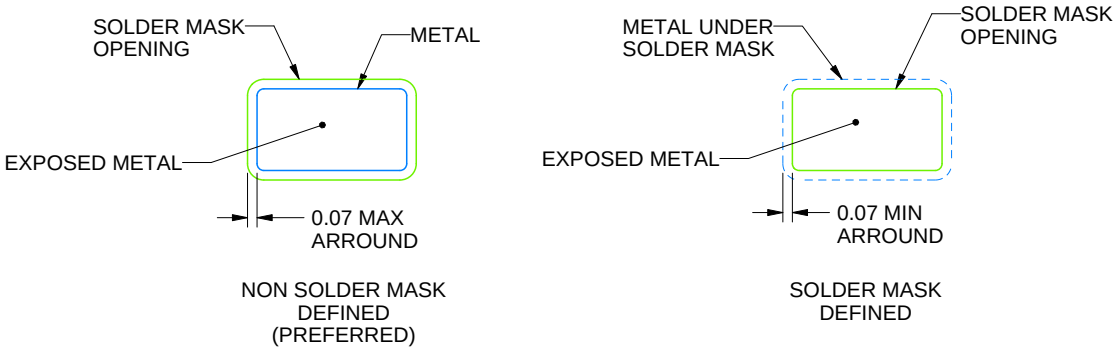
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

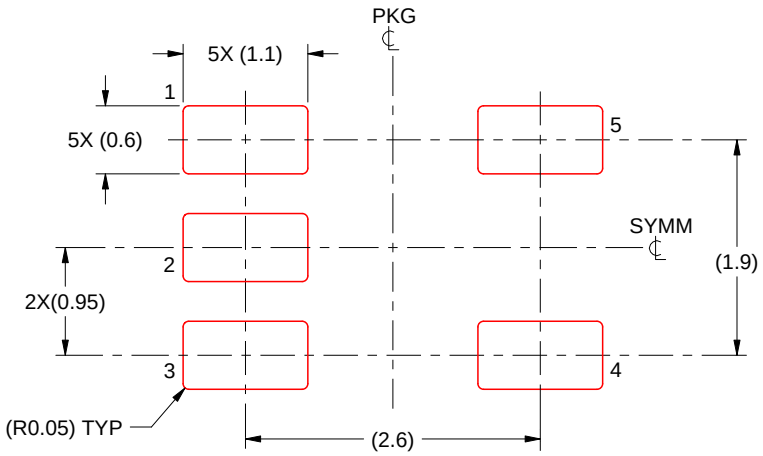


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265