TI Designs

Simple Open Real-Time Ethernet (SORTE) Device With PRU-ICSS Reference Design

Description

This TI Design implements a simple open real-time Ethernet (SORTE) device with the programmable real-time unit and industrial communication subsystem (PRU-ICSS). SORTE protocol enables customer applications to exchange process data between the master and devices in a 4-µs cycle time. The design contains open source PRU firmware to enable customers to differentiate their products.

The SORTE protocol includes device discovery, parametrization, PHY and cable delay measurement, synchronization, and process data exchange.

Resources

TIDEP0086	Design Folder
AM3359	Product Folder
TLK110	Product Folder
DP83822I	Product Folder
TMDSICE3359	Tools Folder

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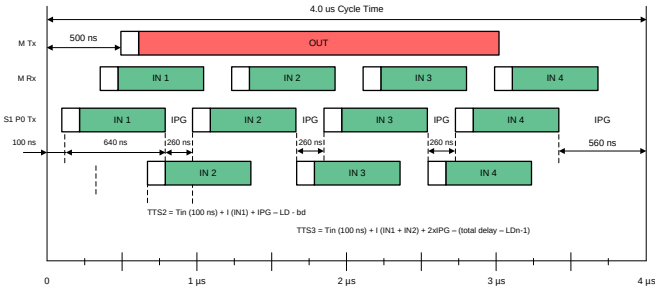
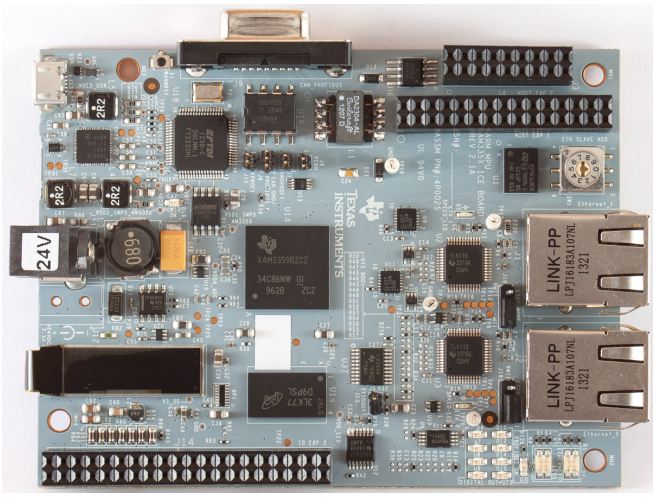
Features

- SORTE Device Reference Implementation
- Enables 4-µs Cycle Time to Exchange Process Data
- PRU Firmware Provided in Source Code
- Fully-Customizable PRU Firmware

Applications

- Industrial Ethernet
- Motion Control
- Programmable Logic Controllers (PLC)
- Industrial I/O Modules
- Industrial Sensors and Actuators
- Servo and Stepper Drives
- Chip-to-Chip Communication Interface





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1 System Overview

1.1 System Description

Industrial Ethernet exists in the factory automation and control market in different type of standards like EtherCAT®, PROFINET®, Sercos III, Ethernet Powerlink, Ethernet/IP, and many more. Those existing standards support a minimum process data cycle time of 31.25 µs for PROFINET and 12.5 µs for EtherCAT.

The SORTE protocol is a TI-developed, industrial Ethernet protocol that supports 4-µs cycle time. The SORTE protocol operates on the PRU-ICSS, which is an industrial peripheral inside Sitara™ and KeyStone™ processors from TI. SORTE operates exclusively on the PRU-ICSS; therefore, the ARM® Cortex®-A8, A9, or A15 processors – depending on the device family – are available for industrial applications.

PRU-ICSS supports many industrial Ethernet protocols through its multiprotocol support, which means that a PRU firmware is loaded into the PRU-ICSS to enable a specific industrial Ethernet protocol. The PRU-ICSS supports on-the-fly and cut-through Ethernet frame processing in real-time. Aside from its multiprotocol support, the PRU-ICSS supports even more functions beyond what is required for today's industrial Ethernet protocols.

With the ability to reduce the cycle time down to 4 µs even further enables new kind of industrial applications. One example application is featured in TIDEP0061[2], a 4-axis CNC router driving stepper motors. This TI Design shows how to control up to four stepper motors from a central control unit over 4-µs cycle time, which enables a 250-kHz control loop.

This TI Design describes the SORTE device implementation on the PRU-ICSS peripheral. The TI Design shows the different industrial Ethernet operation modes including auto-forwarding (AF), host receive (HR), cut-through (CT), and time-triggered-send (TTS). The application example on top of the SORTE protocol controls the digital 8-bit output LEDs on the TMDSICE3359 evaluation module (EVM).

The SORTE device functions together with the SORTE master available as the TI Design TIDEP0085[1].

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
4-µs cycle time	Industrial Ethernet between master and up to four devices
Automatic device detection	Automatic detection of devices at startup of industrial Ethernet
Automatic device configuration	Automatic configuration of devices at startup of industrial Ethernet

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1.3 Block Diagram

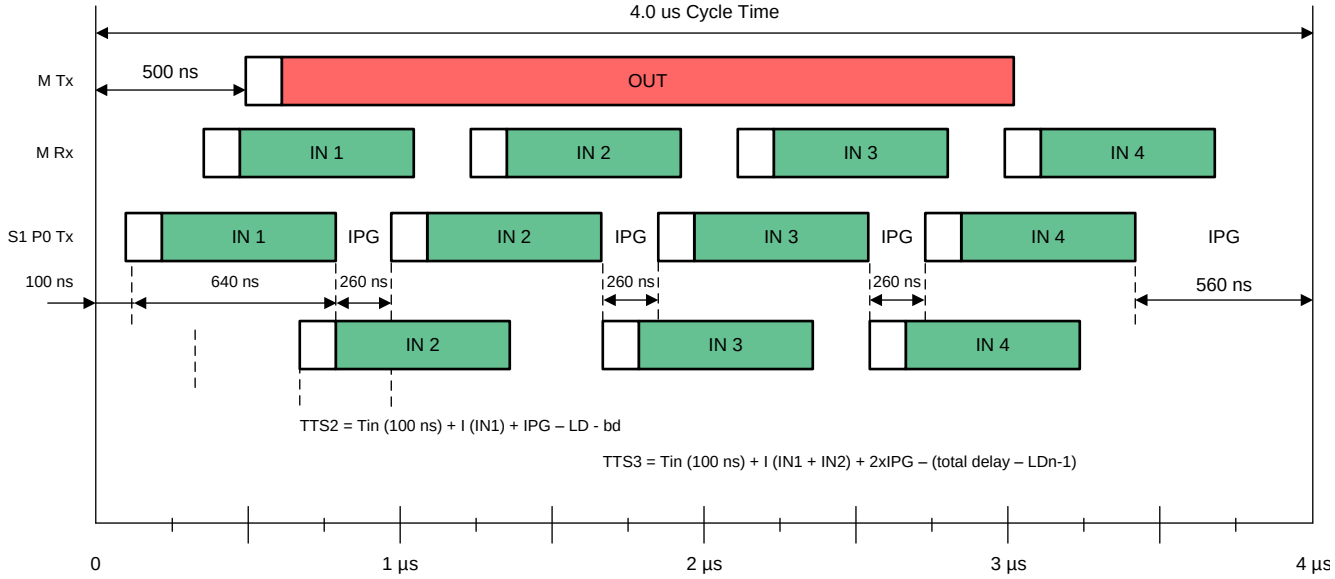

Figure 1. Block Diagram

1.4 Highlighted Products

1.4.1 AM3359

- Up to 1-GHz Sitara ARM Cortex-A8 32-bit RISC processor
- NEON™ SIMD coprocessor
- 32KB of L1 Instruction and 32KB of data cache with single-error detection (parity)
- 256KB of L2 cache with error correcting code (ECC)
- 176KB of on-chip boot ROM
- 64KB of dedicated RAM
- Emulation and debug - JTAG
- Interrupt controller (up to 128 interrupt requests)

PRU-ICSS:

- Supports protocols such as EtherCAT, PROFIBUS, PROFINET, EtherNet/IP, and more
- Two PRUs 32-bit load and store RISC processor capable of running at 200 MHz
- 8KB of instruction RAM with single-error detection (parity)
- 8KB of data RAM with single-error detection (parity)
- Single-cycle, 32-bit multiplier with 64-bit accumulator
- Enhanced GPIO module provides shift-in or shift-out support and parallel latch on external signal
- 12KB of shared RAM with single-error detection (parity)
- Three 120-byte register banks accessible by each PRU INTC for handling system input events
- Local interconnect bus for connecting internal and external masters to the resources inside the PRU-ICSS
- Peripherals inside the PRU-ICSS:
  - One universal asynchronous receiver and transmitter (UART) port with flow control pins, supports up to 12 Mbps
  - One enhanced capture (eCAP) module
  - Two MII Ethernet ports that support industrial Ethernet, such as EtherCAT

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  - One management data input and output (MDIO) port

On-chip memory (shared L3 RAM)

- 64KB of general-purpose on-chip memory controller (OCMC) RAM
- Accessible to all masters

External memory interfaces (EMIF):

- mDDR(LPDDR), DDR2, DDR3, and DDR3L controller:
  - mDDR: 200-MHz clock (400-MHz data rate)
  - DDR2: 266-MHz clock (532-MHz data rate)
  - DDR3: 400-MHz clock (800-MHz Data Rate)
  - DDR3L: 400-MHz clock (800-MHz data rate)
  - 16-bit data bus
  - 1GB of total addressable space
  - Supports one x16 or two x8 memory device configurations
- General-purpose memory controller (GPMC)
- Flexible 8-bit and 16-bit asynchronous memory interface with up to seven chip selects (NAND, NOR, Muxed-NOR, or SRAM)
- Uses BCH code to support 4-, 8-, or 16-bit ECC
- Uses hamming code to support 1-bit ECC

See the *AM335x Sitara Processors* data sheet for a complete list of features.

1.4.2 DP83822I

- IEEE 802.3u compliant: 100BASE-FX, 100BASETX and 10BASE-Te
- MII, RMII, and RGMII MAC Interfaces
- Low-power single supply options:
  - 1.8-V average (AVD) < 120 mW
  - 3.3-V AVD < 220 mW
- ±16-kV HBM ESD Protection
- ±8-kV IEC 61000-4-2 ESD Protection
- Start of frame detect for IEEE 1588 time stamp
- Fast link-down timing
- Auto-crossover in force modes
- Operating temperature: –40 to 125°C
- I/O voltages: 3.3 V, 2.5 V and 1.8 V
- Power savings features:
  - Energy efficient Ethernet (EEE) IEEE 802.3az
  - Wake-on-LAN (WoL) support with magic packet detection
  - Programmable energy savings modes
- Cable diagnostics
- BIST
- Management data clock (MDC) and MDIO interface

See the *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver* data sheet for a complete list of features.

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1.4.3 TMDSICE3359 Industrial Communication Engine EVM

Hardware specifications:

- AM3359 ARM Cortex-A8
- DDR3, NOR flash, and SPI flash
- Organize light-emitting diode (OLED) display
- TPS65910 power management 24-V power supply
- USB cable for JTAG interface and serial console

Software and tools:

- SYS/BIOS real-time operating system (OS)
- Starterware base port
- TI's Code Composer Studio™ (CCS) integrated development environment (IDE)
- Application stack for industrial communication protocols
- Sample industrial applications

Connectivity:

- PROFIBUS interface
- CANOpen
- EtherNet/IP
- PROFINET
- Sercos III
- Digital inputs and outputs (I/O)
- SPI
- UART
- JTAG

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2 System Design Theory

2.1 Real-Time Ethernet

In the context of industrial Ethernet, *real time* does not mean fast. Real time refers to an event, such as the cycle time to exchange process data occurring at a deterministic time (see Figure 2). If the cycle time does not occur within the expected time, there is latency. Measuring latency over many cycle times results in determine the jitter of an industrial Ethernet network. *Jitter* is the deviation of the time when the deterministic event occurred. Typically a system must keep the jitter to a minimum. In industrial Ethernet, active components such as the Ethernet physical (PHY) device and the media access control unit (MAC) introduce jitter.

Another network parameter is *runtime delay*, which is the time that it takes for an Ethernet frame to get from the sender to the receiver. Runtime delay is a constant parameter and generated by every network component, such as the Ethernet cable, MAC, and PHY. Because runtime delay is constant, delay can get compensated during the engineering phase of the network or measured by the network devices during run time.

Cycle time is a constant time period when network devices exchange process data. The particular industrial Ethernet standard dictates the minimum cycle time; in the previous example, PROFINET cannot have a faster cycle time than 31.25 µs.

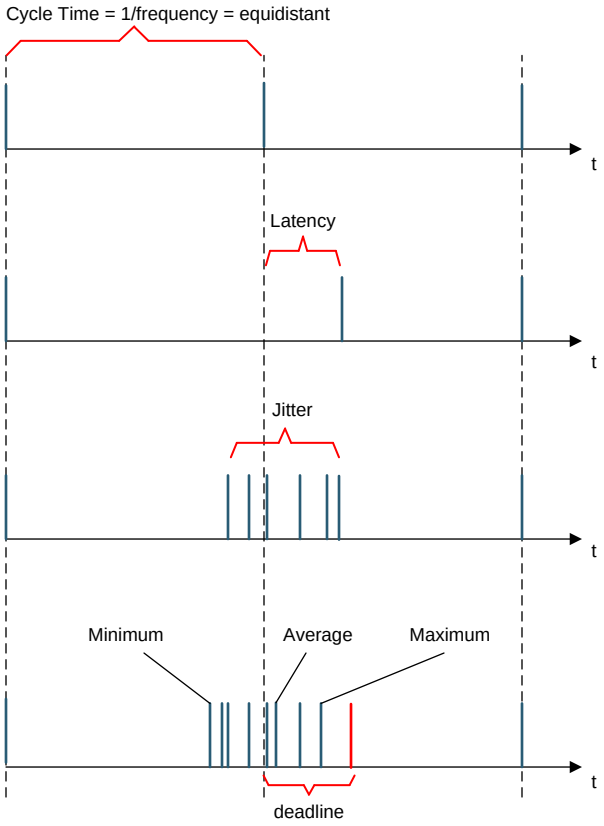

Figure 2. Definition of Real Time

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2.2 SORTE Protocol

The SORTE protocol is a TI-developed industrial Ethernet protocol that supports 4-µs cycle time. The SORTE protocol operates on the PRU-ICSS, which is an industrial peripheral within Sitara and KeyStone processors from Texas Instruments. SORTE protocol operates exclusively on the PRU-ICSS; therefore, the ARM Cortex-A8, A9 or A15 processors – depending on the device family – are available for industrial applications.

The SORTE protocol differentiate between two network components: the master and one or more devices. Figure 3 shows the SORTE network topology.

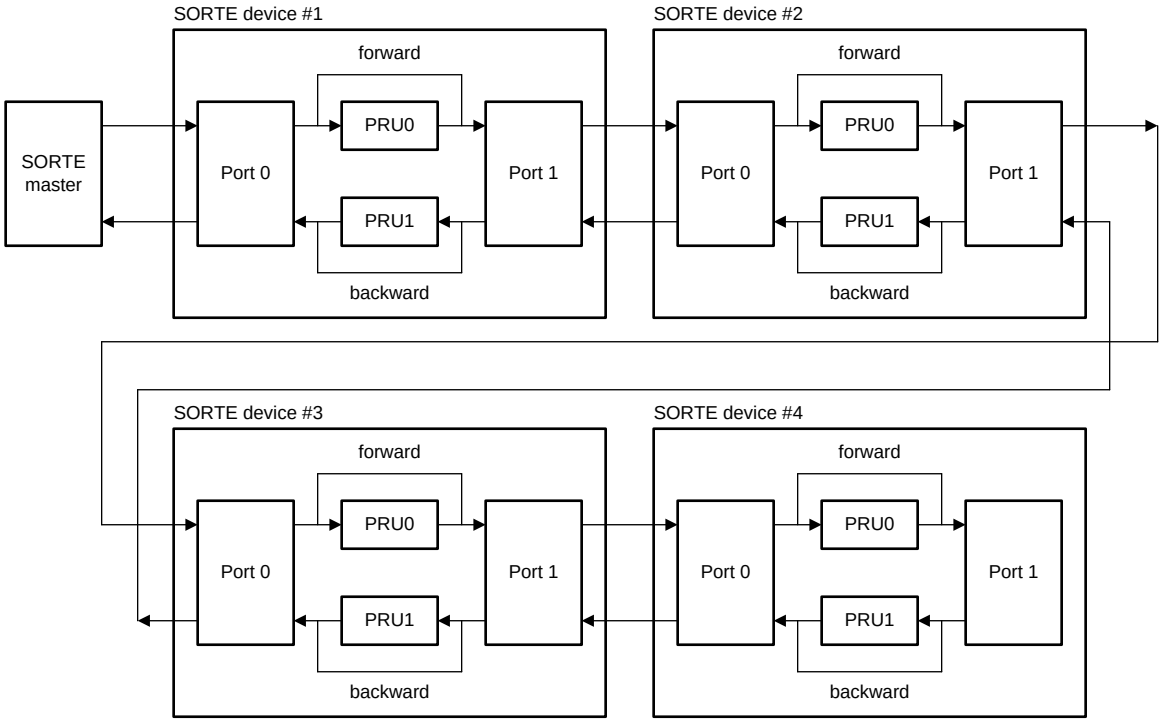

Figure 3. SORTE Network Topology

The SORTE master is documented in the TI Design TIDEP0085[1].

The SORTE device is documented in this TI Design.

SORTE protocol has different types of states before the cycle exchange of process data is started.

- Discovery - The master detects the number of devices in the industrial Ethernet network. This state automatically assigns addresses to devices and completes exchanges of I/O capabilities.
- Parameterization - The master sends the network, application, diagnostic, and error parameters.
- Synchronization - There are two parts in this state. First, the Ethernet transmission delay from each network master to device and from device to device is measured. Second, the master synchronizes the devices to the masters' internal reference time.
- IO exchange - This is the operational state. The master and the devices exchange process data with a 4-µs cycle time.
- Alarm, Link-loss, Reconnect - Depending on the severity of detected error or topology change, this state can result in a retrain of the SORTE protocol.

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Figure 4 shows a diagram of the SORTE protocol states.

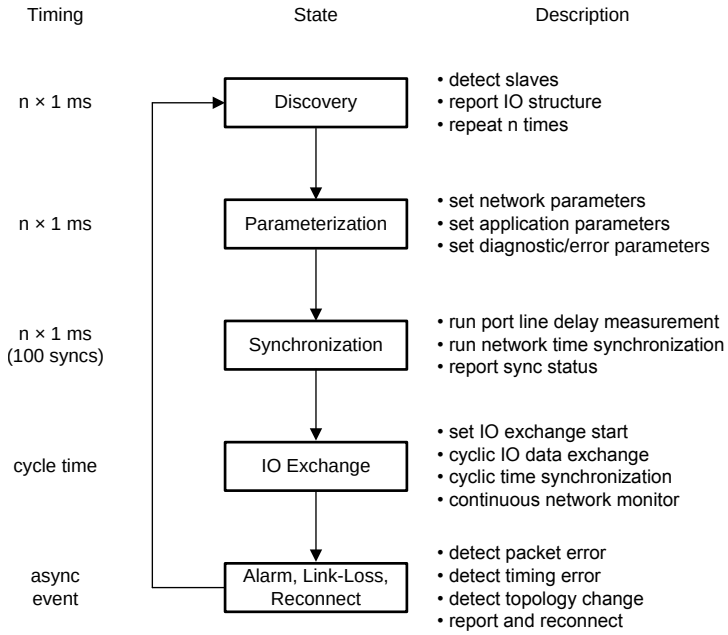

Figure 4. SORTE Protocol State Diagram

The industrial Ethernet port is configured for the following port configurations:

- AF - The Ethernet frame is forwarded automatically from the receiving port to the transmitting port without PRU interaction. PRU has the option to receive the frame through L2 RX buffer. See HR configuration.
- Auto-forward with loopback (AF-LP) - The Ethernet frame is forwarded automatically from the receiving port to the transmitting port without PRU interaction. In the LP case the receiving and transmitting port is the same port number.
- CT - The Ethernet frame is received into RX L2 buffer. PRU analyzes the header and pushes the frame content into second port TX FIFO
- HR - The PRU is receiving the Ethernet frame through RX L2 FIFO. This configuration works in conjunction with AF.
- Host send (HS) - The PRU is transmitting an Ethernet frame through the TX FIFO. This configuration is a PRU local generated frame.
- TTS - The PRU preload the TX FIFO with the frame content and enables TTS though IEP timer. When TTS is activated, the TX FIFO starts to transmit the TTS content.

2.3 SORTE Slave Implementation

2.3.1 Overview

The SORTE slave protocol requires for the AF mode the TX_AUTO_SEQUENCE function of PRU-ICSS, which is available in TI Sitara and KeyStone processor devices that support all industrial protocols. Check the device feature comparison table in the device's data manual. The SORTE device implementation has been tested on the Sitara AM3359 device. Customers can also port the PRU firmware implementation to other TI processors with PRU-ICSS.

All real-time critical tasks of the SORTE protocol are operated inside the PRU-ICSS.

Each PRU handles one receive port and one transmit port. The typical configuration is that PRU0 receives from Port 0 and transmits to Port 1 while the PRU1 receives from Port 1 and transmits to Port 0. The Ethernet frame path and the PRU that handles the frames from the SORTE master is referred as *forwarding* path. The reverse frame direction is referred as *backward* path.

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Figure 5 shows the Ethernet port assignments for PRU0 and PRU1.

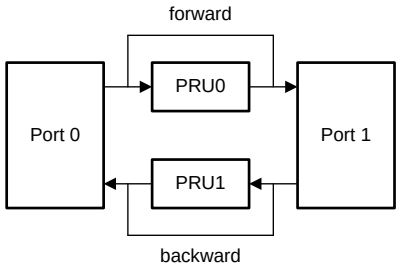

Figure 5. Ethernet Port Assignment for PRU0 and PRU1

The TI Design uses the following naming convention when referring to I/O data:

- I/O data is detected from the SORTE master point of view
- Input data is data that is sent by the devices to the master
- Output data is sent by the master and used by the devices

2.3.2 PRU Firmware

This section is divided into IEP timer usage and the PRU firmware software structure.

2.3.2.1 IEP Timer Usage

Depending on the SORTE protocol state, the IEP timer is used in different ways. In IO exchange state, the IEP timer wraps around with the cycle time, while in all other states, the IEP timer is free running. The eight compare registers CMP0 to CMP7 are used for the following purposes:

- CMP0 - cycle time in IO exchange state; not used in other states
- CMP1 - not used
- CMP2 - not used
- CMP3 and CMP4 - Time-triggered-send (TTS) event generation used by SORTE protocol
- CMP5 - not used
- CMP6 - not used
- CMP7 - not used

NOTE: CMP0, CMP1, CMP6 and CMP7 are used to generate SYNC0 pulse with TI design TIDEP0061[2].

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2.3.2.2 SORTE Device Software File Structure

The SORTE device is written in PRU assembly language and consists of different file modules. The overall function flow is shown in Figure 6.

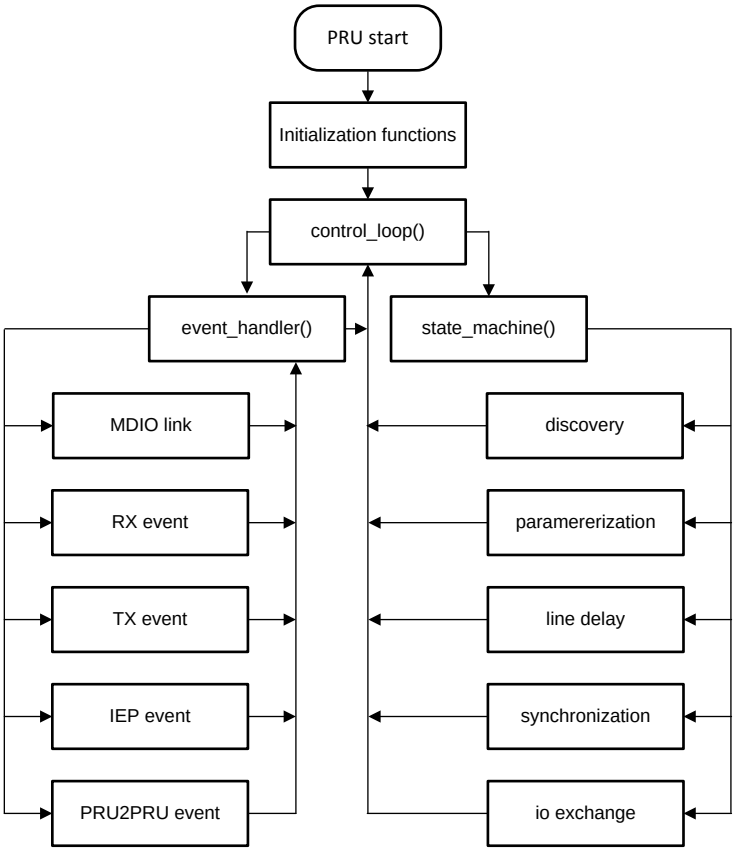

Figure 6. SORTE Device Firmware Flow Chart

The SORTE device contains of the following source files:

- main.asm - contains the initialization routine and the main control loop
- event_handler.asm - INTC event handler service routines
- state.asm - SORTE device state machine
- discovery.asm - contains the discovery state implementation
- param.asm - contains the parameterization state implementation
- line_delay.asm - contains the line delay measurement of the synchronization state implementation
- sync.asm - contains the timer synchronization state implementation
- ioex.asm - contains the IO exchange state implementation

The following subsections describe the specific function implementation of each of the files.

2.3.2.3 main.asm

The file performs the following tasks:

- PRU register initialization
- Resetting and configuring of the MII_RT module
- Generating MDIO LINK event to read in current Ethernet link status
- Configuration of IEP timer and IEP timer events
- Control loop, which calls INTC event handler and the SORTE state machine

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2.3.2.4 event_handler.asm

The file performs the following tasks:

- Checks if an PRU INTC event is pending
- Reads out the INTC event and executes the event handler routing
  - MDIO link event - occurs with Ethernet port link change
  - IEP event - occurs when compare register value match with IEP counter
  - PRU to PRU event - occurs when one PRU needs to trigger an event in the second PRU
  - RX EOF event - occurs when a frame was completely received
    - This event validates CRC checksum in some SORTE states. The event does also trigger the start of a SORTE state transition

2.3.2.5 state.asm

The file perform the following tasks:

- Depending on the current SORTE device and PRU port state, calls the SORTE state handler function:
  - Discovery
  - Parameterization
  - Synchronization
  - IO exchange

2.3.2.6 discovery.asm

This file performs the following tasks:

- Detection of which port is the forward direction port and the backward direction port
- Assignment of device address
- Exchange the amount of I/O data that are transmitted in IO exchange state

2.3.2.7 param.asm

This file performs the following tasks:

- Both PRU port directions are in AF mode
- PRU in forward direction receives the param frame from the master and stores the frame content in PRU shared memory
- PRU in backward direction ignore the frame
- Last device loops back the param frame to the master

2.3.2.8 line_delay.asm

This file perform the following tasks:

- The port of forward direction is configured as HS.
- The port in backward direction is configured as AFLP.
- PRU measures the line delay between the forward direction port and the next SORTE device.

2.3.2.9 sync.asm

This file performs the following tasks:

- Both ports are in AF and HR mode
- Time stamping of SYNC frame
- Synchronization of the device time to the master time

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2.3.2.10 ioex.asm

This file performs the following tasks:

- The port of forward direction is configured in AF with HR.
- The port of backward direction is dynamically switched between TTS and AF.
- PRU in forward direction receives the master data frame and extracts the devices process data and stores it in PRU shared memory.
- PRU in backward direction starts with TTS of the process input data and switches to AF after TTS data has been sent. With cycle time, the wrap-around switches back to TTS.

2.3.3 ARM® Software

The control unit (SORTE master) and motor unit (SORTE device) use the same ARM application source code. The ARM application reads out the rotary switch on the TMDSICE3359 to determine if this EVM operates as master or device.

The ARM performs the following tasks:

- Configuration of AM3359 pinmuxing for Ethernet ports of ICSS
- MMU configuration
- ICSS initialization
- PRU shared memory initialization and configuration
- CRC8 lookup table generation
- Loading and starting PRU firmware

3 Getting Started Hardware and Software

3.1 Hardware

The following boards are required for this TI Design:

- Between two to five boards of TMDSICE3359 industrial communication engine (ICE) EVMs are from the TI e-store.

Connect an Ethernet cable from the master's RJ45 J2 port to device's RJ45 J2 port. With multiple devices, connect an Ethernet cable from the first device's RJ45 J1 port to the second device's RJ45 J2 port. Follow the same procedure for additional devices.

Power up all SORTE devices before powering up the SORTE master. The SORTE master will detect the connected SORTE devices and will proceed to IO exchange state.

3.2 Software

Download the software package and import the software projects into CCS. There are two CCS projects:

- SORTE_app - ARM application
- SORTE_SLAVE - Device PRU firmware

Compile each project individually. Compile the SORTE_slave project first, as it createes PRU C-header for the SORTE_app project. Download the SORTE_app.out file through JTAG to each TMDSICE3359 EVM. Alternatively, copy the file *SORTE_app_ti.app* to a bootable micro SD card and rename the file to *app*. Insert the micro SD card into the micro SD card interface of the TMDSICE3359 EVM, and press the reset button or power cycle the board. The application software is getting executed.

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4 Testing and Results

The setup consists of one SORTE master connected to four SORTE devices. Figure 7 shows the measurements on the first SORTE device of the Ethernet PHY with 4-µs cycle time. Port 0 is connected through the Ethernet cable to the master, and Port 1 is connected towards the second devices. The network is in IO exchange state.

- Port 0 RX_DV shows the reception of the master frame.
- Port 0 TX_EN shows the forward transmission of master frame.
- Port 1 RX_DV shows the received device frames; the three frames are forwarded to the master through PORT 0 TX_EN.

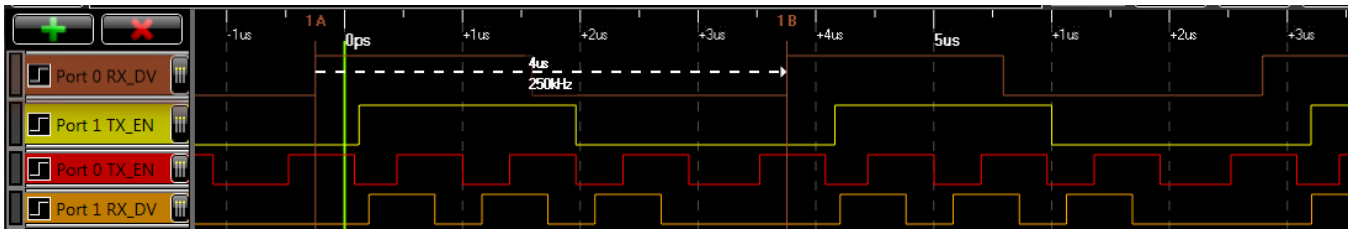

Figure 7. Industrial Ethernet With 4-µs Cycle Time

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDEP0086.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP0086.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDEP0086.

5.4 Altium Project

To download the Altium project files, see the design files at TIDEP0086.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDEP0086.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDEP0086.

6 Software Files

TI will release the software files on a public GIT tree to maintain version control. Please contact your TI representative for further information.

7 Related Documentation

1. Texas Instruments, *Simple Open Real-Time Ethernet Master with PRU-ICSS Reference Design*, TIDEP0085 TI Design (TIDUCK4)
2. Texas Instruments, *4-Axis CNC Router With 250-kHz Control Loop Reference Design*, TIDEP0061 TI Design (TIDUBY0)

7.1 Trademarks

All trademarks are the property of their respective owners.

8 Terminology

- CCS - Code Composer Studio
- ICSS - Industrial Communication System
- INTC - Interrupt Controller inside PRU-ICSS
- PRU - Programmable Real-Time Unit
- SORTE - Simple Open Real-Time Ethernet

9 About the Author

THOMAS MAUER is a System Engineer in the Factory Automation and Control Team at Texas Instruments Freising. He is responsible for developing reference design solutions for the industrial segment. Thomas brings his extensive experience in industrial communications like Industrial Ethernet and fieldbuses and industrial applications to this role. Thomas earned his degree in Electrical Engineering (Dipl. Ing. (FH)) at the University of Applied Sciences in Wiesbaden, Germany.

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