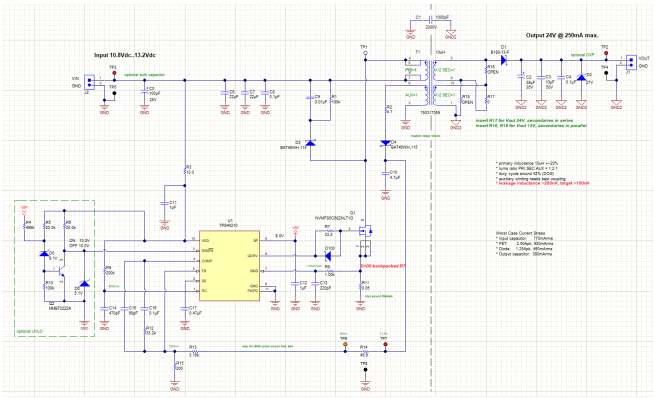
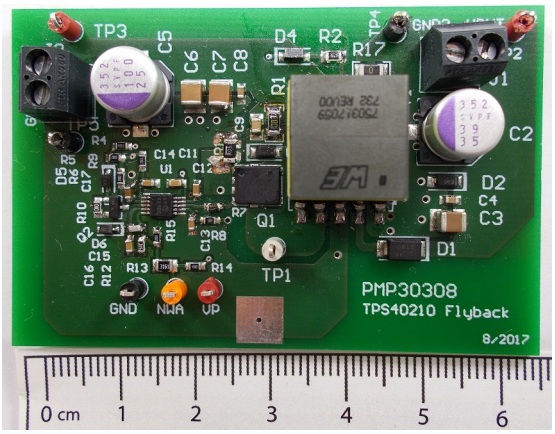
Test Report: PMP30308
Isolated 6-W DCM Flyback Reference Design

Description

This reference design converts an input voltage of about 12V to an isolated output voltage of 24V @ 250mA$_{max}$. Low cost due to TPS40210 controller primary side regulation. A typical application may be IGBT-Driver and interface isolation.





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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
V_{IN}	10.8V to 13.2V
V_{OUT}	12V @ 250mA_{max}
Nominal switching frequency	200kHz

1.2 Considerations

Optional UVLO switches ON at 10.31V and OFF at about 10.03V input voltage.

Unless otherwise mentioned all measurements were done with 12V nominal input voltage and 0.25A full load output current (resistive load).

Primary side regulation

Pro

- The optocoupler is omitted. Therefore the are no issue with the aging problem of the optocoupler
- lower part count

Cons

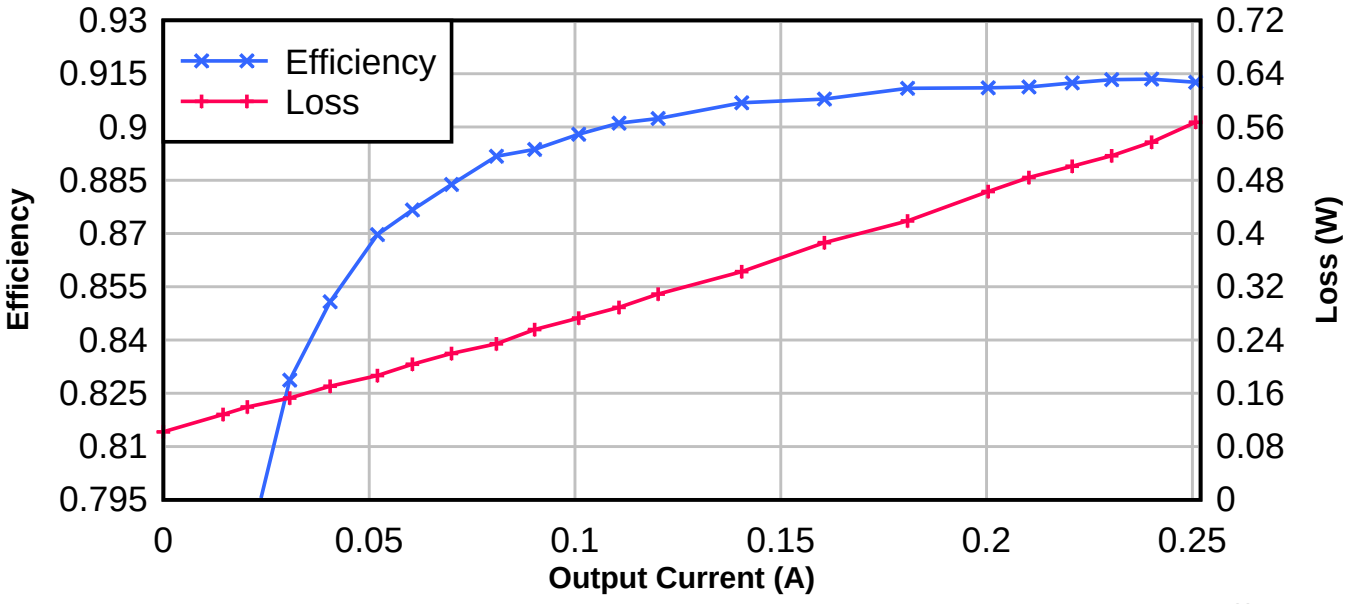
- load regulation depends on the coupling of the transformer
- the transformer must have an auxiliary winding (possible workaround is dedicated IC for primary side regulation flyback like LM5180)

2 Testing and Results

2.1 Efficiency Graphs

Electronic load was used.

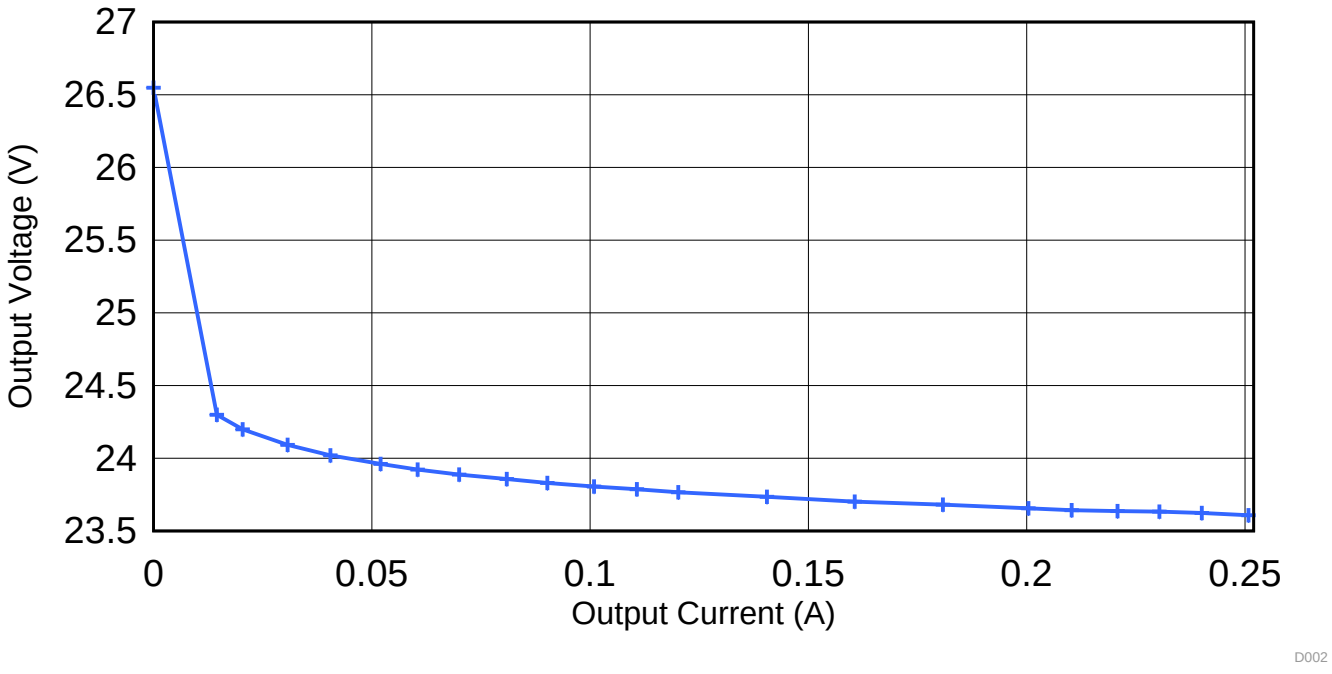
Figure 1. Efficiency and Loss vs Output Current



2.2 Load Regulation

Electronic load was used.

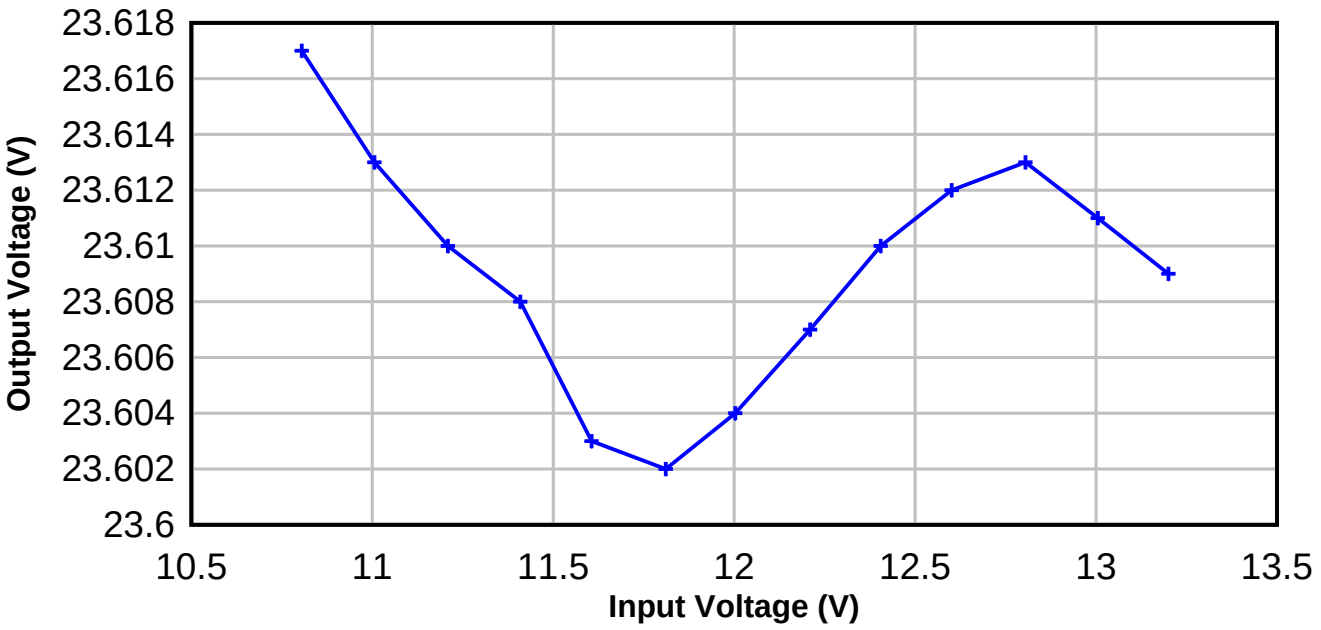
Figure 2. Output Voltage vs Output Current



Load regulation in between 10mA and 250mA load current is better than 3% !

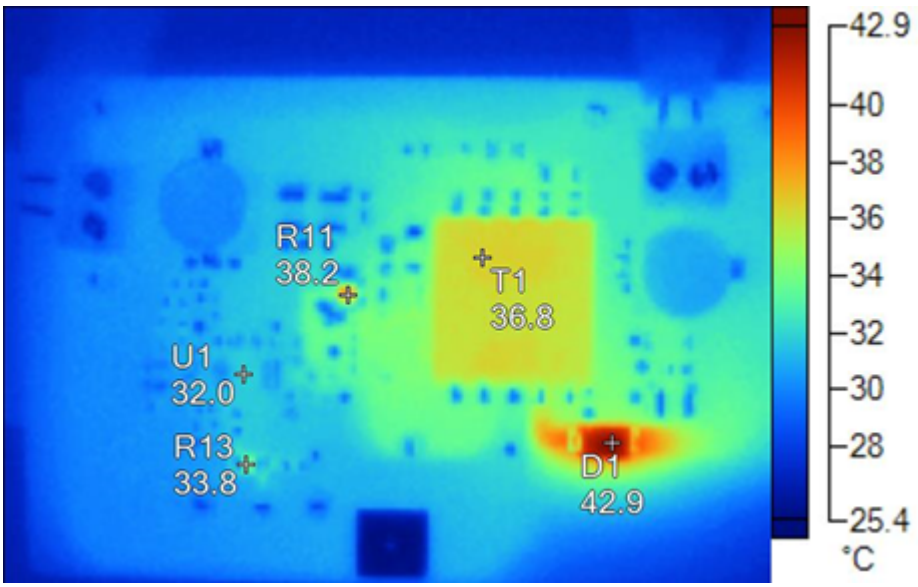
2.3 Line Regulation

Figure 3. Output Voltage vs Input Voltage



2.4 Thermal Images

Figure 4. Thermal Image for 12V Input Voltage and 250mA Output Current



Name	Temperature
D1	42.9°C
R11	38.2°C
R13	33.8°C
T1	36.8°C
U1	32.0°C

The thermal stress at this 6W design is fairly low due to reasonable full load efficiency >91%.

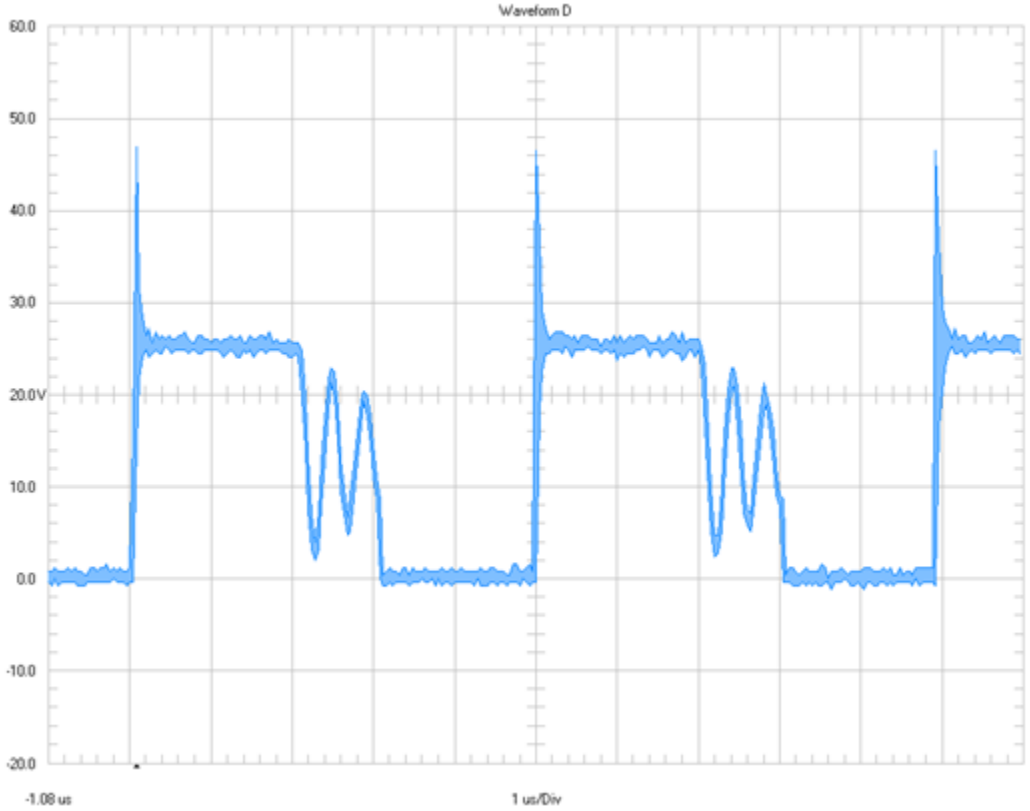
3 Waveforms

3.1 Switching

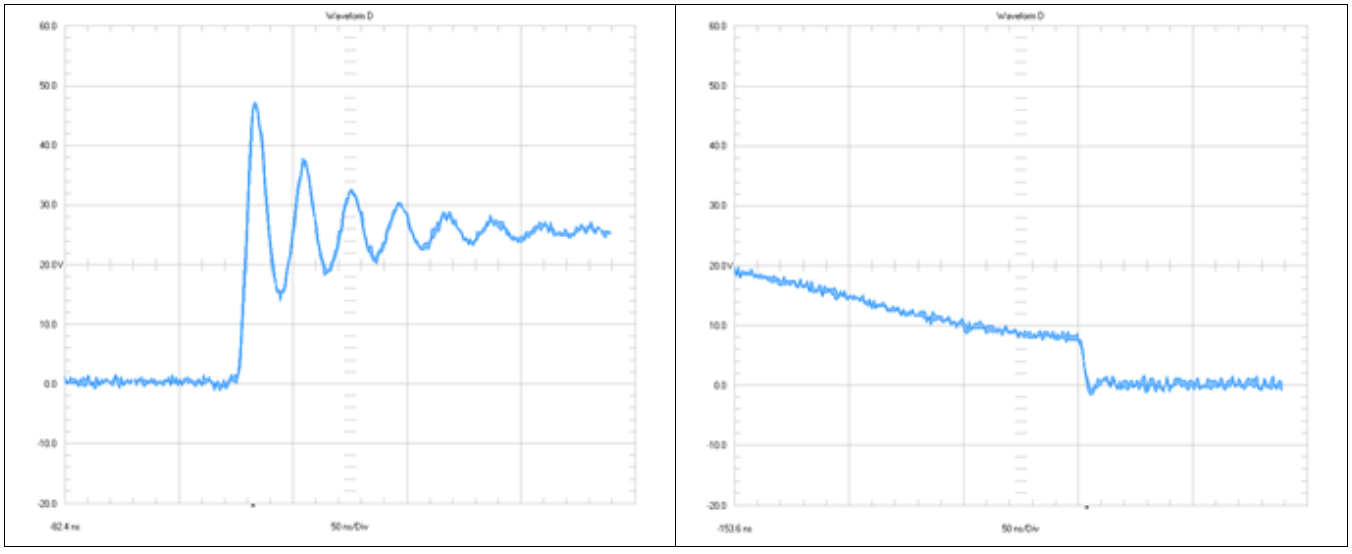
All waveforms in this chapter were done with full bandwidth setting.

3.1.1 Transistor Q1

Figure 5. Switchnode Voltage Q1 Drain to GND



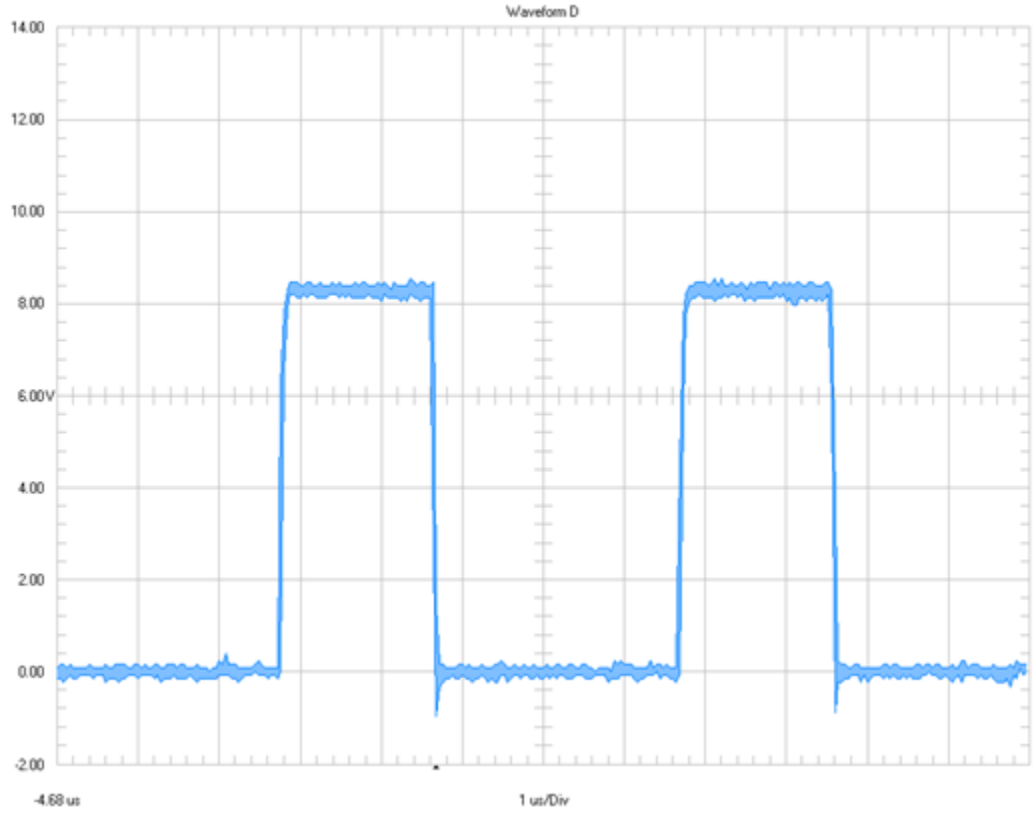
- 10V/div
- 1µs/div



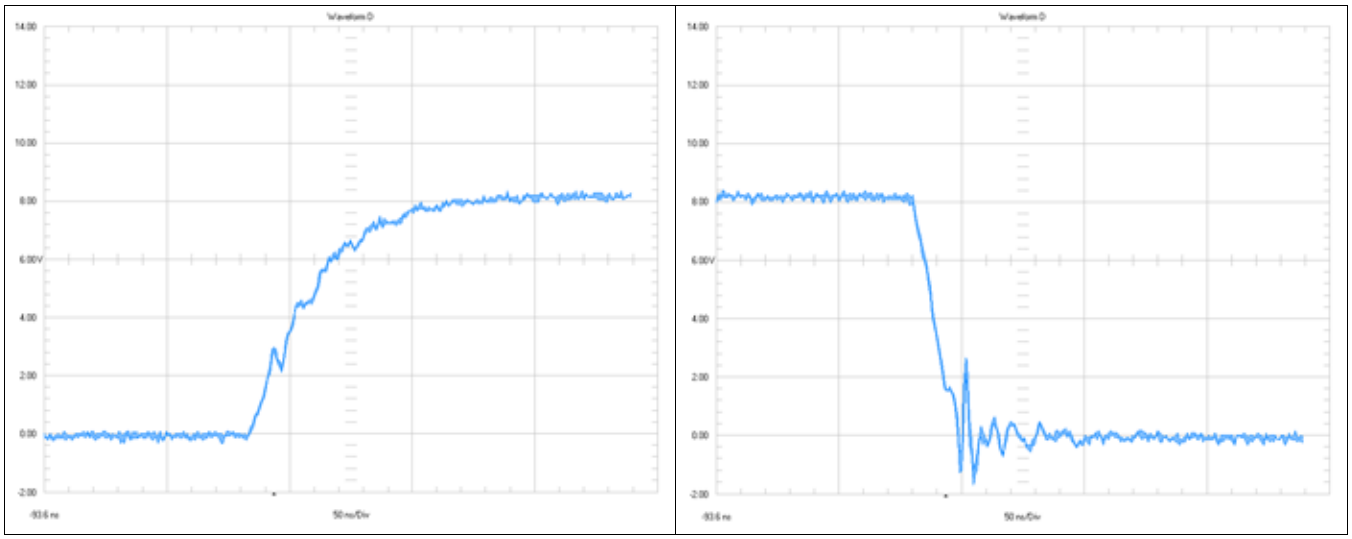
- 50ns/major div

3.1.2 Transistor Q1 Gate

Figure 6. Q1 Gate to GND



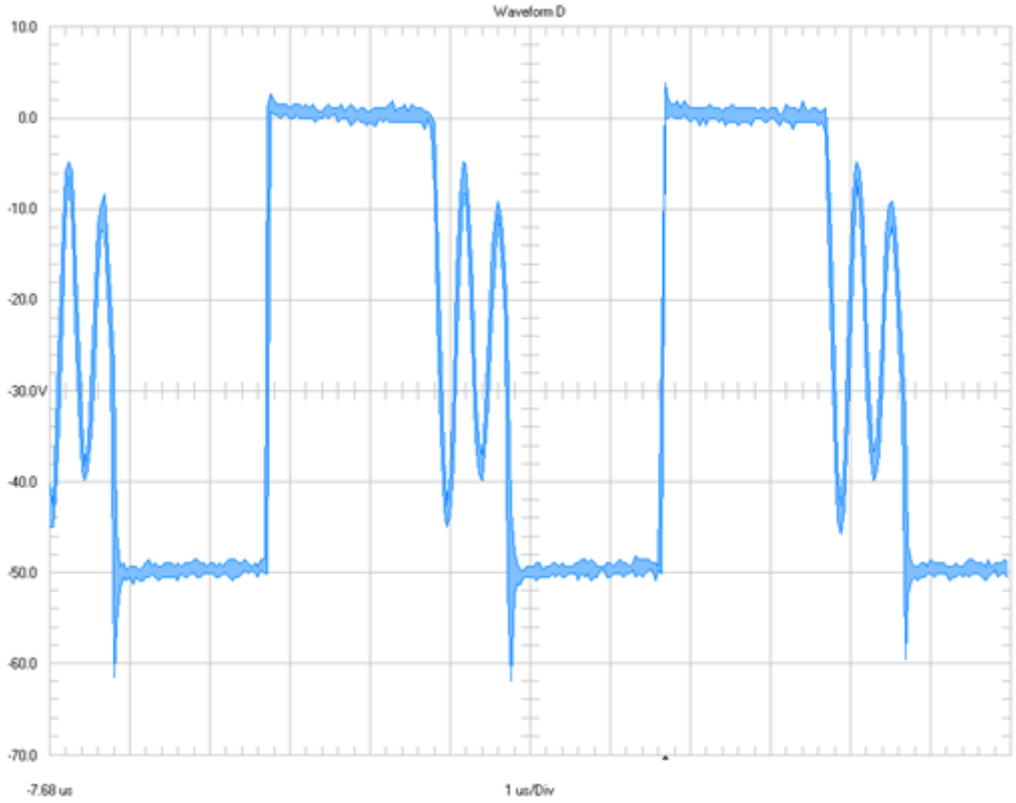
- 2V/div
- 1µs/div



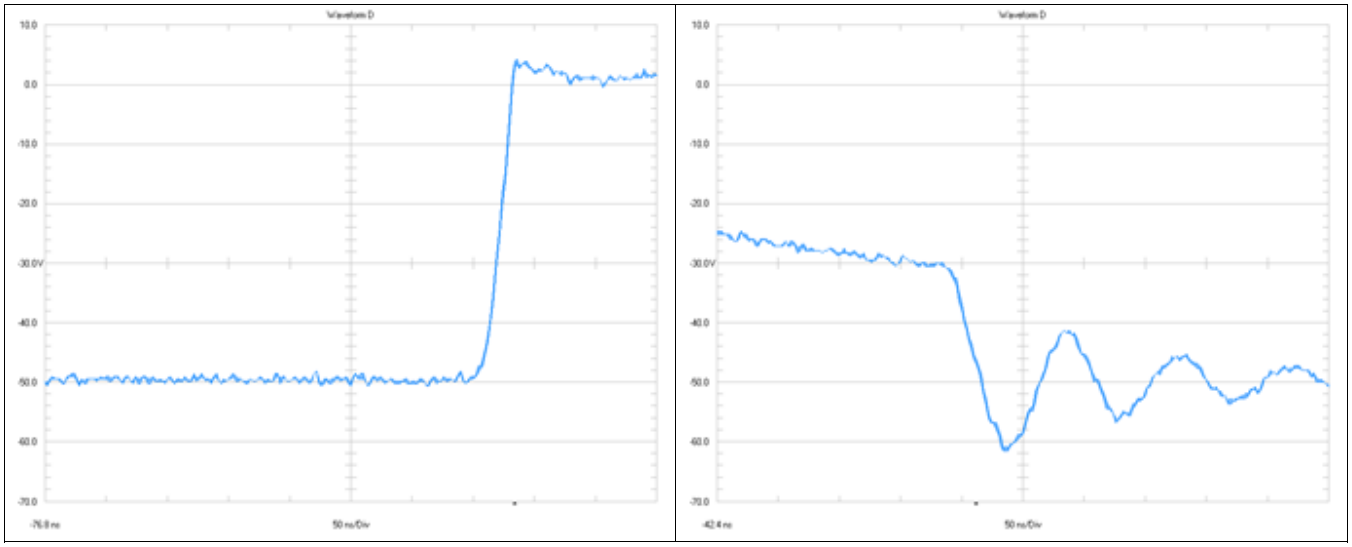
- 50ns/major div

3.1.3 Diode D1

Figure 7. Diode D1 referenced to VOUT



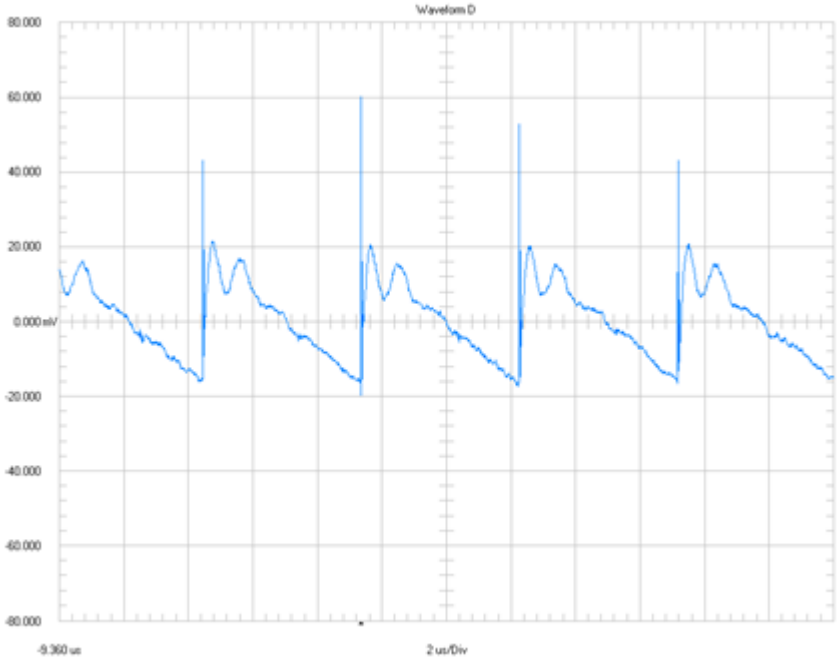
- 10V/div
- 1µs/div



50ns/major div

3.2 Output Voltage Ripple

Figure 8. Output Ripple Voltage (AC Coupled)

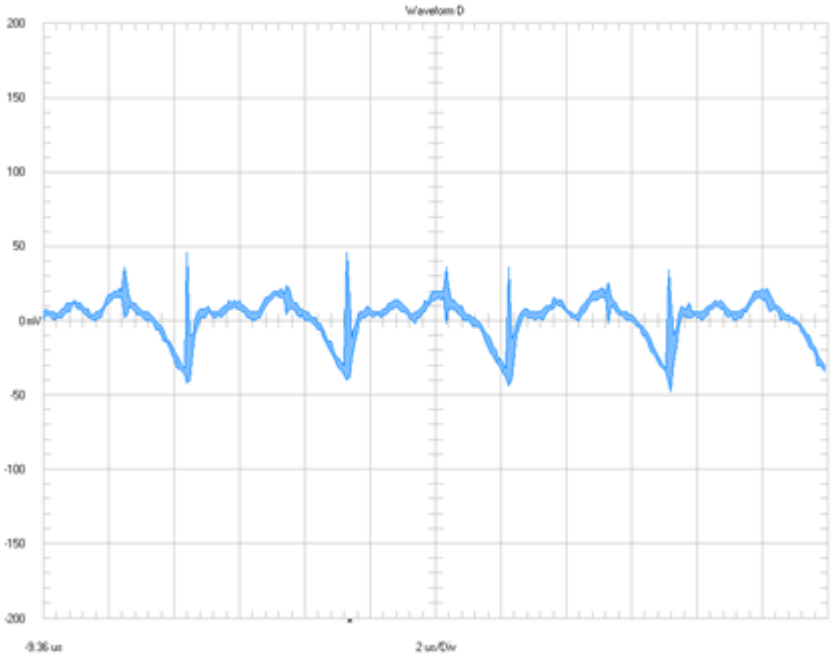


- 20mV/div (20MHz bandwidth setting)
- 2µs/div

The thermal stress at this 6W design is fairly low due to reasonable full load efficiency >91%.

3.3 Input Voltage Ripple

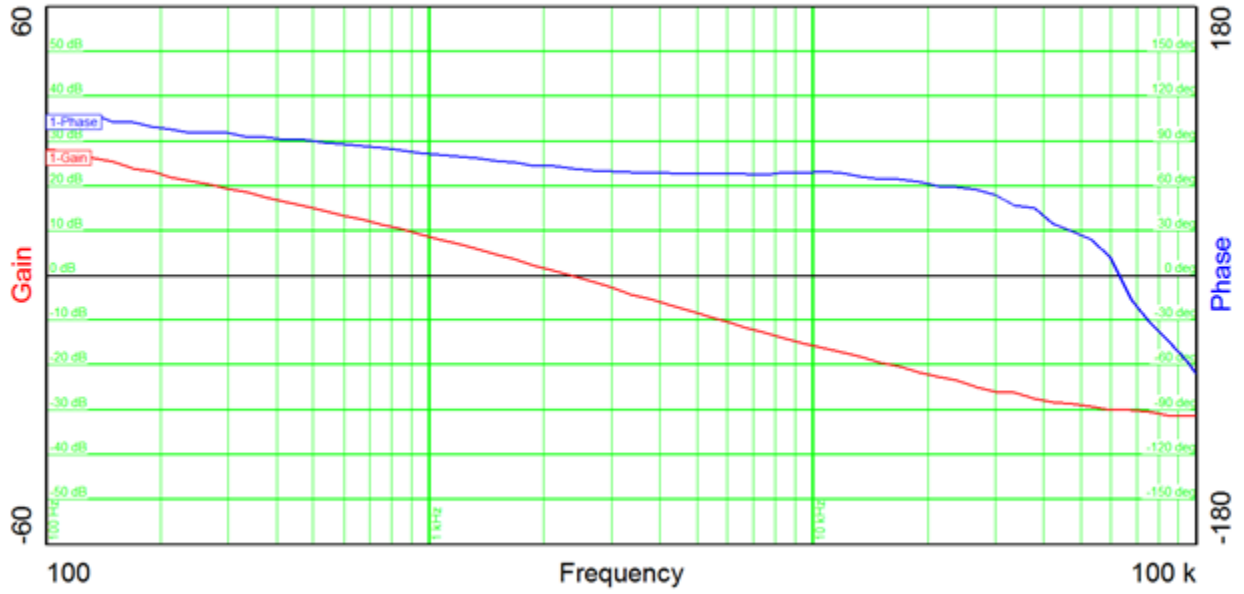
Figure 9. Input Voltage Ripple (AC Coupled)



- 50mV/div (20MHz bandwidth setting)
- 2µs/div

3.4 Bode Plot

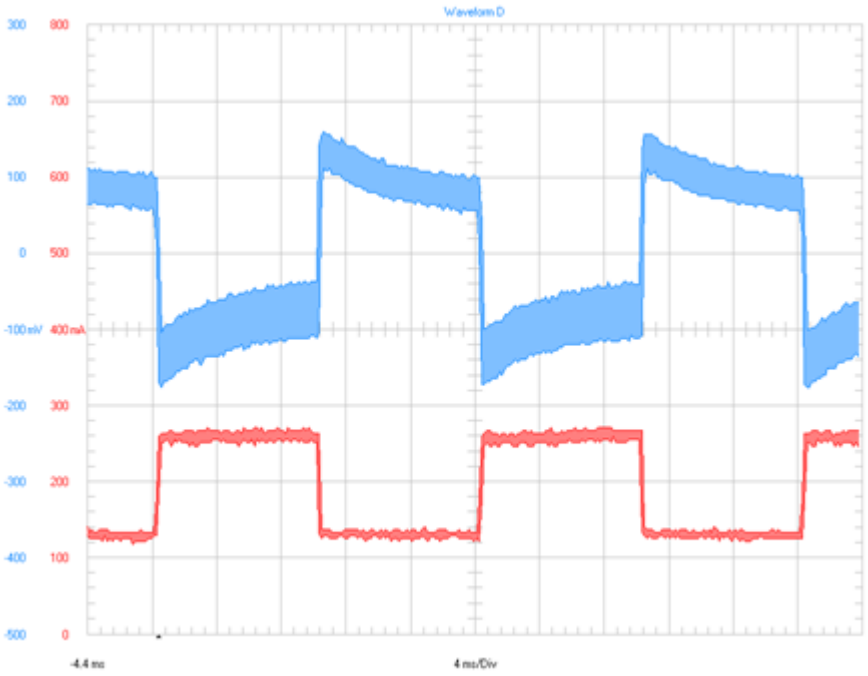
Figure 10. Loop Response with ~0.25A Output Current and ~12V Input Voltage



	12V
Bandwidth (kHz)	2.35
Phasemargin	72°
slope (20dB/decade)	-1.23
gain margin (dB)	-30
slope (20dB/decade)	+0.01
freq (kHz)	63

3.5 Load Transients

Figure 11. Load Transient (0.125A / 0.25A 50Hz with Electronic Load N3305A)

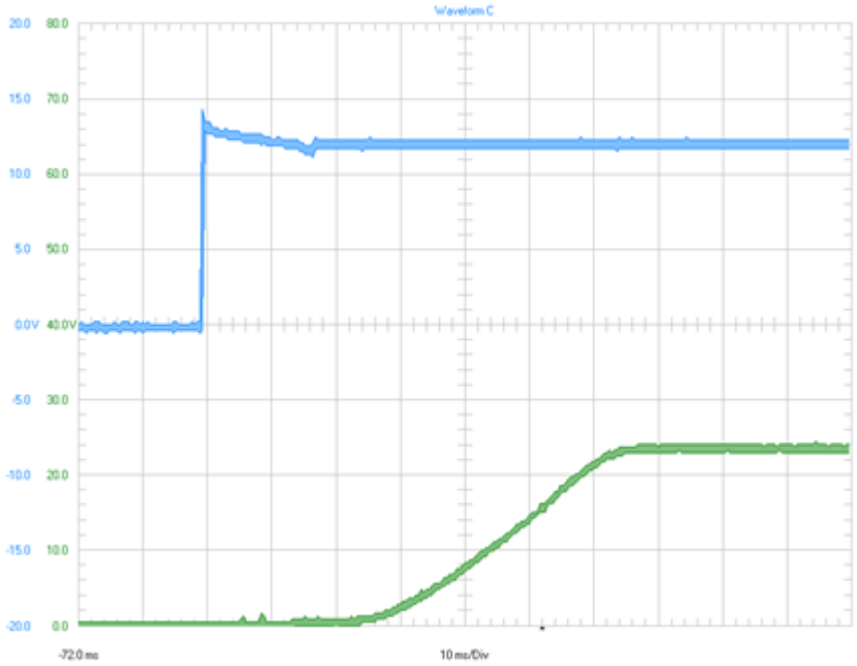


- Channel 1 (blue): output voltage => 100mV/div (20MHz bandwidth setting)
- Channel 2 (red): Output Current => 100mA/div (10kHz bandwidth setting)
- 4ms/div
  The DC error is related to limited load regulation by primary side regulation;
  The dynamic load deviation due to 50% load transient is only 100mV, so less than 0.5% !

3.6 Start-up Sequence

The power supply was connected.

Figure 12. Start-up with Electronic Load

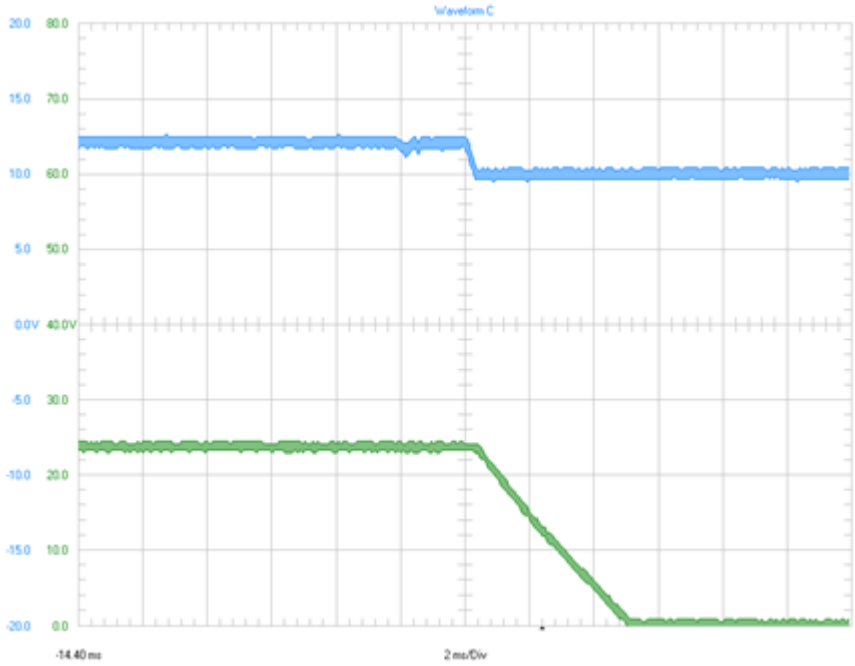


- Channel 1 (blue): input voltage => 5V/div
- Channel 2 (green): output voltage => 10V/div
- 10ms/div

3.7 Shut-Down Sequence

The power supply was disconnected

Figure 13. Shut-down with Electronic Load



- Channel 1 (blue): input voltage => 5V/div
- Channel 2 (green): output voltage => 10V/div
- 2ms/div

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2018) to A Revision	Page
• Changed Output Voltage vs Output Current graph	3

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