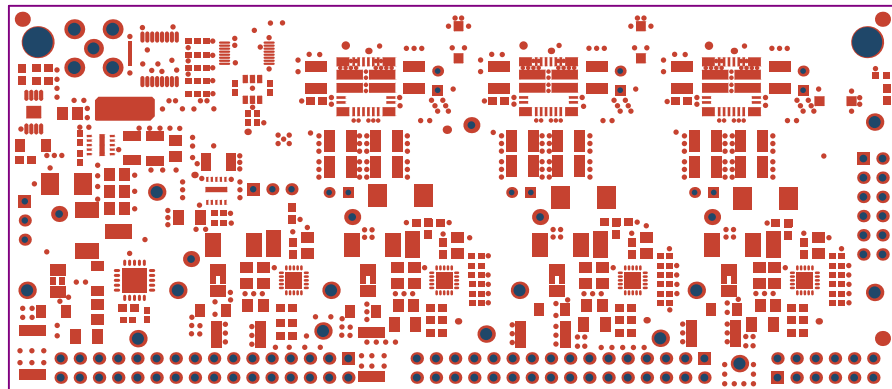
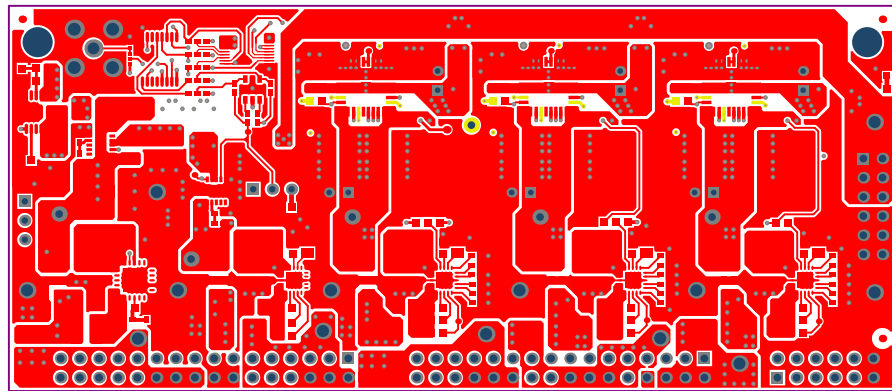


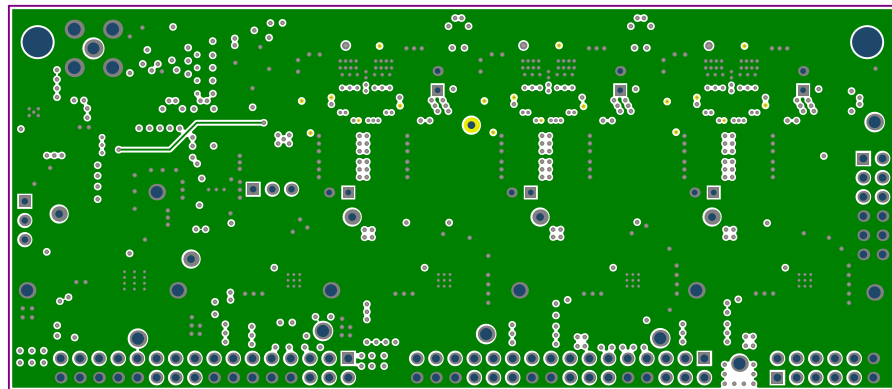
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01027	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Top Overlay	TID #: 01027		
PLOT NAME = Top Overlay	GENERATED : 2/18/2019 12:26:44 PM	TEXAS INSTRUMENTS	



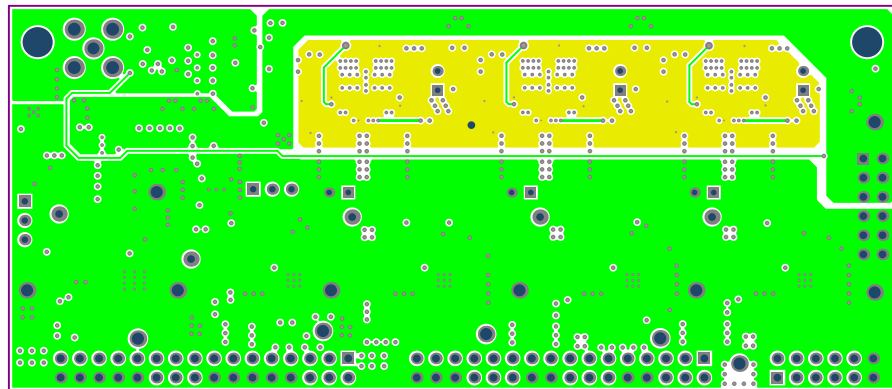
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01027	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Top Solder	TID #: 01027		
PLOT NAME = Top Solder Mask	GENERATED : 2/18/2019 12:26:44 PM	TEXAS INSTRUMENTS	



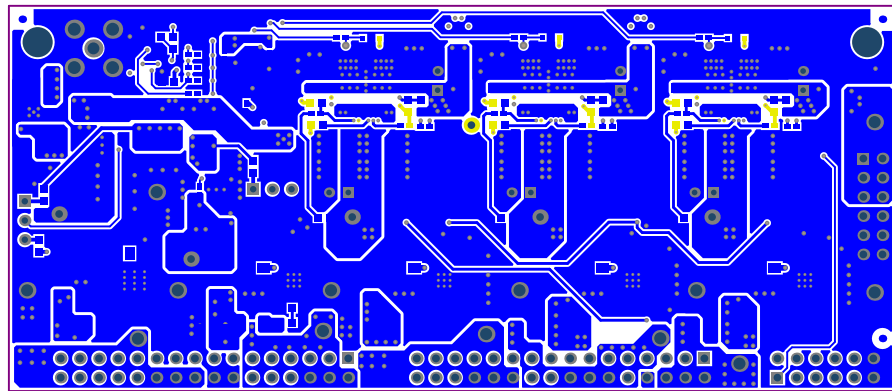
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01027	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Top Layer	TID #: 01027		
PLOT NAME = Top Layer	GENERATED : 2/18/2019 12:26:44 PM	TEXAS INSTRUMENTS	



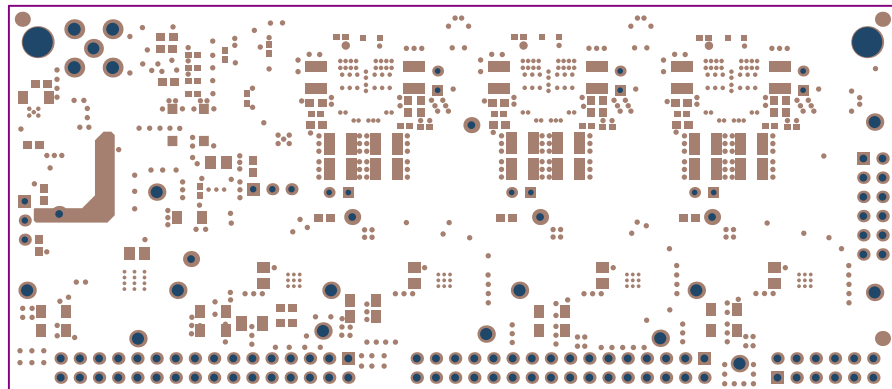
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01027	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = GND	TID #: 01027		
PLOT NAME = GND Layer	GENERATED : 2/18/2019 12:26:45 PM	TEXAS INSTRUMENTS	



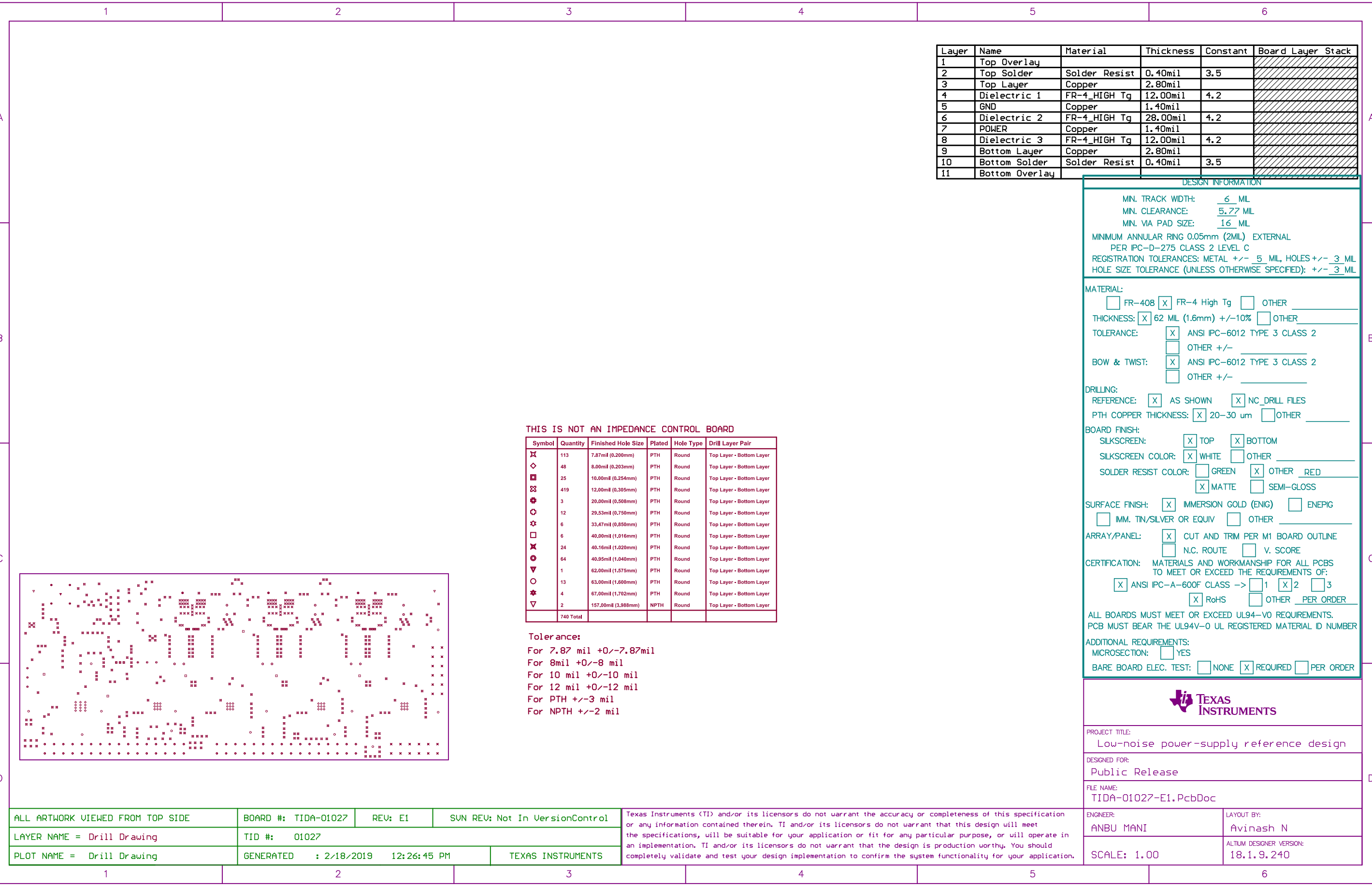
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01027	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = POWER	TID #: 01027		
PLOT NAME = POWER Layer	GENERATED : 2/18/2019 12:26:45 PM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01027	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Bottom Layer	TID #: 01027		
PLOT NAME = Bottom Layer	GENERATED : 2/18/2019 12:26:45 PM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01027	REV: E1	SUN REV: Not In VersionControl
LAYER NAME = Bottom Solder	TID #: 01027		
PLOT NAME = Bottom Solder Mask	GENERATED : 2/18/2019 12:26:45 PM	TEXAS INSTRUMENTS	



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	2.80mil		
4	Dielectric 1	FR-4_HIGH Tg	12.00mil	4.2	
5	GND	Copper	1.40mil		
6	Dielectric 2	FR-4_HIGH Tg	28.00mil	4.2	
7	POWER	Copper	1.40mil		
8	Dielectric 3	FR-4_HIGH Tg	12.00mil	4.2	
9	Bottom Layer	Copper	2.80mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 6 MIL
 MIN. CLEARANCE: 5.27 MIL
 MIN. VIA PAD SIZE: 16 MIL
 MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER_RED
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

THIS IS NOT AN IMPEDANCE CONTROL BOARD

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair
⊗	113	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer
◇	48	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer
■	25	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer
⊗	419	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer
⊗	3	20.00mil (0.508mm)	PTH	Round	Top Layer - Bottom Layer
⊗	12	29.53mil (0.750mm)	PTH	Round	Top Layer - Bottom Layer
⊗	6	33.47mil (0.850mm)	PTH	Round	Top Layer - Bottom Layer
□	6	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer
⊗	24	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer
⊗	64	40.95mil (1.040mm)	PTH	Round	Top Layer - Bottom Layer
▽	1	62.00mil (1.575mm)	PTH	Round	Top Layer - Bottom Layer
○	13	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer
⊗	4	67.00mil (1.702mm)	PTH	Round	Top Layer - Bottom Layer
▽	2	157.00mil (3.988mm)	NPTH	Round	Top Layer - Bottom Layer
	740 Total				

Tolerance:
 For 7.87 mil +0/-7.87mil
 For 8mil +0/-8 mil
 For 10 mil +0/-10 mil
 For 12 mil +0/-12 mil
 For PTH +/-3 mil
 For NPTH +/-2 mil

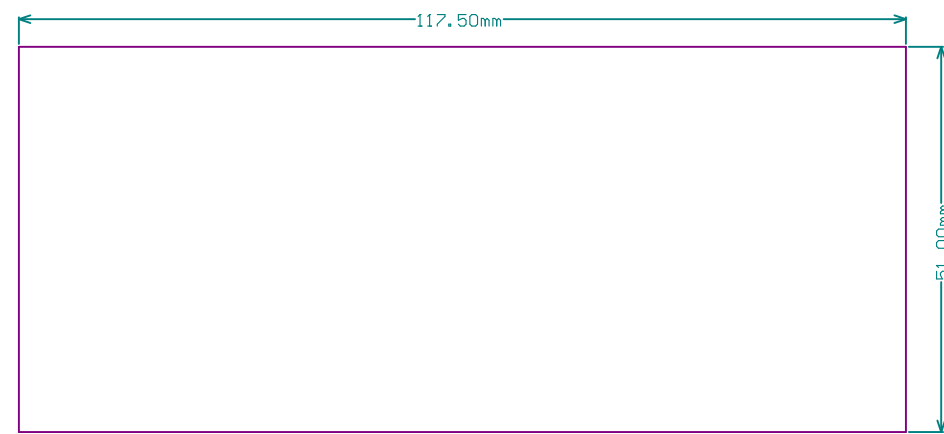
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01027	REV: E1	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	ENGINEER: ANBU MANI	LAYOUT BY: Avinash N
LAYER NAME = Drill Drawing	TID #: 01027	GENERATED : 2/18/2019 12:26:45 PM			SCALE: 1.00	ALTIM DESIGNER VERSION: 18.1.9.240
PLOT NAME = Drill Drawing	TEXAS INSTRUMENTS					

TEXAS INSTRUMENTS

PROJECT TITLE:
Low-noise power-supply reference design

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-01027-E1.PcbDoc



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01027	REV: E1	SUN REV: Not In VersionControl
LAYER NAME =	TID #: 01027		
PLOT NAME = Board Dimensions	GENERATED : 2/18/2019 12:26:49 PM	TEXAS INSTRUMENTS	

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