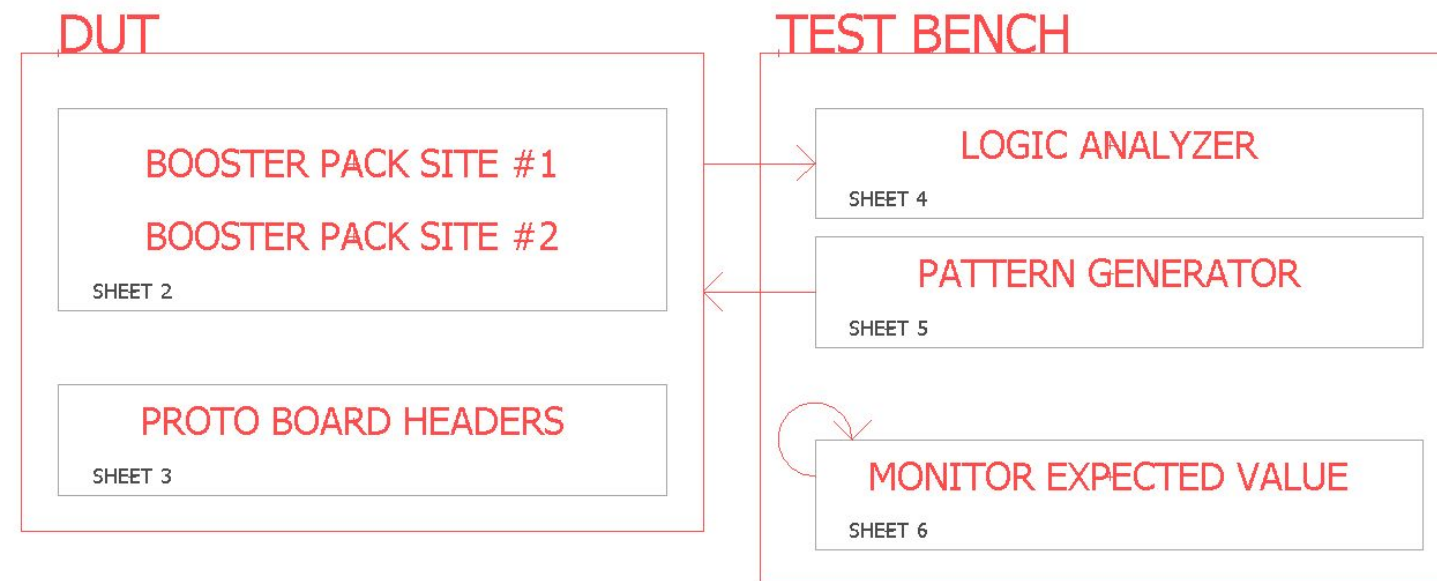


Revision History

Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

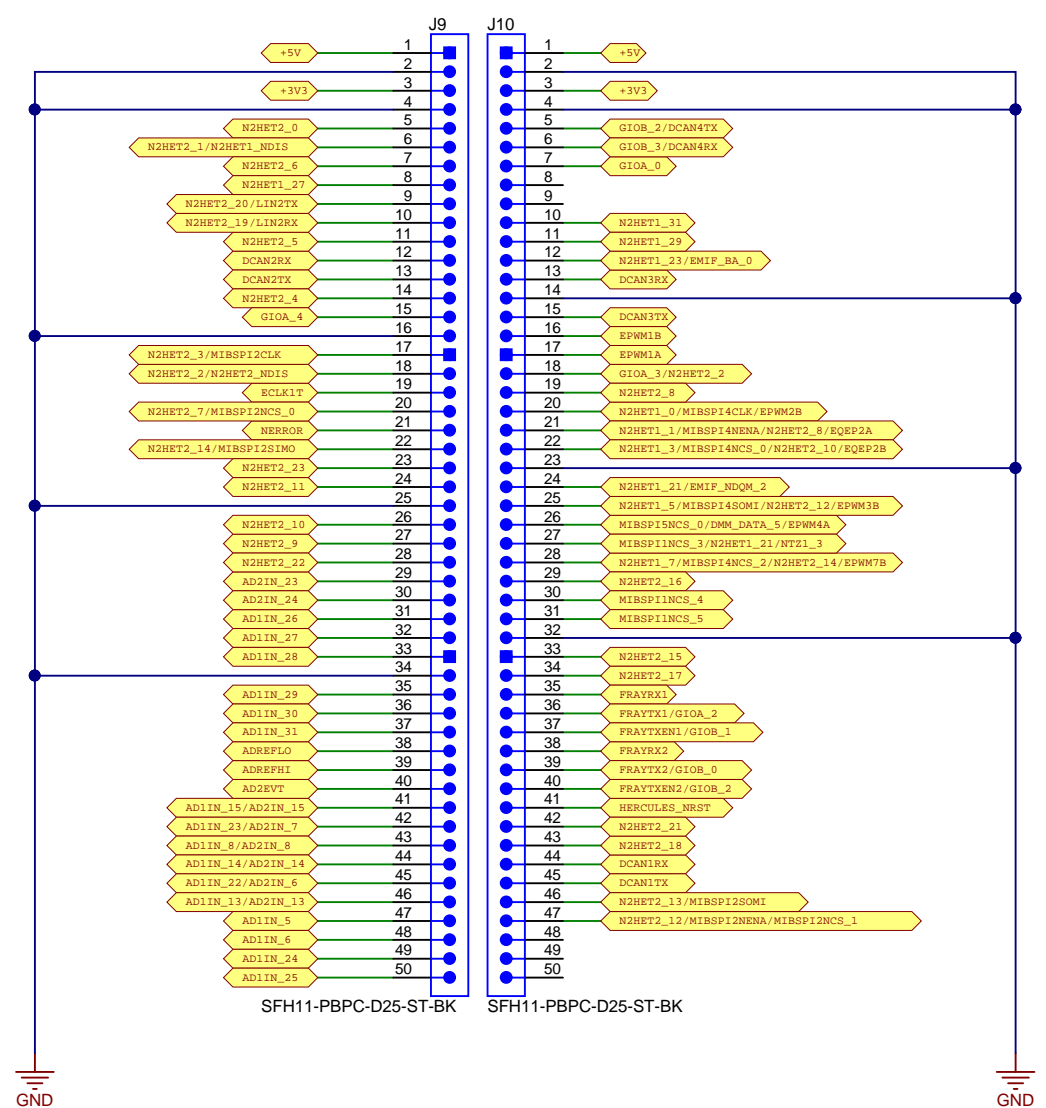
LAUNCHXL2-RM57L HET TEST BOARD



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TID #: TIDM-HAHCPTO	Project Title: Test Board for TIDM-HAHCPTO		
Number: TIDM-HAHCPTO	Rev: A	Sheet Title: Block Diagram	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 3	
Drawn By: Anthony Seely	File: TIDM-HAHCPTO-Test-CoverSheet.SchDoc	Size: B	
Engineer: Anthony Seely	Contact: http://www.ti.com/support		

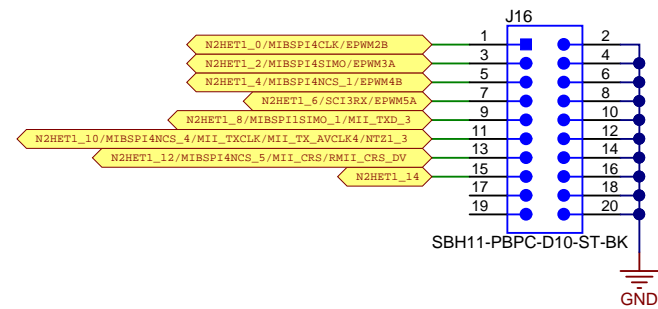
PROTO BOARD HEADERS



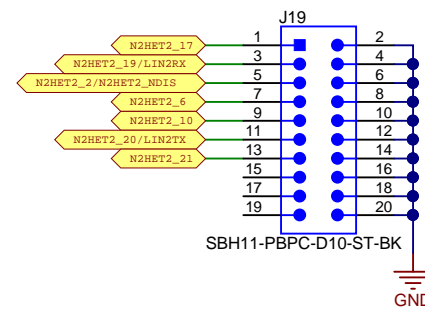
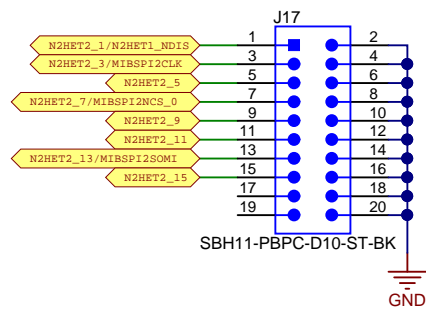
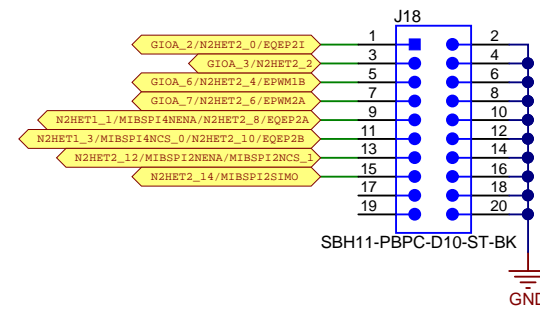
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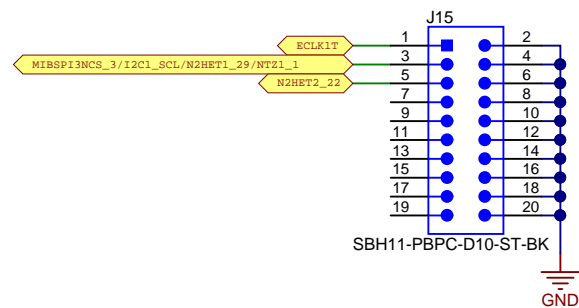
HET1 PATTERN GEN



HET2 PATTERN GEN



PATTERN GEN CLOCK & WAIT

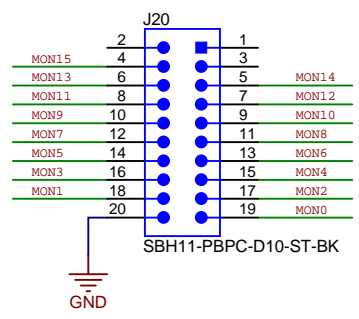
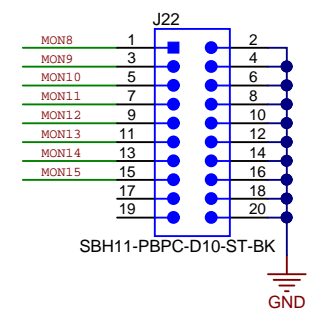
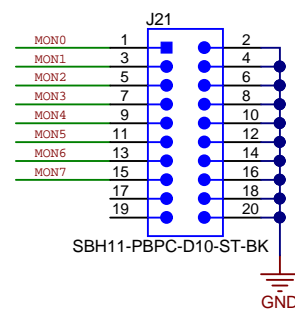


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TID #: TIDM-HAHSCPTO	Project Title: Test Board for TIDM-HAHSCPTO	
Number: TIDM-HAHSCPTO	Rev: A	Sheet: 2 of 3
SVN Rev: Version control disabled	Assembly Variant: 001	Size: B
Drawn By: Anthony Seely	File: TIDM-HAHSCPTO-Test_PatGen.SchDoc	http://www.ti.com
Engineer: Anthony Seely	Contact: http://www.ti.com/support	© Texas Instruments 2016

GENERATE EXPECTED PATTERN

MONITOR EXPECTED PATTERN



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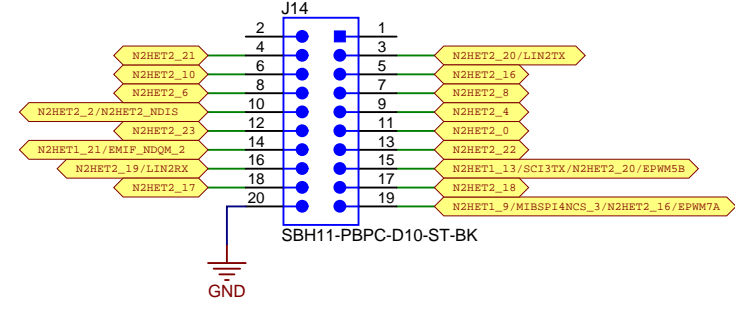
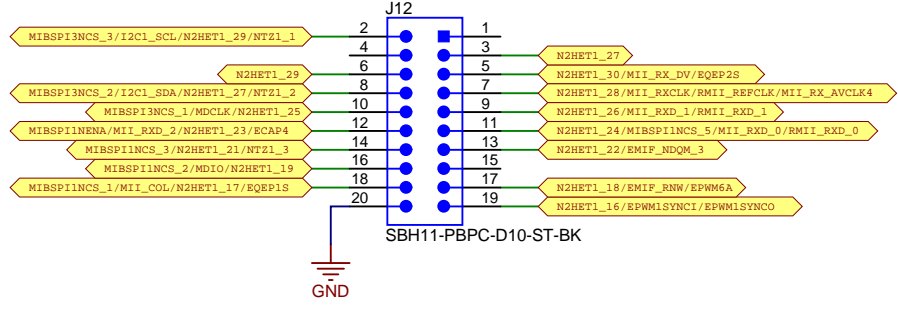
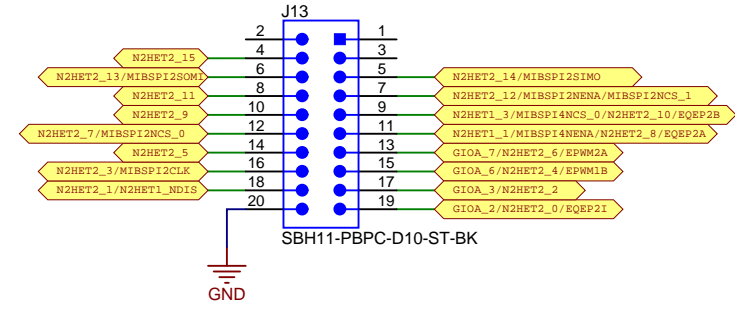
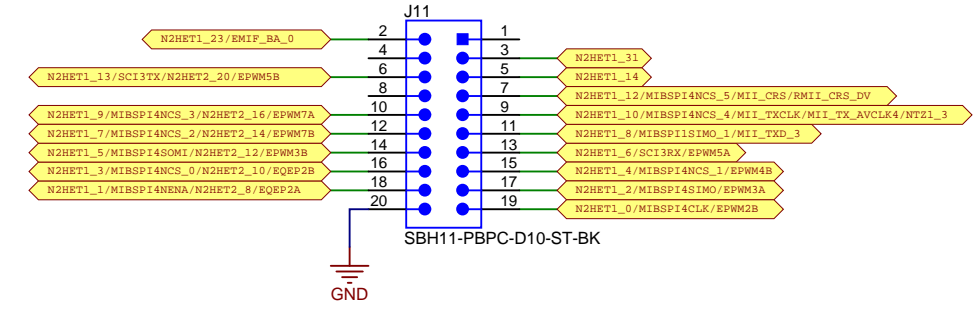
Orderable: ChangeMe!	Designed for: Public Release	Mod. Date: 5/17/2016
TID #: TIDM-HAHCPTO	Project Title: Test Board for TIDM-HAHCPTO	
Number: TIDM-HAHCPTO Rev: A	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 2 of 3
Drawn By:	File: TIDM-HAHCPTO-Test_Monitor.SchDoc	Size: B
Engineer: Anthony Seely	Contact: http://www.ti.com/support	http://www.ti.com

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HET1 LOGIC ANALYZER

HET2 LOGIC ANALYZER



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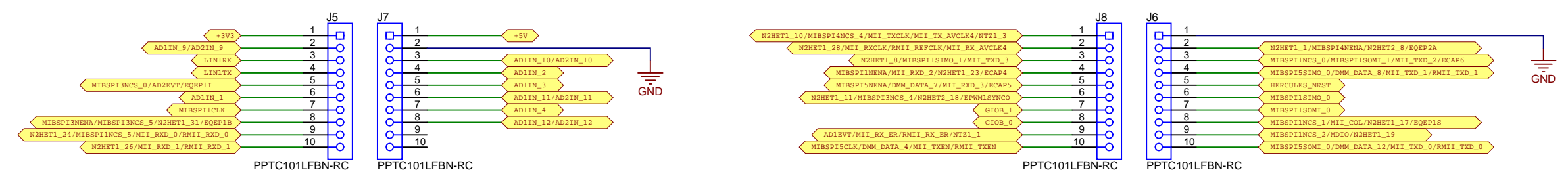
Orderable: ChangeMe!	Designed for: Public Release	Mod. Date: 5/17/2016
TID #: TIDM-HAHSCPTO	Project Title: Test Board for TIDM-HAHSCPTO	
Number: TIDM-HAHSCPTO Rev: A	Sheet Title: Logic Analyzer Headers	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 2 of 3
Drawn By: Anthony Seely	File: TIDM-HAHSCPTO-Test_LogicAna.SchDoc	Size: B
Engineer: Anthony Seely	Contact: http://www.ti.com/support	



BOOSTER PACK SITE 1



BOOSTER PACK SITE 2



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TID #: TIDM-HAHSCPTO	Project Title: Test Board for TIDM-HAHSCPTO		
Number: TIDM-HAHSCPTO Rev: A	Sheet Title: Booster Pack		
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 2 of 3	
Drawn By: Anthony Seely	File: TIDM-HAHSCPTO-Test_BoosterPack.SchDoc	Size: B	
Engineer: Anthony Seely	Contact: http://www.ti.com/support		

H1 1 NY PMS 440 0025 PH H2 1 NY PMS 440 0025 PH H3 1 NY PMS 440 0025 PH H4 1 NY PMS 440 0025 PH

FID1 FID2 DNP FID3

PCB Number: TIDM-HAHSCTO
PCB Rev: A

PCB LOGO
Texas Instruments

PCB LOGO
Pb-Free Symbol

PCB LOGO
FCC disclaimer

Variant/Label Table	
Variant	Label Text
001	standard

LBL1
PCB Label
Size: 0.65" x 0.20"


ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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TID #: TIDM-HAHSCTO	Project Title: Test Board for TIDM-HAHSCTO		
Number: TIDM-HAHSCTO Rev: A	Sheet Title:		
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 3 of 3	
Drawn By:	File: TIDM-HAHSCTO-Test_Hw.SchDoc	Size: B	http://www.ti.com
Engineer: Anthony Seely	Contact: http://www.ti.com/support		

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