Layer Stack Up D			
Layor Nano	Gerber	Copper Thickness	Dielectric Naterial
Top Solder Mask	(.GTS)		Solder Resist
Top Layer	GIL	1.4mil	FR-4
MidLayerI	(.61)	1.4mil	FR-4
MidLayer2	(.62)	1.4mil	FR-4
Bottom Layer	(.GBL)	[.≁míl	18-4
Bottom Solder Mask	(.GBS)		Solder Resist



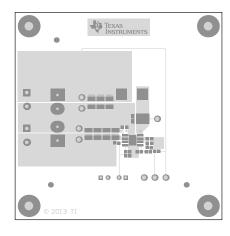
221 Binstall label in sikscreened box after final wash. Text shall be 8 pt font. Text shall be per Table I 222 BiThese assemblies are ESD sensitive, ESD precautions shall be observed. 223 BiThese assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable. 224 BiThese assemblies must comply with worksamping standards IPC-h-63D class 2., unless otherwise specified.

	H2	
LBLI		
PWR558 Rev.A		
		२१म-१३ १८-मर
J4 J3 TP8 TP7 TP6		
H3 © 2013 TI	н	

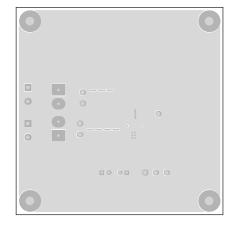
TABLE 1		
Variant	Label text	
Standard Assembly	TPS54540EVH-558	

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED, AND MAY NOT BE IN BILL OF MATERIALS ASSEMBLY VARIANT: [No Variations]

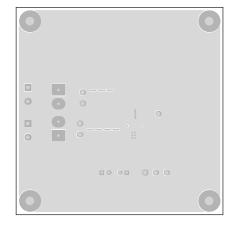
PCB VIEWED FROM TOP SIDE	BOARD #: PWR558	REV: A	SVN REV:	: Not In VersionControl
IGNORE -> MopBowedtaytline				
PLOT NAME = Top Overlay	GENERATED : 6/3/20	13 1:11:21	PM	TEXAS INSTRUMENTS



Top Solder

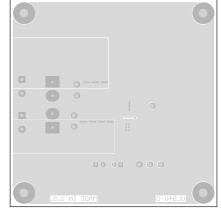


M1 Board Outline



M1 Board Outline

Bottom Layer



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