Technical Article How a DC/DC Converter Package and Pinout Design Can Enhance Automotive EMI Performance



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It is well known that printed circuit board (PCB) layout is pivotal to help reduce electromagnetic interference (EMI) from DC/DC buck or boost converters. This is critical for automotive applications that require ultra-low EMI, such as automotive gateway modules and radar sensing systems.

The schematic of Figure 1 illustrates two critical loops for a synchronous buck converter circuit. Minimizing the power loop area in the layout is essential because of its proportionality to parasitic inductance and related H-field propagation.

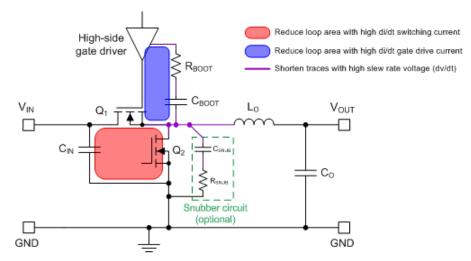


Figure 1. Simplified Synchronous Buck Converter Schematic with Critical Loops and Traces Identified for EMI

Also important is the boot capacitor loop shown in Figure 1. An optional series boot resistor, designated R_{BOOT} , controls the turn-on speed of the high-side MOSFET. The boot resistor slows the gate drive current profile and thus reduces the SW voltage and current slew rates during MOSFET turn-on. Another option is an RC snubber from SW to GND. Of course, snubbers and gate resistors increase power dissipation, leading to a trade-off between EMI and efficiency. Other techniques are required to mitigate EMI, given that efficiency and thermal performance are also important.

DC/DC Converter Package and Pinout Design

Figure 2 provides the schematic of a 60-V synchronous buck converter with both pinout and package optimized for EMI performance when operating in high-performance automotive applications such as body electronics and ADAS. The schematic highlights the high-current traces (VIN, PGND, SW connections), noise-sensitive nets (FB) and high *dv/dt* circuit nodes (SW, BOOT).

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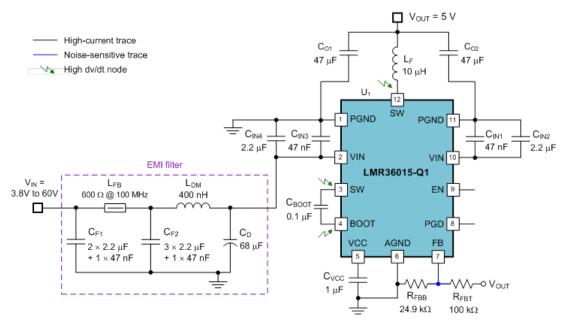


Figure 2. DC/DC Converter with EMI-optimized Package and Pinout. Included Is a Two-stage EMI Input Filter

1. Pinout

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The converter IC in Figure 2 has the benefit of a symmetrical and balanced pin arrangement for VIN and PGND. It uses two input loops in parallel that result in effectively half the parasitic loop inductance. These loops are labeled IN1 and IN2 in the PCB layout diagram shown in Figure 3. Two capacitors with small 0402 or 0603 case size, designated as C_{IN1} and C_{IN3} , are placed as close as possible to the IC to configure minimum input loop areas. The circulating currents create opposing magnetic moments that result in H-field cancellation and hence lower effective inductance. To further reduce parasitic inductance, a continuous ground plane for return current underneath the IN1 and IN2 loops on layer 2 of the PCB – immediately below the top layer power circuit – supports a field self-cancellation effect.

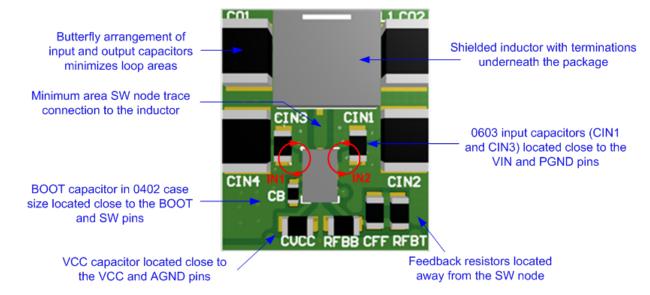


Figure 3. Power Stage Layout Routed Only on the Top Layer of the PCB



The output current loops are similarly optimized as well by using two ceramic output caps, C_{O1} and C_{O2} , one on each side of the inductor. Having two parallel ground return paths from the output splits the return current in two, helping to mitigate output noise and ground bounce effect.

The SW pin in located at the center of the IC such that the radiated e-field is shielded by adjacent VIN and PGND pins on both sides of the IC. GND plane copper shields the polygon pour connecting the IC's SW pin to the inductor terminal. The single-layer SW and BOOT layout implies that vias with high *dv/dt* do not appear on the bottom side of the PCB. This avoids e-field coupling to the reference ground plane during the EMI test.

2. Package

In tandem with optimized pinout, DC/DC converter IC package design is a key attribute in the quest to improve EMI signature. As an example, HotRodÔ package technology from TI uses a flipped-chip-on-leadframe (FCOL) technique that eliminates power device wire bonds that might otherwise result in higher package parasitic inductance. The IC is flipped upside down and copper posts on the IC are soldered directly to the leadframe. This construction method enables small solution size and low profile as each pin is attached directly to the leadframe. Most relevant from an EMI perspective, the HotRod package lowers package parasitic inductance versus traditional wire-bond packages, resulting in much lower noise and ringing during the switching transitions.

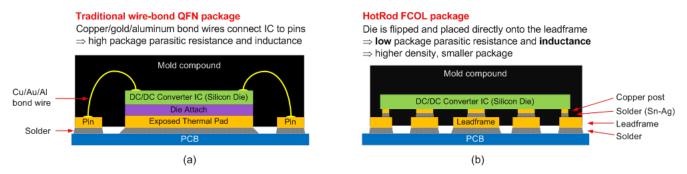




Figure 5 shows the conducted emissions measured from 150kHz to 108MHz for the circuit in Figure 3. The results are in compliance with EN 55025 Class 5 requirements for automotive, even without a CM choke, snubbers or metal case shielding.

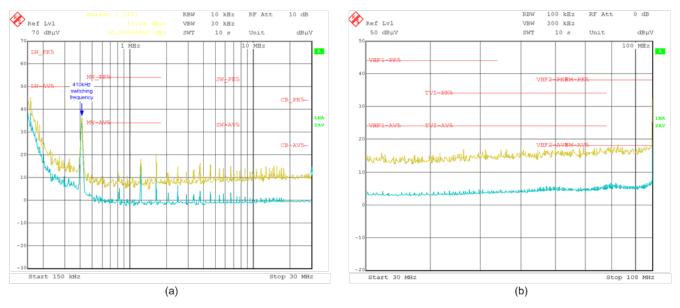


Figure 5. Conducted Emissions Results Meeting EN 550525 Class 5 Limits: 150kHz to 30MHz – Includes LW, MW, SW and CB Bands (a); 30MHz to 108MHz – Includes VHF, TV and FM Bands (b)

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Summary

New generations of power converters show significantly improved performance in terms of advanced packaging and pinout design. Converter package type is an important selection criterion for EMI mitigation, particularly as it enables lower parasitic inductance and thus minimal SW voltage ringing. Furthermore, a carefully-designed pinout leads to a better PCB layout with optimized input capacitor placement. Ultimately, the required EMI filter has a smaller footprint and lower total cost – key attributes in automotive ADAS and body applications.

Additional Resources

- Read the TI E2ETM Behind the Wheel blog, "There are more ways than you think to reduce conducted EMI."
- Take the EMI training webinar, "Reduce EMI and shrink solution size with HotRod packaging."
- Examine these reference designs from the TI Designs library:
 - Automotive Stand-alone Gateway Reference Design with Ethernet and CAN.
 - Automotive 77GHz Radar Module Reference Design with Object Data Output.
 - Two-stage Power Supply Reference Design for Field Transmitters.
- Download these white papers:
 - "An overview of conducted EMI specifications for power supplies."
 - "Simplify low EMI design with power modules."
- Order the evaluation modules for the LMR36015-Q1, LMR33630-Q1 and LM53635-Q1 family of HotRod converters.

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