

K2G AUDIO DAUGHTER CARD

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REV	B
VER	1.2

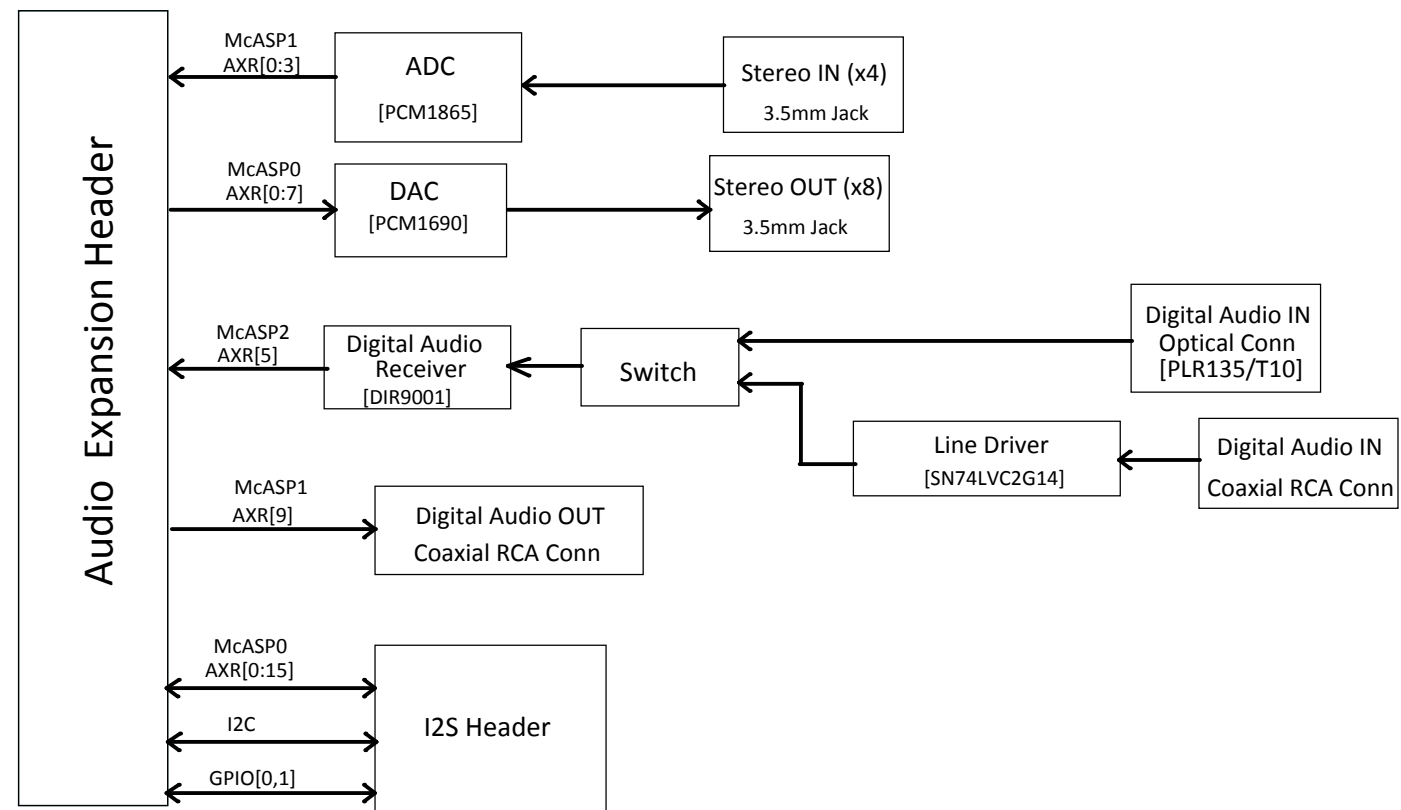
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VERSION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR
0.1	28st JUL 2015	INITIAL DRAFT	MISTRAL DESIGN TEAM
1.0	13th AUG 2015	BASELINED SCHEMATICS	MISTRAL DESIGN TEAM
1.1	16th SEP 2015	CUSTOMER COMMENTS UPDATED	MISTRAL DESIGN TEAM
1.2	21st SEP 2015	BASELINED SCHEMATICS FOR BETA	MISTRAL DESIGN TEAM

Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title REVISION HISTORY	
AUD K2G	 	Size C	Document Number MS_TI_AUDK2G_SCH_REVB
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BLOCK DIAGRAM



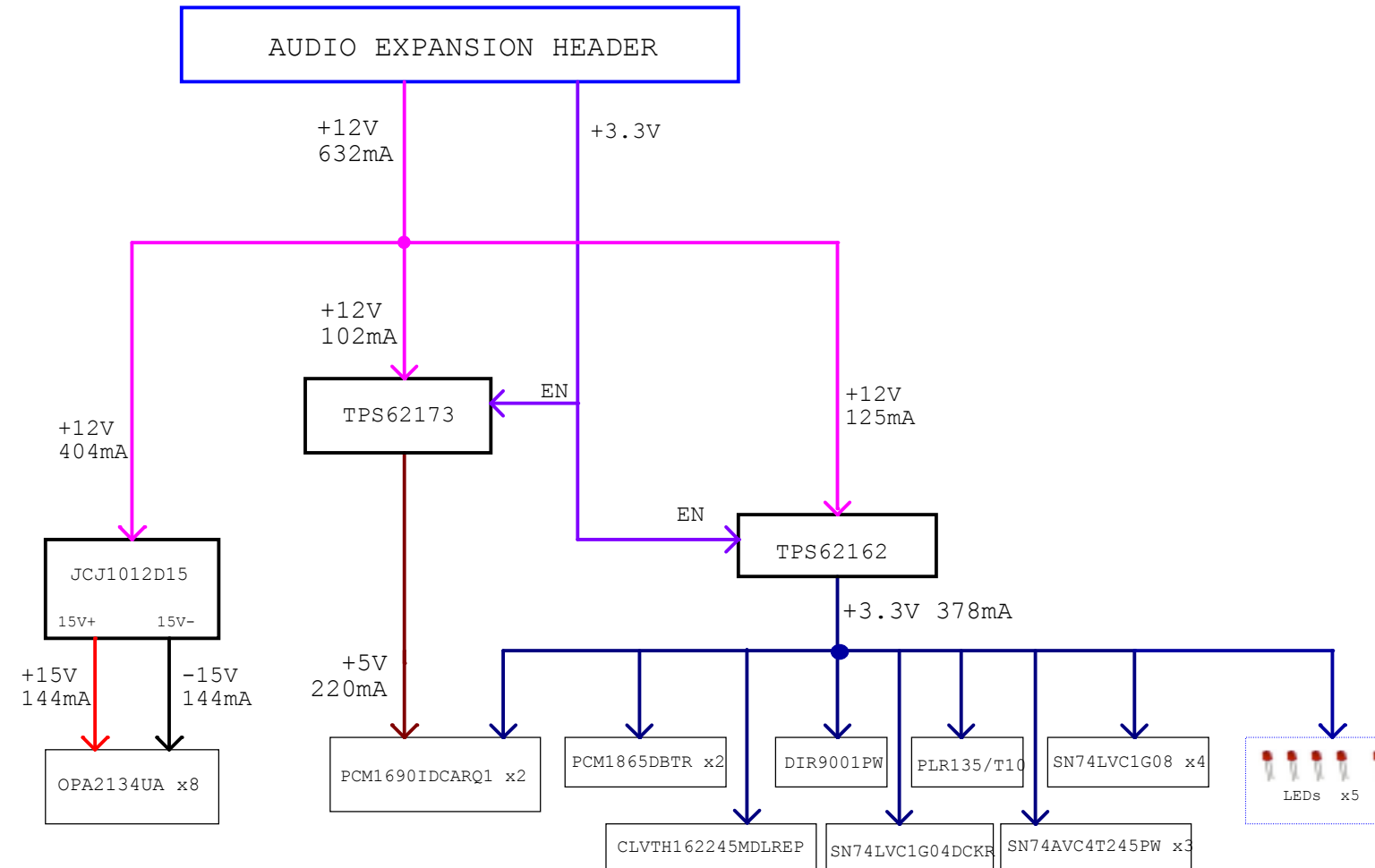
I2C Device Address

I2C Device	Address	
PCM1865DBTR	ADC1	0x4A
PCM1865DBTR	ADC2	0x4B
PCM1690IDCARQ2	DAC0	0x4D
PCM1690IDCARQ1	DAC1	0x4C

McASP CONFIGURATION

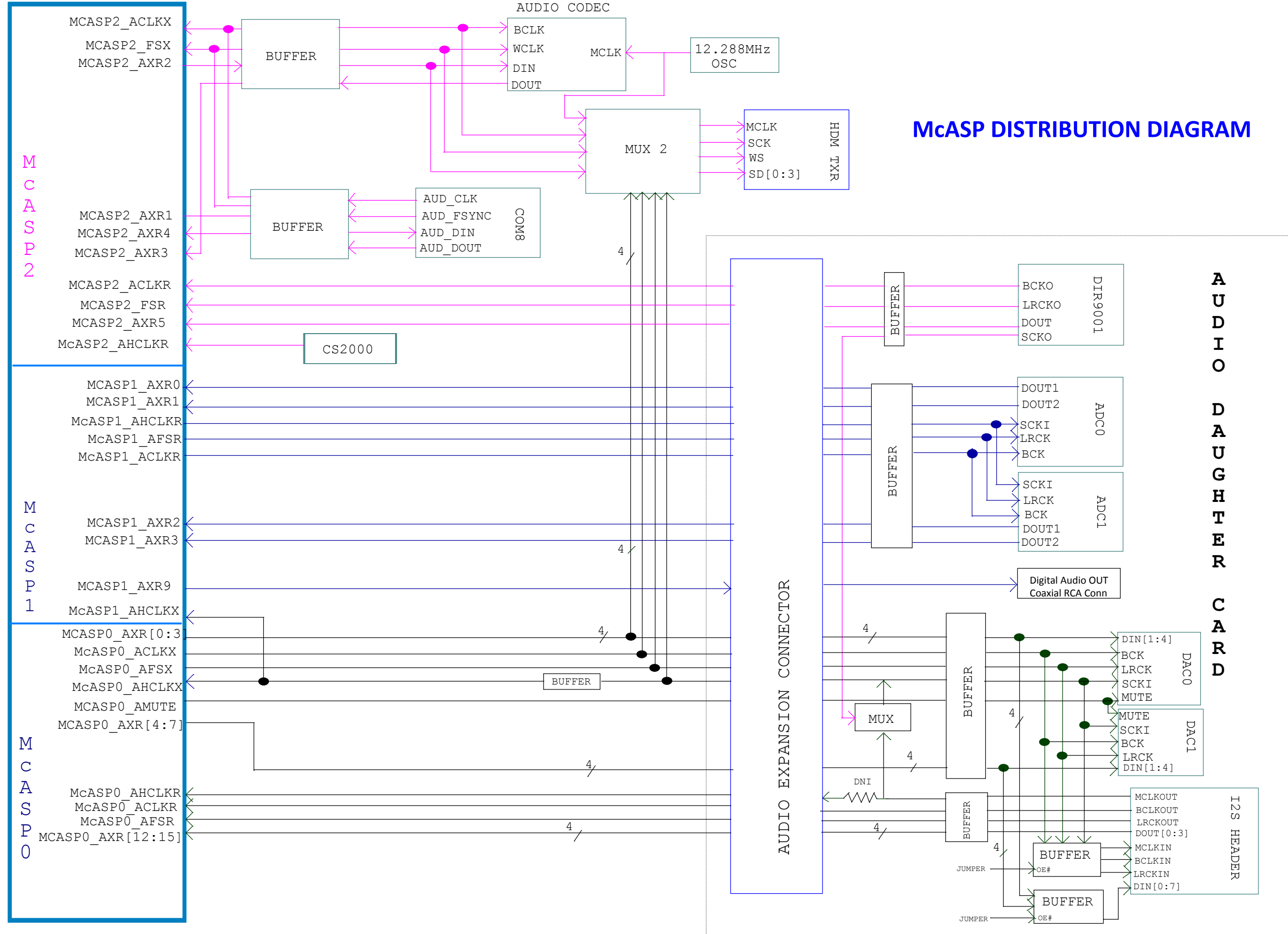
McASP PORT	DEVICES	DEVICE MODE
McASP0	DAC- PCM1690 x2	SLAVE
	I2S HEADER	MASTER
McASP1	ADC- PCM1865 x2	SLAVE
McASP2	HDMI TRANSMITTER (DEFAULT)	SLAVE
	AUDIO CODEC AIC3106	
	DIR9001 (DEFAULT)	MASTER
COM8		

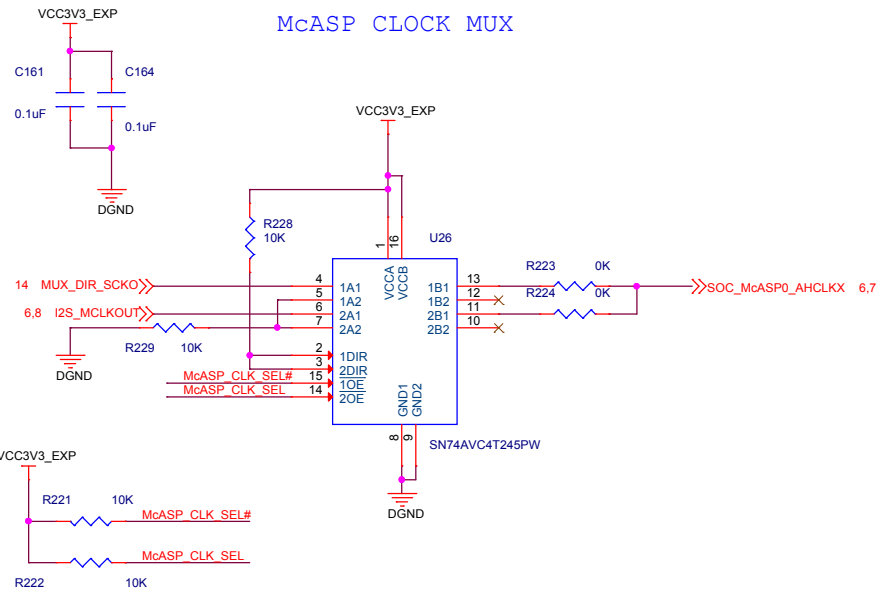
POWER FLOW DIAGRAM



Project :	Designed for TI by Mistral Solutions Pvt Ltd	Title POWER FLOW DIAGRAM	
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McASP DISTRIBUTION DIAGRAM





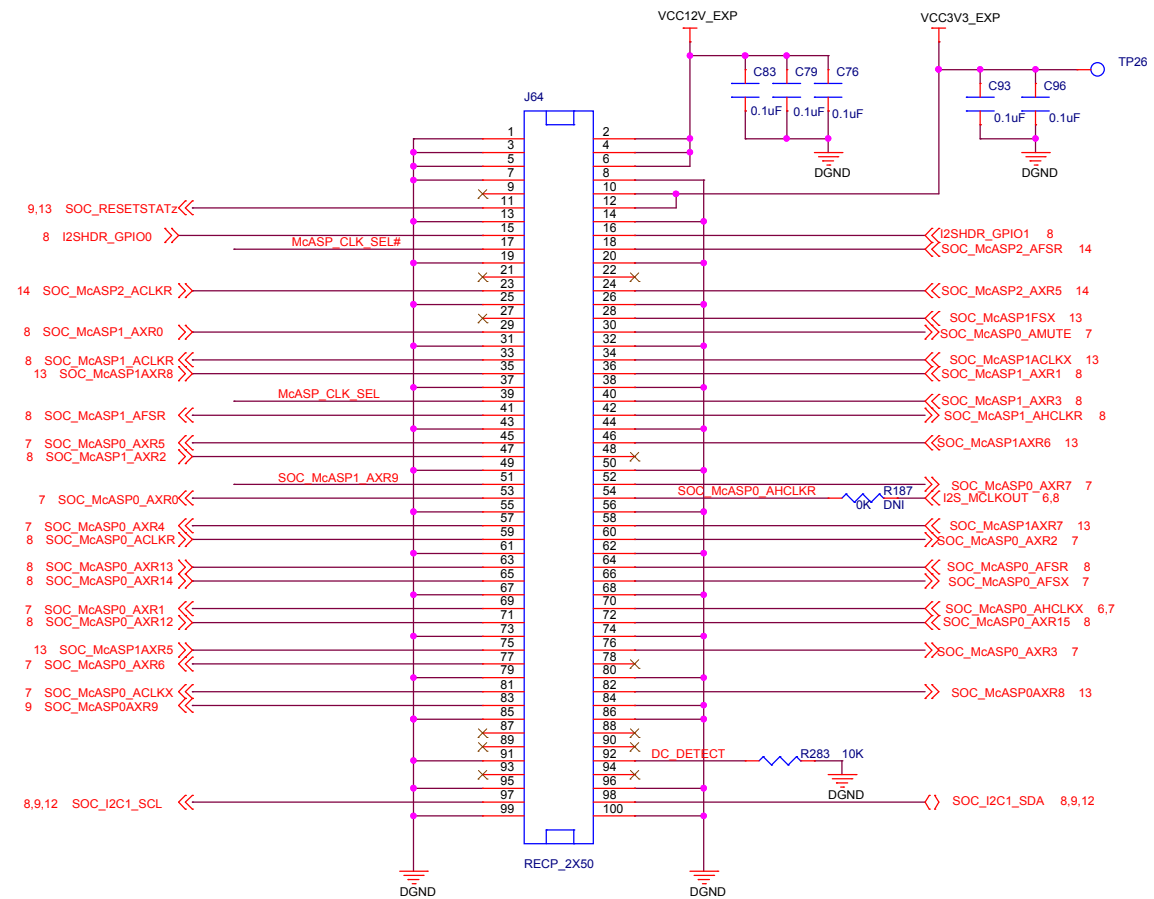
McASP CLOCK SELECTION

McASP_CLK_SEL#	McASP_CLK_SEL	SOC_McASP0_AHCLKX
H	L	I2S
L	H	DIR

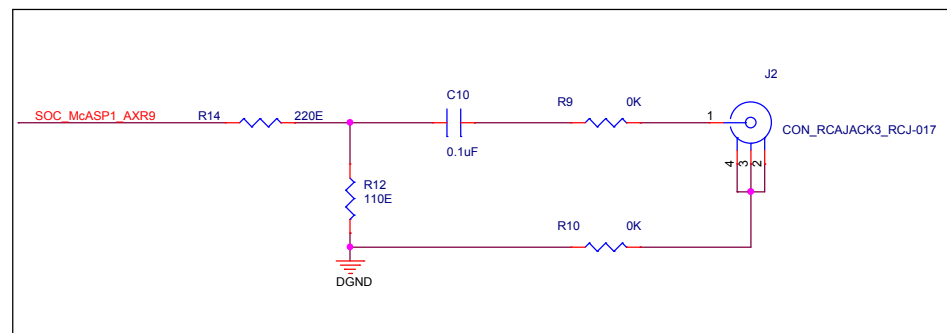
Note:
For SoC-generated AHCLKX0, set MUX to I2S mode and disconnect any I2S source connected to the I2S header.

GPIOs ON AUDIO_CARD	SOC SIGNAL
McASP_CLK_SEL	SOC_McASP1AXR4/GPIO0_132
PCM1690_RST#	SOC_McASP0AXR9/GPIO1_10
DAC0_AMUTEI#	SOC_McASP0_AMUTE
DAC1_AMUTEI#	SOC_McASP0_AMUTE
DIR_RST#	SOC_McASP0AXR8/GPIO1_09
DIR_AUDIO#	SOC_McASP1AXR6/GPIO0_134
DIR_EMPH	SOC_McASP1AXR7/GPIO0_135
DIR_ERROR	SOC_McASP1AXR8/GPIO0_136
DIR_CLKST	SOC_McASP1AXR5/GPIO0_133
DIR_FSOUT0	SOC_McASP1ACLKX/GPIO0_124
DIR_FSOUT1	SOC_McASP1FSX /GPIO0_125
McASP_CLK_SEL#	SOC_SPI2_SCS0 /GPIO0_101
DC_DETECT	GFMCBE1N/GPIO0_21
I2SHDR_GPIO0	SOC_SPI2_MOSI
I2SHDR_GPIO1	SOC_SPI2_MISO

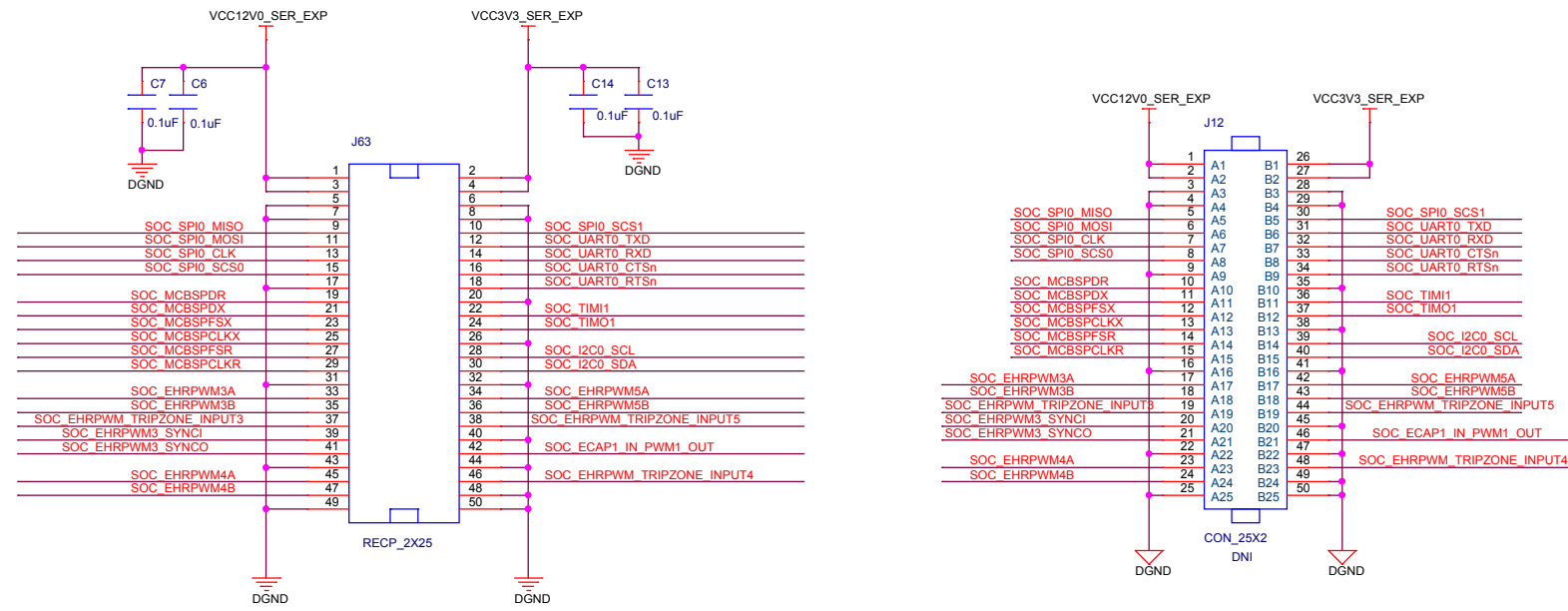
AUDIO EXPANSION CONN



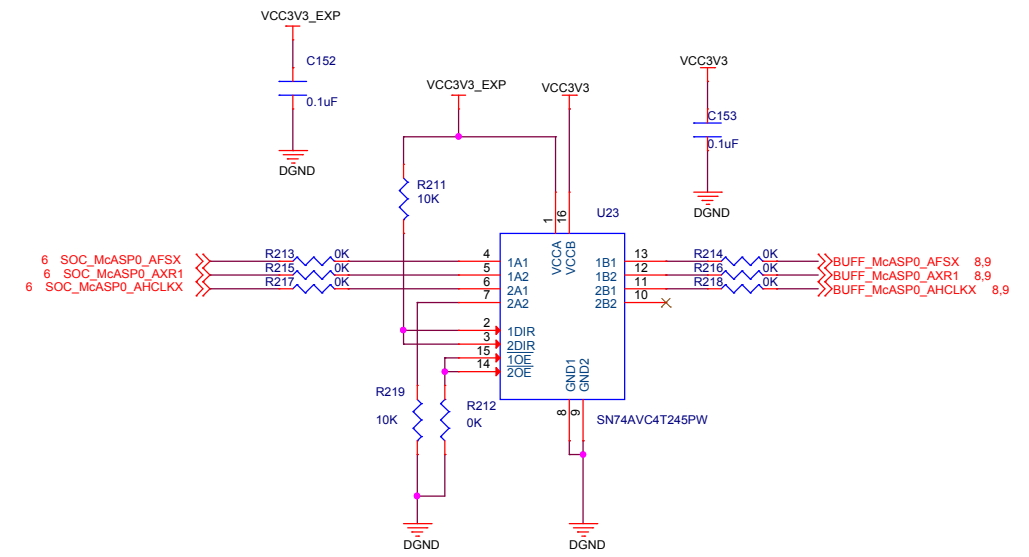
DIT



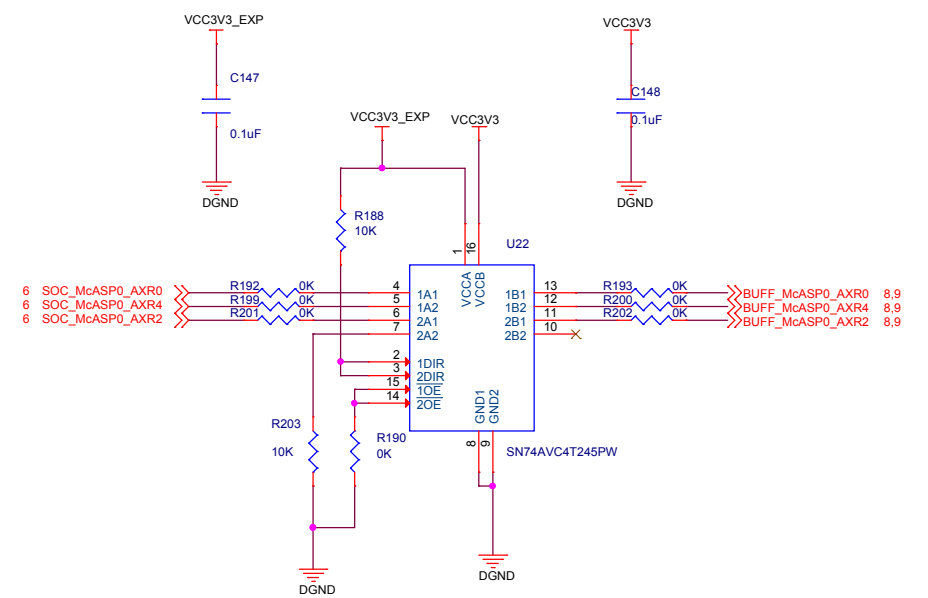
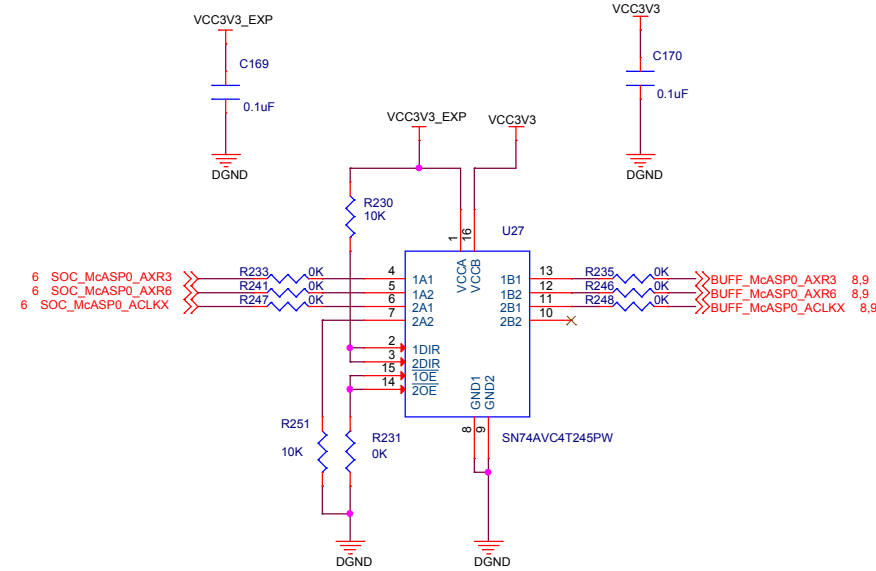
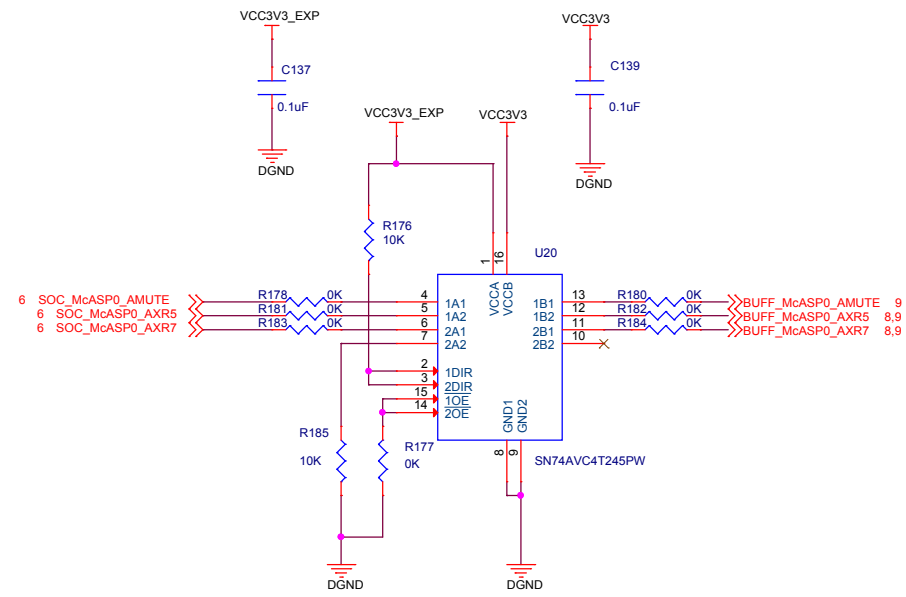
SERIAL EXPANSION CONN



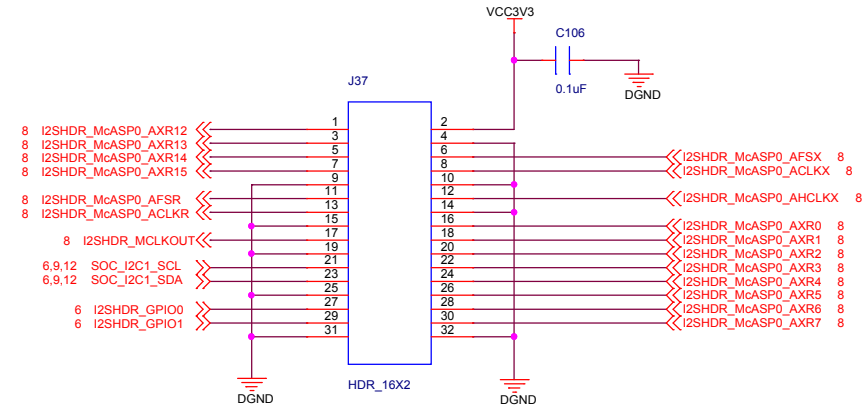
DAC CLOCK AND DATA BUFFER



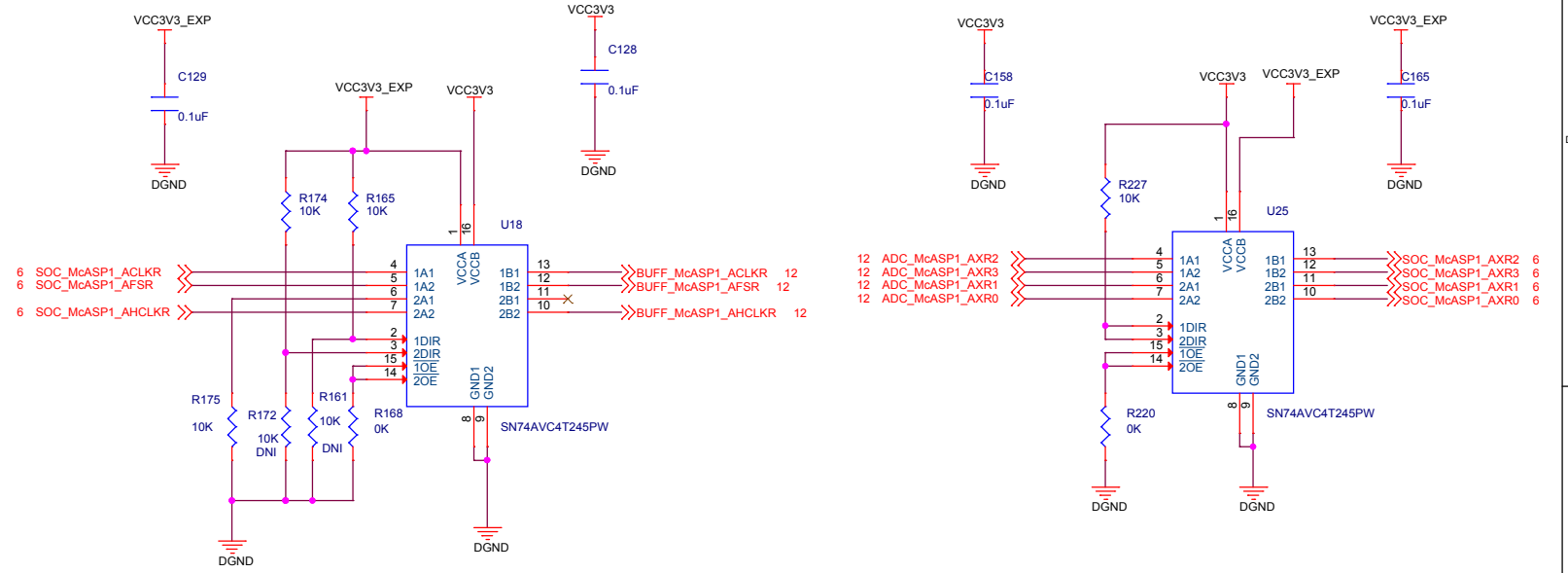
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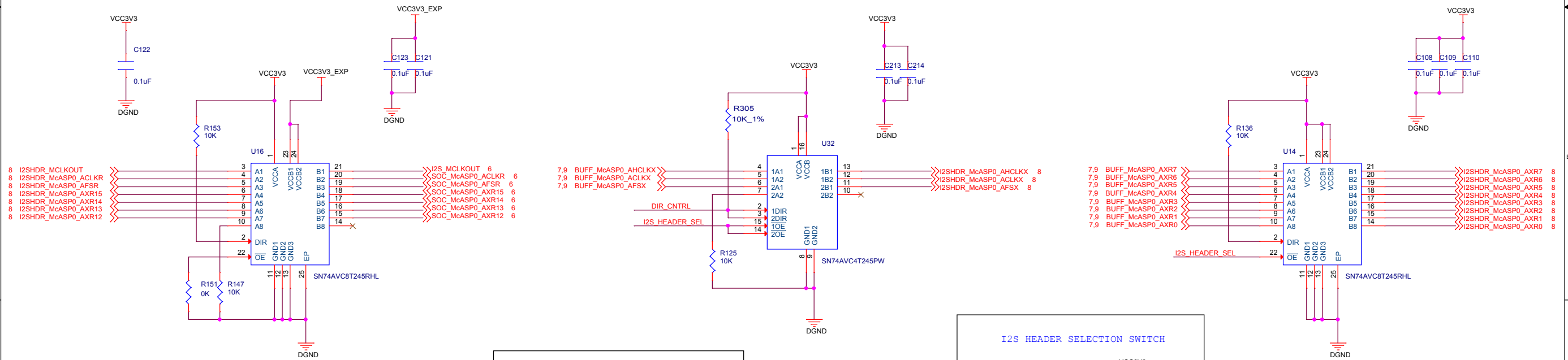
I2S HEADER



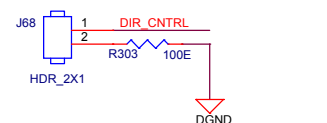
ADC CLOCK & DATA BUFFER



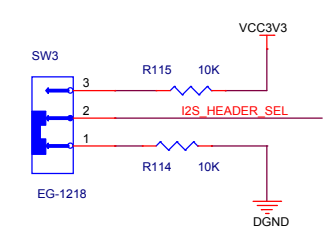
I2S CLOCK AND DATA BUFFER



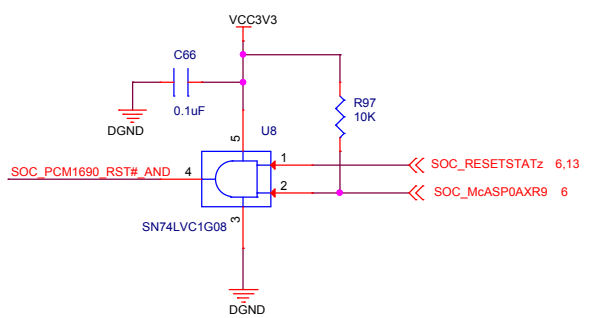
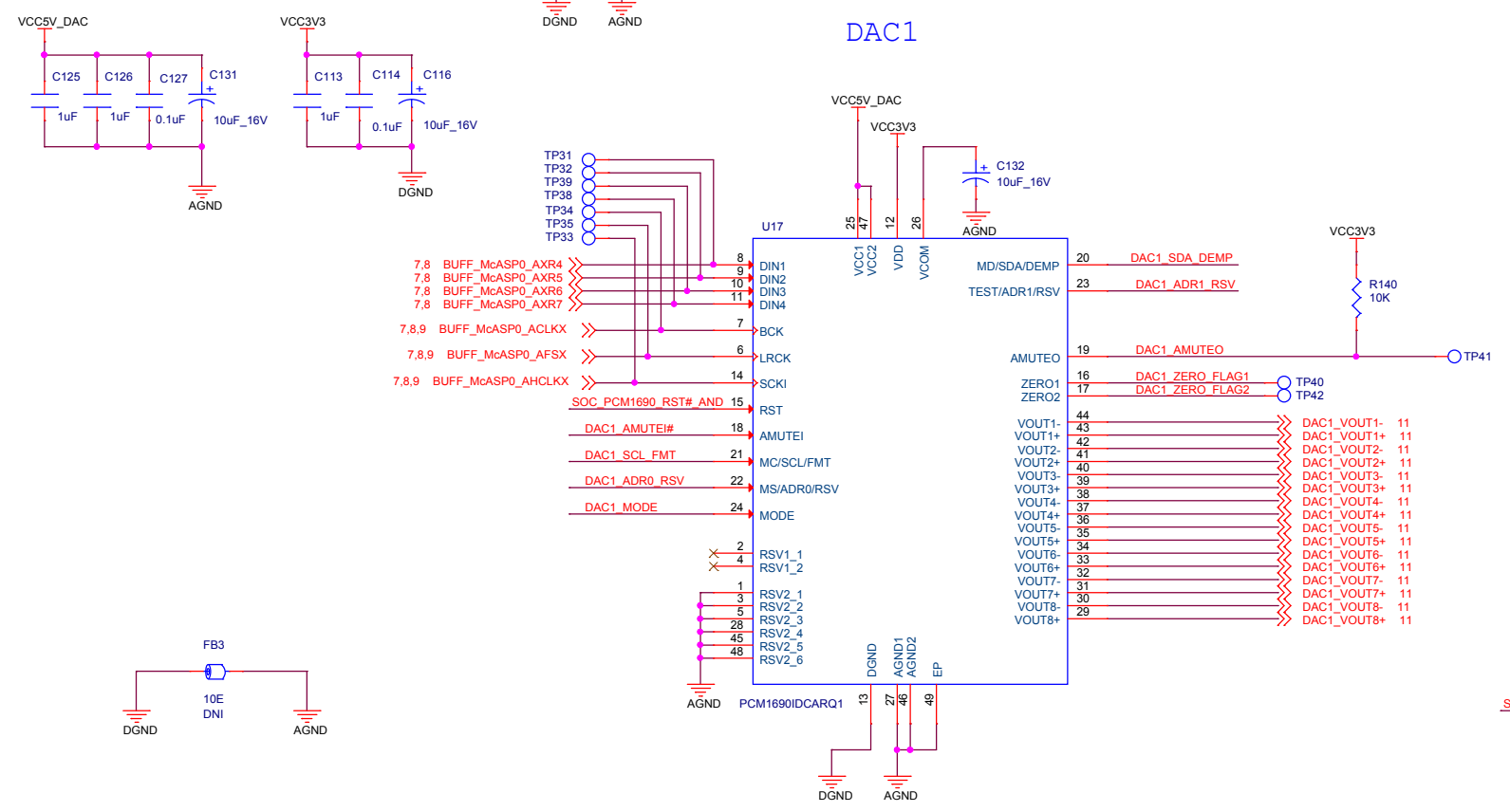
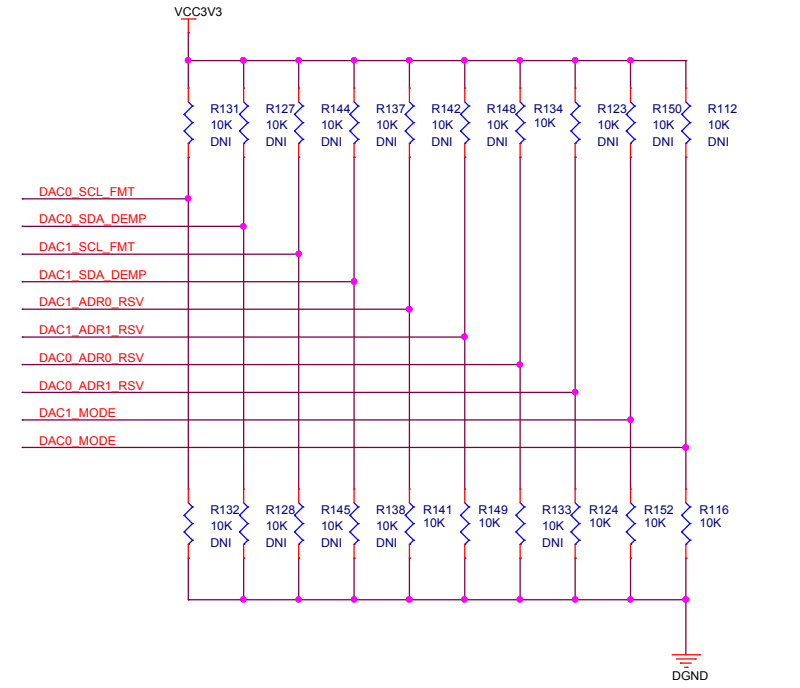
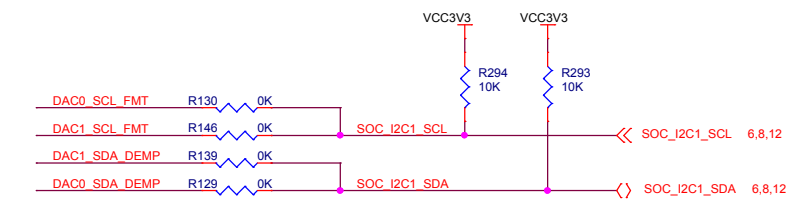
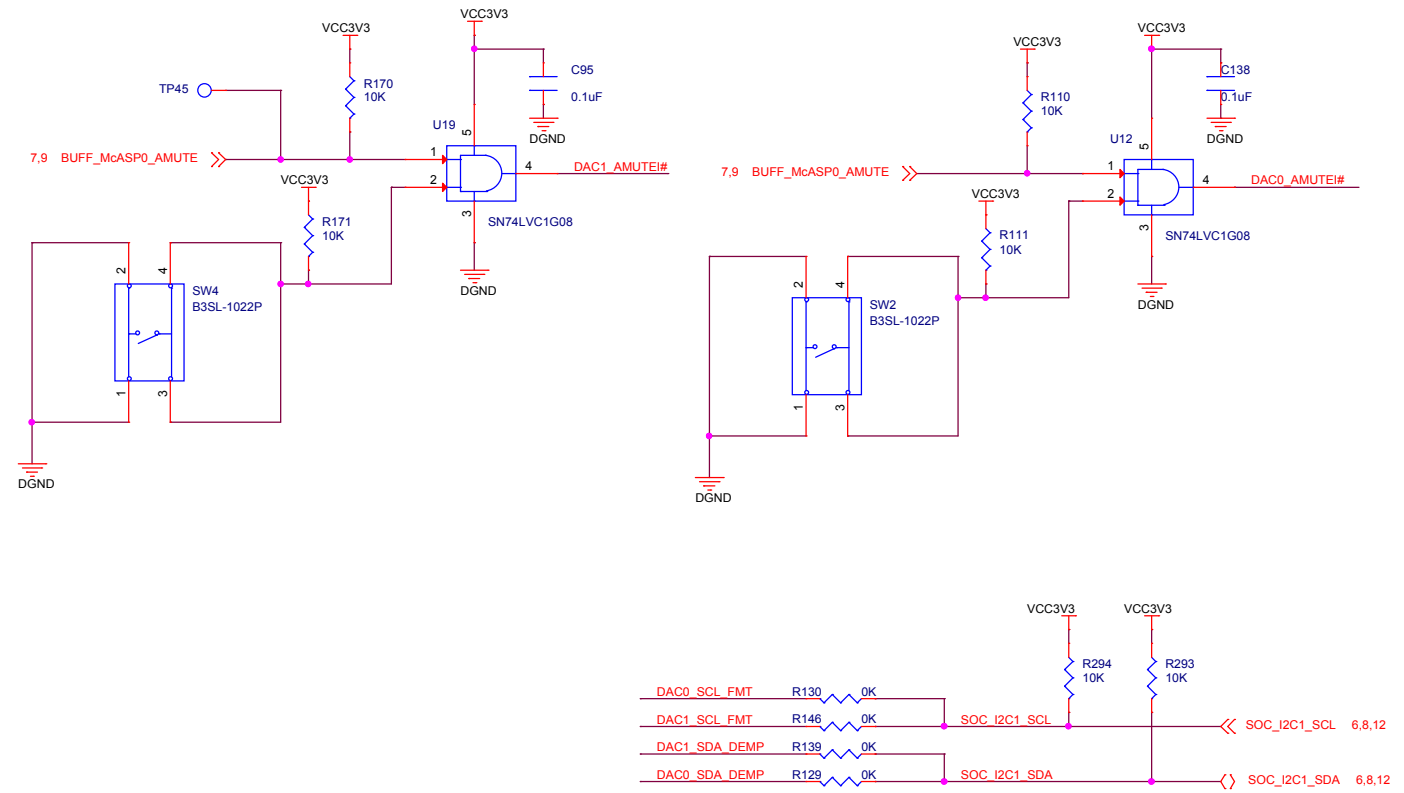
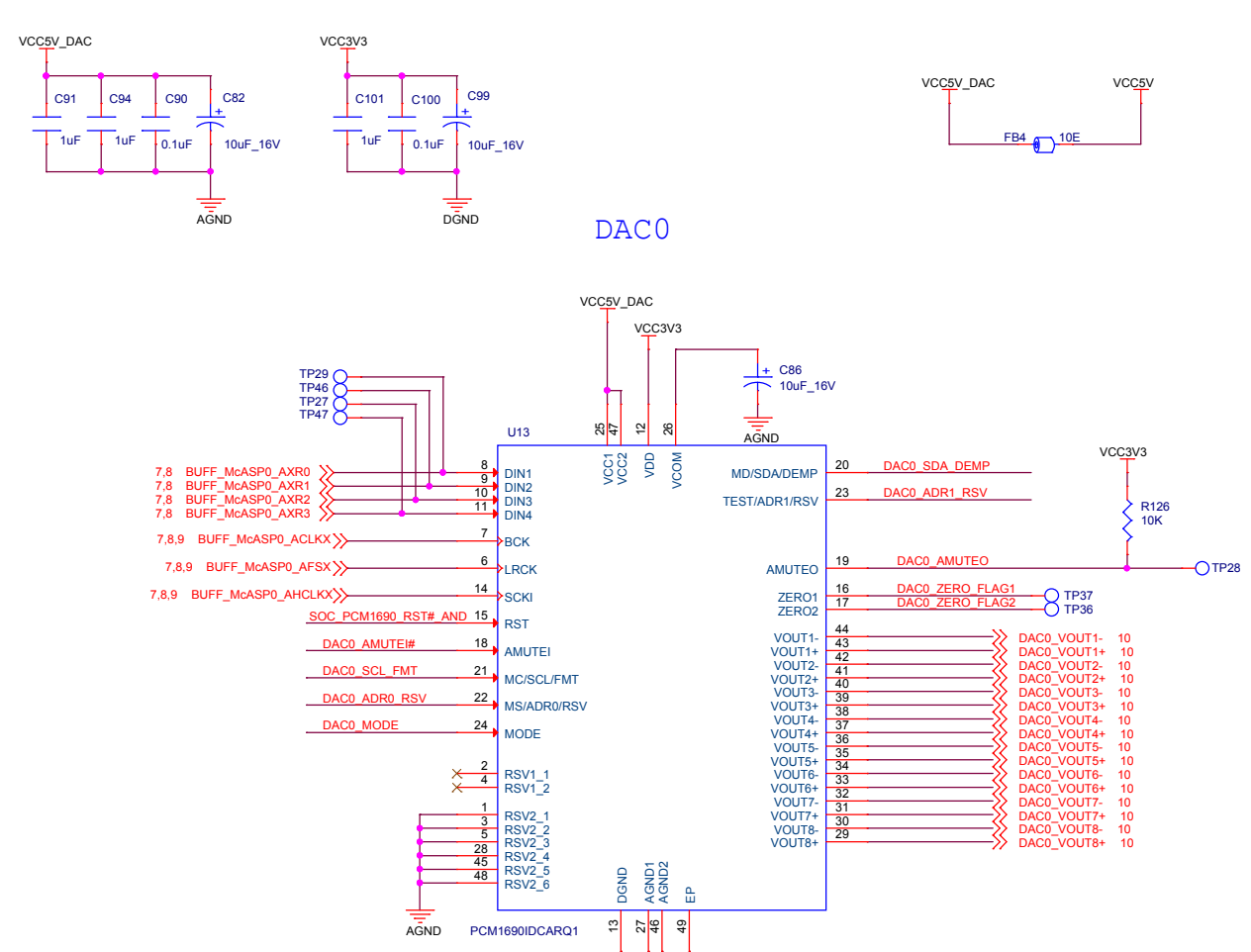
INSTALL JUMPER FOR TX SLAVE MODE



I2S HEADER SELECTION SWITCH

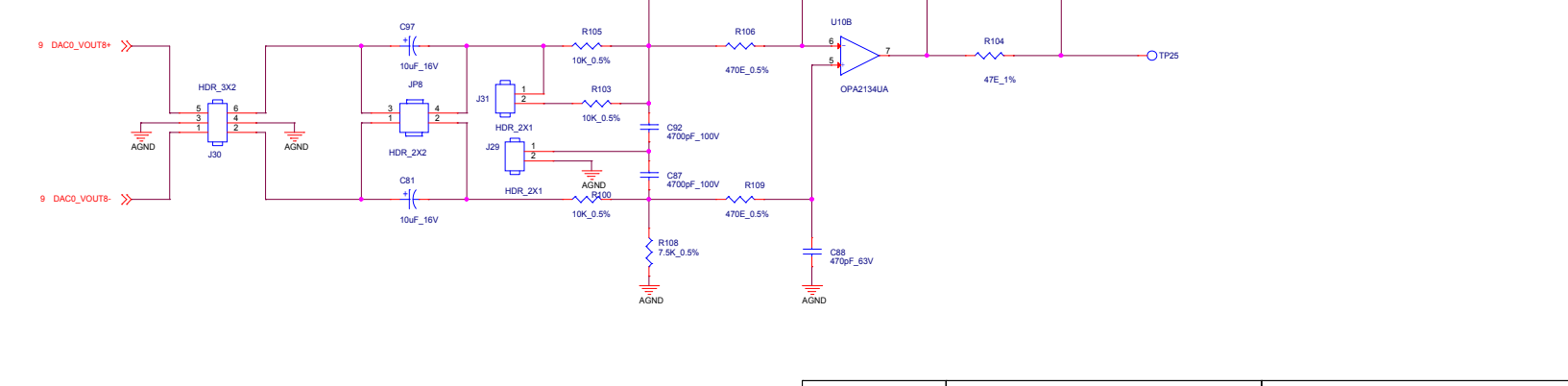
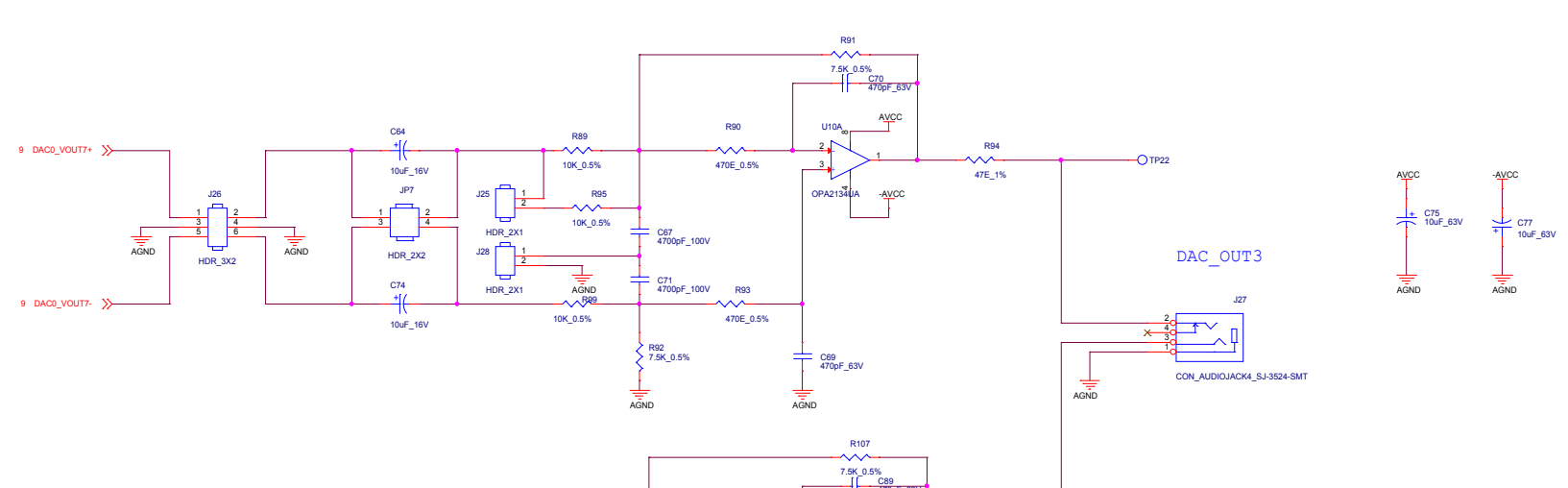
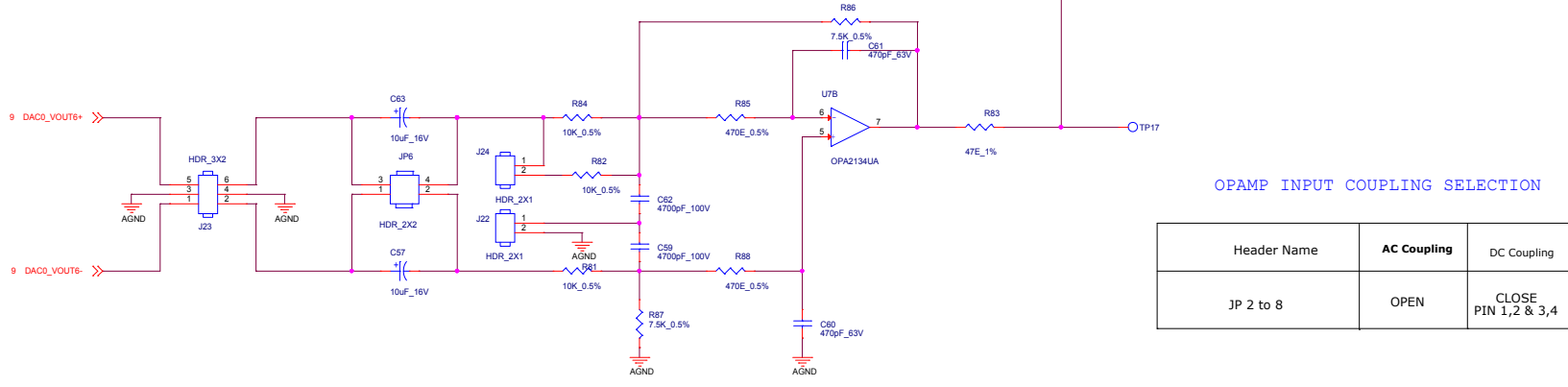
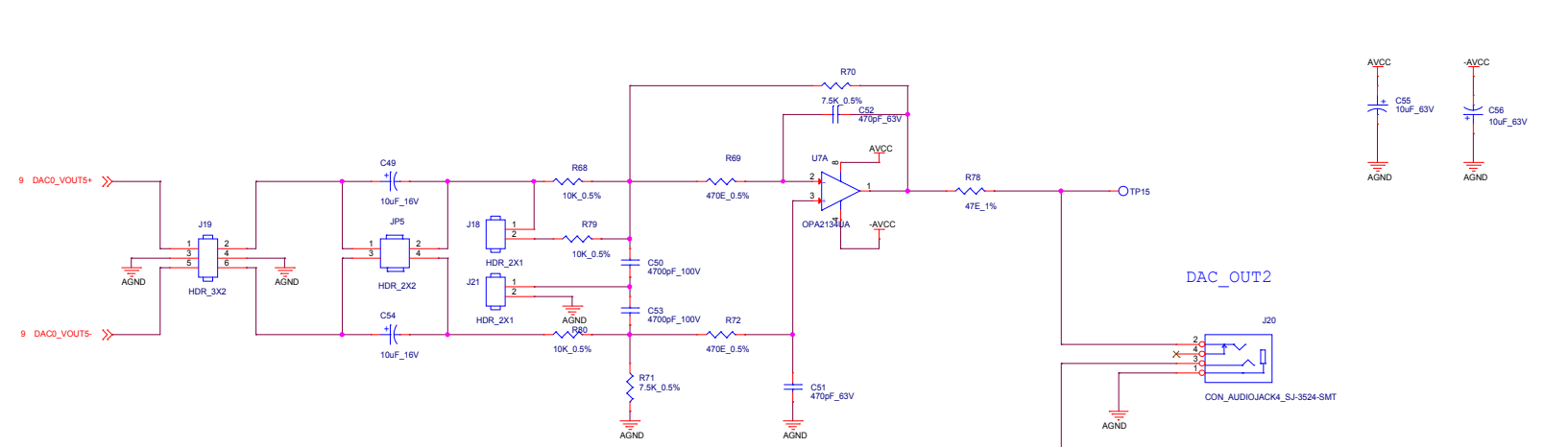
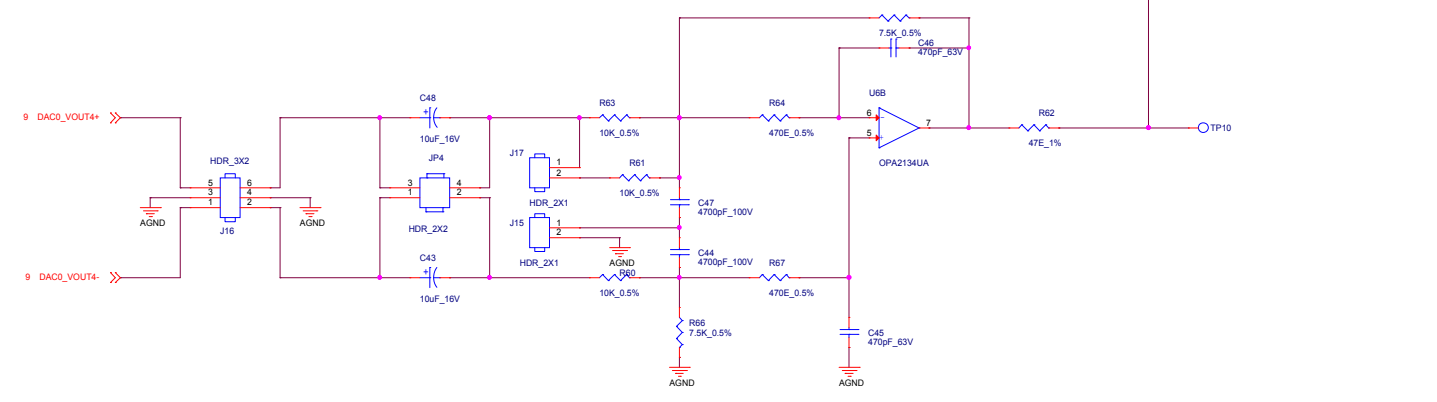
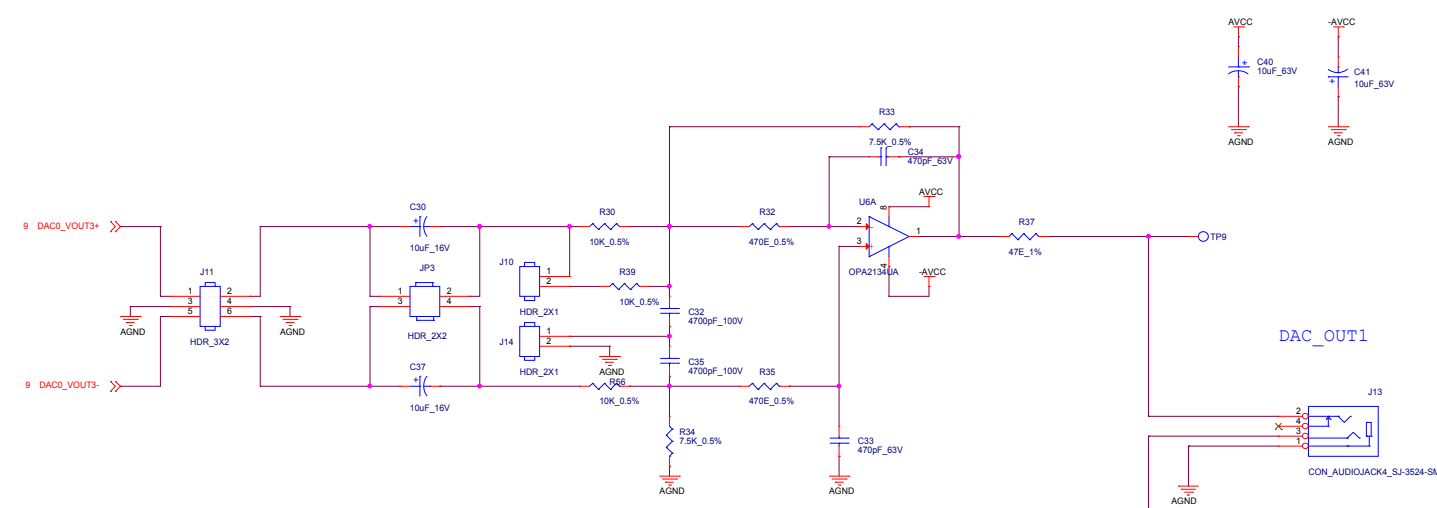
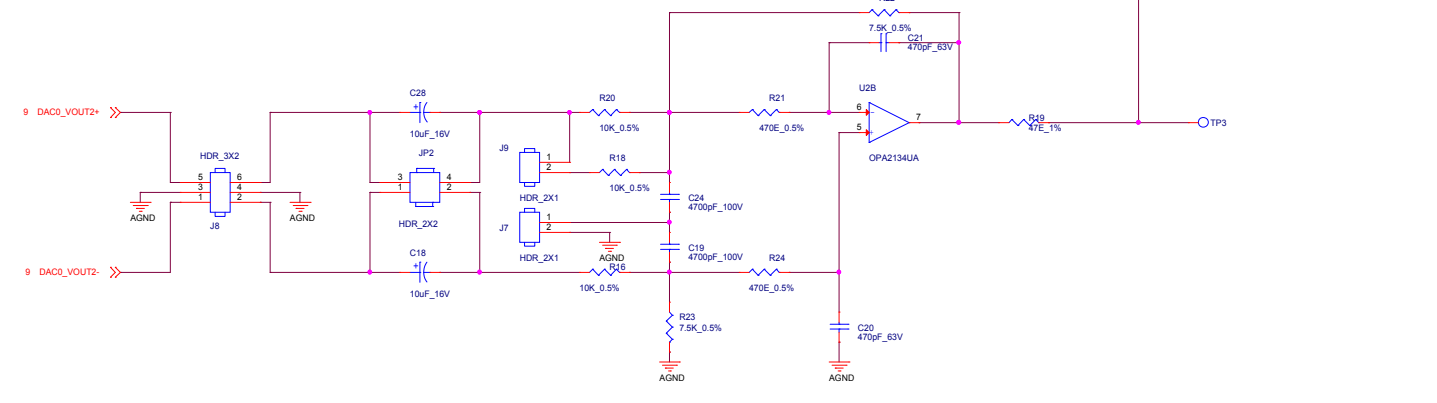
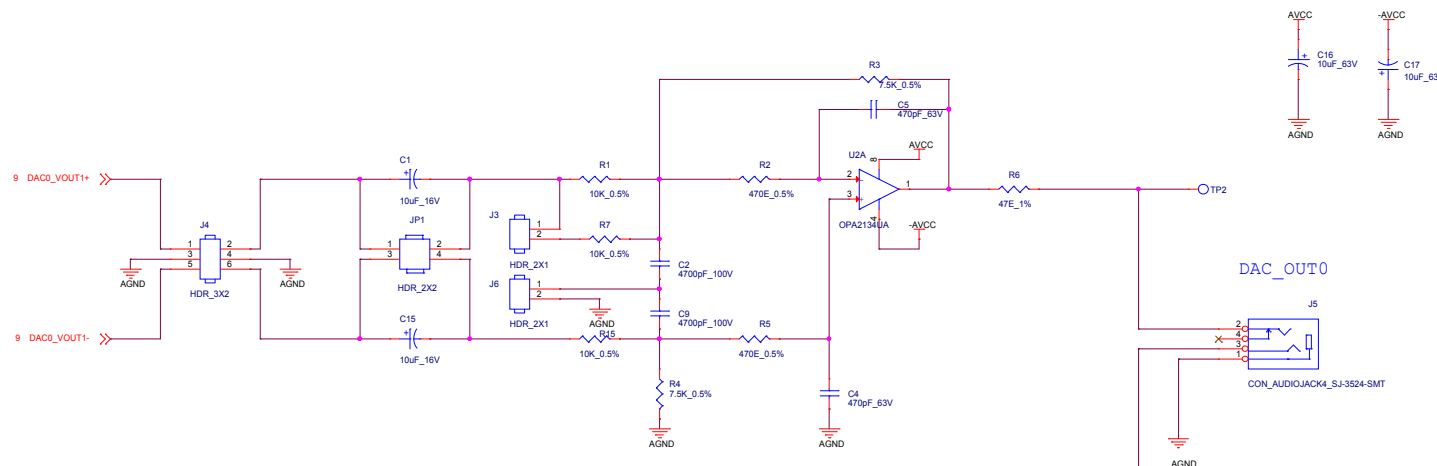


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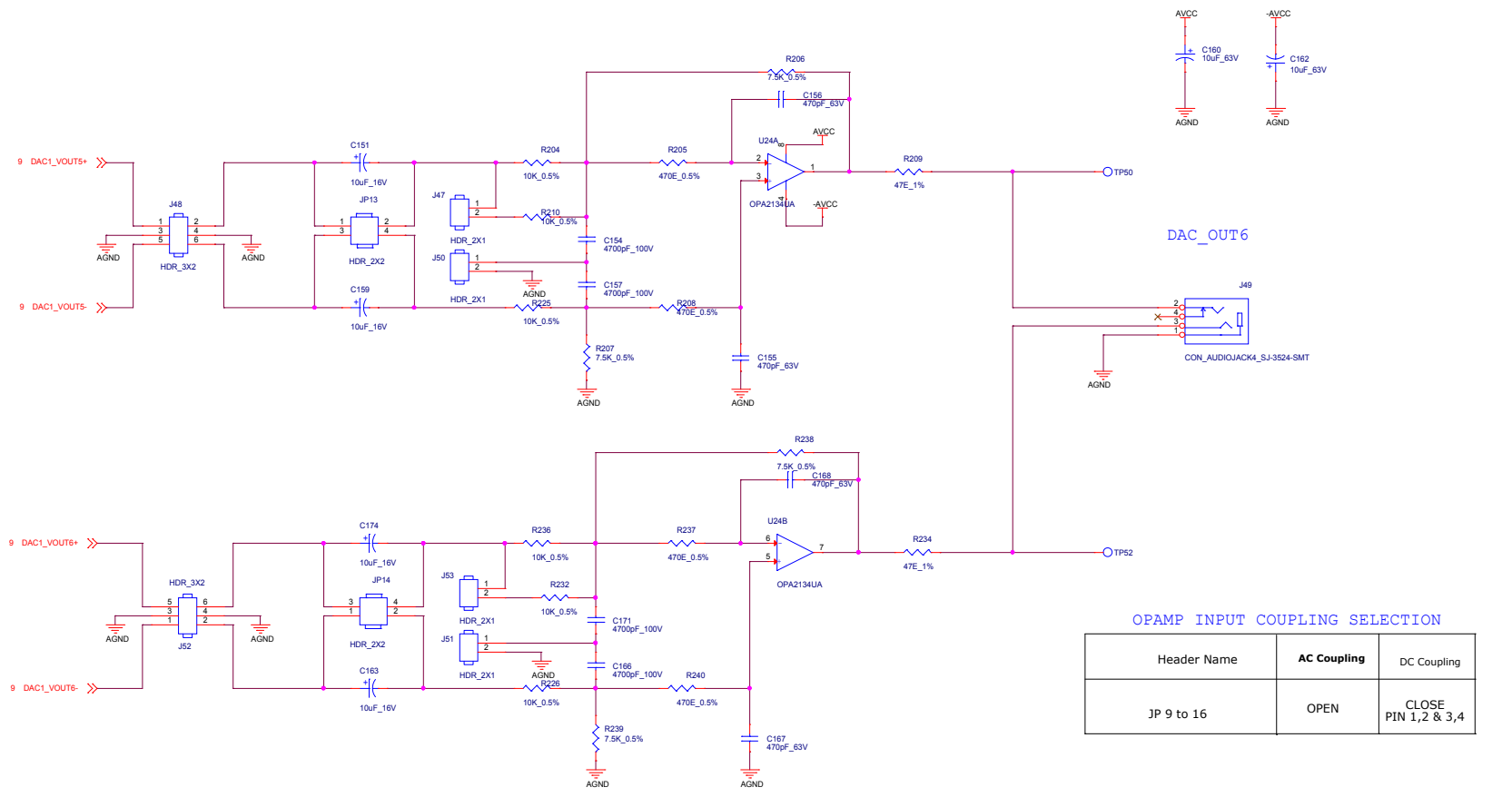
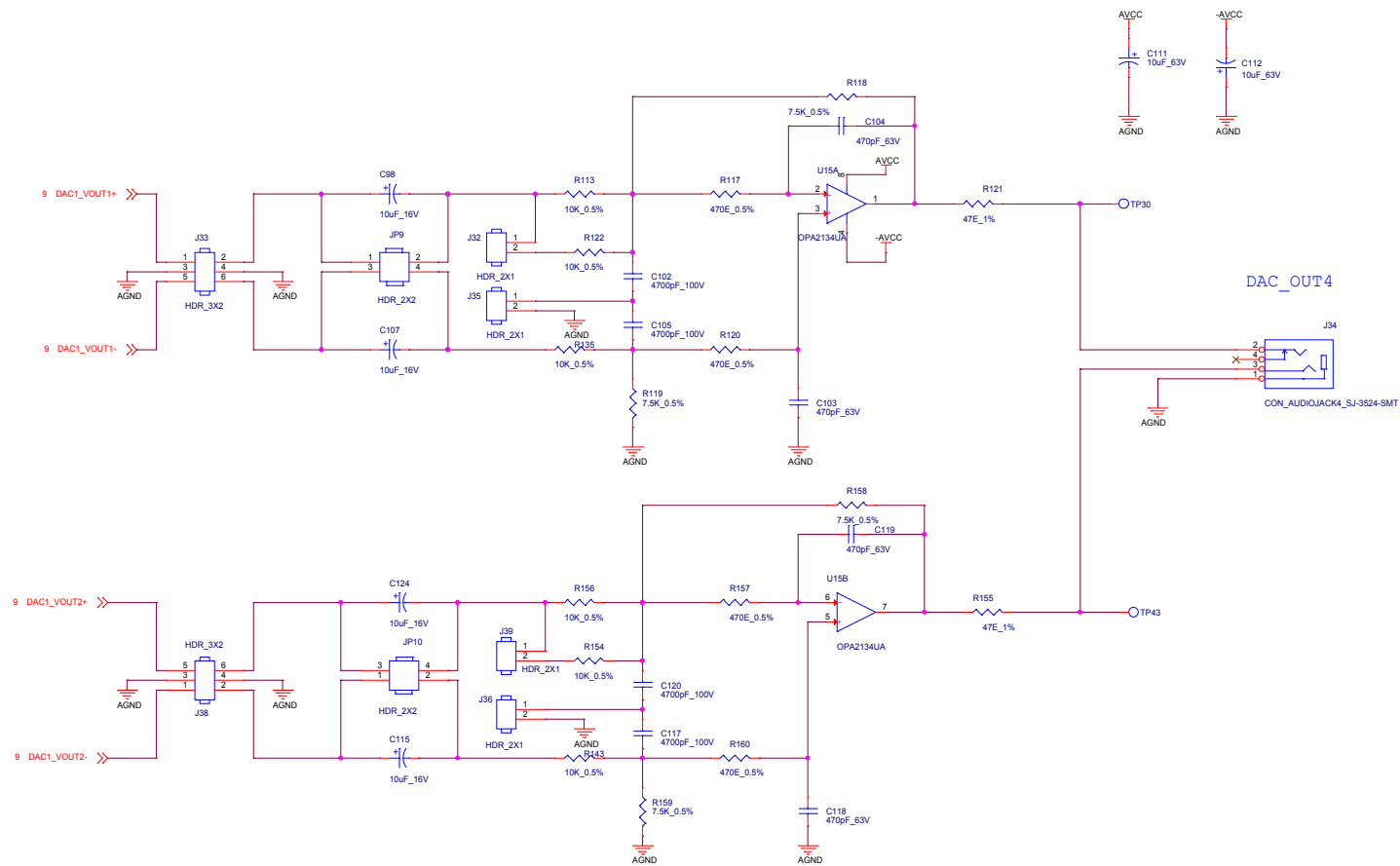
DAC MODE SELECTION

DACx_MODE	Control Port Mode Selection
Tied to DGND	I2C
Left Open	Hardware Mode
Tied to VCC3V3	SPI



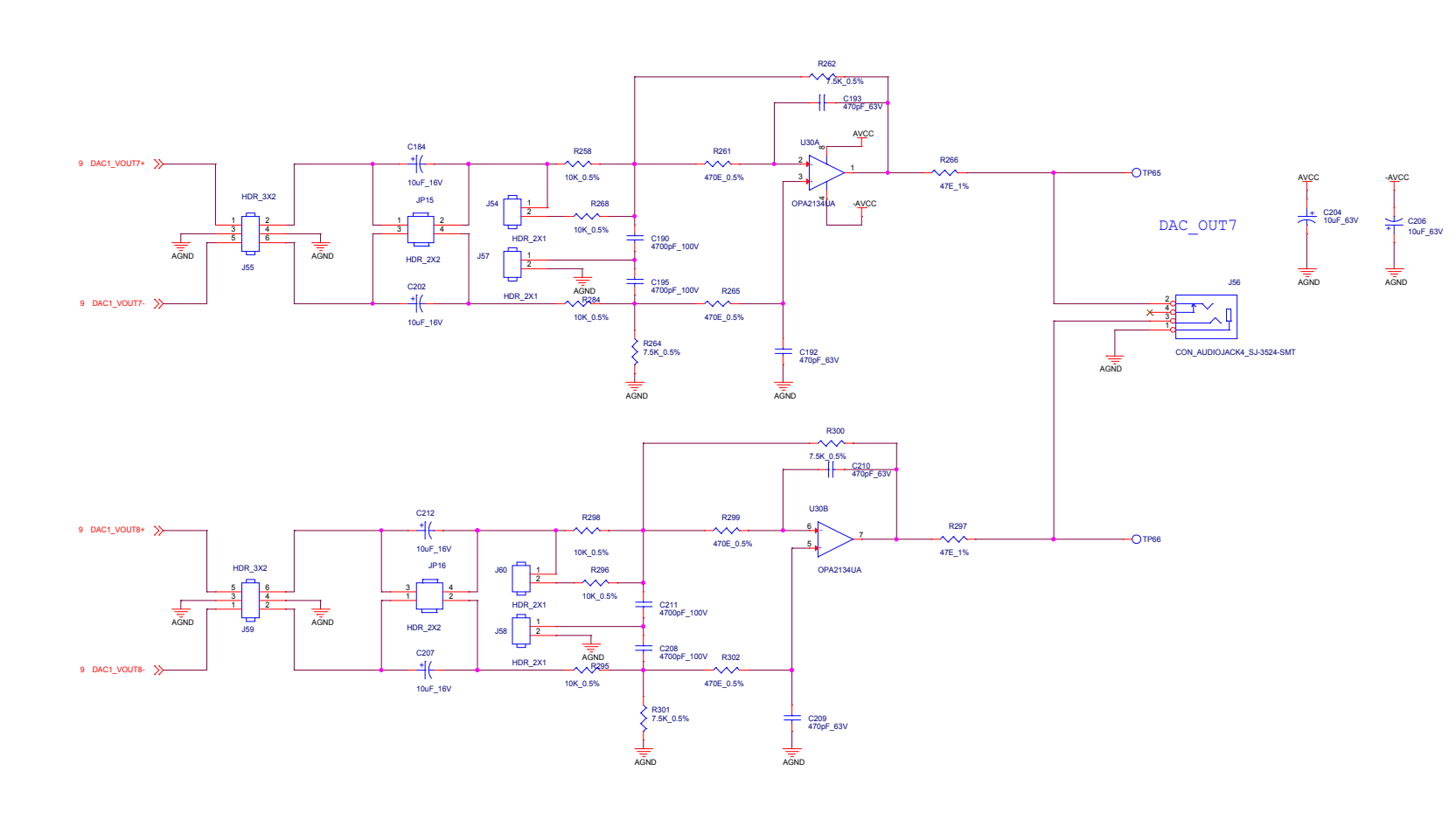
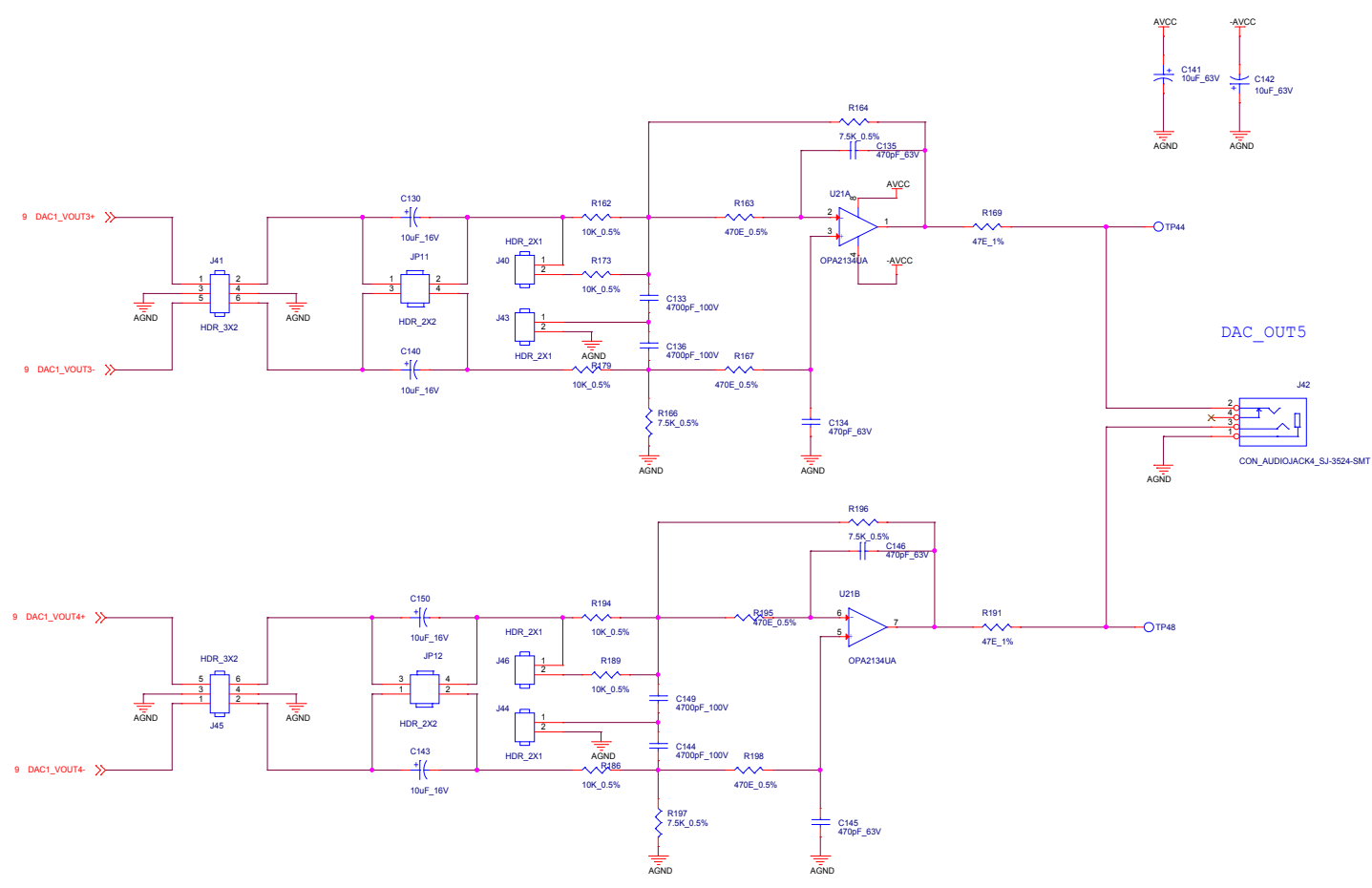
OPAMP INPUT COUPLING SELECTION

Header Name	AC Coupling	DC Coupling
JP 2 to 8	OPEN	CLOSE PIN 1,2 & 3,4

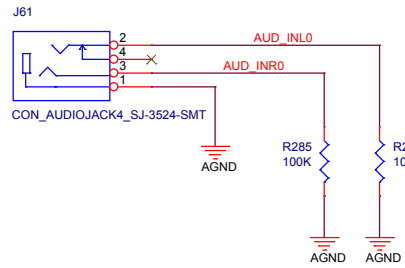


OPAMP INPUT COUPLING SELECTION

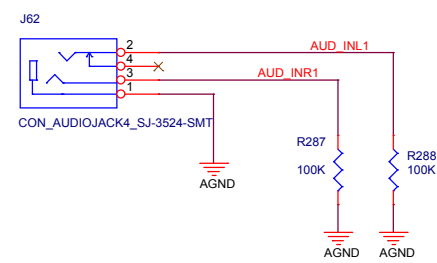
Header Name	AC Coupling	DC Coupling
JP 9 to 16	OPEN	CLOSE PIN 1,2 & 3,4



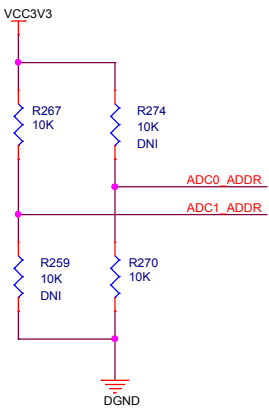
ADC_IN0



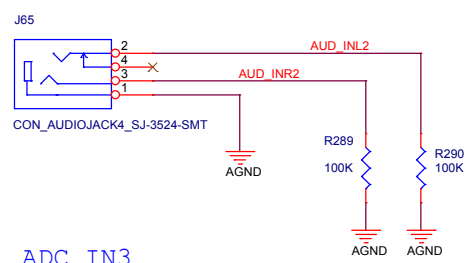
ADC_IN1



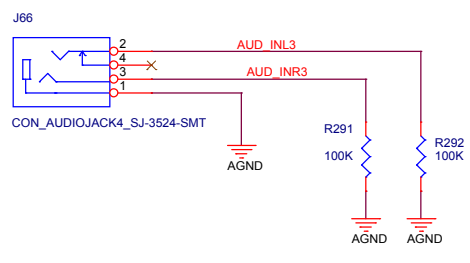
I2C ADDRESS SELECTION



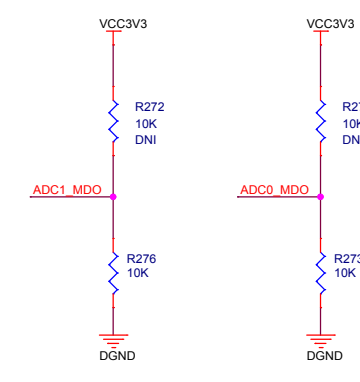
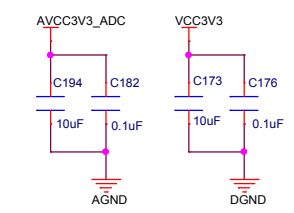
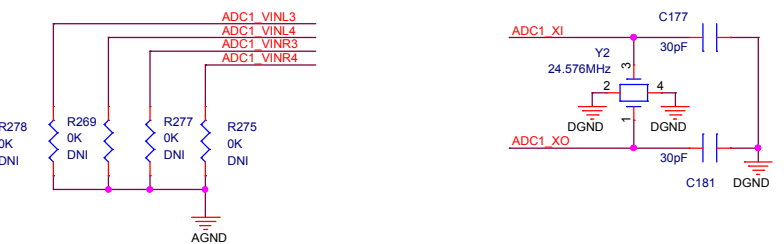
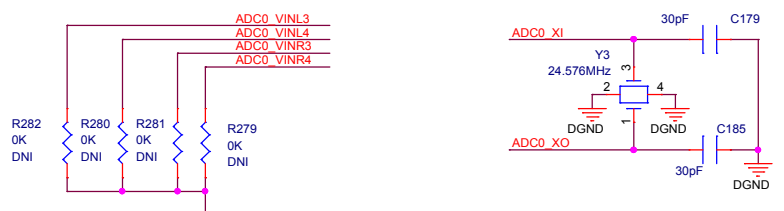
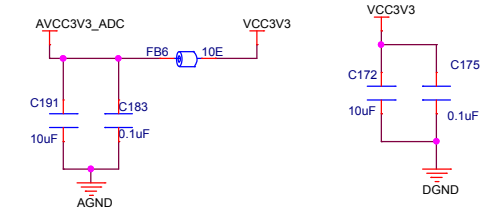
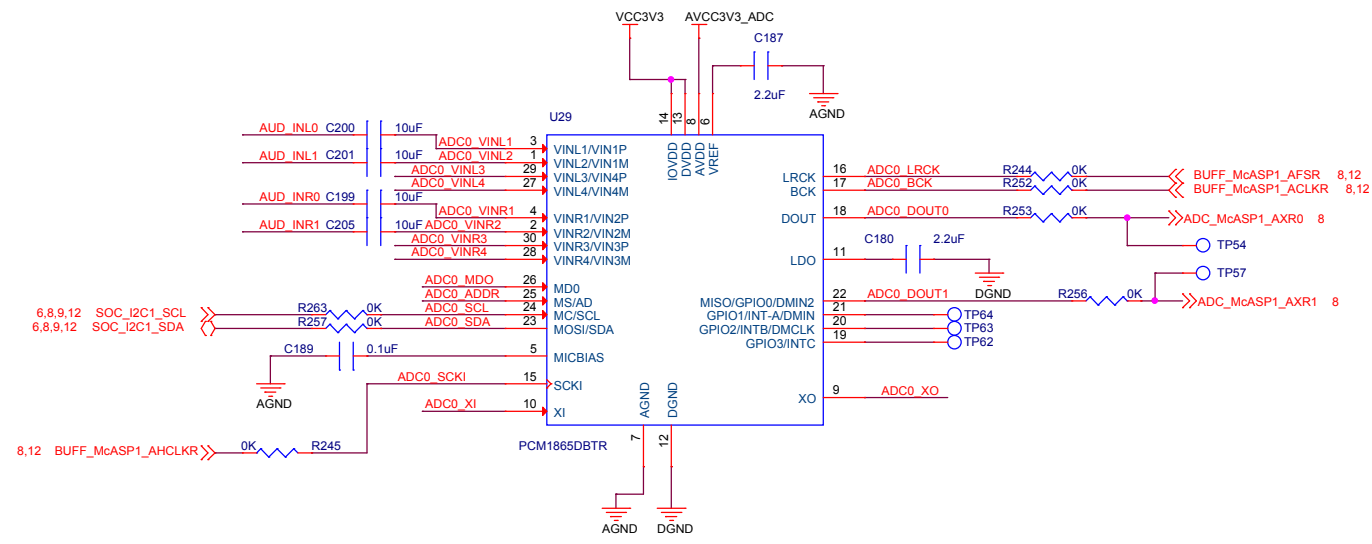
ADC_IN2



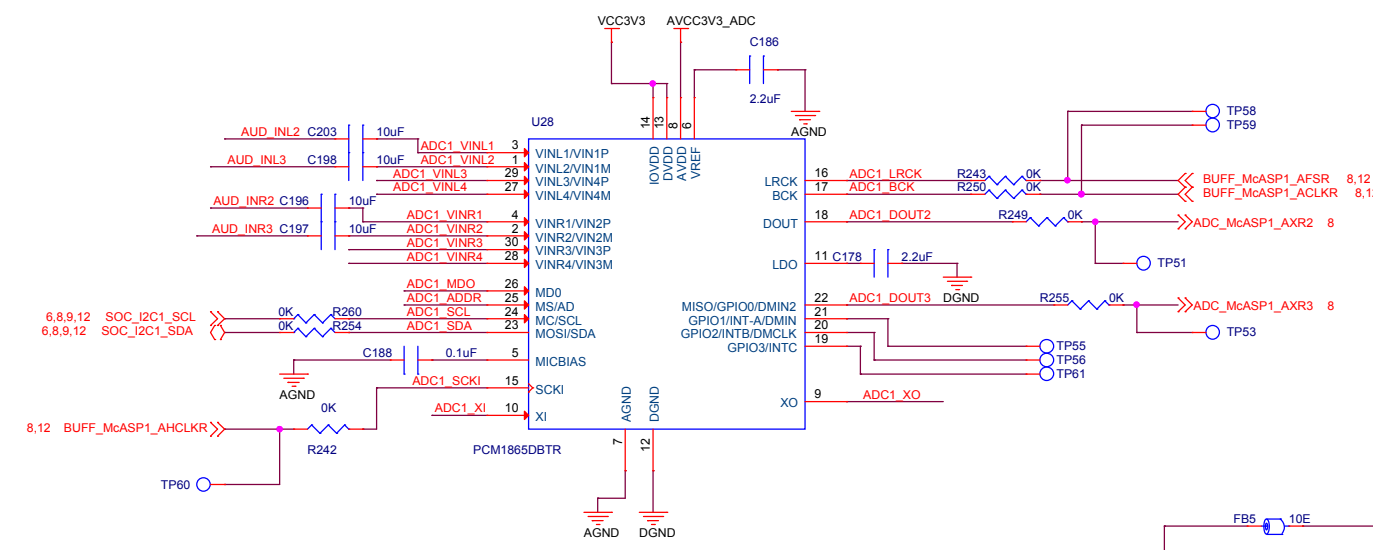
ADC_IN3



ADC0

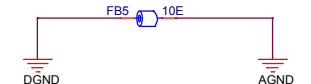


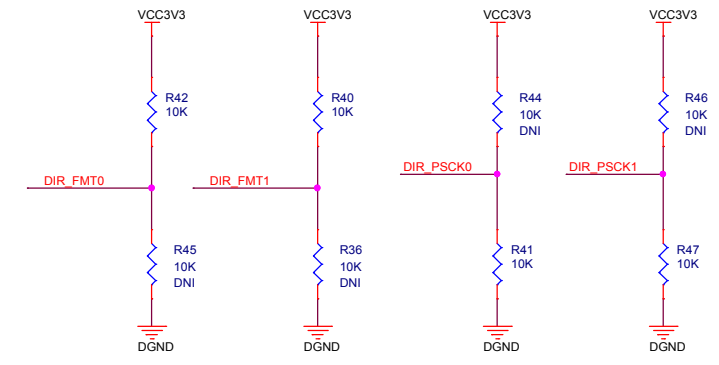
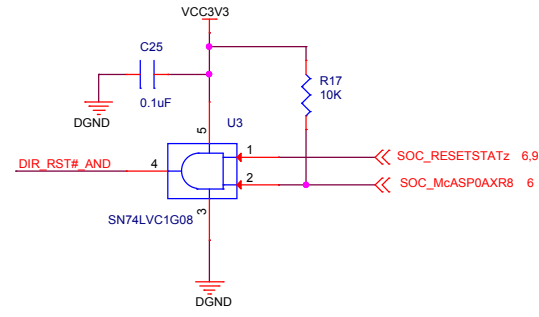
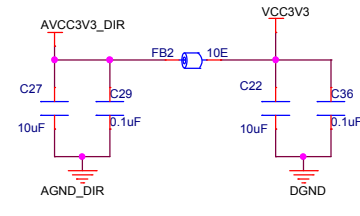
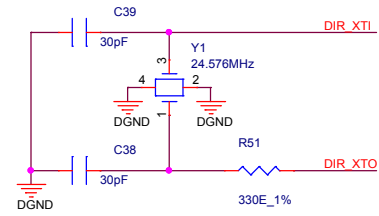
ADC1



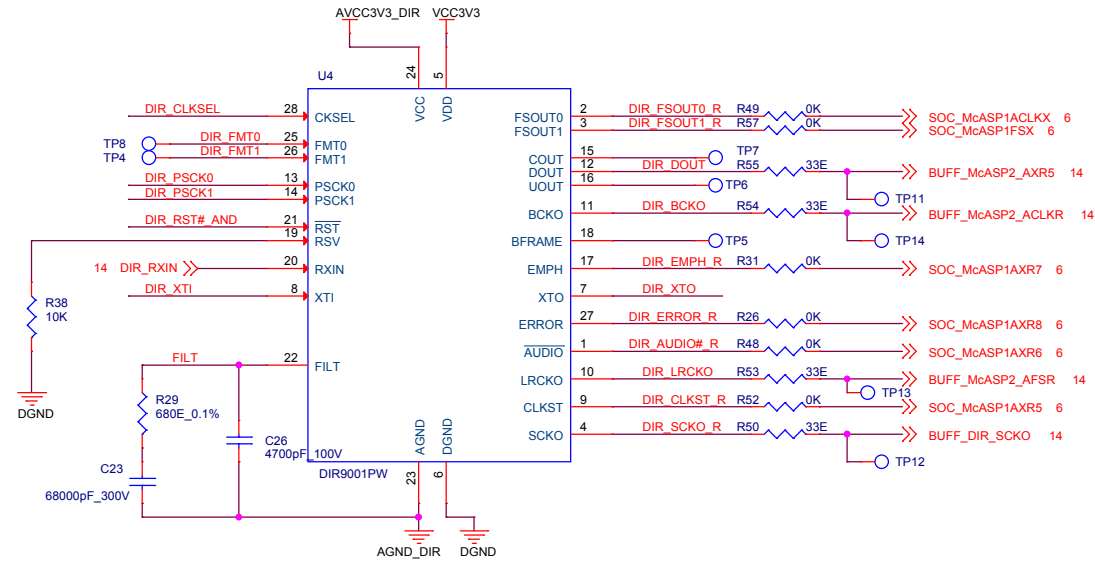
ADC MODE SELECTION

MDO	Interface Selection
L	I2C
H	SPI





DIR9001



SERIAL AUDIO DATA OUTPUT FORMAT SELECTION

FMT[1:0] SETTINGS		DOUT SERIAL AUDIO DATA OUTPUT FORMAT
FMT1	FMT0	
L	L	16-bit, MSB-first, right-justified
L	H	24-bit, MSB-first, right-justified
H	L	24-bit MSB-first, left-justified
H	H	24-bit, MSB-first, I2S

SYSTEM CLK FREQUENCY OF PLL SELECTION

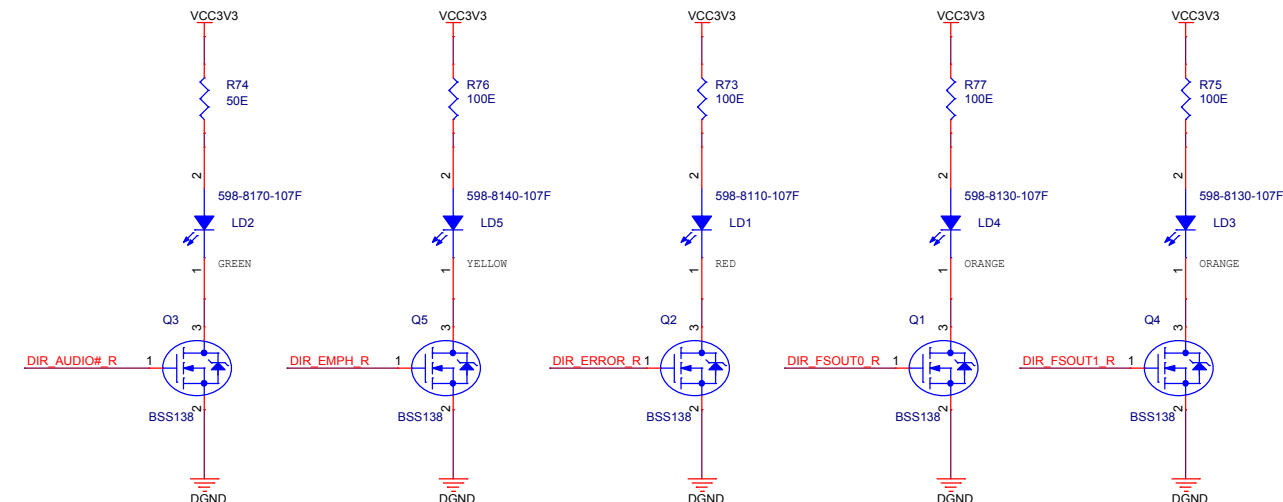
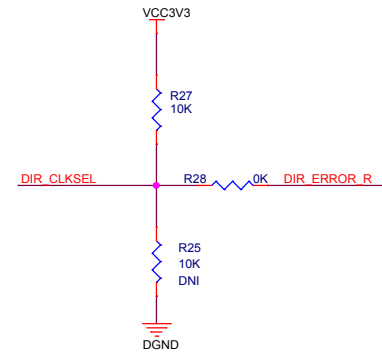
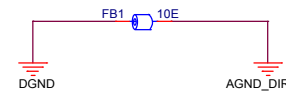
PSCK[1:0] SETTING		OUTPUT CLOCK FROM PLL SOURCE		
PSCK1	PSCK0	SCKO	BCKO	LRCKO
L	L	128 fs	64 fs	fs
L	H	256 fs	64 fs	fs
H	L	384 fs	64 fs	fs
H	H	512 fs	64 fs	fs

LED STATUS TABLE

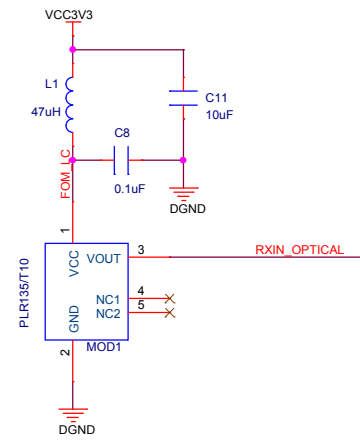
STATUS	LED1	LED2	LED3	LED4	LED5
Non Audio Sample Word	ON	OFF	OFF	OFF	OFF
Pre-Emphasis (50 ms/15 ms)	OFF	ON	OFF	OFF	OFF
Internal PLL or Data parity error	OFF	OFF	ON	OFF	OFF
Sample Frequency Result Output 0	OFF	OFF	OFF	ON	OFF
Sample Frequency Result Output 1	OFF	OFF	OFF	OFF	ON

DIR Operation Mode and Clock Source

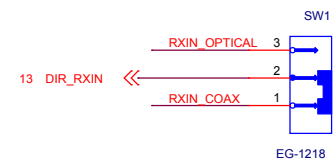
Operation Mode	CLKSEL	ERROR Pin Status	SCKO, BCKO, LRCKO CLOCK SOURCE
PLL	L	H	PLL (VCO) free-running Clock
		L	PLL recovered clock
XTAL	H	H	XTAL clock
		L	XTAL clock
AUTO	Connected to ERROR Pin	H	XTAL clock
		L	PLL recovered clock



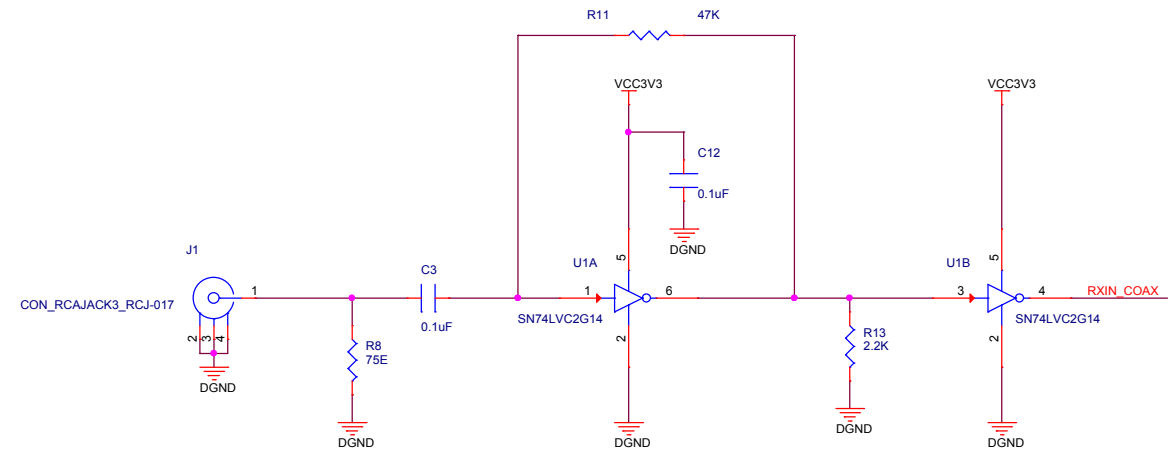
FIBER OPTIC RECEIVER MODULE



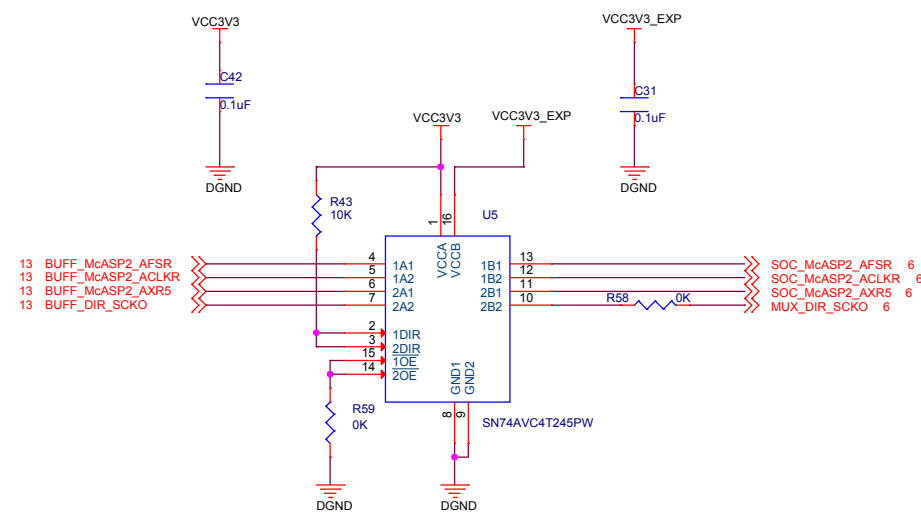
INPUT SELECTION SWITCH



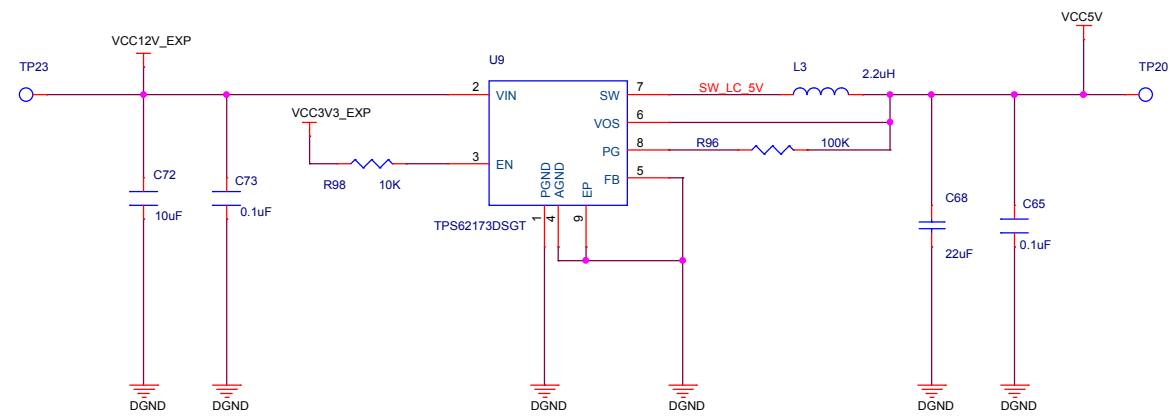
COAXIAL RCA CONNECTOR & LINE DRIVER



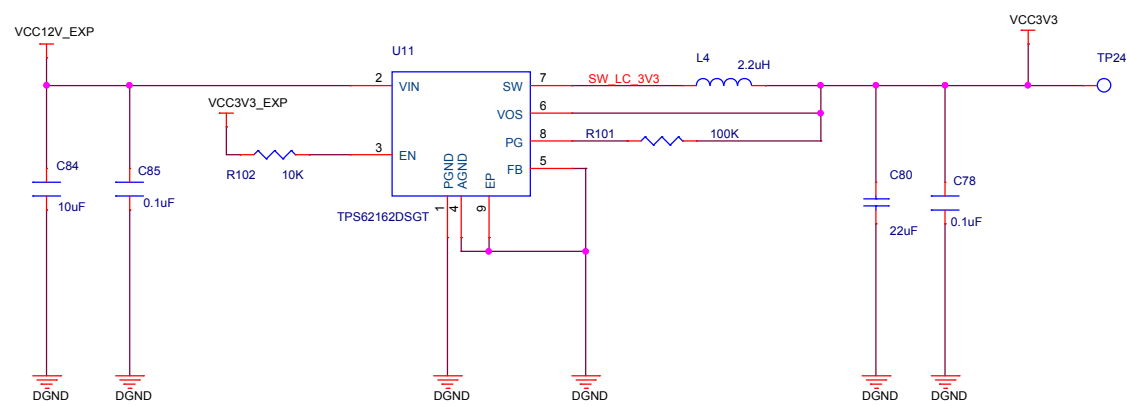
DIR CLOCK AND DATA BUFFER



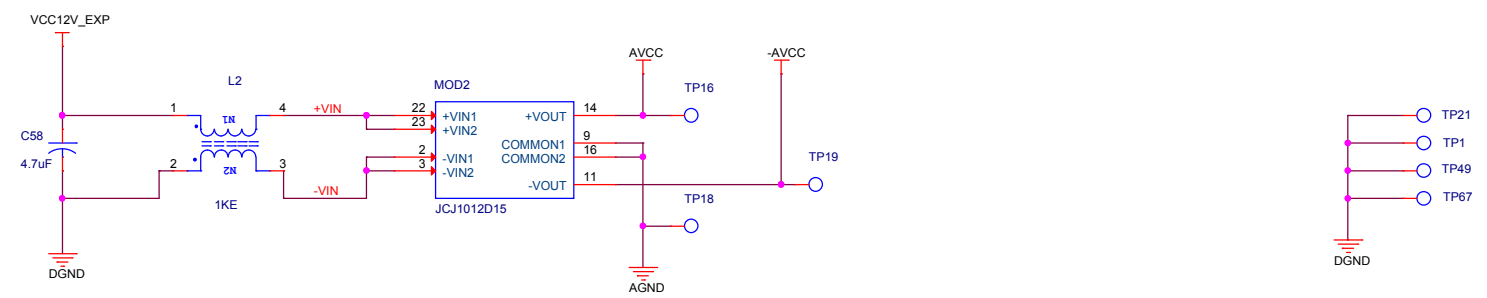
12V TO 5V SUPPLY



12V TO 3.3V SUPPLY



OPAMP POWER +/-15V



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