Application Report
SPRAAY1B–January 2018–Revised April 2019

TMS320TCI6484 and TMS320C6457 SERDES Implementation Guidelines

ABSTRACT

This document contains implementation instructions for the two serializer/deserializer-based interfaces (SerDes) on the TMS320TCI6484 and TMS320C6457 DSP devices:

- Serial RapidIO (SRIO)
- Serial Gigabit Media Independent Interface (SGMII)

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Trademarks

1 Introduction

1.1 Purpose and Scope

The goal of TMS320TCI6484 and TMS320C6457 collateral material is to make system implementation easier for the customer by providing the system solution. For these SerDes-based interfaces, it is not assumed that the system designer is familiar with the industry specifications, SerDes technology, or RF/microwave PCB design. However, it is still expected that the PCB design work be supervised by a knowledgeable high-speed digital PCB designer and an assumption is made that the PCB designer is using established high-speed design rules.

This document is intended to aid in the hardware design and implementation of a TMS320TCI6484-based or a TMS320C6457-based system. The document should be used along with the device-specific data manual and relevant user guides, application reports, standards, and specifications (see Section 4).

1.2 Overview

Serial RapidIO is an industry-standard high-speed switched-packet interconnect. SGMII is a standard used for gigabit Ethernet connections from MAC to MAC or MAC to PHY.

For each of these interfaces, physical layer data transmission uses analog SerDes to feed low-output-swing differential current-mode logic (CML) buffers. Proper printed circuit board (PCB) design for these interfaces resembles analog or RF design, and is very different than traditional parallel digital bus design.

Due to this analog nature of SerDes based interfaces, it is not possible to specify the interface in a traditional DSP digital interface manner. Furthermore, it is undesirable to specify the interface in terms of the raw physical requirements laid out by the industry standard specifications. Understanding these specifications and producing a compliant PCB based on the explicit and implicit requirements demands significant time, experience, and expensive tools.

For the TMS320TCI6484 and TMS320C6457 SerDes based interfaces, the approach is to reduce the specifications to a set of easy-to-follow PCB routing rules and system configurations. TI has performed the simulation and system design work to ensure the appropriate interface requirements are met. This document describes guidelines that, when followed, result in board level implementations that meet the interface requirements.

1.3 Industry Standards Compatibility

All SerDes interfaces are configured as point-to-point connections. It is assumed that the connection is made between the TMS320TCI6484 and TMS320C6457 and another device compliant to the appropriate industry standard. The list of supported standards is given below. Note that this document deals with the physical layer and, therefore, it is the electrical specifications in these standards that are relevant. For more information regarding protocol compliance (1), see the device-specific user's guides.

- Serial RapidIO: This is electrically compliant with Serial RapidIO specification revision 1.2
- SGMII: This is electrically compliant with SGMII revision 1.8 with the following clarifications
  - It does not implement the separate clock signaling
  - It must be AC-coupled and may require external terminations (see Section 3.1)

2 PCB Routing Rules

2.1 Minimum PCB Stack Up

The minimum PCB stack up for routing the TMS320TCI6484 or TMS320C6457 device is considered to be a six-layer stack up as described in Table 1.

Table 1. Minimum PCB Stack Up

Layer	Type	Description
1	Signal	Top routing
2	Plane	Ground
3	Plane	Split power
4	Signal	Internal routing
5	Plane	Ground
6	Signal	Bottom routing

Additional layers may be added as needed. All layers with SerDes traces must be able to achieve 100-Ω differential impedance.

(1) Electrical compatibility does not guarantee interoperability with devices

2.2 General Trace/Space and Via Sizes

The key concern for SerDes signal traces is the need to achieve 100-Ω differential impedance. This differential impedance is impacted by trace width, trace spacing, distance between planes, and dielectric material. Verify with a proper PCB manufacturing tool that the trace geometry for all SerDes traces results in exactly 100-Ω differential impedance traces.

Of secondary concern is the insertion loss caused by the traces. Due to the skin effect, wider traces have lower losses than narrower traces. Therefore, longer SerDes runs should use wider traces for lower loss. However, be aware that layers in the stack up that are set to 100-Ω differential impedance with wider traces may be less desirable for routing other signals. Table 2 shows recommendations for minimum trace width by SerDes signal run length.

Table 2. Minimum Trace Width

Signal Run Length (Up To)	Minimum Trace Width
10 inch / 25 cm	4 mil / 0.1 mm
20 inch / 50 cm	6 mil / 0.15 mm
30 inch / 75 cm	8 mil / 0.2 mm

Standard via sizes that allow escape from a 0.8-mm pitch device can be used (8-mil holes, 18-mil pads). Micro or blind/buried vias are neither required nor prohibited.

The PCB BGA pad requirements for the TMS320TCI6484 and TMS320C6457 devices are documented by the *Flip Chip Ball Grid Array Package Reference Guide*, available at http://www.ti.com. The TMS320TCI6484 and TMS320C6457 are 0.8-mm ball pitch parts and should follow the 0.8-mm guidelines. The PCB BGA pad requirements for the SerDes link partner device should follow its manufacturer's guidelines.

2.3 SerDes Interface Routing Requirements

The approach for specifying suitable SerDes routing breaks the physical connection down into three component pieces: receiver end, transmitter end, and interconnect. The receiver and transmitter end are the pieces closest to the packages of the connected devices. The receiver end goes from the BGA pads to the AC-coupling capacitors. The transmitter end is simply the BGA escape paths for the differential pairs. The interconnect joins the receiver and transmitter ends.

2.3.1 Receiver End

For the receiver end, it is strongly recommended to route the trace from the BGA pad to the capacitor pad on the top layer. This avoids a via escape between the BGA pad and the capacitor. This style of connection is possible on Serial RapidIO ports and the SGMII port. On the other side of the capacitor, it is recommended to via to another layer. The trace widths and separation should be altered based on the board stack up to meet the 100-Ω differential impedance requirement. Traces may be necked down to escape the BGA, if necessary.

2.3.2 Transmitter End

The transmitter end should use standard via escapes to internal layers. Internal layers are recommended for their superior shielding characteristics. The trace widths and separation should be selected based on the board stack up to meet the 100-Ω differential impedance requirement. Traces may be necked down to escape the BGA, if necessary.

2.3.3 Interconnect

The geometry of the traces to link the transmitter and receiver ends is determined by the placement in the target system and any board-to-board connections. The trace can be placed as required, as long as it meets the following requirements:

- Edge-coupled, matched-length (± 10 mils) differential pair
- No stubs

- Maximum trace lengths:
  - SRIO: No more than 30 inches (75 cm) pin-to-pin, for 8-mil (0.2 mm) wide traces over FR4 material
  - SGMII: No more than 20 inches (50 cm) pin-to-pin, for 6-mil (0.15 mm) wide traced over FR4 material
- 100-Ω differential impedance
- Areas where desired differential pair separation cannot be maintained (connections to devices or connectors) should be kept to an absolute minimum
- Do not route across splits in the neighboring reference plane
- No more than three sets of vias (not including via for BGA breakouts)
- Whenever possible use the majority of via length to transfer signal layers in order to avoid via stubs
- Other signals are separated by at least 2× the differential spacing
- Internal layers are strongly preferred — avoid top and bottom layers
- A SerDes trace should be routed either as a stripline between two reference planes (either ground or power) or as a microstrip directly over or under a reference plane (either ground or power)
- If connectors are used, they must be of a suitable 100-Ω differential-impedance, high-speed type, and count as 1 inch of trace for each connector pair
- If cabling is used, it must be of a suitable controlled-impedance type (100-Ω differential or 50-Ω single ended), and counts as 1 inch of trace for each 1 foot of cable
- If a mid bus probe is used, it must follow both TI's and the probe manufacturer's guidelines, and counts as 2 inches of trace
- There is no requirement that the lengths of different differential pairs to be matched to each other.

2.3.4 Mid Bus Probe (Optional)

A mid bus probe can be used to observe traffic flowing down a link. Because the probe requires a special attachment point, it can degrade signal quality. The following rules must be observed to include a mid bus probe:

- Follow the probe manufacturer's guidelines for probe pads and layout
- If the stubs can be kept under 250 mils (6.35 mm) then connecting the probe lands as stubs to the transmission line is acceptable
- If the stubs cannot be kept under 250 mils (6.35 mm) then the probe lands should be connected in-line with the rest of the transmission line

2.3.5 Connectors (Optional)

Any connectors used must be controlled impedance (50-Ω single ended or 100-Ω differential) and suitable for microwave transmissions. Suitable connectors are typically categorized as backplane type connectors. The connectors should have less than 1-dB insertion loss below 6 GHz. Some suggested connectors are:

- CN074 - AMC Connector
- Tyco Z-DO
- Tyco Z-PAK HM Z

2.3.6 Cabling (Optional)

Any cabling used must be controlled impedance (50-Ω single ended or 100-Ω differential) and suitable for microwave transmissions. Recommended cable types are listed below:

- 50-Ω Coaxial - commonly used with SMA connectors
  - RG142
  - RG316
  - RG178
- Infiniband - assembled cables available in 1× and 4× widths

2.4 Power Supply Requirements

The power supply and bypassing requirements for SerDes power planes are documented as part of the *TMS320TCI6484 and TMS320C6457 DSPs Hardware Design Guide*.

It is best to use power plane splits to connect the power supply from the filters to the pins. However, traces that are at least 20 mils wide can also be used to access the inner BGA pads.

3 Signal Considerations

The detailed electrical characteristics for the SerDes I/Os are given in the data manual. Due to the point-to-point connectivity and strict routing rules, it is difficult to observe the SerDes waveforms to compare with these electrical characteristics. However, as long as all factors affecting the signal waveform are properly handled, it should not be necessary to observe the waveform.

Other than the routing from device to device (which is described in Section 2), the other factors impacting the signal waveforms are the terminations and SerDes device settings accessible by memory mapped register reads and writes on the TMS320TCI6484 or TMS320C6457 device.

3.1 Terminations

All SerDes-based interfaces should be AC-coupled. As long as the SerDes link partner uses CML logic the AC-coupling capacitor is the only external termination required. For AC-coupling the recommendation is to use an 0402 or smaller 0.1-μF ceramic capacitor placed near the receiver. This should be the case for the Serial RapidIO since that standard calls for CML signals. The SGMII specification calls for low-voltage differential signaling (LVDS) so additional terminations may be required. The need for terminations is dependent on the internal terminations in the link partner device. Examples of LVDS to CML and CML to LVDS conversion are covered in Section 3.1.1 and Section 3.1.2, respectively.

3.1.1 LVDS to CML Example

Figure 1 shows an example of an LVDS to CML connection:

- Requires AC termination because the LVDS common mode voltage is too high for the SerDes receivers
- CML receivers include 100-Ω termination needed by LVDS and include internal biasing (no external biasing needed)

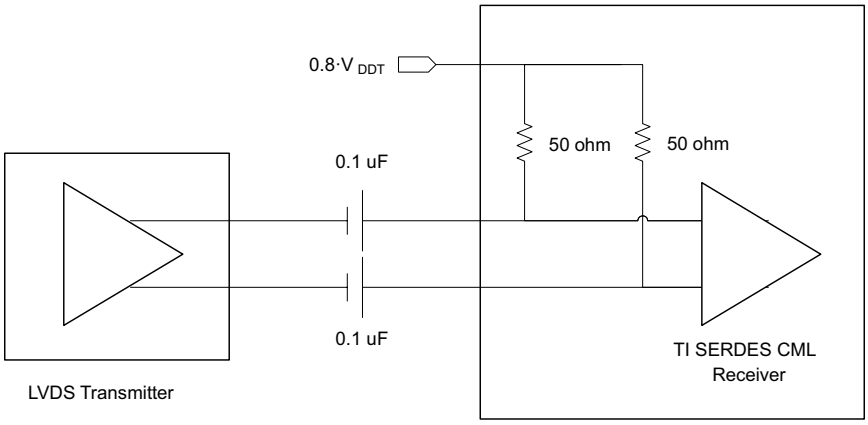

Figure 1. LVDS to CML Connection Basic Diagram

3.1.2 CML to LVDS Examples

Figure 2 shows an example of a CML to LVDS connection:

- Requires AC termination because the common mode voltages are incompatible
- LVDS receivers require 100-Ω terminations and proper biasing
- Some LVDS receivers include 100-Ω termination and some do not
- Some LVDS receivers include internal biasing and some do not

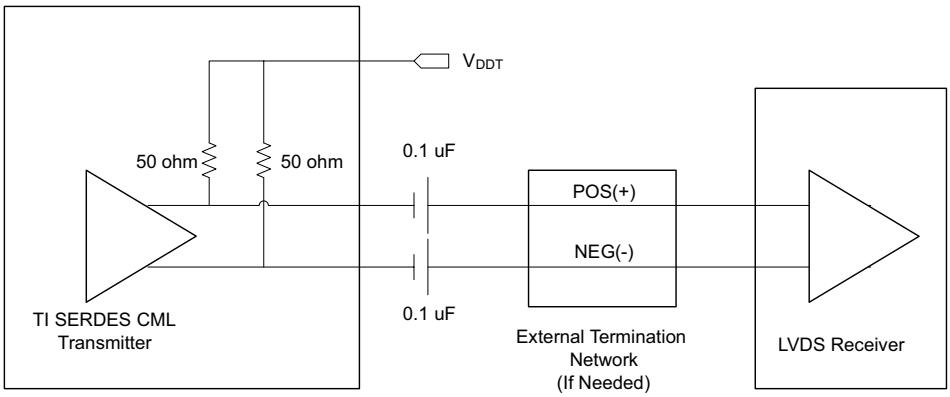

Figure 2. CML to LVDS Connection Basic Diagram

- If the LVDS receiver includes the 100-Ω termination and internal biasing, there is no need for external terminations
- If the LVDS receiver includes neither the 100-Ω or biasing, use the external terminations shown in Figure 3

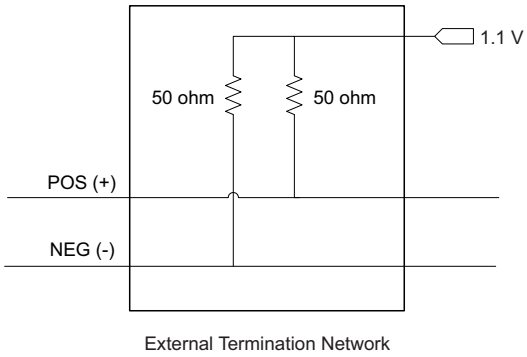

Figure 3. External Terminations: Receiver Has No Internal Terminations

- If the LVDS receiver includes the 100-Ω termination but no biasing, use the external terminations shown in Figure 4

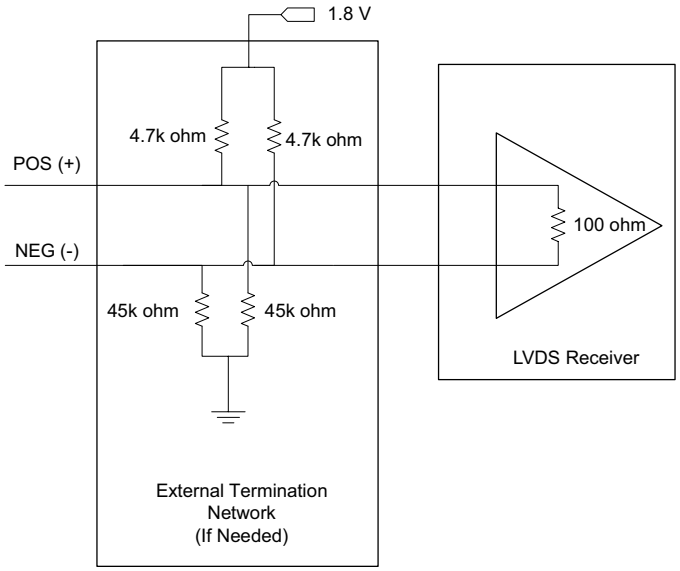

Figure 4. External Terminations: Receiver With 100-Ω Termination

- If the LVDS receiver includes 100-Ω terminations and internal pull-ups (sometimes used for fail-safe), use the type of termination shown in Figure 5. Adjust the external resistor values based on the V_{CC} and internal resistors in order to generate a bias voltage of 1.0 V to 1.2 V.

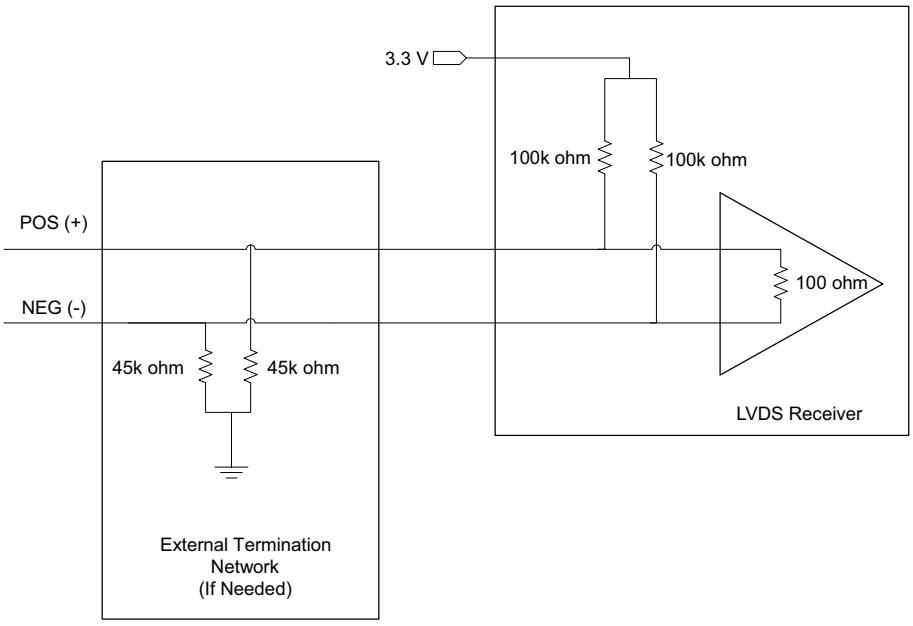

Figure 5. External Terminations: Receiver With 100-Ω Terminations and Pull-Ups

- There are other combinations that may be needed for other types of input buffers. The important factors are to make sure there is a 100-Ω impedance and a bias voltage set around 1.2 V.

3.2 Device Settings

Some of the SerDes register values should be set based on parameters from the physical PCB. Others are not dependent on the PCB, but are set based on an industry standard electrical specification. The following sections describe the recommended settings for the receivers and transmitters. Some of these settings can be adjusted based on characterization of the TMS320TCI6484 or TMS320C6457 device. For more detailed information regarding these registers, see the device-specific peripheral user's guide for SGMII and Serial RapidIO.

3.2.1 Receive Channel Configuration

Table 3 lists the recommended settings for receiver channels. These register settings are described in the device-specific peripheral user's guide.

Table 3. SerDes Receive Channel Configuration Register Settings

Field	Description	Setting	Setting Description
EQ	Equalizer	0001	Fully adaptive equalization
CDR	Clock/data recovery	000	First Order. Sufficient for clocking schemes (asynchronous with low frequency offset).
LOS	Loss of signal detection	00	SRIO/SGMII: Disabled
ALIGN	Comma alignment	01	Aligns incoming serial stream on proper 10-bit sequences.
TERM	Termination	001	Common point is 80% of VDDT. This is the appropriate setting for AC-coupled lines
INVPAIR	Invert polarity	0	Non-inverted — Use this when TXP connects to RXP and TXN connects to RXN
		1	Inverted — Use this when TXP connects to RXN and TXN connects to RXP **Note**: On inverted pairs, polarity inversion can be done at the receiver end or the transmitter end, but not both.
RATE	Operating rate **Note**: For more information, see *TMS320TCI6484 and TMS320C6457 DSPs Hardware Design Guide*.	00	Full rate. Two data samples taken per PLL output clock cycle.
		01	Half rate. One data sample taken per PLL output clock cycle.
		10	Quarter rate. One data sample taken every two PLL output clock cycles.
BUS-WIDTH	Bus width	000	10-bit. All three interfaces use 10-bit character groups.
ENRX	Enable receiver	0	Disabled. For unused lanes.
		1	Enabled. For active lanes.

3.2.2 Transmit Channel Configuration

Table 4 lists the recommended settings for transmitter channels. These register settings are described in the peripheral user's guide.

Table 4. SerDes Transmit Channel Configuration Register Settings

Field	Description	Setting	Setting Description
ENFTP	SGMII (Serdes TX Fixed phase disabled)	0	Arbitrary Phase
	SRIO (Serdes TX Fixed phase enabled)	1	Fixed Phase
DE	De-emphasis **Note**: SGMII connections beyond 20 inches are not recommended.	0000	0 dB — Not Recommended
		0001	–0.42 dB — Not Recommended
		0010	–0.87 dB — Not Recommended
		0011	–1.34 dB — Not Recommended
		0100	–1.83 dB — Not Recommended
		0101	–2.36 dB — Not Recommended
		0110	–2.92 dB —Not Recommended
		0111	–3.52 dB — Not Recommended
		1000	–4.16 dB — Use for lines up to 10 inches (25 cm)
		1001	–4.86 dB — Use for lines up to 14 inches (35 cm)
		1010	–5.61 dB — Use for lines up to 18 inches (45 cm)
		1011	–6.44 dB — Use for lines up to 22 inches (55 cm)
		1100	–7.35 dB — Use for lines up to 26 inches (65 cm)
		1101	–8.38 dB — Use for lines up to 30 inches (75 cm)
SWING	Output swing SGMII connections beyond 20 inches (50cm) are not recommended. SRIO connections beyond 30 inches (76 cm) are not recommended.	000	125 mV — Not Recommended
		001	250 mV — Not Recommended
		010	500 mV — Not Recommended
		011	625 mV — Not Recommended
		100	750 mV — Use for lines up to 10 inches (25 cm)
		101	1000 mV — Use with lines up to 20 inches (50 cm) for SRIO. Use with lines up to 15 inches (37 cm) for SGMII.
		110	1250 mV — Use with lines up to 20 inches (50 cm) for SRIO or SGMII
		111	1375 mV — Not Recommended
CM	Common mode	1	Raised Common Mode — Helpful in preventing signal distortion at SWING amplitudes of more than 750 mV
INVPAIR	Invert polarity **Note**: On inverted pairs, polarity inversion can be done at the receiver end or the transmitter end, but not both ends.	0	Non-inverted — Use when TXP connects to RXP and TXN connects to RXN
		1	Inverted — Use when TXP connects to RXN and TXN connects to RXP
RATE	Operating rate **Note**: For more information, see *TMS320TCI6484 and TMS320C6457 DSPs Hardware Design Guide*.	00	Full rate. Two bits output per PLL output clock cycle.
		01	Half rate. One bit output per PLL output clock cycle.
		10	Quarter rate. One bit output every two PLL output clock cycles.
ENTX	Enable transmitter	0	Disabled. For unused lanes.
		1	Enabled. For active lanes.

4 References

- Texas Instruments: *TMS320TCI6484 and TMS320C6457 DSPs Hardware Design Guide* This document contains information related to powering, clocking, and configuring the TMS320TCI6484 and TMS320C6457 devices.
- Texas Instruments: *High-Speed DSP Systems Design Reference Guide* This document contains general guidance on many matters of high performance DSP system design.
- Texas Instruments: *Flip Chip Ball Grid Array Package Reference Guide* This document provides guidance with respect to PCB design and Texas Instruments BGA packages. It contains PCB design rules, PCB assembly parameters, rework process, thermal management, and troubleshooting tips, plus other critical information.

Serial RapidIO:

- RapidIO specifications can be downloaded from the RapidIO Trade Association's website: http://www.rapidio.org.
- Texas Instruments: *TMS320C6472/TMS320TCI648x DSP Serial RapidIO (SRIO) User's Guide* This document explains the functional operation of the SRIO peripheral.
- Texas Instruments: *TMS320C6457 DSP Serial RapidIO (SRIO) User's Guide* This document explains the functional operation of the SRIO peripheral.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (October 2009) to B Revision	Page
• Update was made in Table 4.	9

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