

# **LM2742,LM2743,LM2744,LM2745,LM2746, LM2747,LM2748**

*Optimizing Power Controller Designs through Effective Utilization of  
Performance Features (Adj Frequency & Sync, Ext Ref, Tracking, & Precision  
Enable)*



Literature Number: SNVA601

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No. 122

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## Optimizing Power Controller Designs through Effective Utilization of Performance Features

— By Ricardo Capetillo, Application Engineer

### Introduction

When system design engineers are in search of power for mixed-signal electronics, they must satisfy performance, cost, efficiency, and space requirements. Electronic equipment such as rack mount servers, communication equipment, laptops, and many consumer electronic goods must conserve space in order to maintain the product's form factor. This article will illustrate how the proper features can help satisfy system specifications and enhance the performance of the power supply and the load.

The following key features will be presented: adjustable switching frequency, feedback voltage accuracy, startup tracking, power sequencing, pre-biased startup, utilizing an external reference, and synchronizing to an external clock. When optimized, these features can reduce EMI, transient response times, transient voltage amplitudes, solution size, output capacitance requirements, and overall BOM costs.

### User-Adjustable Switching Frequency and External Compensation

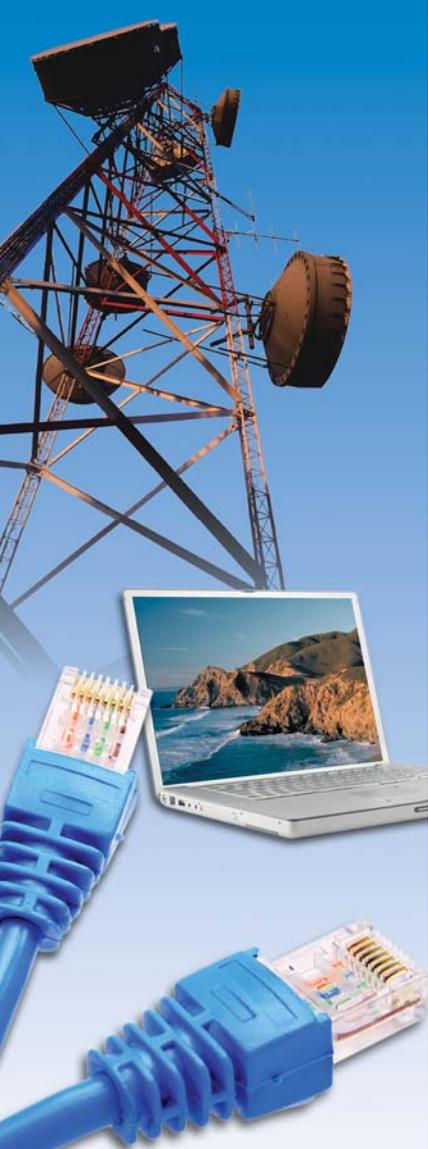
A user-adjustable switching frequency allows the power designer to set the oscillator switching frequency to achieve the desired filter component size and consequently, the solution size. A high switching frequency reduces the power solution footprint by decreasing the size of the charge storage components. This includes input/output capacitors, inductors, and other filtering components.

By moving from a 100 kHz to a 1 MHz switching frequency, typical inductance required decreases tenfold while the volume of the inductor decreases fivefold. (The comparison was done with two shielded drum-core inductors of the same series, with saturation levels 15% apart from each other, the inductor current ripple set to 30% of the maximum load current, and with the following application power parameters:  $V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $I_{LOAD} = 5A$ , see *Figure 1*) Shielded drum-core inductors are a good choice for switch-mode power supplies (SMPSs) that require an inductance value between 0.33  $\mu H$  and 1 mH. These inductors are appropriate for high-frequency, low-EMI, and low-cost applications.

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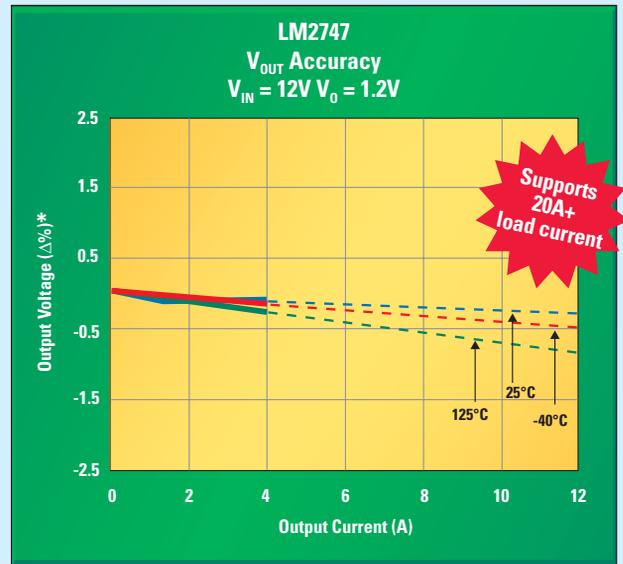
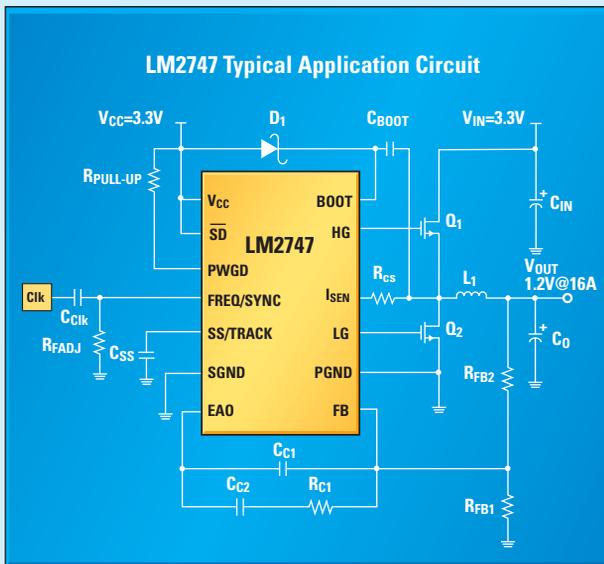
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National's LM274x Family of Controllers Provide Down Conversion to Output Voltages as Low as 0.6V



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Product ID	Operating Frequency	Product Features	Packaging
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LM2743	50 kHz to 1 MHz	Tracking	TSSOP-14
LM2744	50 kHz to 1 MHz	External reference, tracking	TSSOP-14
LM2745	50 kHz to 1 MHz	Pre-bias operation, ext clock 250 kHz to 1 MHz	TSSOP-14
LM2746	50 kHz to 1 MHz	1% accuracy 0°C to 85°C, startup delay	Thermally-enhanced TSSOP-14
LM2747	50 kHz to 1 MHz	1% accuracy -40°C to +125°C, pre-bias operation, external clock, programmable soft-start	TSSOP-14
LM2748	50 kHz to 1 MHz	Pre-bias operation, 1.5% accuracy	TSSOP-14

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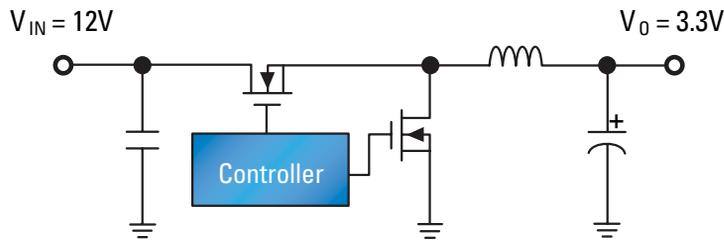


Figure 1. Simplified Buck Controller Circuit

The output capacitor also decreases in size as the switching frequency increases. Assume that multi-layer ceramic capacitors (MLCCs) for the output filter have been selected and that the equivalent series resistance (ESR) is low enough that the output voltage ripple is capacitive. An SMPS design with a 100 kHz switching frequency, 1.5A peak-to-peak AC current, and a 50 mV output voltage ripple, requires 37.5  $\mu\text{F}$  capacitance. The typical capacitance requirement decreases tenfold when operating at a 1 MHz switching frequency and the case size transitions from a 1210 MLCC to a 0603 case representing almost a 20x reduction in volume.

In this example, design for the output filter components only considered voltage and current ripple without examination of load and line transients. The availability of external compensation gives the power supply designer the flexibility to optimize the feedback loop without oversizing the output capac-

itance. For example, to decrease the output voltage transient, one can take advantage of the wide gain bandwidth product of the error amplifier. A high closed-loop bandwidth frequency decreases the time required for the error amplifier to react to load and line transients. As a typical rule of thumb, a bandwidth designed at one-tenth to one-fifth of the switching frequency results in a high-performance loop response. *Figures 2 and 3* show the result of increasing the bandwidth. The SMPSs underwent the same test conditions: equal slew rates, 350 mA to 8A load transient step, 440  $\mu\text{F}$  output capacitance, and equal feedback-loop-gain phase margin ( $48^\circ$ ).

In the example, the output voltage transient decreased by approximately  $\pm 80$  mV. The external compensation provides the flexibility to fine-tune the speed of the loop response while maintaining the same output capacitance.

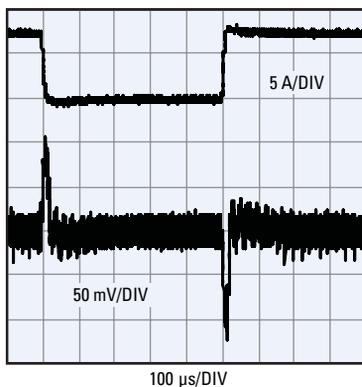


Figure 2. 26 kHz Bandwidth

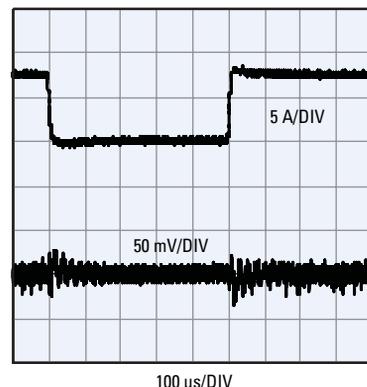


Figure 3. 119 kHz Bandwidth

## Optimizing Power Controller Designs through Effective Utilization of Performance Features

### Feedback Voltage Accuracy

The demand for faster processing speeds, conservation of battery life, and thermal considerations have driven digital processors to decrease their operating voltage. To maintain predictable logic level states, it is particularly significant for the SMPS to have tight feedback voltage accuracy across an extended die temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Capacitance reduction is also feasible when using a  $\pm 1\%$  feedback accuracy device over  $\pm 2\%$  devices. According to FPGA power requirements, an output voltage response to a line or load transient must not exceed  $\pm 5\%$  of the nominal 1.2V supply voltage.

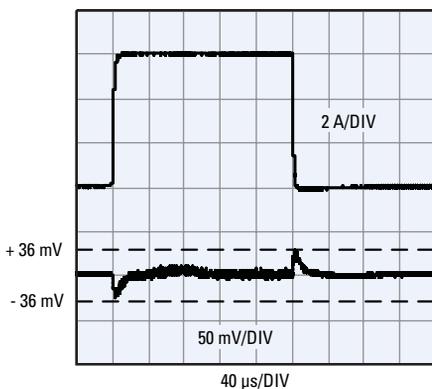
With a  $\pm 2\%$  DC accuracy device, this leaves the output voltage supply with only  $\pm 36\text{ mV}$  of allowable voltage swing. With a device DC accuracy of  $\pm 1\%$ , the allowable output voltage budget is now wider at  $\pm 48\text{ mV}$ .

In a typical example as shown in *Figures 4* and *5*, based upon a 350 mA to 6A load transient response, equal loop gain bandwidth and phase margin, a 1% device accuracy over a 2% device realizes a 50% reduction in output capacitance. A tighter feedback voltage accuracy specification can translate into lower-value capacitors, saving costs and total solution size.

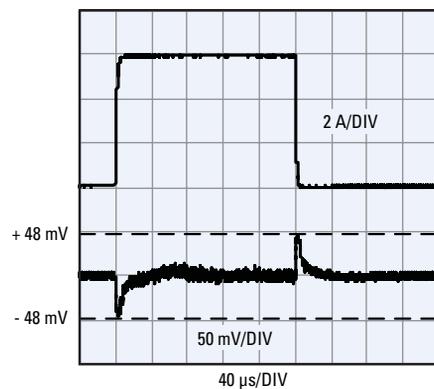
### Tracking and Precision Enable Features

Modern mixed-signal systems require multiple voltage supply rails which power the processor core, I/O, and other analog and digital circuits. Each voltage rail calls for a different voltage and load rating. The startup timing of each voltage rail, in reference to each other, is a critical requirement. Keeping the voltage differential minimized during powerup and/or keeping them sequenced will prevent latch-up, bus contention, and undesirable transistor logic states.

The precision enable feature provides sequential timing necessary for proper startup. A second method of sequencing is the tracking feature; this gives control to the master power supply over the slave's startup rise time. Two common tracking methods are ratio-metric, where the supply voltages reach their regulation point at the same time, and simultaneous startup, where the supply voltages increase with equal slew rates, as shown in *Figures 6* and *7*, respectively. Tracking and precision enable features allow several voltage rails to reach their nominal voltages within a specified target time.



**Figure 4. 2% Accurate Device with 940  $\mu\text{F}$  of Output Capacitance**



**Figure 5. 1% Accurate Device with 470  $\mu\text{F}$  of Output Capacitance**

## Optimizing Power Controller Designs through Effective Utilization of Performance Features

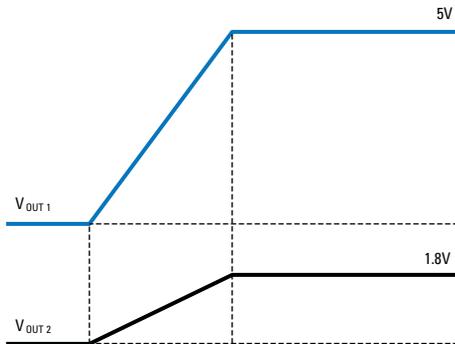


Figure 6. Ratio-Metric Tracking

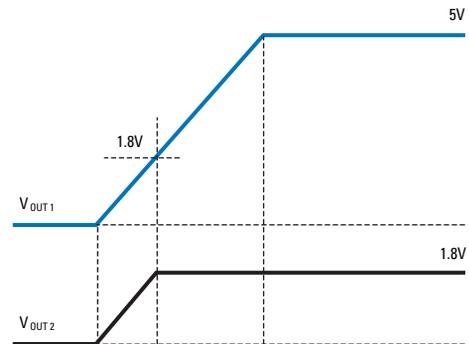


Figure 7. Simultaneous Tracking

### Pre-Biased Startup Feature

In reference to the SMPS, pre-biased startup is defined as starting up into a biased output rail. Common output voltage pre-biased situations include redundant power supplies, multiphase voltage regulator modules, or cycling of the SMPS under no load or light load conditions. Discharging the output capacitor may lead to conditions such as the voltage and current of one rail sneaking into the output of another rail through a parasitic p-n junction, which potentially may cause the leakage component to fail. Other loads may trigger the output POWER GOOD flag, output undervoltage protection, and/or the output current protection of the voltage regulator IC.

In many situations, accidentally discharging a pre-biased load on the output rail of a SMPS is not acceptable. Only regulators with synchronous rectification have the ability to discharge the output capacitor in a pre-biased condition through the

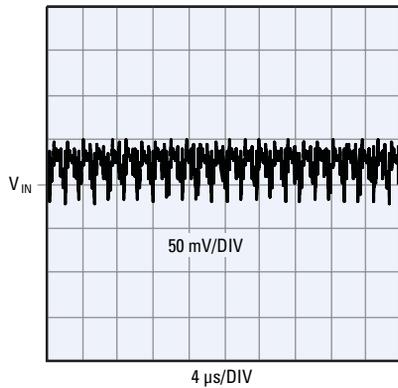
low-side MOSFET. Synchronous SMPSs equipped with soft-start pre-biased circuitry are able to sustain a charged output capacitor during the powerup period. This feature prevents the inadvertent discharge of the output rail during a pre-bias startup.

### External Reference Feature

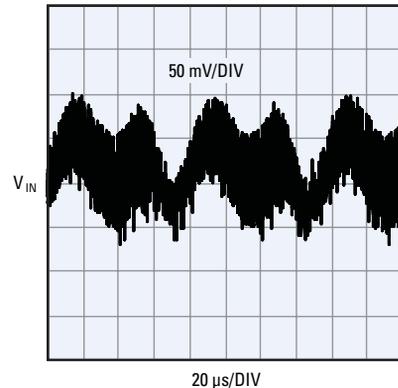
Regulators with an external reference feature can be advantageous in specific applications. One example of where the external reference feature proves beneficial is meeting double data rate (DDR) and DDR2 SDRAM termination specifications. DDR and DDR2 memory require a single power source for primary supply voltages (VDD) to ensure that all voltage levels track each other, especially critical during powerup. At initial powerup, all supply power should be stable and meet specification timing. The external reference voltage is expected to equal 1/2 VDD and must track variations in the DC voltage level. *Figure 8* shows a typical application circuit for a DDR2 solution.



## Optimizing Power Controller Designs through Effective Utilization of Performance Features



**Figure 9. Two Independent Internal Oscillators, Synchronized**



**Figure 10. Two Independent Internal Oscillators, Not Synchronized**

### Conclusion

The selection of appropriate devices with proper features can help satisfy system specifications and enhance the performance of the power supply and the load. Key features presented in this article: adjustable switching frequency, feedback voltage accuracy, startup tracking, power sequencing, pre-biased startup, utilizing an external reference, and synchronizing to an external clock, are incorporated in National Semiconductor's family of LM2742 through LM2748 high-performance controllers.

### References

1. *LM2747 Product Folder:*  
[www.national.com/pf/LM/LM2747.html](http://www.national.com/pf/LM/LM2747.html)
2. *Application Notes:*  
*AN-1603: LM274x Reference Designs:*  
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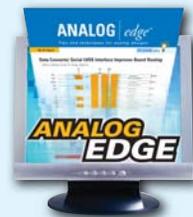
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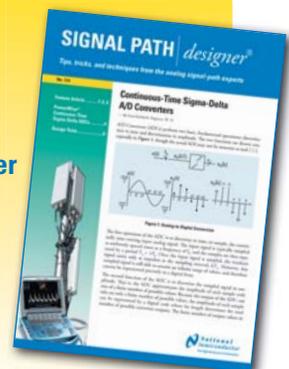


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