

AN-2119 LM8850 Evaluation Board Application Note

1 General Description

The LM8850 evaluation board is a working demonstration of a step-up DC-DC converter that has been optimized for use with a super-capacitor. The super-capacitor protects a battery from power surges and enables new high-power applications in mobile device architectures. The LM8850 creates an ideal rail from 3.6V to 5.7V from an input voltage range of 2.3V to 5.5V, V_{IN} must be 10% lower than expected V_{OUT}.

An I^2C interface controlling multiple output voltage settings, input current limits, and load currents up to 1A provides superior user flexibility. The LM8850 operates in Auto mode, where the converter is in PFM mode at light loads and switches to PWM mode at heavy loads or in forced PWM mode. Hysteretic PFM extends the battery life by reducing the quiescent current to 7μ A (typ.) during light load and standby conditions. Synchronous operation provides true shutdown isolation and improves the efficiency at medium to full load conditions.

High switching frequency enables smaller passive components. Internal compensation is used for a broader range of inductor and output capacitor values to meet system demand and achieve small system solution size.

2 Typical Application Circuit with Super-Capacitor

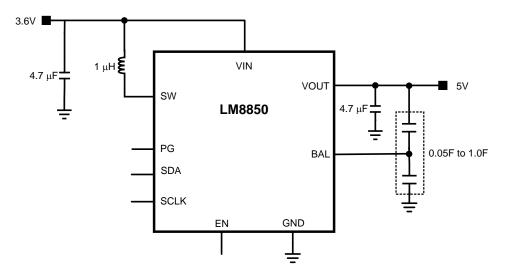


Figure 1. Typical Application



3 Connection Diagram and Package Mark Information

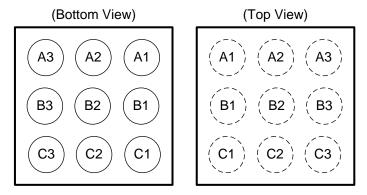


Figure 2. 9-Bump DSBGA Package

4 Block Diagram

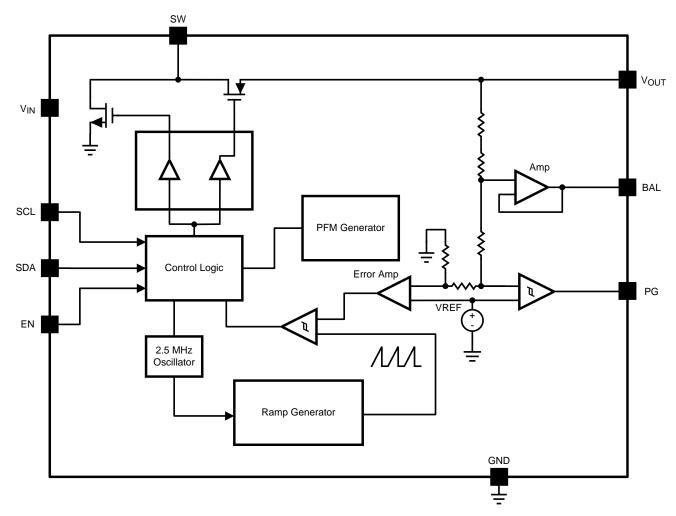


Figure 3. Block Diagram



www.ti.com Pin Descriptions

5 Pin Descriptions

Table 1. Pin Descriptions

Pin #	Name	Description	
A1	VIN	Power Supply Input. Connect to input filter capacitor (see Typical Application Circuit).	
A2	SW	Switching node. Connection to the internal NFET switch and PFET synchronous rectifier.	
А3	GND	Ground Pin	
B1	SDA	l ² C data (Use a 2kΩ pullup resistor.)	
B2	PG	Power Good indicator	
В3	VOUT	Output pin.	
C1	SCLK	l ² C Clock (Use a 2KΩ pull up resistor.)	
C2	EN	Enable pin. The device is in shutdown when voltage to this pin is < 0.4V and enabled when > 1.2V. Do not leave this pin floating.	
C3	BAL	Balancing pin for active voltage balancing of super-capacitor.	

6 Board Operation

To operate the LM8850, connections to VIN, Ground and the jumper on the enable pin must be in the H position. To start out, supply 3.6V to VIN. With a valid supply, Vout should power up to 5V within 5 seconds.

Once enabled, the LM8850 charges the supercapacitor utilizing all of the default settings in the registers. The I²C must be used to change the default settings and this can only be done with the LM8850 enabled. Once a register is written to, the changes will transition immediately. Every time the EN pin transitions from VIL to VIH, registers 0 and 1 are reset to their defaults settings and any settings needed bust rewritten into the appropriate registers.

7 I²C-Compatible Chip Address

The device address for LM8850 is 60 (HEX).

Register Name	Location Type		Register	
CONTROL	00	R/W	Control Register 0 (Figure 4)	
CONTROL	OL 01 R/W C		Control Register 1 (Figure 5)	



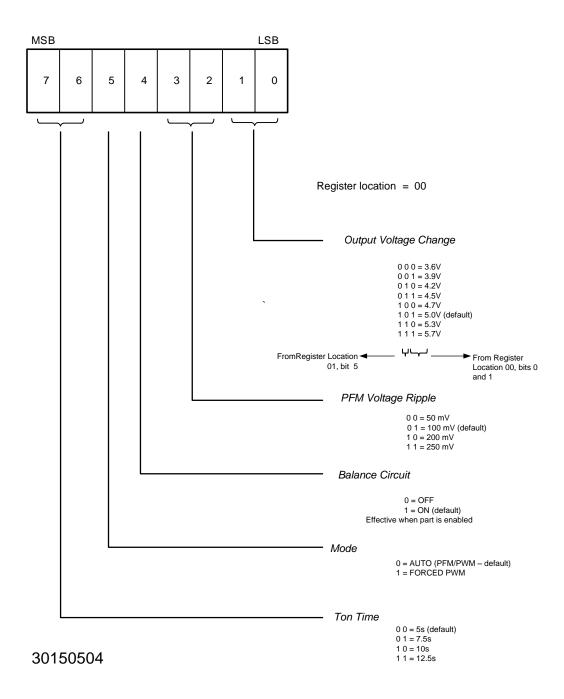


Figure 4. CONTROL Register 0
Register Location = 00



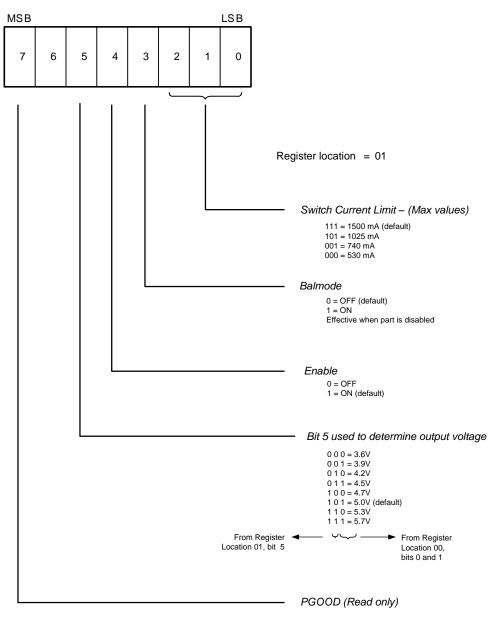
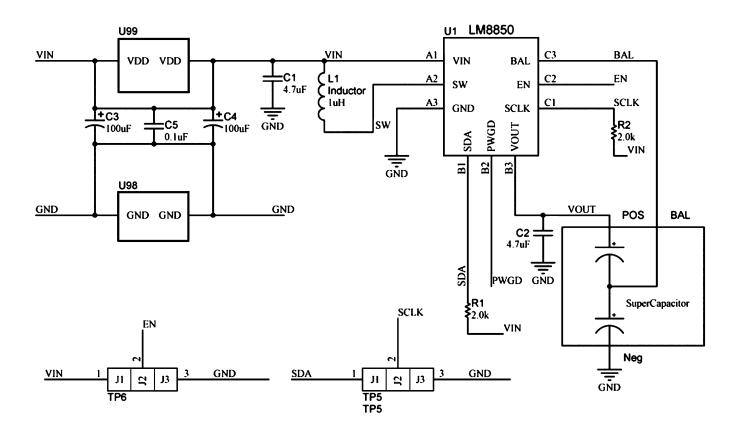


Figure 5. CONTROL Register 1
Register Location = 01



8 LM8850 Evaluation Board Schematic



9 LM8850 Evaluation Board Bill of Materials

Table 2. Bill of Materials

Item	Qty	Value	Part Number	Description
C1 (CIN)	1	10 μF	C1608X5R0J106M	0603, 6.3V, TDK
C2 (COUT)	1	4.7 μF	CL10A475KP8NNNB	0603, 10V, SAMSUNG
C3 = C4 (FILTER CAP)	2	100 µF	TPSC107M006R0075	0805, 10V, AVX
C5 (AC FILTER CAP)	1	100 nF	CL05F104Z05NNB	0402, 10V, SAMSUNG
L1	1	1μF	KSLI-252012AG-1R0	2520, 1.5A, HITACHI
VDD CONNECTOR	1	-	93K4533	NEWARK
GND CONNECTOR	1	-	80P3616	NEWARK
SuperCapacitor	1	500Mf	EDLC272020-501-2F-50	Super Capacitor
U1	1		LM8850	Boost Regulator
Total	10			



10 LM8850 Evaluation Board Layers

There are a few solder mask openings for various supercapacitor packages. If you plan on changing to a different supercapacitor than what is initially assembled, be sure assemble using the best solder pad openings for your supercapacitor footprint. Below, in the circled areas, are the initial pads used for the TDK supercap initially assembled. If the given pads aren't acceptable, the solder mask can be removed to expose the copper for any footprint needed.

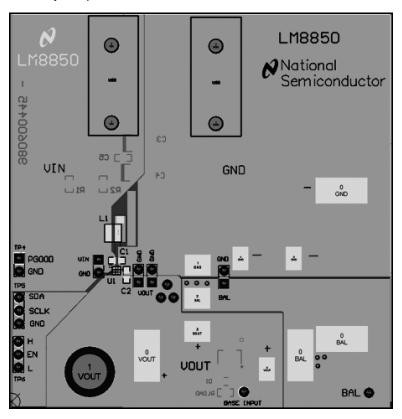


Figure 6. Top Layer



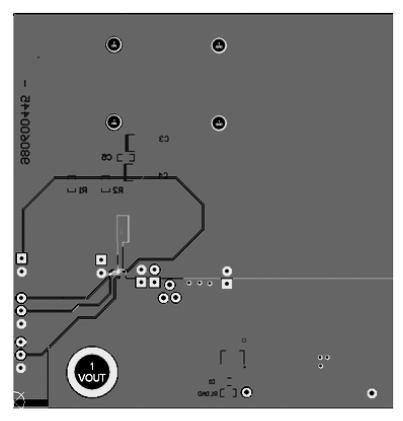


Figure 7. Mid- Layer 1

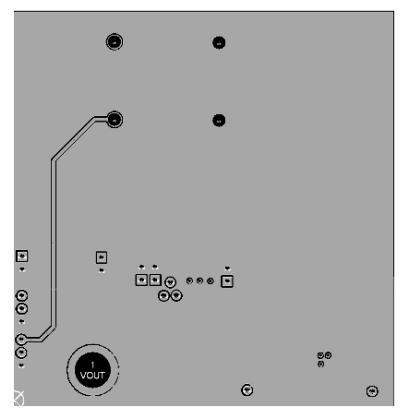


Figure 8. Mid- Layer 2



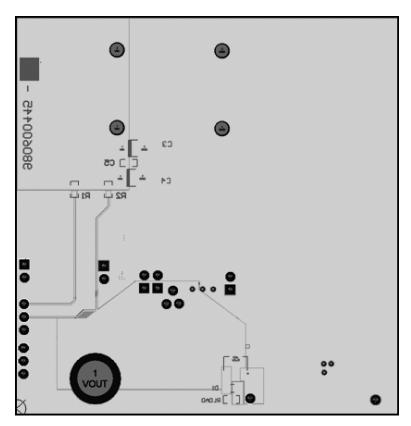


Figure 9. Bottom Layer

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