ADC12QS065

Data Converter Serial LVDS Interface Improves Board Routing

Literature Number: SNAA110

Vol. III, Issue 8

ANALOG | edge℠

DESIGN | idea: Serial LVDS Improves Routing ▶ ▶

Featured Products

Differential, High-Speed Op Amps

The LMH6550 and LMH6551 are high-performance voltage feedback differential amplifiers. The fully differential topology allows balanced inputs to the ADCs and can be used as single-ended-to-differential or used as differential-to-differential. These amplifiers also have the high speed and low distortion necessary for driving high-performance ADCs, as well as the current-handling capability to drive signals over balanced transmission lines like CAT-5 data cables. The LMH6550/51 can handle a wide range of video and data formats.

With external gain set resistors, the LMH6550/51 can be used at any desired gain. Gain flexibility coupled with high speed makes these amplifiers suitable for use as IF amplifiers in high-performance communications equipment.

LMH6550 Features

- 400 MHz, -3 dB bandwidth (V_{OUT} = 0.5 V_{PP})
- 90 MHz, 0.1 dB bandwidth
- -92/-103 dB HD2/HD3 at 5 MHz (changed order)
- 3000 V/µs slew rate
- -68 dB balance error (V_{OUT} = 1.0 V_{PP}, 10 MHz)
- 10 ns shutdown/enable

LMH6551 Features

- 370 MHz, -3 dB bandwidth (V_{OUT} = 0.5 V_{PP})
- 50 MHz, 0.1 dB bandwidth
- -94/-96 dB HD2/HD3 at 5 MHz (changed order)
- 2400 V/µs slew rate
- -70 dB balance error (V_{OUT} = 0.5 V_{PP}, 10 MHz)
- Single +3.3V, +5V, or ±5V supply voltages

The LMH6550/51 is ideal for use in applications requiring a differential A/D driver, video twisted pair, differential line driver, single end-to-differential converter, high-speed differential signaling, IF/RF amplifier, or SAW filter buffer/driver.

The LMH6550/51 are available in the space-saving SOIC-8 and MSOP-8 packaging.

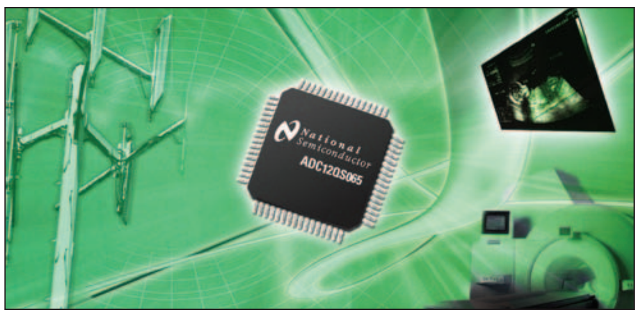
www.national.com/pf/LM/LMH6550.html
www.national.com/pf/LM/LMH6551.html

Low-Power, High-Performance Quad 12-Bit A/D Converter with Serialized LVDS Outputs

The ADC12QS065 is a low-power, high-performance, 4-channel analog-to-digital converter with serialized LVDS outputs. This A/D converter digitizes signals to 12-bit resolution at sampling rates up to 65 MSPS while consuming a typical 187.5 mW per ADC from a single 3.0V supply. Sampled data is transformed into high-speed serial LVDS output data streams. Clock and frame LVDS pairs aid in data capture. The six differential pairs of the ADC12QS065 transmit data over backplanes or cable and simplify PCB design. In addition, the reduced cabling, PCB trace count, and connector size greatly reduce system cost.

Features

- Serialized LVDS outputs allow for lower pin count packages
- Saves space for number of channels
- Pin assignment optimized for board layout
- Low power consumption
- Excellent signal-to-noise ratio, THD, and crosstalk
- Samples signals as fast as 65 MSPS



The speed, resolution, and single-supply operation of the ADC12QS065 make it well suited for a wide variety of applications in ultrasound, medical imaging, communications, portable instrumentation, and digital video.

Operating over the industrial (-40°C to +85°C) temperature range, the ADC12QS065 is available in a TQFP-64 package.

www.national.com/pf/DC/ADC12QS065.html

DESIGN | *idea*

Robert LeBoeuf
Senior IC Design Engineer
National Semiconductor

Data Converter Serial LVDS Interface Improves Board Routing

Systems often require signaling where common-mode signals are not welcome or difficult to handle. Some designs turn single-ended signals from the output of transducers to fully differential signals, then send this signal to a differential-input ADC downstream. The advantage of this is that most noise that gets introduced on this differential line is common to both lines. (This is assuming that the differential lines are laid out symmetrically.)

After the input signals are converted to digital data, they must be transmitted to a DSP or an ASIC/FPGA for processing. This is where fully-differential output signaling can come in handy. Output signals that are fully differential source and sink a current through two symmetric lines. An example of such signaling is the LVDS (Low Voltage Differential Signal) format. The ADC12QS065 uses LVDS to solve all of these system issues (*Figure 1*).

The ADC12QS065 contains four 12-bit ADCs in one chip. Each of its inputs accepts fully-differential signals. The input common-mode voltage may be derived from the common-mode output reference voltages VCOM12 and VCOM34 that are supplied by the ADC12QS065. The ADC12QS065 also has the option of using a fully-differential, or single-ended clock source. To utilize the LVDS clock simply provide LVDS signals to the CLK and CLKB, terminating close to the input

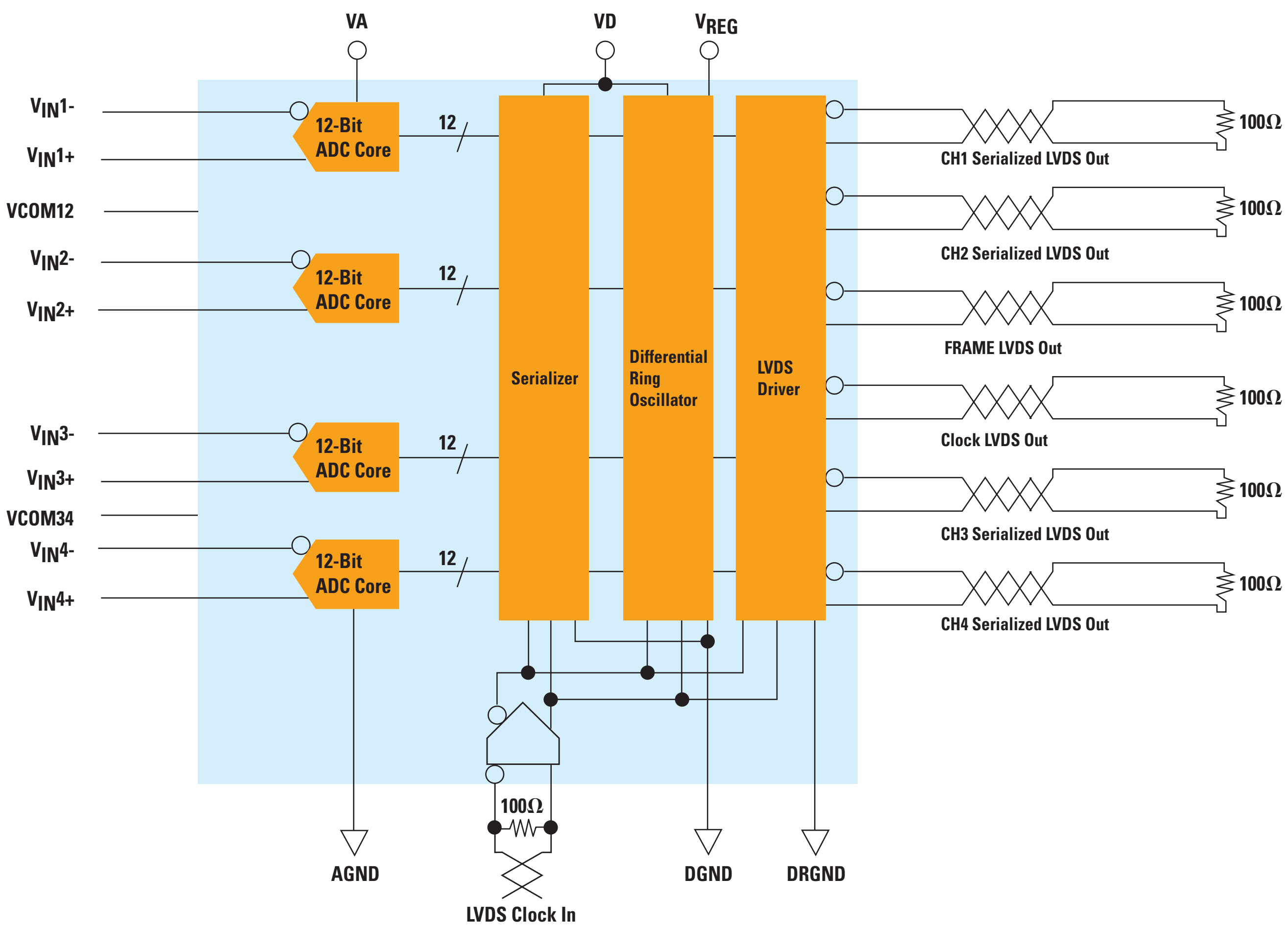


Figure 1. ADC12QS065 Simplified Block Diagram

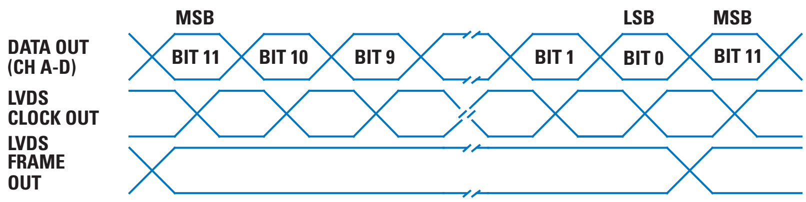


Figure 2. Output Timing Diagram

pins. If a single-ended CMOS clock is desired, then CLKB is tied low, and no termination resistor is required.

The output of each ADC gets serialized using a differential ring oscillator. The input clock input is multiplied by 12, and converted to an LVDS clock output for data capture. An LVDS FRAME signal, at the input clock rate, is also generated at the output to identify the sample number (*Figure 2*).

The output timing offers easy data capture for an FPGA. The output FRAME signals when sampled data is ready to be sent. The MSB of each of the 4 output channels is present, followed by an LVDS CLOCK OUT transition. The LVDS CLOCK OUT signal is offset from the DATA OUT by a quarter cycle to ease clock management. Each data bit is captured on a CLOCK OUT transition. Another advantage of using LVDS is that these signals may be sent down a twisted pair that uses the EIA/TIA 568 standard. Twisted pairs that meet this standard have a characteristic impedance of 100Ω. Conductors that are close together and carry opposite currents produce very low radiation. This is welcome in areas where high SNR requirements are present.

To further illustrate this point, *Figure 3* shows two 4-channel, 12-bit ADCs. The ADC on the left has the traditional single-ended parallel CMOS output. 49 traces are required (4x12+1) to send the converter output to the digital processor. If the output bits are serialized, each channel would have a single pair of differential lines. An output clock and frame signal wires are also illustrated.

Because LVDS uses current from the supply by 'steering' current from one LVDS terminal or the other, current is constantly being drawn from the supply. This reduces the switching load that would otherwise be present on the supply lines. The advantage to this is that lower supply noise is induced on the supply line, reducing the decoupling capacitor size, and relaxing layout requirements.

Serial LVDS allows for an even smaller package and is very effective in signal transmission. In many applications, however, low power consumption is very important. Every milliwatt of power saved per channel makes a significant difference in systems requiring several channels of data. Therefore, in addition to quiet drivers, the ADC12QS065 has three separate power supplies. Each supply can be connected making it a single-supply ADC, or kept separate. Separate supplies further isolate each part of the internal circuitry of the ADC. This may be achieved with one supply and passive filters employed at each power supply input, or separate supplies altogether. Another advantage separate supplies is the output driver voltage may be reduced as low as 2.5V, to save on power consumption.

The ADC12QS065 also has the ability to have its internal references powered down to allow the reference to be driven externally. This allows multiple ADCs to be 'ganged' together, by connecting all the V_{REF}Ps and V_{REF}Ns together, respectively. This eases system calibration requirements by helping to insure that the gain and offset of each chip match.

It's clear that if systems allow for differential signaling, it is advantageous in terms of low common-mode noise induction, reduced power supply transients, and low digital radiation on the output lines. The ADC12QS065 offers a fully-differential conversion, from the analog input, clock input, to the serialized LVDS outputs. This ability to separate the power supplies allows for further analog-digital domain separation, and offers lower power consumption. ■

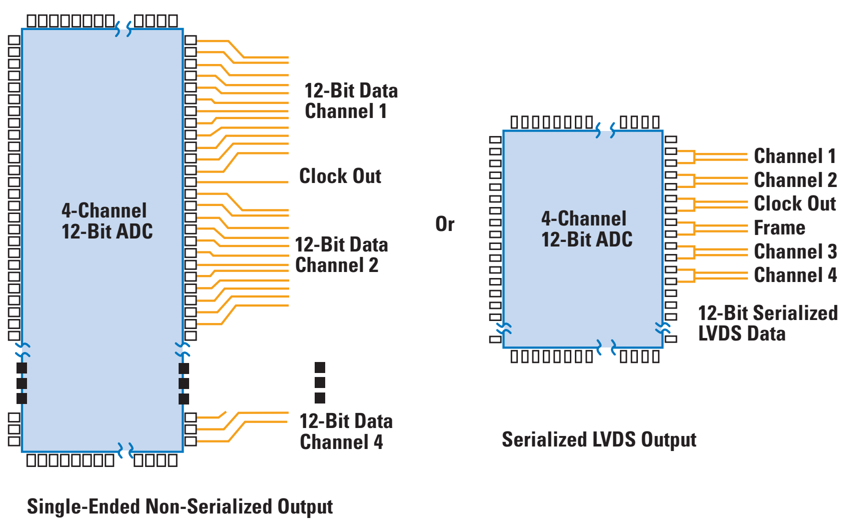


Figure 3. CMOS vs LVDS Board Layout Comparison

Featured Products

High-Performance, Low-Power, Dual 8-Bit, 500 MSPS A/D Converter

The ADC08D500 is the industry's lowest power dual 8-bit 500 MSPS analog-to-digital converter. It digitizes two signals to 8-bit resolution at sampling rates up to 800 MSPS or one signal at sampling rates up to 1.6 GSPS. Consuming a typical 1.4 W at 500 MSPS from a single 1.9V supply, this device is guaranteed to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier, and the self-calibration scheme enable a very flat response of all dynamic parameters beyond Nyquist.

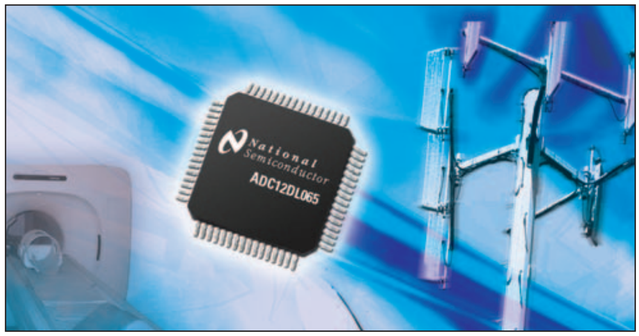
Features

- 7.5 Effective Number of Bits (ENOB) at Nyquist (typ)
- Bit error rate 10^{-18} (typ)
- Single +1.9V (±0.1V) operation
- Interleave mode for 2x sampling rate
- Choice of SDR or DDR output clocking
- Multiple ADC synchronization capability
- Serial interface for extended control
- Fine adjustment of input full-scale range and offset

The ADC08D500 is ideal for use in direct RF down conversion, digital oscilloscopes, satellite set-top boxes, communications systems, and test instrumentation.

This A/D converter is available in a thermally-enhanced exposed pad LQFP-128 and operates over the industrial (-40°C to +85°C) temperature range.

www.national.com/pf/DC/ADC08D500.html



Dual 12-Bit, 65 MSPS, 3.3V, 360 mW A/D Converter

The ADC12DL065 is a dual, low-power CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 65 MSPS. This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize power consumption while providing excellent dynamic performance and a 250 MHz full power bandwidth. Operating on a single +3.3V power supply, the ADC12DL065 achieves 11.0 effective bits at Nyquist and consumes just 360 mW at 65 MSPS, including the reference current. The power down feature reduces power consumption to 36 mW.

Features

- 11.0 ENOB at Nyquist (typ)
- SNR = 68.5 dBc with f_{IN} = 10 MHz (typ)
- SFDR = 85 dBc with f_{IN} = 10 MHz (typ)
- Consumes only 360 mW at 65 MSPS
- Outputs 2.4V to 3.6V compatible
- Power down mode
- Duty cycle stabilizer
- Multiplexed output mode simplifies board routing

The ADC12DL065 is ideal for use in ultrasound and imaging, instrumentation, communications receivers, sonar/radar, xDSL, cable modems, and DSP front ends.

This device is available in a TQFP-64 package and will operate over the industrial temperature range of -40°C to +85°C.

www.national.com/pf/DC/ADC12DL065.html

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
		TI E2E Community Home Page	e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265