

High Speed Communications Solutions

TSW2000: TLK1201A and CDC7005

Low-Power, CPRI-Compliant Gigabit SerDes with Low-Jitter Clock Distribution Device

Today's wireless infrastructure equipment suppliers require solutions that can be easily integrated into their architectures without sacrificing performance and flexibility. Texas Instrument's Gigabit SerDes device, TLK1201A, and its low jitter clock distribution device, CDC7005, provide a powerful combination for implementing CPRI-compliant links from 600 Mbps to 1.3 Gbps.

TI introduces the TSW2000 evaluation module (EVM) which provides a complete solution for implementing CPRI-compliant data links using TI's TLK1201A Gigabit serializer/deserializer (SerDes) along with the CDC7005 clock synchronizer. The TLK1201A is a Gigabit Ethernet-compliant SerDes that is capable of transmitting and receiving serial line rates data from 600 Mbps to 1.3 Gbps point-to-point.

Serial point-to-point links over copper cable and FR4 backplanes can easily be implemented using the TLK1201A and CDC7005. The TLK1201A's low-power dissipation of 300 mW enables equipment suppliers to stay within constrained power budgets while system port density increases.

Key Features – TLK1201A

- 600 Mbps to 1.3 Gbps data rate range
- <300 mW power dissipation
- Single 2.5 V supply

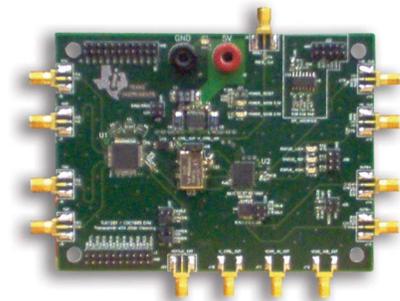
Key Features – CDC7005

- Jitter cleaner
- Five independent frequency outputs selectable by /2ⁿ
- LVPECL interface
- Single 3.3 V supply

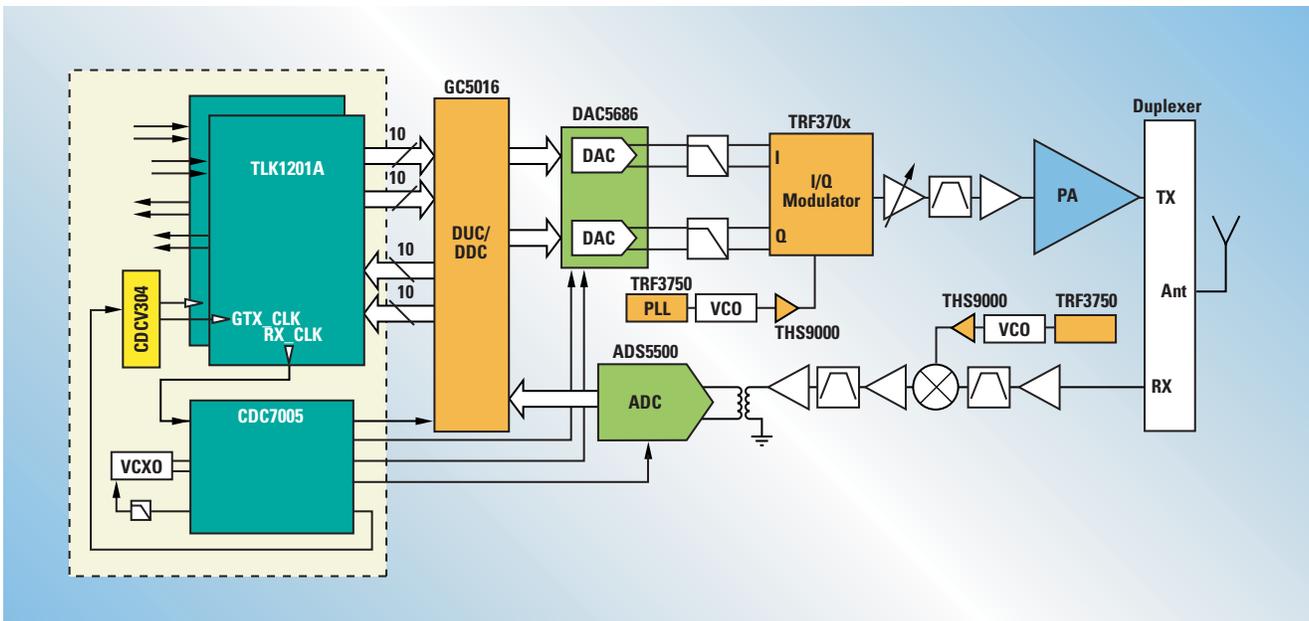
Applications

- Wireless base station receivers
- Radio card to controller card links
- Medical imaging and monitoring
- Communication test equipment
- Digital imaging
- Data communications equipment

TSW2000 Evaluation Module



TSW2000: TLK1201A and CDC7005 Solution as an Integral Part of the Radio Unit



In order to achieve the full performance of the TLK1201A, a suitable low-jitter reference clock is required at the desired sampling rate. The CDC7005 is a high performance, low-jitter clock solution that synchronizes an on-board voltage controlled crystal oscillator (VCXO) to an external reference clock.

The CDC7005 has five independent outputs that can be used to satisfy the most stringent clocking requirements. Each output can be independently divided down by 2^n ($n = 0$ to 4) to supply the clock signal for a multitudinous of devices within the BTS including SerDes, digital up and down converters (DUC/DDC), digital-to-analog converters (DAC), and other analog-to-digital converters (ADC).

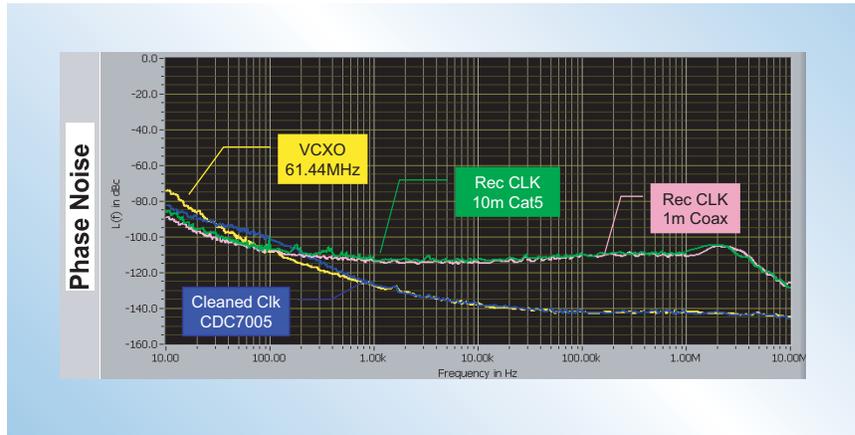
The TSW2000 EVM is equipped with a low-phase noise 122.88/61.44 MHz VCXO. Once

proper reference frequency and programming is applied, the CDC7005 supplies the clock source suitable for high speed SerDes devices like the TLK1201A. The EVM provides a complete reference solution for implementing CPRI-compliant physical layer solutions (614.4 Mbps/1.2288 Gbps)

along with the requisite reference clocking. The TSW2000 is intended to help systems developers quickly and economically implement standards-compliant physical layer solutions with their systems.

For more information about the TSW2000, please visit us at www.ti.com/hscsolutions

TSW2000: PhaseNoise Measurements at 61.44 MHz



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