TPS50601SPEVM, 6-A/12-A, SWIFT™ Regulator Evaluation Module

This user's guide contains background information for the TPS50601 as well as support documentation for the TPS50601 evaluation modules (TPS50601SPEVM-S and TPS50601SPEVM-D). Also included are the performance specifications, the schematic, and the bill of materials for TPS50601SPEVM.

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1 Introduction

1.1 Background

The TPS50601 dc/dc converter is designed to provide up to a 6-A output in single phase operation and up to 12 A in dual phase operation, when each phase is configured to provide 6-A per phase.

TPS50601 Dual EVM can also be configured such that each phase provides 3 A and with current sharing between phase 1 and phase 2 total of 6 A can be provided to meet system needs. This configuration will provide higher reliability (MTBF) for system needs due to reduced stresses on components and higher efficiency.

The TPS50601 implements split-input power rails with separate input voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 6.3 V while the control input (VIN) is rated for 3 V to 6.3 V. The TPS50601 provides both inputs but is designed and tested using the PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate features of TPS50601 as well as provide flexibility so input, output capacitors and output inductors as well as other components such as frequency adjust, output voltage and compensations components can be modified to meet their needs when designing with the TPS50601 regulator. The switching frequency is externally set at a nominal 100 kHz. TPS50601 will operate with switching frequency of 100-kHz to 1-MHz range. For the EVM 100 kHz was selected as it would provide higher efficiency. The high-side and low-side MOSFETs are incorporated inside the TPS50601 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS50601 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS50601 provides adjustable slow start, tracking, and undervoltage lockout inputs. The absolute maximum input voltage is 7 V for the TPS50601SPEVM.

The TPS50601SPEVM can also be configured to operate as two single voltages; i.e. 2.5 V and 1.8 V or a dual phase operation such that the two phases can be paralleled thus being capable of providing 12-A steady state load to meet system needs. Operating two TPS50601 circuits in parallel which will allow increased current capability also requires certain techniques that will allow the two converters (phases) to share equal current. The user's guide will highlight the configurations required to meet the high current system needs. A separate application note will detail the design details.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS50601SPEVM	VIN = 4.25 V to 6.3 V (VIN start voltage = 4.42 V)	0 A to 6 A

1.2 Performance Specification Summary

A summary of the TPS50601SPEVM performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 5 V and an output voltage of 2.5 V, unless otherwise specified. The TPS50601SPEVM is designed and tested for V_{IN} = 4.25 V to 6.3 V with the VIN and PVIN pins connect together with the J2/J5 jumper. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS50601SPEVM Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range (PVIN = VIN)			4.25	5	6.3	V
V_{IN} start voltage				4.42		V
V_{IN} stop voltage				4.25		V
Output voltage set point				2.49		V
Output current range	V_{IN} = 4 V to 7 V		0		6	A
Line regulation	I_O = 3 A, V_{IN} = 4.25 V to 6.3 V			0.1		%
Load transient response	I_O = 1.5 A to 4.5 A	Voltage change		160		mV
		Recovery time		320		µs
	I_O = 4.5 A to 1.5 A	Voltage change		150		mV
		Recovery time		320		µs
Loop bandwidth	V_{IN} = 5 V, I_O = 6 A			8.9		kHz
Phase margin	V_{IN} = 5 V , I_O = 6 A			55		°
Input ripple voltage	I_O = 6 A			150		mVPP
Output ripple voltage	I_O = 6 A			25		mVPP
Output rise time				4		ms
Operating frequency				100		kHz
Maximum efficiency	TPS50601SPEVM , V_{IN} = 5 V, I_O = 2 A			93		%

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS50601. Some modifications can be made to this module. Layout of EVM is made thus making it easy for customer to modify the configuration to meet their needs to adjust for different input, output capacitors and output inductors.

1.3.1 Output Voltage Set Point

The output voltage is set by the resistor divider network of R15 and R38. R15 is fixed at 10 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R38. Changing the value of R38 can change the output voltage above 0.8 V. The value of R38 for a specific output voltage can be calculated using Equation 1.

$$R38 = \frac{(V_{REF} \cdot R15)}{V_{OUT} - V_{REF}} \quad (1)$$

Where V_{REF} = 0.795 V

Table 3 lists the R38 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 135 ns, and the maximum duty cycle is less than 85%. The values given in Table 3 are standard values, not the exact value calculated using Equation 1.

Table 3. Output Voltages Available

Output Voltage (V)	R38 Value (kΩ)
1.2	20
1.8	8.06
2.5	4.7
3.3	3.2

1.3.2 Maximum Duty Cycle Limit

The TPS50601 can operate at high duty cycle as long as the boot capacitor voltage is higher than the preset BOOT-PH UVLO threshold which is typically 2.1 V.

Refer to Figure 17 in the datasheet (SLVSA94) for max duty cycle limits for operation over different operating frequencies.

Duty cycle can be calculated based on Equation 2:

$$D(V_{IN}) = \frac{V_{OUT} + I_{OUT\_max} \bullet R_{Tesr} + I_{OUT\_max} \bullet R_{ds\_low}}{V_{IN} - I_{OUT\_max} \bullet R_{ds\_high} + I_{OUT\_max} \bullet R_{ds\_low}} \quad (2)$$

Where

$R_{Tesr} = R_{dcr} + R_{trace}$
R_{dcr} is the DC resistance of the inductor.
R_{trace} is the DC trace resistance (miscellaneous drop).
R_{ds_high} is the maximum R_{DS} of the high side MOSFET.
R_{ds_low} is the maximum R_{DS} of the low side MOSFET.

1.3.3 Slow-Start Time

The slow-start time can be adjusted by changing the value of C33. Use Equation 3 to calculate the required value of C33 for a desired slow-start time

$$C33(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)} \quad (3)$$

The EVM is set for a slow-start time of 4 ms using C33 = 0.01 µF and I_{SS} = 2.5 µA.

1.3.4 Track In

Many of the common power supply sequencing methods can be implemented using TPS50601 as outlined in the datasheet (SLVSA94) per Figure 22, Figure 23 and Figure 24. Ratio-metric or simultaneous tracking can be implemented using resistor divider R27 and R28 on EVM.

1.3.5 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R6 and R7. The EVM is set for a start voltage of 4.42 V and a stop voltage of 4.23 V using R6 = 10 kΩ and R7 = 2.5 kΩ. Use Equation 4 and Equation 5 to calculate required resistor values for different start and stop voltages.

Where I_h = 3 µA, I_p = 3.2 µA, $V_{ENRISING}$ = 1.131 V, $V_{ENFALLING}$ = 1.09 V.

$$R6 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (4)$$

$$R7 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R6(I_p + I_h)} \quad (5)$$

2 Synchronization (SYNC)

An external synchronization mode requires that an external sync signal be applied at J12. This signal must be within 10% of converter switching frequency. EVM is set to operate at switching frequency of 100 kHz set by resistor R8. Applying an external sync signal of 100 kHz at J12 with synchronize the two phases in dual mode configuration.

Maximum duty cycle is limited by minimum on time as specified in the datasheet.

2.1 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected together using a jumper across J2/J5. The single input voltage is supplied at J7. If desired, these input voltage rails may be separated by removing the jumper across J2/J5. Two input voltages must then be provided at both J7 (PVIN) and J8 (VIN).

3 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS50601-SP evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

3.1 Input/Output Connections

The TPS50601SPEVM is provided with input/output connectors and test points as shown in Table 4. A power supply capable of supplying 18 A must be connected to J7 through a pair of 16 AWG wires. The jumper across J2/J5 must be in place. See Section 2.1 for split-input voltage rail operation. The load must be connected to J10/J9 through a pair of 16 AWG wires. The maximum load current capability must be 6 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP9/TP15 is used to monitor the output voltage with TP10 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	PVIN input voltage connector (see Table 1 for V_{IN} range)
J8	VIN input voltage connector. Not normally used.
J2/J5	PVIN to VIN jumper. Normally closed to tie VIN to PVIN for common rail voltage operation.
J3/J6	2-pin header for enable. Connect EN to ground to disable, open to enable.
J1/J4	Connecting phase 1 output to phase 2 output for Dual Operation
J12	External Sync connection
J9/J10	V_{OUT}, 2.5 V at 6 A maximum for Single EVM and 12 A for Dual EVM
TP1	PVIN test point at PVIN connector
TP2	GND test point at PVIN connector
TP3	VIN test point at VIN connector
TP4	GND test point at VIN connector
TP17/TP20	Cold note probe to monitor Switch/Phase node
TP18/TP19	Cold nose probe to monitor output voltage/ripple
TP9/TP15	Output voltage test point at VOUT connector
TP10/TP16	GND test point at VOUT connector
TP6/TP11	PWRGD test point

3.2 Efficiency

The efficiency of this EVM peaks at a load current of about 2 A and then decreases as the load current increases towards full load. Figure 1 shows the efficiency for the TPS50601SPEVM at an ambient temperature of 25°C.

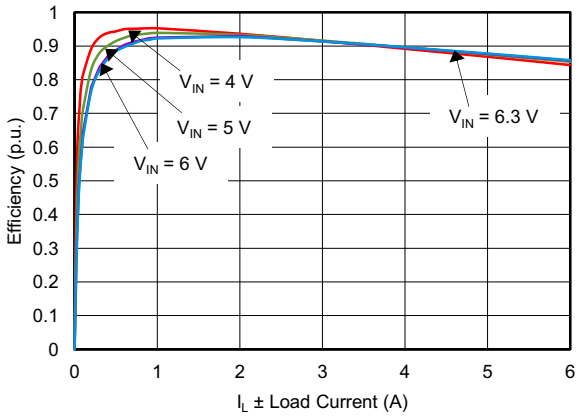


Figure 1. TPS50601SPEVM Efficiency

Figure 2 shows the efficiency for the TPS50601SPEVM at lower output currents below 0.10 A at an ambient temperature of 25°C.

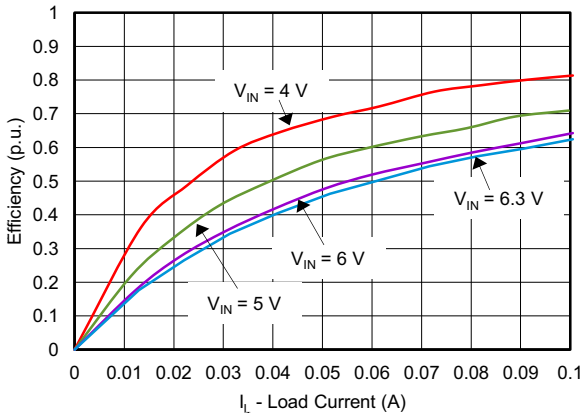


Figure 2. TPS50601SPEVM Low-Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

3.3 Output Voltage Line Regulation

Figure 3 shows the line regulation for the TPS50601SPEVM.

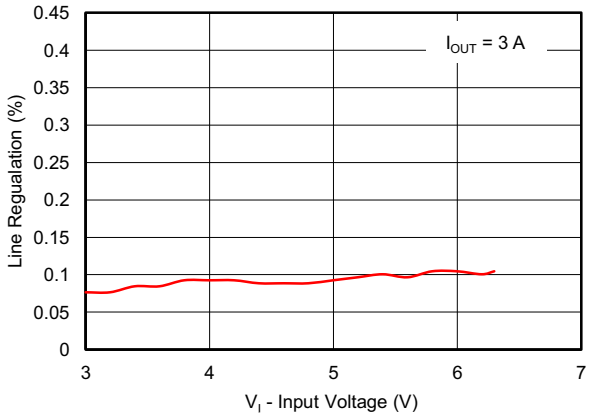


Figure 3. TPS50601SPEVM Line Regulation

3.4 Load Transients

Figure 4 shows the TPS50601SPEVM response to load transients. The current step is from 25% to 75% of maximum rated load at 5-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

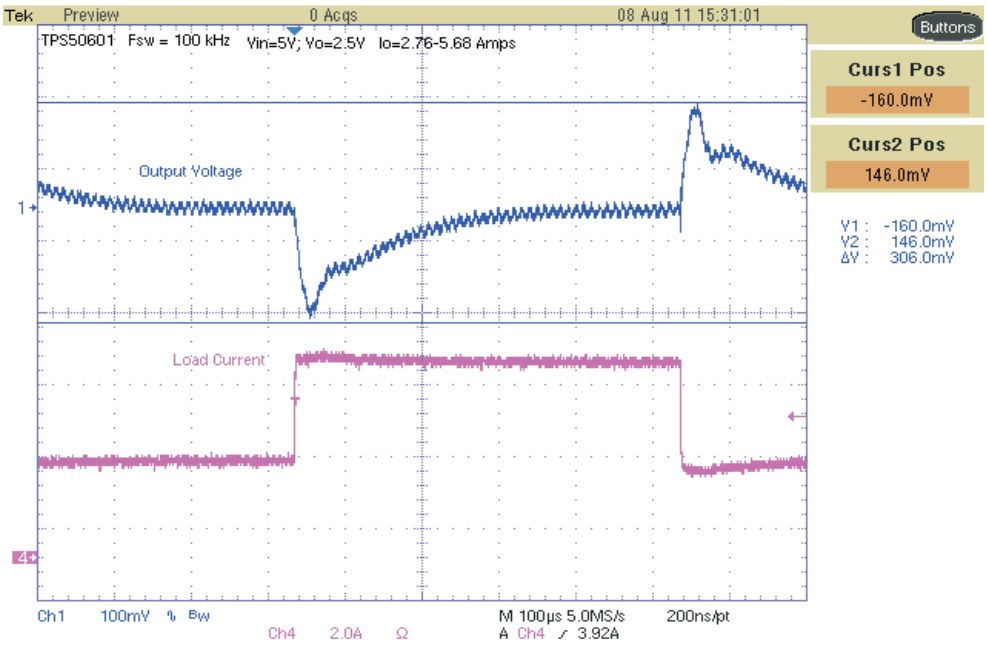


Figure 4. TPS50601SPEVM Transient Response

3.5 Power Stage Gm

Figure 5 below shows the plot of the power stage Gm (output load vs. comp pin voltage).

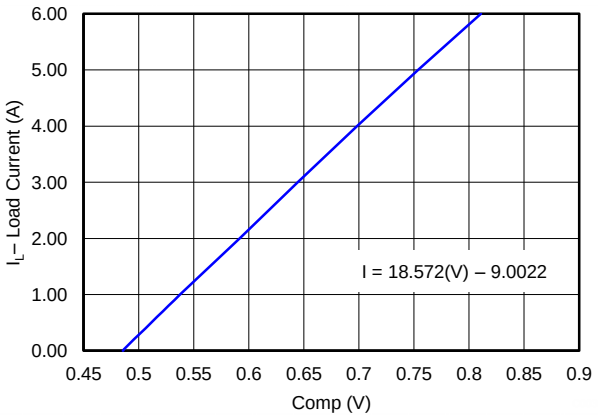


Figure 5. Power Stage Gm

3.6 Loop Characteristics

Figure 6 shows the TPS50601SPEVM loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 5 V. Load current for the measurement is 6 A.

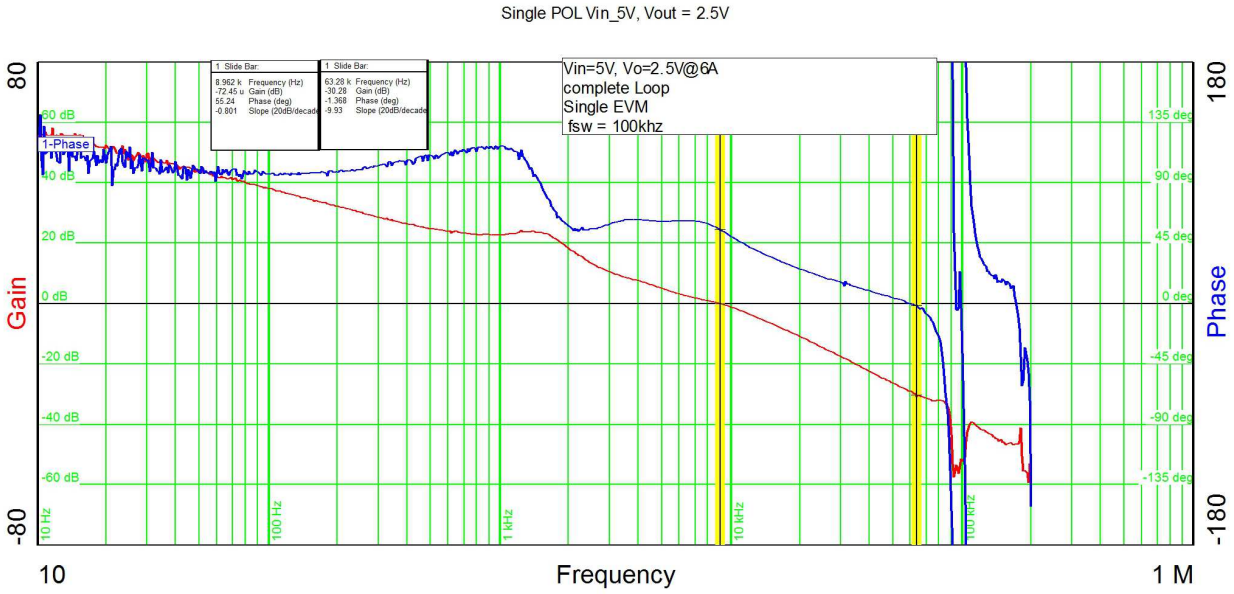


Figure 6. TPS50601SPEVM Loop Response
V_{IN} = 5V, V_{OUT} = 2.5V @ 6A

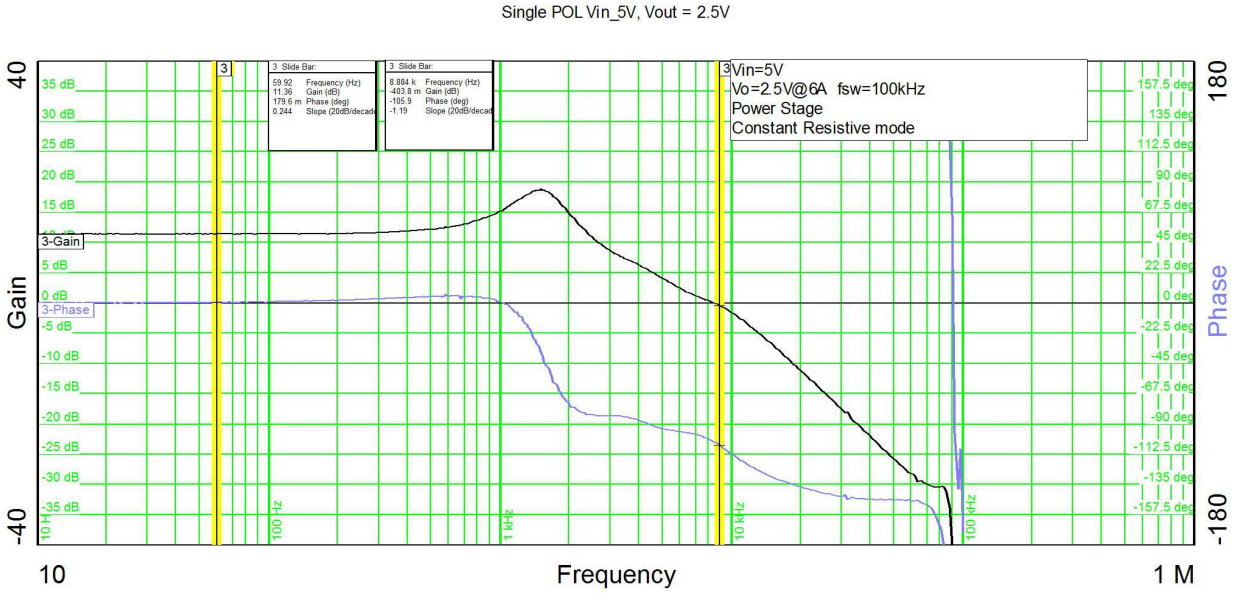


Figure 7. TPS50601SPEVM Power Stage
V_{IN} = 5V, V_{OUT} = 2.5V @ 6A

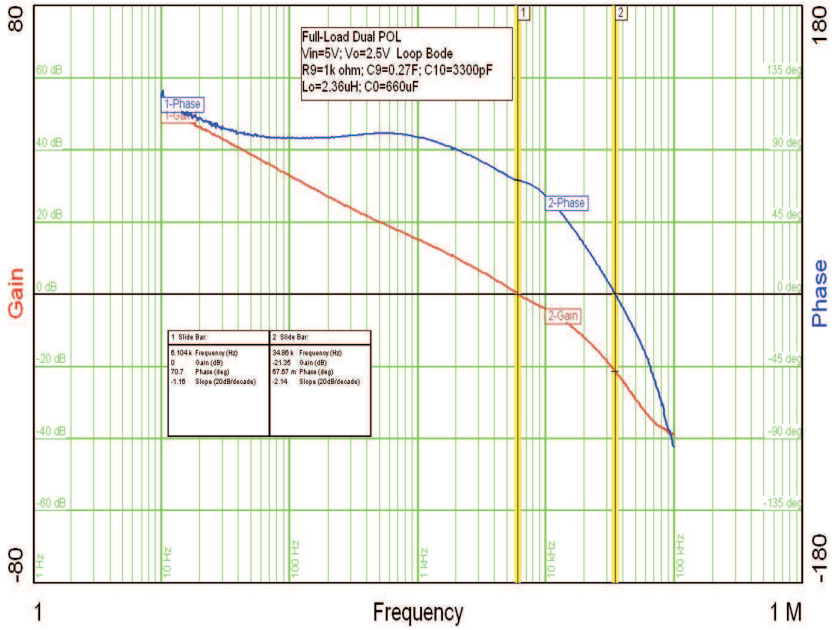


Figure 8. TPS50601SPEVM Loop Response Dual Mode
V_{IN} = 5V, V_{OUT} = 2.5V @ 12A

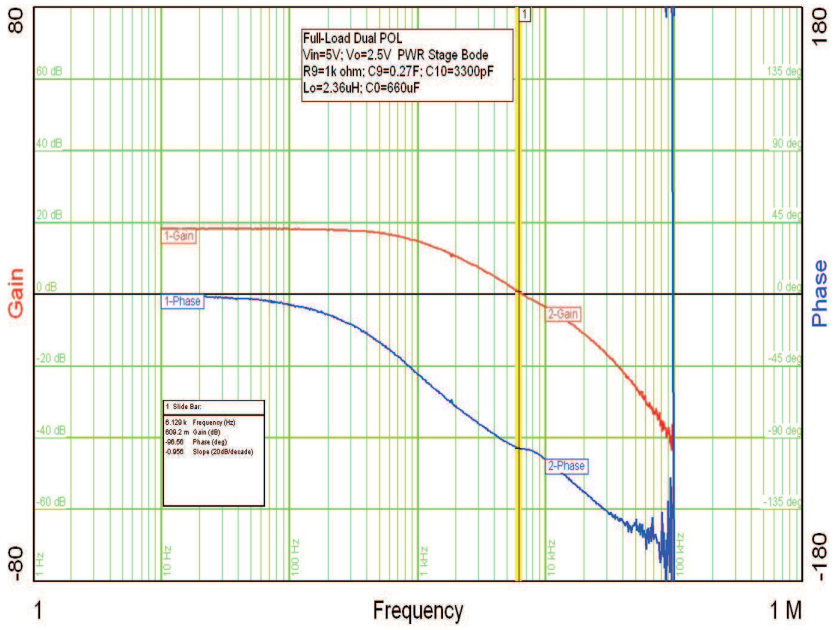


Figure 9. TPS50601SPEVM Power Stage Dual Mode
V_{IN} = 5V, V_{OUT} = 2.5V @ 12A

3.7 Output Voltage Ripple

Figure 10 shows the TPS50601SPEVM output voltage ripple. The output current is the rated full load of 6 A and V_{IN} = 5 V. The ripple voltage is measured at TP18, with oscilloscope bandwidth limited to 20 MHz.

Figure 10. TPS50601SPEVM Output Ripple

3.8 Input Voltage Ripple

Figure 11 shows the TPS50601SPEVM input voltage. The output current is the rated full load of 6 A and V_{IN} = 5 V. The ripple voltage is measured directly across the input capacitors.

Figure 11. TPS50601SPEVM Input Ripple

3.9 Dual Phase Waveform

Waveform highlights

- Output ripple (channel 3)
- Inductor current in phase 1 (channel 4)
- Switch node phase 1 (channel 1)
- Switch node phase 2 (channel 2)

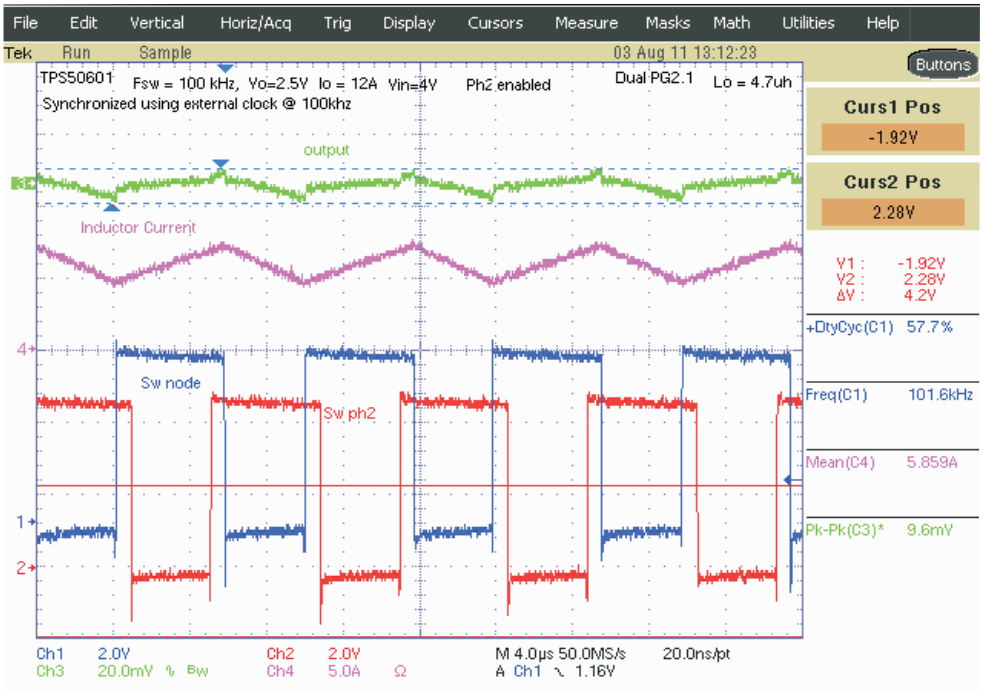


Figure 12. Dual Phase Waveform
V_{IN} = 4V, V_{OUT} = 2.5V @ 12A , f_{SW} = 100kHz

3.10 Current Sharing

An important performance criteria of the parallel design (paralleling two phases) is the ability to equally share current between the two converters of U1 and U2.

Current sharing performance is shown in Figure 13.

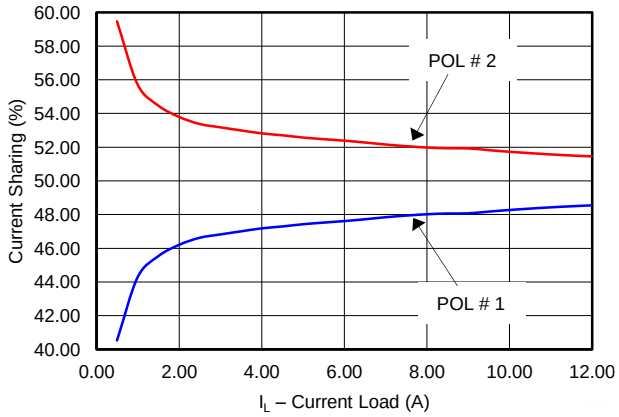


Figure 13. Current Sharing vs Load Current at Dual POL

3.11 Powering Up

Figure 14 and Figure 15 show the start-up waveforms for the TPS50601SPEVM. In Figure 14, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R6 and R7 resistor divider network. In Figure 15, the input voltage is initially applied and the output is inhibited by using a jumper at J3/J6 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 2.5 V. The input voltage for these plots is 5 V and the load is 6 A.

Figure 14. TPS50601SPEVM Start-Up Relative to V_{IN}

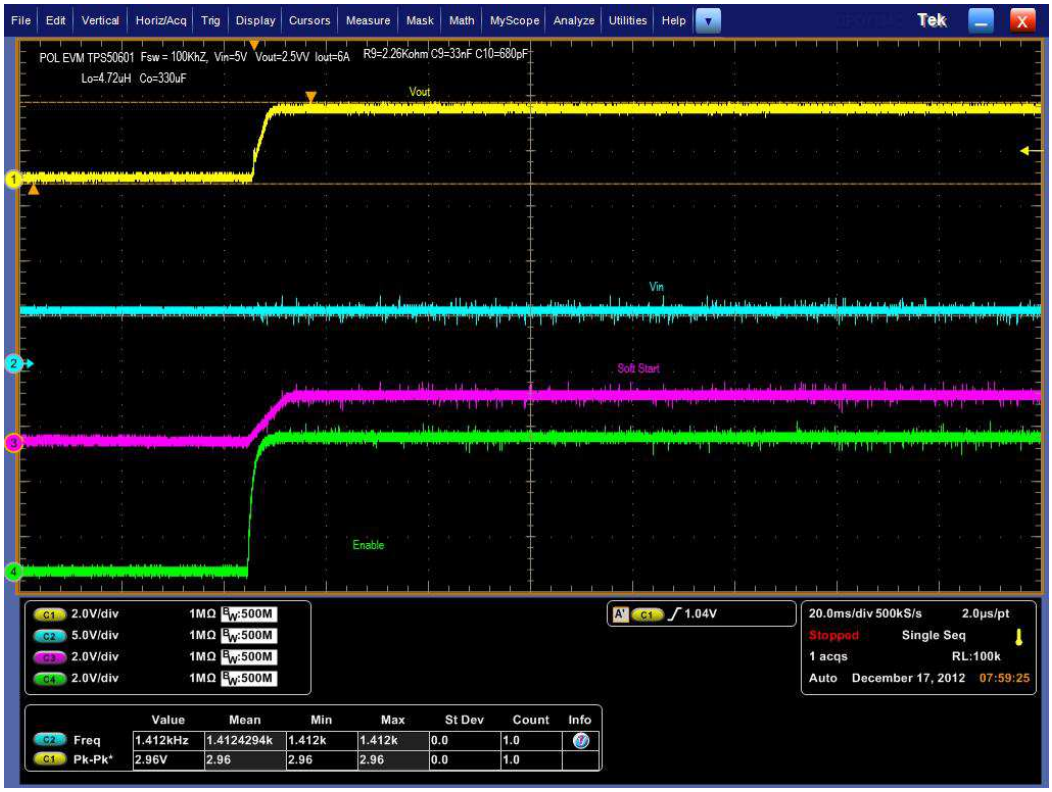


Figure 15. TPS50601SPEVM Start-up Relative to Enable

4 Board Layout

This section provides a description of the TPS50601SPEVM, board layout, and layer illustrations.

4.1 Layout

The board layout for the TPS50601SPEVM is shown in Figure 16 through Figure 20. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for P_{VIN}, V_{IN}, V_{OUT}, and V_{PHASE}. Also on the top layer are connections for the remaining pins of the TPS50601SPEVM and a large area filled with ground. The bottom and 2nd internal ground layers contain ground planes. TPS50601SPEVM is mounted on the bottom layer, thermal pad and pin1 (analog ground) of TPS50601SPEVM is connected to 3rd layer. 3rd layer is Analog ground and is connected to power ground at the output. The top side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board. Vias directly under the TPS50601SPEVM device provides a thermal path from the top-side ground plane to the bottom-side ground plane and connecting to layer 3 (analog ground).

The input decoupling capacitors (C6, C7, C22, C39 and C3, C4, C40, C41, C19, C20, C46, C47) and bootstrap capacitor (C27, C36) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation. Hooks are placed allowing the user to run bode plots on the unit by replacing R16 with a 50Ω resistor. For the TPS50601SPEVM, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage set point divider, frequency set resistor, slow start capacitor and compensation components are terminated to analog ground using a wide ground trace separate from the power ground pour. Analog ground is connected to power ground at the output.

PWB is made larger than required to provide flexibility for the customer to add additional capacitors on both input and output as well as replace output inductors to meet their system needs.

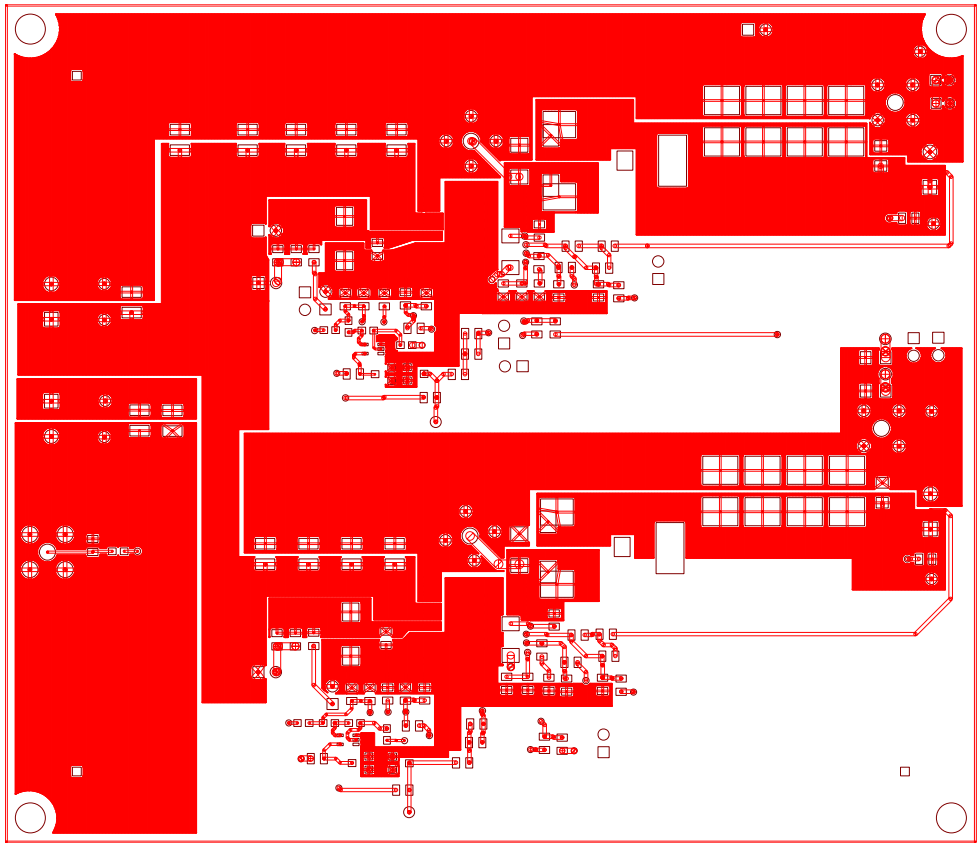


Figure 16. TPS50601SPEVM Top-Side Layer

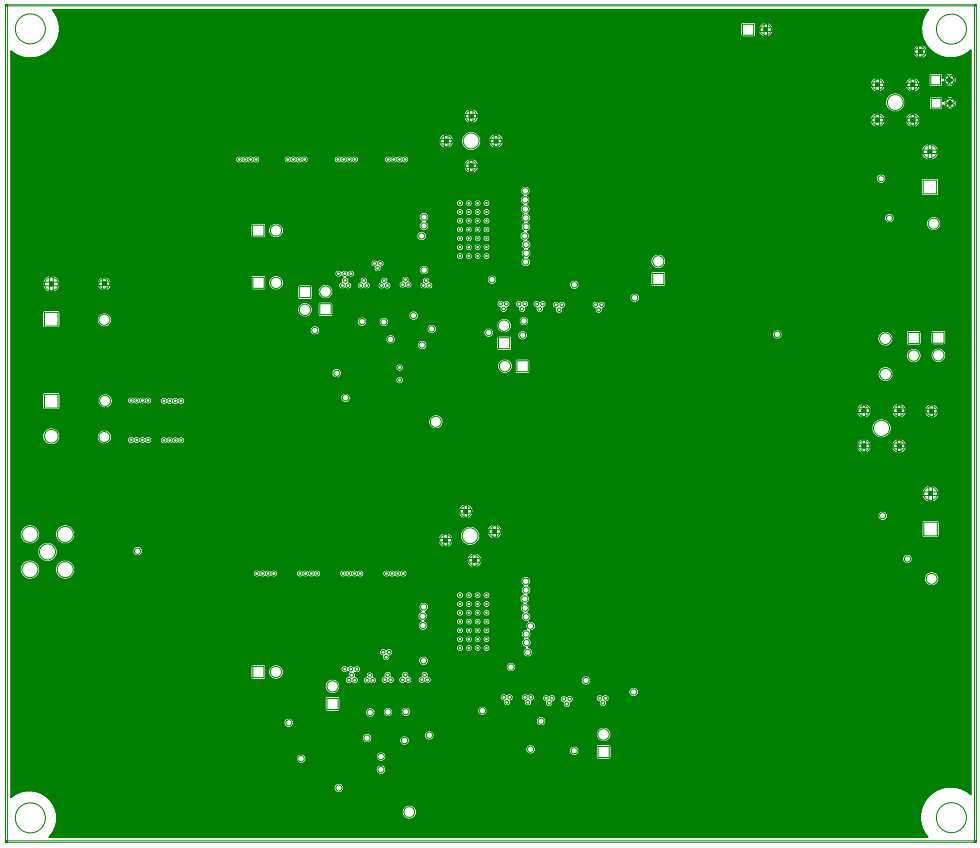


Figure 17. TPS50601SPEVM Layer 2

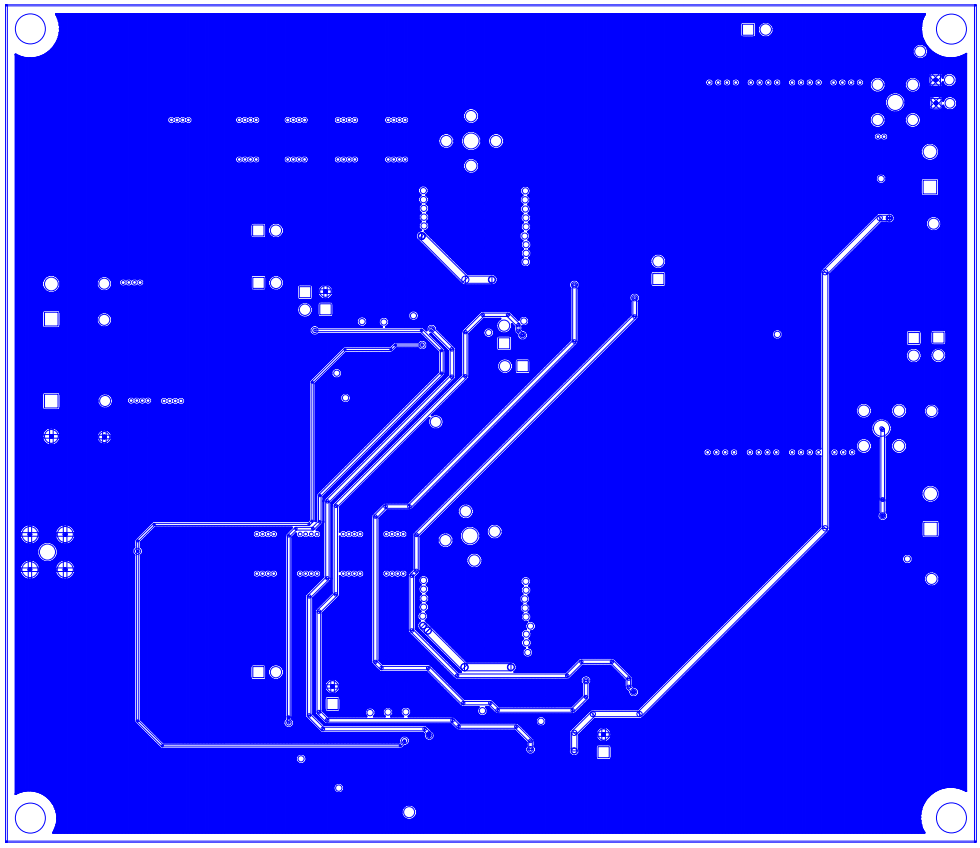


Figure 18. TPS50601SPEVM Layer 3

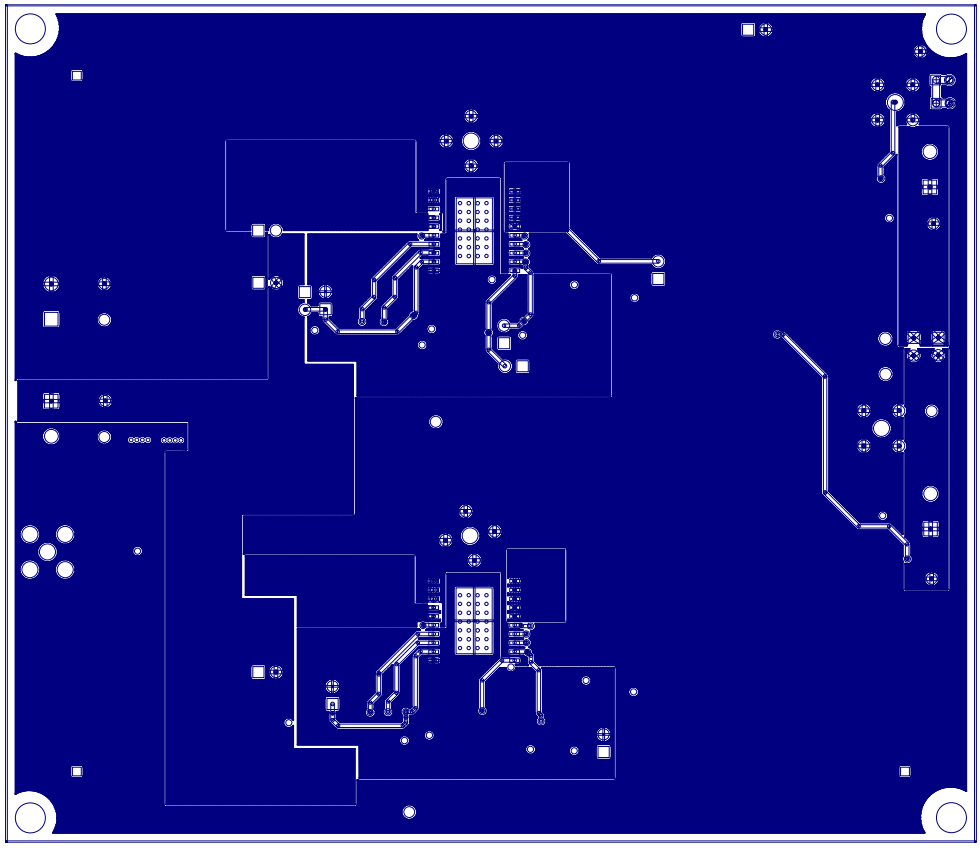


Figure 19. TPS50601SPEVM Bottom-Side Layer

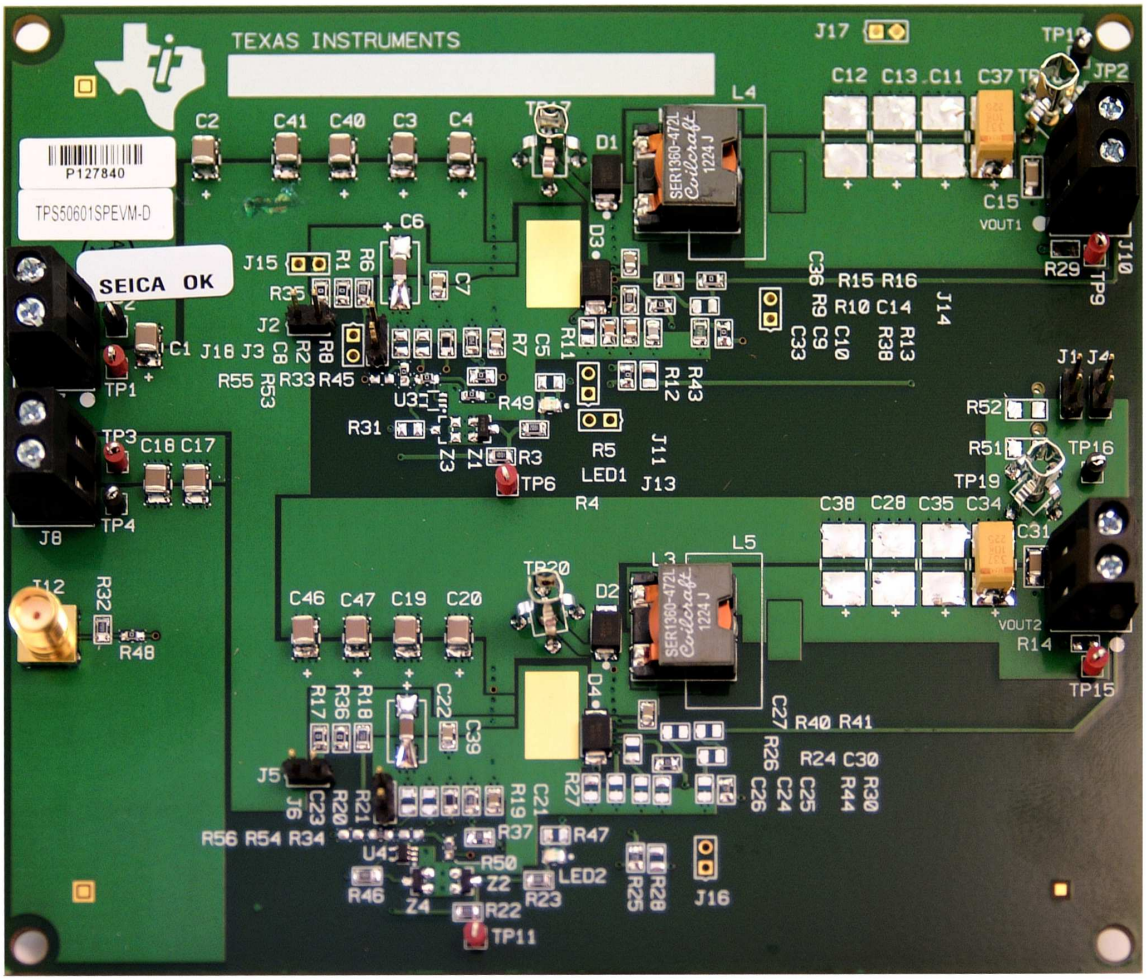


Figure 20. TPS50601SPEVM Bottom-Side Assembly

4.2 Estimated Circuit Area

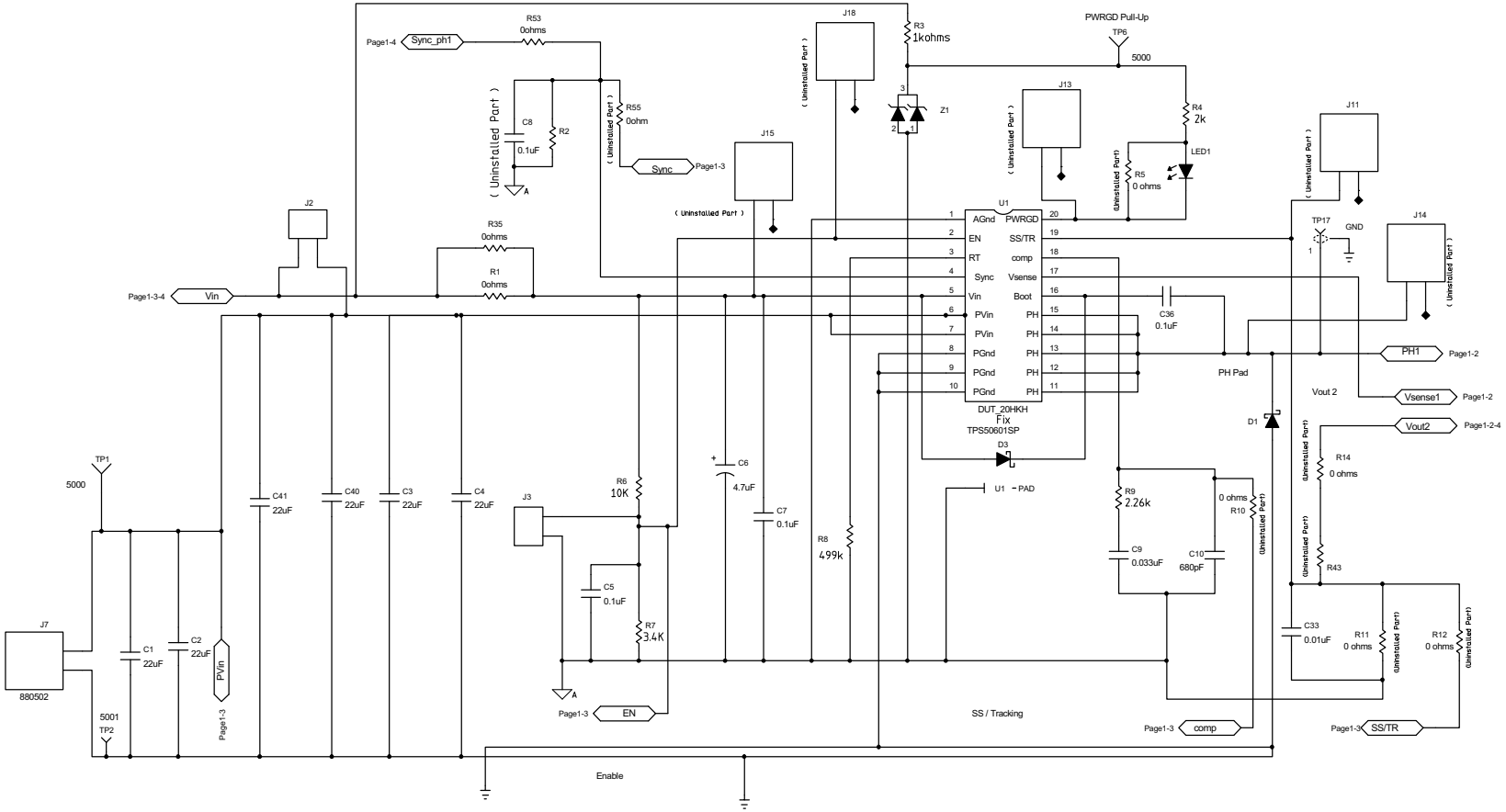
The estimated printed-circuit board area for the components used in this design is TBD in^2 (TBD mm^2). This area does not include test points or connectors. For size critical applications the area can be further reduced by selecting smaller size components; i.e. 0402 instead of 0805 and operating at higher frequency.

5 Schematic and Bill of Materials

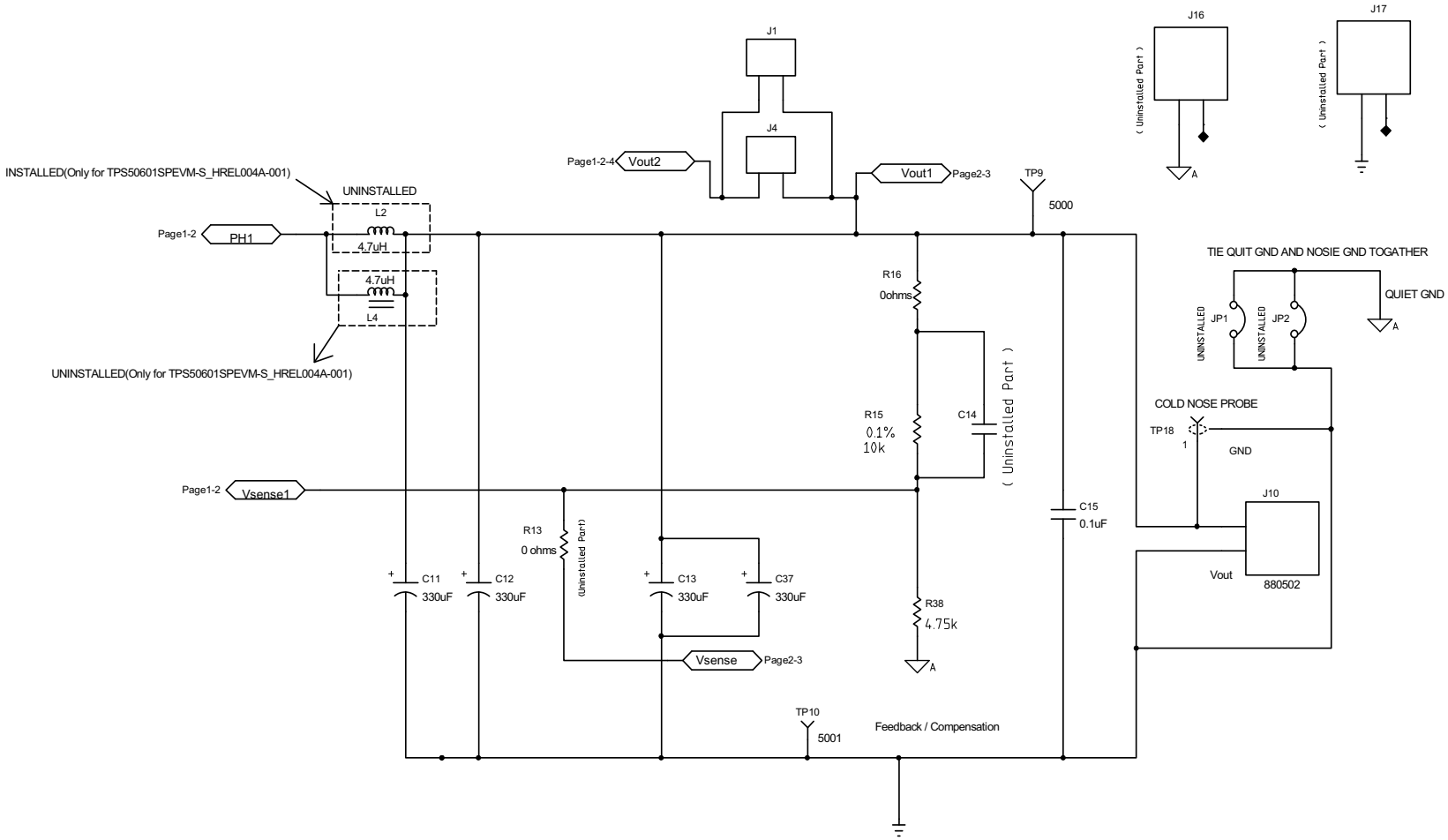
This section presents the TPS50601SPEVM schematics and bill of materials.

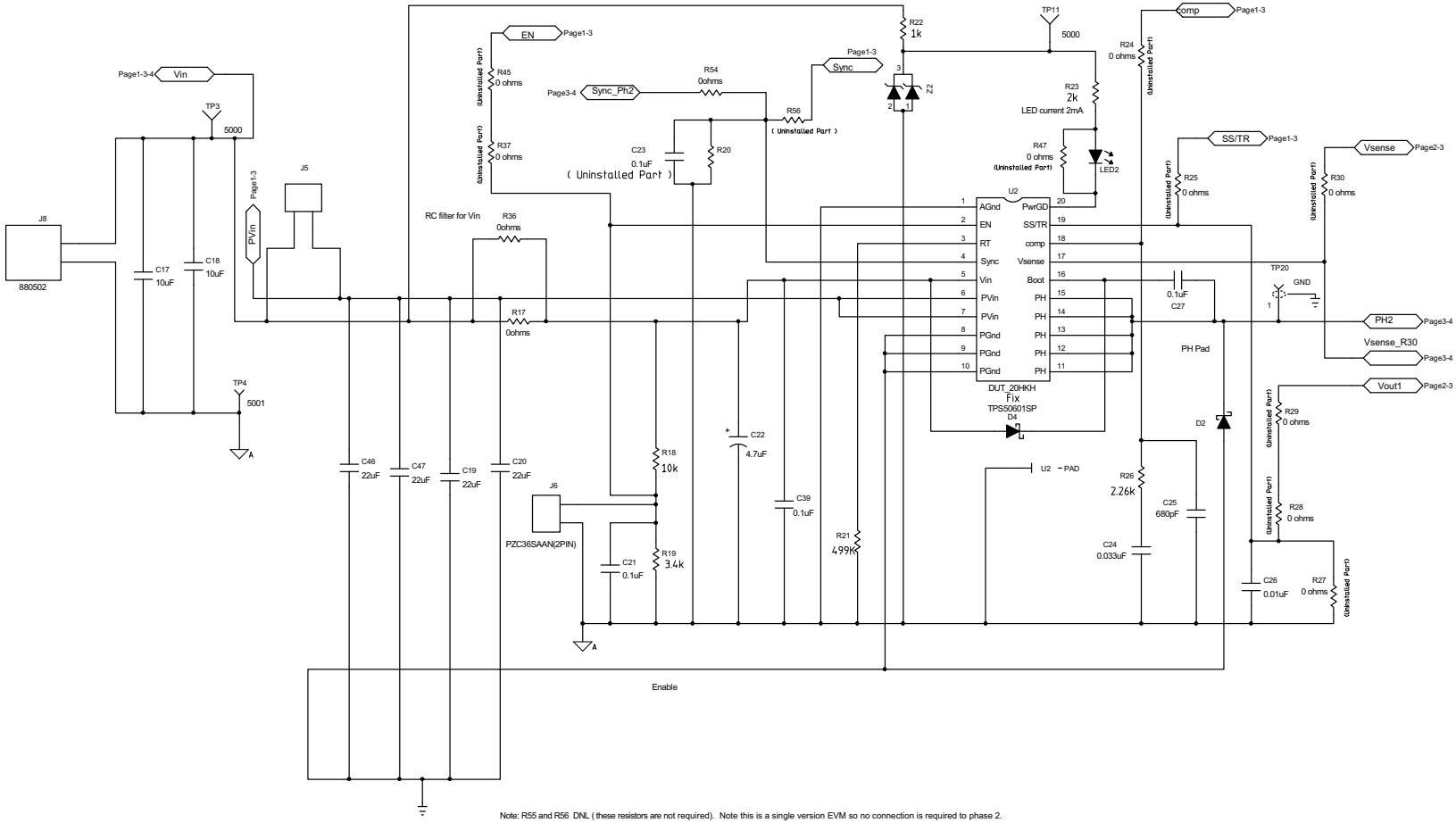
5.1 Schematic

See the following pages for the TPS50601SPEVM schematics.

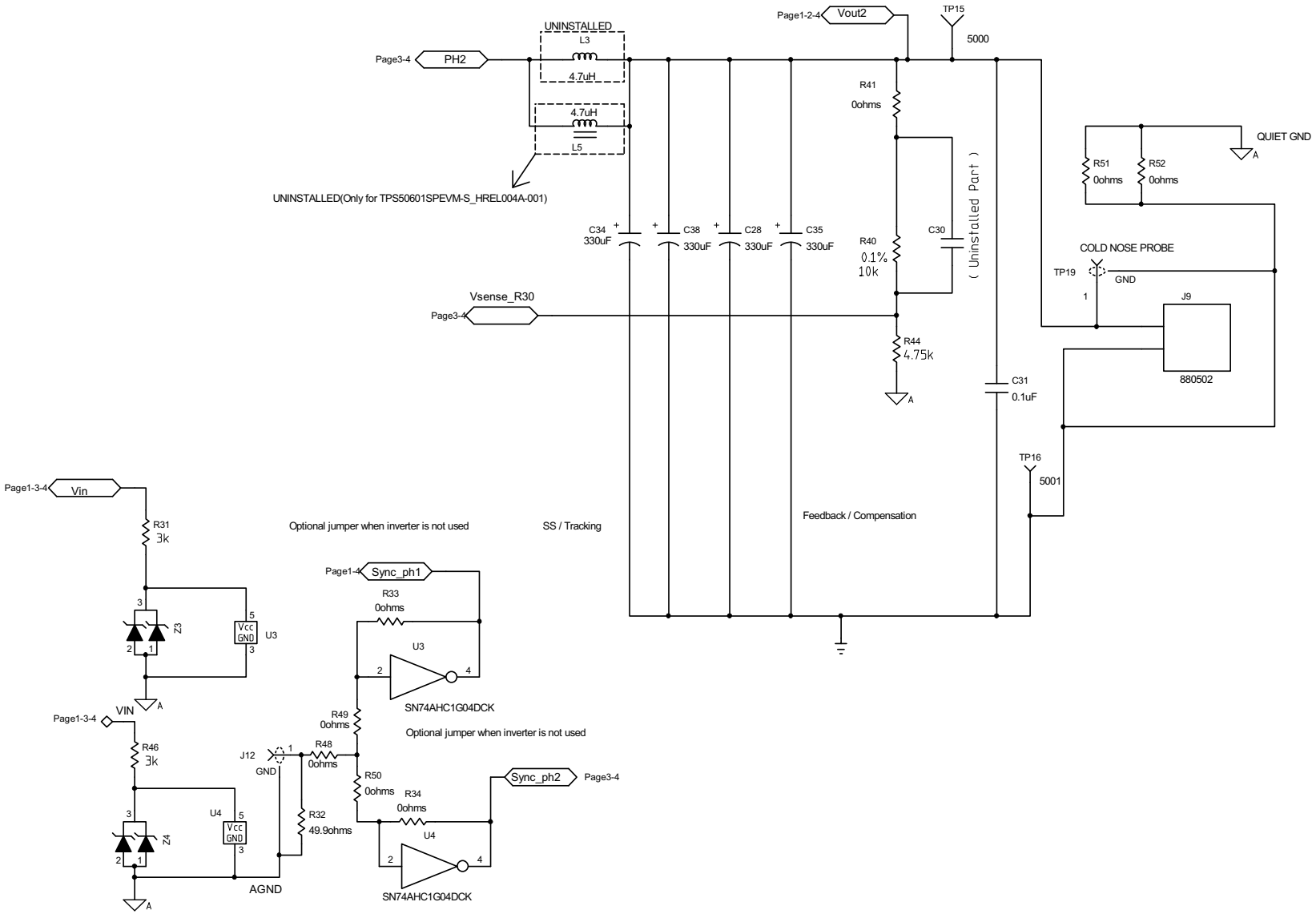


Note: R55 and R56 DNL (these resistors are not required). Note this is a single version EVM so no connection is required to phase 2.





Note: R55 and R56 DNL (these resistors are not required). Note this is a single version EVM so no connection is required to phase 2.



5.2 Bill of Materials

Table 5. TPS50601SPEVM Single Phase Bill of Materials

Item	Count	MFR	Part Number	RefDes	Description	Value	Comment
2	3	AVX	08055C104JAT2A	C5, C7,C36	CAP,SMT,0805	CAPACITOR,SMT,0805,CERAMIC,0.1uF,50V,5%,X7R	
3	1	TDK	C2012C0G1E333J	C9	CAP,SMT,0805	CAPACITOR,SMT,0805,CERAMIC,0.033uF,25V,5%,COG(NP0)	
4	1	TDK	C2012X7R1H103K	C33	CAP,SMT,0805	50V, 10%, 0.01uF	
5	1	MURATA	GRM2165C1H681JA01D	C10	CAP,SMT,0805	CAPACITOR,SMT,0805,CERAMIC,680pF,50V,5%,C0G(NP0)	
6	1	KEMET	C1206C104J4GACTU	C15	CAP,SMT,1206	CAPACITOR,SMT,1206,CERAMIC,0.1uF,16V,5%,COG	
7	2	AVX	12103D106KAT2A	C17, C18	CAP,SMT,1210	CER,CAP,SMT,10uF,25V,10%,X5R	
8	6	TDK	C3225X7R1C226K	C1, C2, C3, C4,C40, C41,	CAP,SMT,1210	CAPACITOR,SMT,1210,CERAMIC,22uF,16V,10%,X7R	
9	4	KEMET	T530X337M010ATE006	C37	CAPACITOR,SMT,TANTALUM	CAPACITOR,SMT,TAN,330uF,10V,20%	
10	3	MOLEX/BEAU	39544-3002	J7, J8, J10	CONN, THRU, 2P	TERMINAL BLOCK .2 CTR, 2P	
11	1	AMPHENOL	901-144-8	J12	CONNECTOR,SMA	SMA COAX STRAIGHT PCB CURRENT P/N IS 901-144-8RFX	
12	2	DIODES INC	B230-13F	D1, D3	DIODE,SMT,SMB	DIODE,SCHOTTKY,SMT, DIODES,INC.	
13	2	SULLINS / DIGIKEY	PZC36SAAN(2PIN)	J2, J3	HEADER,THU,2P	HEADER,2PIN,3A,GOLD,100LS,-65~125C,TL=120	
14	1	TI	TPS50601HKHMPR	U1	IC,SMT,CFP20	CERAMIC FLAT PACK 20 PIN	
16	1	COILCRAFT	SER1360-472KL	L2	INDUCTOR,SMT,2P	INDUCTOR,SMT,3P,4.7uH	Manual assembly
18	1	LITEON	LTST-C171KFKT	LED1	LED,SMT,0805	LED,SMT,0805,ULTRA-BRIGHT RED ORANGE,2.0V	
19	1	VISHAY	CRCW0603000Z	R53	RES,SMT,0603	RESISTOR,SMT,0603,0603,1/10W,0 OHM,ZERO OHM	
20	3	VISHAY	CRCW0603000Z	R33, R48, R49	RES,SMT,0603	RESISTOR,SMT,0603,0603,1/10W,0 OHM,ZERO OHM	
22	3	VISHAY	CRCW0805000Z	R1, R16, R35	RES,SMT,0805	RESISTOR,SMT,0805,THICK FILM,0 OHM,1/8W	
23	1	VISHAY	CRCW08051001F	R3	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,1%,1/8W,1.00K	
25	1	VISHAY	CRCW08052001F	R4	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,1%,1/8W,2.00K	
26	1	VISHAY	CRCW08052261F	R9	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,1%,1/8W,2.26K	
27	1	VISHAY	CRCW0805342F	R7	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,1%,1/8W,3.4K	Manual assembly
28	1	VISHAY	TNPW08054K72B	R38	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,0.1%,1/8W,4.70K	Manual assembly
29	1	VISHAY	CRCW080549R9F	R32	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,1%,1/8W,49.9 OHM	
32	1	VISHAY	CRC0805103F	R6	RES,SMT,0805	RESISTOR,SMT,0805,THICK FILM,1%,1/8W,10K	Manual assembly
33	1	MULTICOMP	RG2012P-4993-B-T5	R8	RES,SMT,0805	RESISTOR,SMT,0805,THIN FILM,499KOHM,0.1%,1/10W	
34	1	VISHAY	RG2012P-103-B-T5	R15	RES,SMT,0805	RESISTOR,SMT,0805,10K OHM,0.1%,1/10W	
36	2	TEKTRONIX	131-5031-00	TP17, TP18	TEST PROBE	TEST POINT PROBE ADAPTER 5PIN THRU	

Table 5. TPS50601SPEVM Single Phase Bill of Materials (continued)

Item	Count	MFR	Part Number	RefDes	Description	Value	Comment
37	3	KEYSTONE ELECTRONICS	5000	TP1, TP3, TP6, TP9	TESTPOINT,THU, 1P	TESTPOINT,THU,MINIATURE,0.1LS,120TL, RED	
38	3	KEYSTONE ELECTRONICS	5001	TP2, TP4, TP10	TESTPOINT,THU, 1P	TESTPOINT,THU,MINIATURE,0.1LS,120TL, BLACK	
40	1	VISHAY	DZ23C5V1-V	Z1	ZENER DIODE,SMT,SOT-23-3	DUAL SMALL SIGNAL ZENER DIODES,5.1V	
41	1	TDK	C3216X7R1C475	C6	CAP,SMT,1206	CAPACITOR,SMT,1206,CERAMIC,4.7uF,16V,10%,X7R	Manual assembly
42	1	PCB	-	TPS50601SPEVM	-		

Notes

1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Items highlighted in red populate for single EVM. Note exceptions on comment line.

Table 6. TPS50601SPEVM Dual Phase Bill of Materials

Item	Count	MFR	Part Number	RefDes	Description	Value	Comment
1	6	AVX	08055C104JAT2A	C5, C7, C21, C27, C36, C39	CAP,SMT,0805	CAPACITOR,SMT,0805,CERAMIC,0.1uF,50V,5%,X7R	
2	1	TDK	C2012X7R1E274J	C9	CAP,SMT,0805	CAPACITOR,SMT,0805,CERAMIC,0.27uF,25V,5%,X7R	Manual assembly
3	1	TDK	C2012X7R1H103K	C33	CAP,SMT,0805	50V, 10%, 0.01uF	
4	1	MURATA	C2012C0G1E332J	C10	CAP,SMT,0805	CAPACITOR,SMT,0805,CERAMIC,3300pF,50V,5%,C0G(NP0)	Manual assembly
5	2	KEMET	C1206C104J4GACTU	C15, C31	CAP,SMT,1206	CAPACITOR,SMT,1206,CERAMIC,0.1uF,16V,5%,COG	Manual assembly
6	2	AVX	12103D106KAT2A	C17, C18	CAP,SMT,1210	CER,CAP,SMT,10uF,25V,10%,X5R	
7	10	TDK	C3225X7R1C226K	C1, C2, C3, C4, C19, C20, C40, C41, C46, C47	CAP,SMT,1210	CAPACITOR,SMT,1210,CERAMIC,22uF,16V,10%,X7R	
8	2	KEMET	T530X337M010ATE006	C34, C37	CAPACITOR,SMT,TANTALUM	CAPACITOR,SMT,TAN,330uF,10V,20%	
9	4	DIODES INC	B230-13F	D1, D2, D3, D4	DIODE,SMT,SMB	DIODE,SCHOTTKY,SMT,DIODES,INC.	
10	4	MOLEX/BEAU	39544-3002	J7, J8, J9, J10	CONN, THRU, 2P	TERMINAL BLOCK .2 CTR, 2P	Manual assembly
11	1	AMPHENOL	901-144-8	J12	CONNECTOR,SMA	SMA COAX STRAIGHT PCB CURRENT P/N IS 901-144-8RFX	
12	6	SULLINS / DIGIKEY	PZC36SAAN(2PIN)	J1, J2, J3, J4, J5, J6	HEADER,THU,2P	HEADER,2PIN,3A,GOLD,100LS,-65~125C,TL=120	
13	2	TI	TPS50601HKHMPR	U1, U2	IC,SMT,CFP20	CERAMIC FLAT PACK 20 PIN	
14	1	TI	SN74AHC1G04DCK	U4	IC,SMT,SC70-5	SINGLE INVERTER GATE	
15	2	COILCRAFT	SER1360-472KL	L2, L3	INDUCTOR,SMT,2P	INDUCTOR,SMT,3P,4.7uH	Manual assembly
16	2	LITEON	LTST-C171KFKT	LED1, LED2	LED,SMT,0805	LED,SMT,0805,ULTRA-BRIGHT RED ORANGE,2.0V	
17	2	VISHAY	CRCW0603000Z	R53, R54	RES,SMT,0603	RESISTOR,SMT,0603,0603,1/10W,0 OHM,ZERO OHM	
18	4	VISHAY	CRCW0603000Z	R33, R48, R49, R50	RES,SMT,0603	RESISTOR,SMT,0603,0603,1/10W,0 OHM,ZERO OHM	
19	5	VISHAY	CRCW0805000Z	R1, R16, R17, R35, R36	RES,SMT,0805	RESISTOR,SMT,0805,THICK FILM,0 OHM,1/8W	
20	2	VISHAY	CRCW08051001F	R3, R22	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,1%,1/8W,1.00K	
21	8	VISHAY	CRCW08050000F(UN)	R10, R12, R13, R24, R25, R30, R37, R45	RES,SMT,0805	RESISTOR,SMT,0805,THICK FILM,0 OHM,1/8W	Manual assembly
22	2	VISHAY	CRCW08052001F	R4, R23	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,1%,1/8W,2.00K	
23	1	VISHAY	CRCW0805102F	R9	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,1%,1/8W,1.00K	Manual assembly
24	2	VISHAY	CRCW0805342F	R7, R19	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,1%,1/8W,3.4K	Manual assembly
25	1	VISHAY	TNPW08054K72B	R38	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,0.1%,1/8W,4.70K	Manual assembly
26	1	VISHAY	CRCW080549R9F	R32	RES,SMT,0805	RESISTER,SMT,0805,THICK FILM,1%,1/8W,49.9 OHM	
27	1	PANASONIC	ERJ-6ENF3001V	R46	RES,SMT,0805	RESISTOR,SMT,0805,THICK FILM,1%,1/8W, 3.0K	
28	2	VISHAY	CRC0805103F	R6, R18	RES,SMT,0805	RESISTOR,SMT,0805,THICK FILM,1%,1/8W,10K	Manual assembly
29	2	MULTICOMP	RG2012P-4993-B-T5	R8, R21	RES,SMT,0805	RESISTOR,SMT,0805,THIN FILM,499KOHM,0.1%,1/10W	Manual assembly

Table 6. TPS50601SPEVM Dual Phase Bill of Materials (continued)

Item	Count	MFR	Part Number	RefDes	Description	Value	Comment
30	1	VISHAY	RG2012P-103-B-T5	R15	RES,SMT,0805	RESISTOR,SMT,0805,10K OHM,0.1%,1/10W	Manual assembly
31	4	TEKTRONIX	131-5031-00	TP17, TP18, TP19, TP20	TEST PROBE	TEST POINT PROBE ADAPTER 5PIN THRU	
32	6	KEYSTONE ELECTRONICS	5000	TP1, TP3, TP6, TP9, TP11, TP15	TESTPOINT,THU, 1P	TESTPOINT,THU,MINIATURE,0.1LS,120TL, RED	
33	4	KEYSTONE ELECTRONICS	5001	TP2, TP4, TP10, TP16	TESTPOINT,THU, 1P	TESTPOINT,THU,MINIATURE,0.1LS,120TL, BLACK	
34	2	UNINSTALLED	2163S-02-ND(UN)	JP1, JP2	UNINSTALLED	UNINSTALLED	
35	3	VISHAY	DZ23C5V1-V	Z1, Z2, Z4	ZENER DIODE,SMT,SOT-23-3	DUAL SMALL SIGNAL ZENER DIODES,5.1V	
36	2	TDK	C3216X7R1C475	C6, C22	CAP,SMT,1206	CAPACITOR,SMT,1206,CERAMIC,4.7uF,16V,10%,X7R	Manual assembly
37	1	PCB	-	TPS50601SPEVM	-		

Notes

1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Items highlighted in red do not populate for dual EVM. Note exceptions on comment line.

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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