

TPS40070/71 Errata

1 Parts Affected

- TPS40070
- TPS40071

2 Symptoms

2.1 Soft-Start Latch Off During Over Current

- **Cause:** A glitch occurs on the internal run signal which causes the device to latch off.
- **Corrective Action:** Limit soft-start capacitor to 22 nF maximum.

2.2 Cross Conduction During Start Up

- **Cause:** Predictive gate drive timing issue with low pulse width.
- **Corrective Action:** Limit maximum soft start time per formula found in data sheet.

$$t_{START} \leq \frac{D_{MIN}}{f_{SW}} \times 10^{-7} \text{ ms}$$

Where:

- D_{MIN} is the minimum operating duty cycle.
- F_{SW} is the converter switching frequency.

2.3 Low Frequency Ripple on Output Voltage

- **Cause:** Internal charge pump causes ripple on the unbuffered reference.
- **Corrective Action:** None with current silicon. Effect has been noted on the data sheet.

2.3.1 Output Ripple Consideration

In addition to the typical output ripple associated with switching converters, which can vary from 5 mV to 150 mV, the TPS40070/71 exhibits a low-frequency ripple from 5 mV to 50 mV. The ripple, a consequence of the charge pump in the driver supply regulator, is well bounded under changes in line, load and temperature. The ripple frequency does vary with the converter switching frequency and can vary from 10 kHz to 60 kHz.

2.4 Cross Conduction During Marginal Over Current

- **Cause:** Over current pulse shifts predictive gate drive timing. This produces short pulse/long pulse.
- **Corrective Action:** OCP set point should be at least 20% higher than the maximum output current.

2.5 High-Side FET Latches On when Starting Up into a Short Circuit

- **Cause:** Substrate injection from SW pin can cause shoot through.
- **Corrective Action:** Add 1.5-Ω resistor between switch node and SW pin of device.

Symptoms

2.6 Low-Side Gate Charge Limitation

- **Cause:** Maximum predictive gate drive delay can be as low as 100 ns - this limits size of power FETs (<50-nC FETs).
- **Corrective Action:** Maximum sync FET gate charge is 50 nC.

2.7 High Slew Rate Input Voltage can cause Overshoot and Damage the Device

- **Cause:** If input rises too quickly the device's internal 10-V regulator can over shoot which damages the device.
- **Corrective Action:** Add a small RC on the VDD pin of the device. Details can be found in the data sheet.

2.7.1 SLEW RATE LIMIT ON VDD

The regulator that supplies power for the drivers on the TPS40070/1 requires a limited rising slew rate on VDD for proper operation if the input voltage is above 10 V. If the slew rate is too great, this regulator can over shoot and damage to the part can occur. To ensure that the part operates properly, limit the slew rate to no more than 0.12 V/ μ s as the voltage at VDD crosses 8 V. If necessary, an R-C filter can be used on the VDD pin of the device. Connect the resistor from the VDD pin to the input supply of the converter. Connect the capacitor from the VDD pin to PGND. There should not be excessive (more than a 200-mV) voltage drop across the resistor in normal operation. This places some constraints on the R-C values that can be used. is a schematic fragment that shows the connection of the R-C slew rate limit circuit.

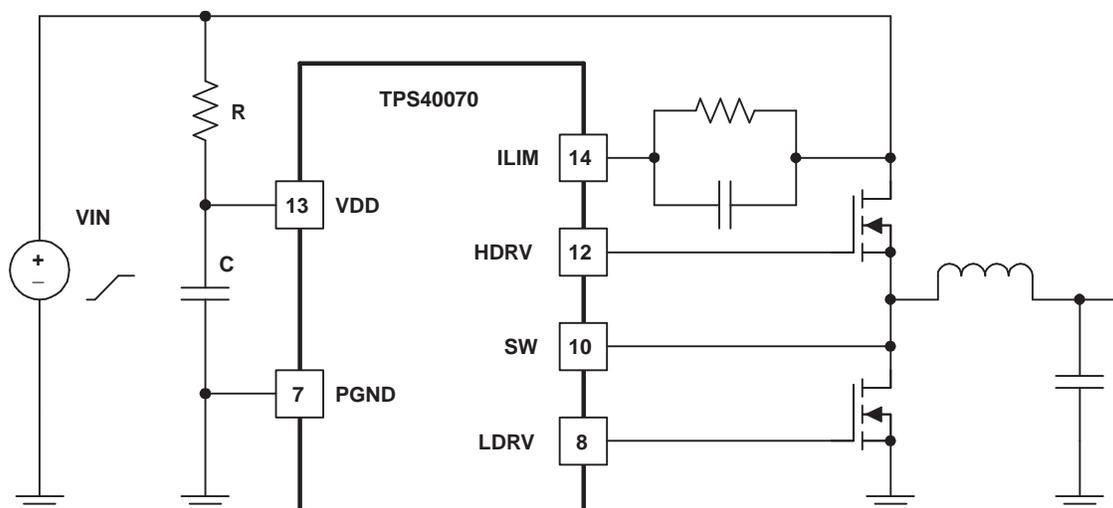


Figure 1. Limiting the Slew Rate

2.8 Overshoot on Output During Shutdown When UVLO is Set Less than 6.5 V

- **Cause:** A race condition exists in the device which causes the output to over shoot.
- **Corrective Action:** Add a 330-k Ω resistor in parallel with the soft-start capacitor.

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