

TPS23841 8-Port, High-Power PoE PSE Controller (PR598)

Reference Design

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1 Introduction

This Reference Design describes the set-up, operation and features of the TPS23841 8-Port, High-Power PoE PSE Controller (PR598). Instructions are provided to configure the assembly to select the desired mode of operation, connect input power, start operation, and interface to the unit with a Graphical User Interface (GUI). The main hardware components are described, and some functional background information is provided. In addition, a board schematic, layout pictorials and list of materials are supplied.

The information in this guide assumes some familiarity with the TPS23841 and basic PoE concepts; however, sufficient information should be provided here to configure the reference design for desired options, start the system, and use it to evaluate the TPS23841 for use in target applications.

2 Hardware Overview

2.1 General Description

The TPS23841 is a high-power, quad-port Ethernet Power Sourcing Equipment (PSE) manager device from Texas Instruments (TI). The TPS23841 controls the detection, classification and powering of compliant Powered Devices (PD's) at up to four PoE-enabled ports. PoE functions are implemented according to the requirements of IEEE specification 802.3af, with the exception of per-port continuous power sourcing and peak current limits. The TPS23841 PSE manager allows a minimum of 570-mA continuous current per port, serving applications needing higher power than the 15.4 W provided by the 802.3af specification.

Please refer to the TPS23841 data sheet, available from the TI web site (www.ti.com), for detailed information on the TPS23841 device.

The PR598 Reference Design employs two TPS23841 devices along with the port components to implement PoE capability on eight 10/100 Ethernet ports. The board can be configured as either an endpoint or midspan PSE. Jumpers are provided for user selection of various PSE parameters. The two TPS23841 devices can operate in Auto Mode (AM) or Power Management Mode (PMM) under the control of the on-board MSP430 microcontroller. In Auto Mode, the TPS23841 hardware controls all aspects of PSE functionality, including Detection, Classification, and power application and removal from ports. In PMM, the TPS23841 functions are controlled by a custom PoE algorithm from TI executing on the MSP430.

2.2 Module Sub-circuits

The major components of the PR598 module are described here. The description assumes the board assembly placed in front of the user, oriented with the longer peripheral dimension horizontal to the user, with the power connectors J2 and J43 and DB9 connector (J1) on the far edge and the PCB silk screen "8-PORT HI-POWER PSE" text facing and closest to the operator.

The board is divided into two isolated supply systems, distinguishable for the most part on the PCB from two top-layer copper plane areas. These planes are separated by a channel starting at the far edge of the board, passing between J2 and J43, and running the width of the board, under components U9 and U10, to the near edge. The PCB design maintains electrical isolation between these two sides. To the right of this line is the TPS23841 circuitry and port components. In a compliant system, this side of the circuit is powered by an isolated supply with a nominal 48-V potential. This supply provides bias for the TPS23841 devices, and is also the source for power switched to the eight PSE ports. On the left-hand side of the board is the MSP430 controller, associated circuitry, and interface connectors. This side of the system is powered by a 3.3-V supply. In typical applications, the controller side may be grounded during operation, either via operation from a non-isolated supply, or via connection to an earth-grounded, higher-level host or PC.

The PR598 board contains two sets of RJ-45 connectors. The row of connectors along the far edge of the board is the set of output RJ-45's, one per port. DC power (and optionally, data) is output at these connectors to a compliant PD. The in-board row of vertical-mount connectors is for input data; data provided at these RJ-45's (e.g., from an external, non-PoE switch) is coupled to the output RJ-45's via the on-board Ethernet transformers, for a complete "power injector" evaluation platform. The port magnetics and Bob Smith terminations are located between the rows of connectors.

The two TPS23841 devices (U8 and U13) and related components are located in the area below the port headers (towards the operator edge of the board). All required passive support components are provided on-board, along with numerous test points for monitoring signals. Between the TPS23841 circuits and the data connectors are two rows of 3-pin PCB headers; these provide for user-configuration of the port pin powering pairs and polarity.

The non-isolated (left-hand plane) side of the board contains the MSP430, host-interface circuitry and connectors, and an optional status LED driver circuit. A group of opto-coupler circuits populates the area between the two supply systems.

The PR598 contains two sets of LED status indicators. These LED's are physically located on the board in the area of the output RJ-45 connectors, grouped about their associated port connector. The first group consists of LED's D25, D27, D29, D31, D62, D64, D66 and D68. These diodes are biased directly from the nominal 48-V applied to powered ports. They provide a direct indication of the associated port's on or off status.

Each of these LED's has an associated jumper (J31 - J34 and J74 - J77) so it can be connected to or removed from the circuit as desired.

The second set of LED's is reference designators D1 – D16, and consists of one green ("powered") and one amber ("fault") LED per port. These LED's are powered by the MSP430 3.3-V supply, driven according to a port status algorithm in the PSE application firmware, such as might be optionally implemented in a PSE system.

3 Module Operation

3.1 Operating Specifications

The TPS23841 8-Port, High-Power PoE PSE Controller (PR598) is intended to allow a large degree of user configuration. This enables evaluation of the TPS23841 PSE device under a wide range of operating modes and conditions as may be encountered in target applications. However, under no circumstances should the assembly be operated beyond the absolute maximum conditions specified in Table 1 below.

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
V48	Input supply, J43-1 ⁽²⁾	-0.5	80	
+3.3V(iso)	Input supply, J43-4 ⁽²⁾	-0.5	6	
3.3V	Input supply, J2-2, J6-1 ⁽³⁾	-0.3	4.1	V
RST, I2C_SDA, I2C_SCL	Applied voltage, J6-2, J6-3, J6-4 ⁽³⁾	-0.3	V(3.3 V) + 0.3	
JTAG	Applied voltage, pins of J7 ⁽³⁾	-0.3	V(3.3 V) + 0.3	
T _{AMB}	Ambient operating temperature range	-40	85	- °C
T _{STG}	Storage temperature range	-55	125	-C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the PCB assembly. These are stress ratings only, and functional operation of the assembly at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect reliability.

⁽²⁾ With respect to J43-3.

⁽³⁾ With respect to J2-4.

The PR598 module is intended for operation under the following conditions.

Ambient operating temperature range

		g oonan	ono		
PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V48	Input supply, J43-1 ⁽¹⁾	21.5	48	57	V
3.3 V	Input supply, J2-2, J6-1 ⁽²⁾		3.3	3.6	v

Table 2. PR598 Recommended Operating Conditions

⁽¹⁾ With respect to J43-3.

⁽²⁾ With respect to J2-4.

T_{AMB}

3.2 Equipment Requirements

The following test and interface equipment (not supplied) is required to use the TPS23841 8-Port, High-Power PoE PSE Controller (PR598).

- Power Supply, 50 VDC, 5 A minimum
- Ethernet CAT-5 patch cables, quantity of 8

For PMM operation, the following equipment is also required in addition to the above items.

- Power Supply, 3.3 VDC, 500 mA minimum
- Personal Computer, running Windows OS (95/98/2000/NT/XP)
- RS-232 serial cable, DB9 to DB9

-40

85

°C

3.3 Power Management Mode Operation

For Auto Mode operation, please refer to section Section 3.7.

3.3.1 Introduction to Power Management Mode

In PMM, the Reference Design operates the two TPS23841 devices in Manual Mode, in which all basic port functions are commanded by a higher-level host controller via the I²C bus. The PR598 uses the MSP430 microcontroller for this host function. The TI PSE application has been pre-loaded on the MSP430 at the factory. PMM is the most versatile operating mode; in addition to the basic PSE functions of Discovery, Classification, and power switching, PMM adds numerous enhancements such as Power Management, AC Disconnect detection, Legacy device detection and Port Mapping.

3.3.2 PMM Configuration

Selection of the PR598 operating mode and other system parameters is user-configurable via shunt jumpers across various two-pin headers. To get started in PMM mode, verify jumpers have been installed at the factory according to the settings shown in Table 3. Headers not listed in Table 3 remain OPEN.

SIGNAL AND CONTROL JUMPERS			
J10, J14			
J9, J11, J13			
J45, J46, J55, J56			
J53, J50, J54			
J52, J88, J89 ⁽¹⁾			
J31 – J34			
J74 – J77			
J12 ⁽²⁾			

Table 3. PMM Shunt Jumper Installation

(1) J52, J88 and J87 on Revision E1 PCB assembly.

⁽²⁾ Applicable to Revision E1 PCB assembly only.

Additional control signal selections are made via jumper settings at several 3-pin PCB headers. For the headers listed in Table 4, connect the center pin to the corresponding pin of the position indicated. Three-pin headers not listed in the table remain OPEN.

Table 4. PMM Mode Select Jumper Positions

JUMPER	POSITION
J4	VCC ⁽¹⁾
J12	MSTR ⁽²⁾
J47	RTN
J49	RTN

⁽¹⁾ Connect to GND on Revision E1 PCB assembly.

⁽²⁾ This connection N/A to Revision E1 assembly.

Slide switches S1, S2 and S7 can be used to simulate logic-level signals of supply rail status. To observe normal powering operation of PD's, at least one of S1 or S2 must be set to the PG position. By default, place both switches in the PG position. Presently, there is no firmware function associated with S7, so this switch's position is a "don't care".

Each TPS23841 in the system must have a unique address on the I²C bus. The MSP430 has been configured at the factory to look for devices at addresses 0x01 and 0x02. The actual hardware addresses of U8 and U13 are set to 0x01 and 0x02, respectively, by setting the individual DIP switches of S3 and S5 to the positions shown in Table 5.

REFERENCE DESIGNATOR	POSITION		
S3-5	OPEN		
S3-4	OPEN		
S3-3	OPEN		
S3-2	OPEN		
S3-1	CLOSED		
S5-5	OPEN		
S5-4	OPEN		
S5-3	OPEN		
S5-2	CLOSED		
S5-1	OPEN		

Table 5. TPS23841 I²C Address Settings⁽¹⁾

⁽¹⁾ DIP position 6 of these switches is not used.

3.3.3 Main Connectors and Input Power

Table 6 lists the main connectors found on the PR598 module, with a brief description of each.

REF. DESIGNATOR	DESCRIPTION		
J1	RS-232 communication to host PC.		
J2	3.3-V non-isolated power connector, controller side.		
J6	Host I ² C interface connector.		
J7	MSP430 JTAG port connector.		
J43	48-V isolated power input connector.		
J86	Expansion out connector (to downstream module).		
J87	Expansion in connector (from upstream module). (Connector N/A to Revision E1 PCB assembly.)		
J57, J89	Alternate port power extraction/monitor taps. (Revision E1 PCB assembly only.)		
J90, J91	Alternate port power extraction/monitor taps. (Connectors N/A to Revision E1 PCB assembly.)		

Table 6. Power and Interface Connectors

The 48-V power for PoE distribution is connected to the module at J43. Connect the high-side (red) to J43-1 and low-side (black) to J43-3. To operate the module in PMM, 3.3-V power must be provided at connector J2; connect the high-side (red) of this supply to J2-2 and the low-side (black) to J2-4.

Also, connect J1 of the board to the COM port of the PC to be used with the board.

Once the supplies and serial cable have been connected, the supplies may be turned on and adjusted to their respective operating voltages (if not already done).

Module Operation

3.4 Configuring Ports for Power Pins and Polarity

In a compliant PoE system, power is delivered to devices over two pre-defined pin/wire pairs of the CAT-5 interconnect. The TPS23841 8-Port, High-Power PoE PSE Controller (PR598) is designed with jumper blocks to allow the user to select how power is applied to the output jack. Table 7 through Table 10 can be used to help the user determine jumper connections needed according to the desired power delivery configuration.

Locate the desired configuration from among the following tables. For each PCB header, adjacent X's in the pin number entries indicate jumper connections to be made. Blank cells after a block name indicate an open header. As the individual header pin numbers are not screened onto the PCB, please refer to the top assembly and top layer pictorials at the end of this document, for identification of header pins. Locate the thru-hole patterns for the rows of headers; pin 1 of each header is easily identified by the square pad. Note that all the headers are oriented in the same direction.

Table 7 set-up configures the PR598 board for spare pair powering, 48 V applied to each port at output pins 4 and 5 (HI) and 7 and 8 (LO).

	JUMPER BLOCK		PIN NUMBERS	
PORT CONFIGURED	Name	1	2	3
	J16	Х	Х	
Dert 0	J27	Х	Х	
Port 0	J36			
	J35			
	J17	Х	Х	
Dart 4	J30	Х	Х	
Port 1	J38			
	J37			
	J15	Х	Х	
Devi 0	J28	Х	Х	
Port 2	J40			
	J39			
	J18	Х	Х	
Dect 0	J29	Х	Х	
Port 3	J42			
	J41			
	J58	Х	Х	
Port 4	J70	Х	Х	
Port 4	J79			
	J78			
	J59	Х	Х	
Dett	J71	Х	Х	
Port 5	J81			
	J80			
	J60	Х	Х	
Devi 0	J72	Х	Х	
Port 6	J83			
	J82			
	J61	х	Х	
Devi 7	J73	Х	Х	
Port 7	J85			
	J84			

Table 7. Spare Pair Configuration

Table 8 set-up configures the PR598 board for spare pair powering, 48 V applied to each port at output pins 7 and 8 (HI) and 4 and 5 (LO). Commonly referred to as "reverse spare pair", this pinout in not defined in the standard, but is available here due to the use of headers/jumpers.

PORT CONFIGURED	JUMPER BLOCK		PIN NUMBERS	
	Name	1	2	3
Dert 0	J16		Х	Х
	J27		Х	Х
Port 0	J36			
	J35			
	J17		Х	Х
	J30		Х	Х
Port 1	J38			
	J37			
	J15		Х	Х
D 4.0	J28		Х	Х
Port 2	J40			
	J39			
	J18		Х	Х
5.40	J29		Х	Х
Port 3	J42			
	J41			
	J58		Х	Х
	J70		Х	Х
Port 4	J79			
	J78			
	J59		Х	Х
Devic	J71		Х	Х
Port 5	J81			
	J80			
	J60		Х	Х
	J72		х	Х
Port 6	J83			
	J82			
	J61		х	Х
	J73		Х	Х
Port 7	J85			
	J84			

Table 8. Alternate Spare Pair Configuration



Module Operation

Table 9 set-up configures the PR598 board for signal pair powering, MDI polarity, 48 V applied to each port at output pins 1 and 2 (HI) and 3 and 6 (LO).

PORT CONFIGURED	JUMPER BLOCK		PIN NUMBERS	
	Name	1	2	3
	J16			
De et a	J27			
Port 0	J36		Х	Х
	J35		Х	Х
	J17			
Dart 1	J30			
Port 1	J38		Х	Х
	J37		Х	Х
	J15			
Dect 2	J28			
Port 2	J40		Х	Х
	J39		Х	Х
	J18			
De de O	J29			
Port 3	J42		Х	Х
	J41		Х	Х
	J58			
Dect 4	J70			
Port 4	J79		Х	Х
	J78		Х	Х
	J59			
Dott 5	J71			
Port 5	J81		Х	Х
	J80		Х	Х
	J60			
Dott 6	J72			
Port 6	J83		Х	Х
	J82		Х	Х
	J61			
Dort 7	J73			
Port 7	J85		Х	Х
	J84		Х	Х

Table 9. Signal	Pair Configuration,	MDI Polarity
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Table 10 set-up configures the PR598 board for signal pair powering, MDI-X polarity, 48 V applied to each port at output pins 3 and 6 (HI) and 1 and 2 (LO).

PORT CONFIGURED	JUMPER BLOCK		PIN NUMBERS		
	Name	1	2	3	
	J16				
	J27				
Port 0	J36	Х	Х		
	J35	Х	Х		
	J17				
Devid	J30				
Port 1	J38	Х	Х		
	J37	Х	Х		
	J15				
Devil 0	J28				
Port 2	J40	Х	Х		
	J39	Х	Х		
	J18				
Devi 0	J29				
Port 3	J42	Х	Х		
	J41	Х	Х		
	J58				
Dort 4	J70				
Port 4	J79	Х	Х		
	J78	Х	Х		
	J59				
Devid	J71				
Port 5	J81	Х	Х		
	J80	Х	Х		
	J60				
Dert C	J72				
Port 6	J83	Х	Х		
	J82	Х	Х		
	J61				
	J73				
Port 7	J85	Х	Х		
	J84	Х	Х		

3.5 Starting PMM Operation, the TPS23841 Control GUI

From a reset condition (power application or assertion of microcontroller reset), the PSE application running on the MSP430 goes through initialization. From that point, it requires a "Start" command from the host to commence PSE operations. A GUI is available from TI to quickly be able to interface to the MSP430 firmware. The GUI runs from a Windows-based PC, and contains the necessary communication protocol and features to control many of the operating parameters of the PSE system. The software-configurable parameters include disconnect policy, Legacy device detection, and power management features and modes. The GUI screen also contains an area for display of real-time port status and parametric data.



Module Operation

Start the GUI on the host PC by running the supplied .exe file. A screen similar to that shown in Figure 1 should be obtained. Each time started, the GUI must determine which version of the protocol is running on the target system. This is done by selecting the Detect Protocol Version function from the File pull-down menu. Subsequently, a quick check of the initial status of the system can be obtained by clicking on the Port Status button above the various TPS #n screen tabs. Once the display data update completes, the Mode field of each port should indicate "Initializing", and the Current(mA), Voltage(V) and Power(mW) fields should all be set to 0.

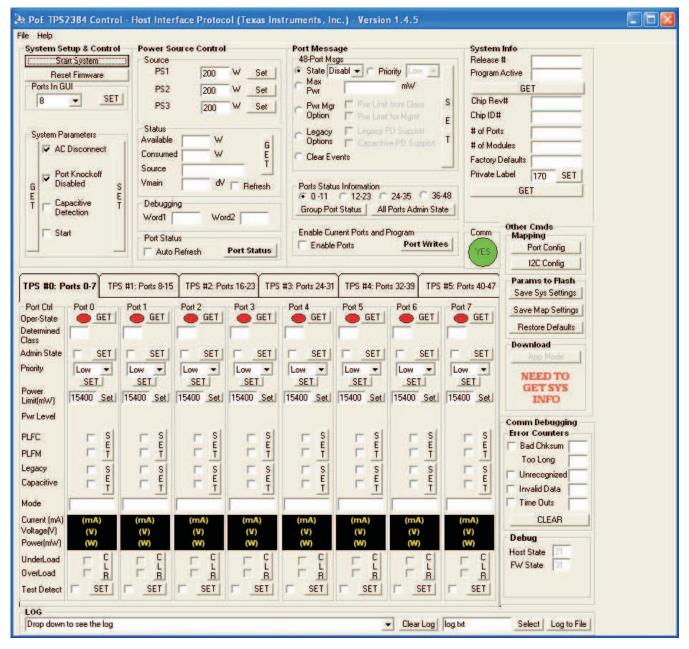


Figure 1. TPS23841 GUI Initial Screen After Launch

In the System Setup & Control panel (top left corner of the window), click on the Start System button. In the Start System dialog box which appears, select the desired disconnect policy from the radial buttons. If desired, enter the appropriate supply capacities (e.g., those of the supplies of the target PSE application) in the Input Power section. Click on the Start System button, and once the "Startup complete" message appears, click on Close. After a brief initialization period, the PSE functions will be actively executing on the module ports.

Port control parameters and status can be passed across the interface on an individual basis using the SET and GET buttons contained within the bounds of each port's display panel. The Port Status and Port Writes buttons just above the TPS #n tabs act on all eight of the currently displayed ports. Select operations can be performed on a system-wide basis using the commands in the Port Message panel in the upper center section of the display window. These messages act on all ports in the system (up to 48 ports). They are sent to the target using the SET button at the right of this panel, with only one command active at a time. Set the active command by clicking on the associated radial button, click on the related checkboxes or pull-down option to establish message content, then click on SET.

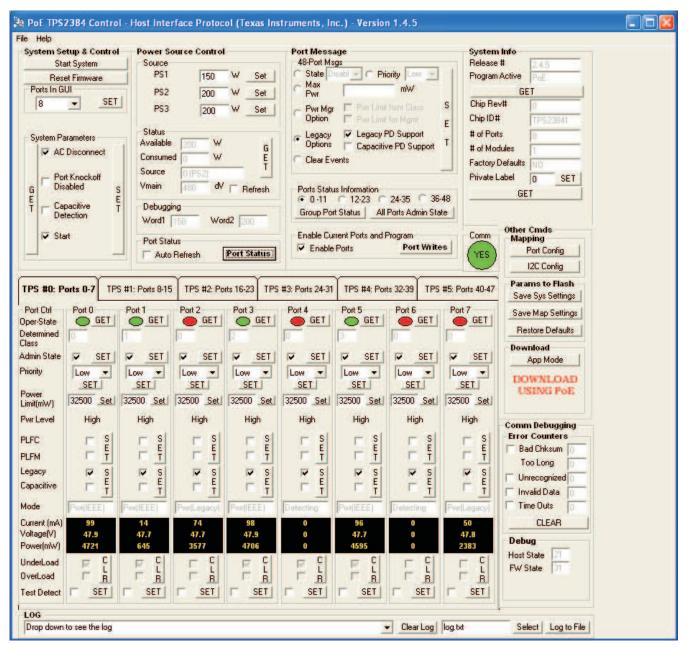


Figure 2. Example GUI Screen During Module Runtime

Once the module is actively searching for and powering devices, a GUI display similar to that shown in Figure 2 should be obtained when the Port Status button is clicked, depending on how many and what type(s) of devices are connected.

3.6 Module Test Points and Hardware Reset

3.6.1 Test Points

The PR598 board has been designed with numerous test points for optional user monitoring of the voltages or signals listed in Table 11. When hooking up measuring equipment, the user must be aware of which side of the isolation barrier the signal is referenced to for proper connection of meter returns and probe grounds. Refer to the assembly schematic when additional clarification is needed.

TEST POINT	SIGNAL NAME	DESCRIPTION
TP1, TP2, TP3, TP57	GND2	Ground reference point for the 3.3-V supply powered side of the system (MPS430 side).
TP4	V48_AC	AC drive signal applied to each of the eight ports.
TP5	V48_SW	High-side of the switched 48-V input power; i.e., load side of the hot swap controller (U7).
TP8	AC_HI	High-side driver control for AC Disconnect generator circuit.
TP9	AC_LO	Low-side driver control for AC Disconnect generator circuit.
TP10	SYN	Clock output of first TPS23841 (U8).
TP11	СТ	Clock oscillator node of first TPS23841 (U8).
TP12		U8 2.5 V reference output.
TP13, TP37	SDA_OUT	I ² C data out line from TPS23841's.
TP14, TP38	SDA_IN	I ² C data in line to TPS23841's.
TP15, TP39	SCL1	I ² C clock on isolated (TPS23841) side of system.
TP16	V3_3	TPS23841 generated 3.3-V voltage source.
TP17, TP21, TP26, TP28, TP41, TP45, TP51, TP52	RTN	Supply return and TPS23841 reference node for 48-V supply powered (isolated) side of the system.
TP18		U8 10 V bias/reference output.
TP19		U8 6.3 V bias voltage output.
TP20, TP44	WD_DIS	Watchdog disable (WD_DIS) input to TPS23841's.
TP22		U8 INT output pin.
TP23, TP47	PORB1	Hardware POR input signal to TPS23841's.
TP27, TP29, TP50, TP53	RTN	Supply return and TPS23841 reference node for 48-V supply powered (isolated) side of the system.
TP34		Sync clock input to second TPS23841 (U13).
TP35		Clock oscillator node of second TPS23841 (U13) (when configured for use).
TP36		U13 2.5 V reference output.
TP40, TP60	VREF	3.3-V voltage source output of U13 (for external reference).
TP42		U13 10 V bias/reference output.
TP43		U13 6.3 V bias voltage output.
TP46		U13 INT output pin.
TP54, TP56	3.3V	3.3 V input power to non-isolated (MSP430) side of the system.
TP55	RST	MSP430 reset signal.
TP58	+48V (ISO)	48-V PoE power supply input.
TP59	GND (ISO)	48-V PoE supply return (RTN node).

Table 11. Board Test Points



3.6.2 Pushbutton Reset

The PR598 contains two pushbutton switches (S4 and S6) for generating a hardware reset of the system, depending on operating mode.

In PMM, press and release the MSP430 RST switch (S6) to effect a system reset. S6 actuates the NMI/RST input of the MSP430 and the PORB pins of the TPS23841 devices. Initialization code on the MSP430 holds the PSE devices in reset after S6 is released. The TPS23841's remain in reset until a subsequent Start command is received.

In AM, press and release the PSE RST switch (S4) to generate a reset signal on the PORB inputs of the TPS23841's. S4 is only connected to the circuit when jumper J50 is installed. S4 is not intended for generating resets in PMM; doing so circumvents the state control of the host microcontroller, which may or may not subsequently be detected and recovered from. Use switch S6 or software resets (e.g., GUI or host command) in PMM.

3.7 Auto Mode Operation

3.7.1 Introduction to Auto Mode

In Auto Mode, the module is configured to place each TPS23841 in Auto Mode. With AM selected, the TPS23841 operates autonomously; all PSE functions including Discovery, Classification and Power Ramp-Up or Down are controlled by on-chip state machines, and port parametric information is compared against on-chip thresholds for decision making. In AM, the chip's I²C engine is still active, so port parametric information can optionally be retrieved for display or use. Auto Mode is the simplest operating mode, in terms of both external hardware requirements and software support.

3.7.2 AM Configuration

AM operation can quickly be selected from the PMM configuration set-up of section 3.3.2 with the relocation of only a couple of jumpers. However, this method requires the use of the 3.3-V supply as in PMM. To switch to AM from the PMM set-up, remove the jumper from header J9, and connect the center pin of J8 to the pin labeled VCC. Remove the shunt from J4, and reconnect the center pin of J4 to the pin labeled GND. (Connect center pin to pull-up to MSP430 VCC, pin closest to resistor R4, on Revision E1 PCB assembly.) Remove the jumper from J14.

If the PMM configuration is not already established, or for a set-up more representative of a real-world AM implementation, install jumpers as shown in Table 12 and Table 13 below.

SIGNAL AND CONTROL JUMPERS
J45, J46, J55, J56
J50, J54
J52, J88, J89 ⁽¹⁾
J31 – J34
J74 – J77

⁽¹⁾ J52, J88 and J87 on Revision E1 PCB assembly.

Table 13. AM Mode Select

JUMPER	POSITION
J48	RTN
J47	RTN
J49	RTN

Connect the 48-V supply high-side (red) to J43-1 and low-side (black) to J43-3. Turn on the 48-V supply. The PSE Controller should start detecting and powering valid PD's as they are connected to the output RJ-45 jacks, while discriminating invalid devices. The PSE RST pushbutton switch (S4) is available to actuate a hardware POR of the TPS23841 devices, as needed or desired.



3.8 Other TPS23841 User-Selectable Options

3.8.1 Watchdog Disable

The TPS23841 device features an on-chip clock watchdog circuit which monitors the device clock and, in Manual Mode, the SCL line of the I²C bus. Watchdog operation is user-selectable via logic input pin. See the TPS23841 data sheet for complete details on the watchdog function.

Connect the center pin of J49 to the pin labeled RTN to enable the watchdog timer; connect J49-center pin to VCC to disable this function.

3.8.2 Alternative A/Alternative B Operation

In Auto Mode, the TPS23841 can be configured to operate as either an Alternative A or Alternative B (2 second detection back-off) PSE. This selection is also made via logic input pin (the device ALTA/B pin).

Connect the center pin of J47 to the pin labeled RTN for Alternative A operation; connect J47-center pin to VCC for Alternative B. In PMM, the ALTA/B input (and consequently, J47 state) are ignored. The PSE application firmware from TI implements Alternative A operation only.

3.8.3 Board Operation from Nominal 24-V Supply

The TPS23841 device and this Reference Design are capable of operation at input supplies down to nearly 21 V. The wide input range is intended to serve various industrial systems operating from a nominal 24-V supply rail, as well as those running at af-compliant voltage levels. Therefore, the TPS23841 can be applied in proprietary, "closed" systems which, while not af-compliant with regards to bus voltage potential, still want to implement PoE functionality in their networked devices.

To configure the PR598 module for operation from 24 V, change resistor R78 to a 2.67-k Ω value. The PCB pattern is sized for a 2512 (1 W) SMD package. After changing the value of R78 as described here, care should be taken during subsequent operation to limit the potential of this 24-V supply (supply input at J43-1) to 30 V maximum.

List of Materials

4 List of Materials

Table 14 PCB Assembly List of Materials (PR598A)

		DECODIPTION	MANUFACTURE		
REF DES	-002	-001	DESCRIPTION	R	PART NUMBER
C6 - C10	5	5	Capacitor, ceramic, 0.1 µF, 25 V, X7R, 20%	Std	Std
C41	1	1	Capacitor, ceramic, 1 µF, 25 V, X7R, 10%	Std	Std
C33, C34, C46, C47, C71, C72, C78, C79	8	8	Capacitor, Film Chip, 0.027 µF, 50 V, 2%	Panasonic	ECHU1H273GX5
C42	1	1	Capacitor, ceramic, 220 pF, 50 V, C0G, 2%	Kemet	C0805C221G5GA C
C75			Capacitor, ceramic, 220 pF, 50 V, C0G, 2%	Kemet	C0805C221G5GA C
C11 - C14, C20, C22, C24, C26, C51 - C54, C60, C62, C64, C66	16	16	Capacitor, ceramic, 0.01 µF, 100 V, X7R, 20%	Std	Std
C1 - C5, C35 - C40, C43, C44, C45, C48, C49, C50, C73, C74, C76, C77, C80	22	22	Capacitor, ceramic, 0.1 µF, 100 V, X7R, 20%	Std	Std
C27 - C30, C67 - C70	8	8	Capacitor, ceramic, 0.22 µF, 100 V, X7R, 10%	ток	C3225X7R2A224 K
C31	1	1	Capacitor, alum. elect., SM, 68 µF, 100 V, 20%	Panasonic	EEV-FK2A680Q
C32	1	1	Capacitor, alum. elect., SM, 220 µF, 100 V, 20%	Panasonic	EEV-FK2A221M
C15 - C19, C21, C23, C25, C55 - C59, C61, C63, C65	16	16	Capacitor, ceramic, 1000 pF, 2000 V, X7R	ток	C4520X7R3D102 K
D1, D3, D5, D7, D9, D11, D13, D15, D25, D27, D29, D31, D51, D53, D62, D64, D66, D68	18	18	Diode, LED, green, 20 mA, 0.9 mcd	Panasonic	LN1371G
D2, D4, D6, D8, D10, D12, D14, D16	8	8	Diode, LED, amber, 20 mA 0.4 mcd	Panasonic	LN1471Y
D17 - D24, D54 - D61	16	16	Diode, TVS, V(RM) = 3.3 V, 350 W Pk	Protek Devices	GBLC03C
D26, D28, D30, D32, D63, D65, D67, D69	8	8	Diode, Zener, 20 V, 3 W	On Semi	1SMB5932BT3
D33 - D36, D70 - D73	8	8	Diode, fast rectifier, 2 A, 100 V	ST	ES2BA
D37, D38, D40, D42 - D45, D47, D74 - D77, D82 - D85	16	16	Diode, Schottky, 1 A, 100 V ST		STPS1H100A
D39, D41, D46, D48, D78 - D81	8	8	Diode, TVS, V(RWM) = 10 V, 400 W Pk	Diodes	SMAJ10A
D49	1	1	Diode, TVS, V(RWM) = 12 V, 400 W Pk	Diodes	SMAJ12A
		4	Diode, TVS, V(RWM) = 58 V, 400 W Pk	Diodes	SMAJ58A
D50	1	1	Didde, 103, v(1000) = 300, 400001 k	Biodoo	0111/1000/1
D50 D52	1	1	Diode, Zener, 5.6 V, 1.5 W	ON Semi	1SMA5919BT3

Table 14. List of Materials

F1 - F8	8	8	Polyswitch, 0.19 Ω max, 72 V max	Raychem	RXE135
J1	1	1	Connector, 9-pin D, right angle, female	Norcomp	182-009-212-171
J2	1	1	Header, 4 pin, 150 mil spacing	Weidmuller	1793810000
J2 socket	1	1	Header, 4 pin, socket, 150 mil spacing	Weidmuller	1798870000
J6, J43	2	2	Header, 6 pin, 150 mil spacing	Weidmuller	1793830000
J6, J43 socket	2	2	Header, 6 pin, socket, 150 mil spacing	Weidmuller	1798890000
J3, J9, J10, J11, J13, J14, J31 - J34, J44, J45, J46, J50 - J56, J74 - J77, J88, J89	26	26	Header, 2 pin, 100 mil spacing	Sullins	PTC36SAAN
J4, J5, J8, J12, J15 - J18, J27 - J30, J35 - J42, J47, J48, J49, J58 - J61, J70 - J73, J78 - J85	39	39	Header, 3 pin, 100 mil spacing	Sullins	PTC36SAAN
J57, J90, J91	3	3	Header, 8 pin, 100 mil spacing	Sullins	PTC36SAAN
J7, J86, J87	3	3	Header, PCB Mnt., Vert., 2 x 7, 100 mil spcng	3M	2514-6002UB
J19, J21, J23, J25, J62, J64, J66, J68	8	8	Connector, jack, modular, 8 position	AMP	556416
J20, J22, J24, J26, J63, J65, J67, J69	8	8	Connector, jack, modular, right angle, 8 position	AMP	520252-4
L1 - L8	8	8	Inductor, 4 line, 500 mA, 5 µH	Coilcraft	TTDLF4500
Q1	1	1	Transistor, NFET, 100 V, 33 A, 44 mΩ	IR	IRF540NS
Q2	1	1	MOSFET, N-channel, V(BR) = 100 V, 170 mA, 6 Ω	Infineon	BSS119E6327
Q3	1	1	MOSFET, N-channel, V(BR) = 25 V, 220 mA, 5 Ω	Fairchild	FDV301N
R28 - R35, R40 - R47, R81 - R88, R93 - R100	32	32	Resistor, chip, 75 $\Omega,$ 1/16 W, 5%	Std	Std
R8, R9, R27, R79, R105	5	5	Resistor, chip, 0 Ω , 1/10 W	Std	Std
R52	1	1	Resistor, chip, 100 Ω , 1/10 W, 5%	Std	Std
R69, R71	2	2	Resistor, chip, 200 Ω, 1/10 W, 5%	Std	Std
R73, R76	2	2	Resistor, chip, 300 Ω , 1/10 W, 5%	Std	
R1, R2, R3, R5, R6, R7, R10, R11, R13, R18, R21 - R26, R80	17	17	Resistor, chip, 330 Ω , 1/10 W, 5%	Std	Std
R70, R77	2	2	Resistor, chip, 1 k Ω , 1/10 W, 5%	Std	Std
R12, R14, R66, R67	4	4	Resistor, chip, 2 k Ω , 1/10 W, 5%	Std	Std
R57 - R60	4	4	Resistor, chip, 3.3 kΩ, 1/10 W, 5%	Std	Std
R74, R75	2	2	Resistor, chip, 3.9 kΩ, 1/10 W, 5%	Std	Std
R48 - R51, R101 - R104	8	8	Resistor, chip, 7.5 kΩ, 1/10 W, 5%	Std	Std
R68	1	1	Resistor, chip, 10 kΩ, 1/10 W, 5%	Std	Std

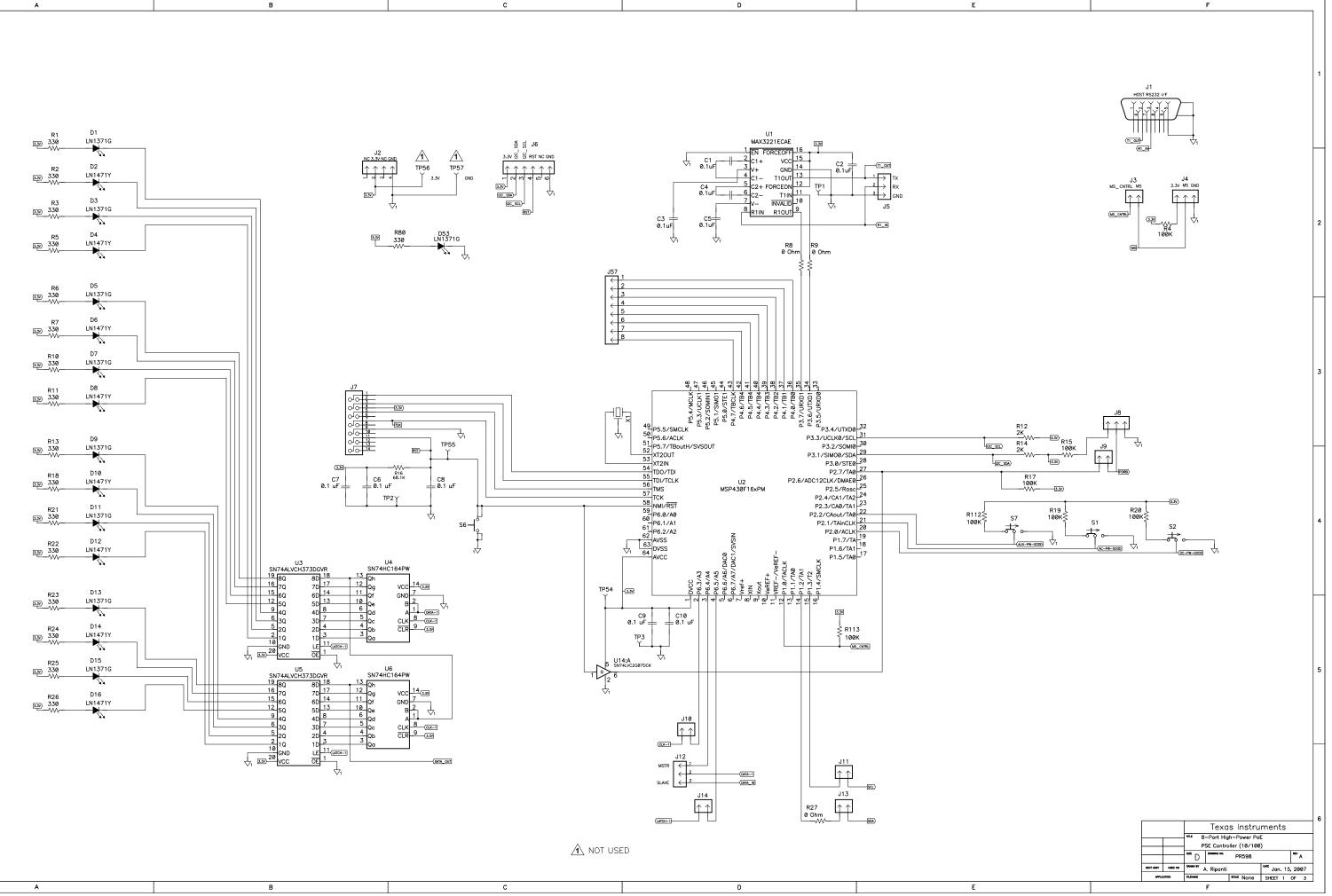
Table 14. List of Materials (continued)

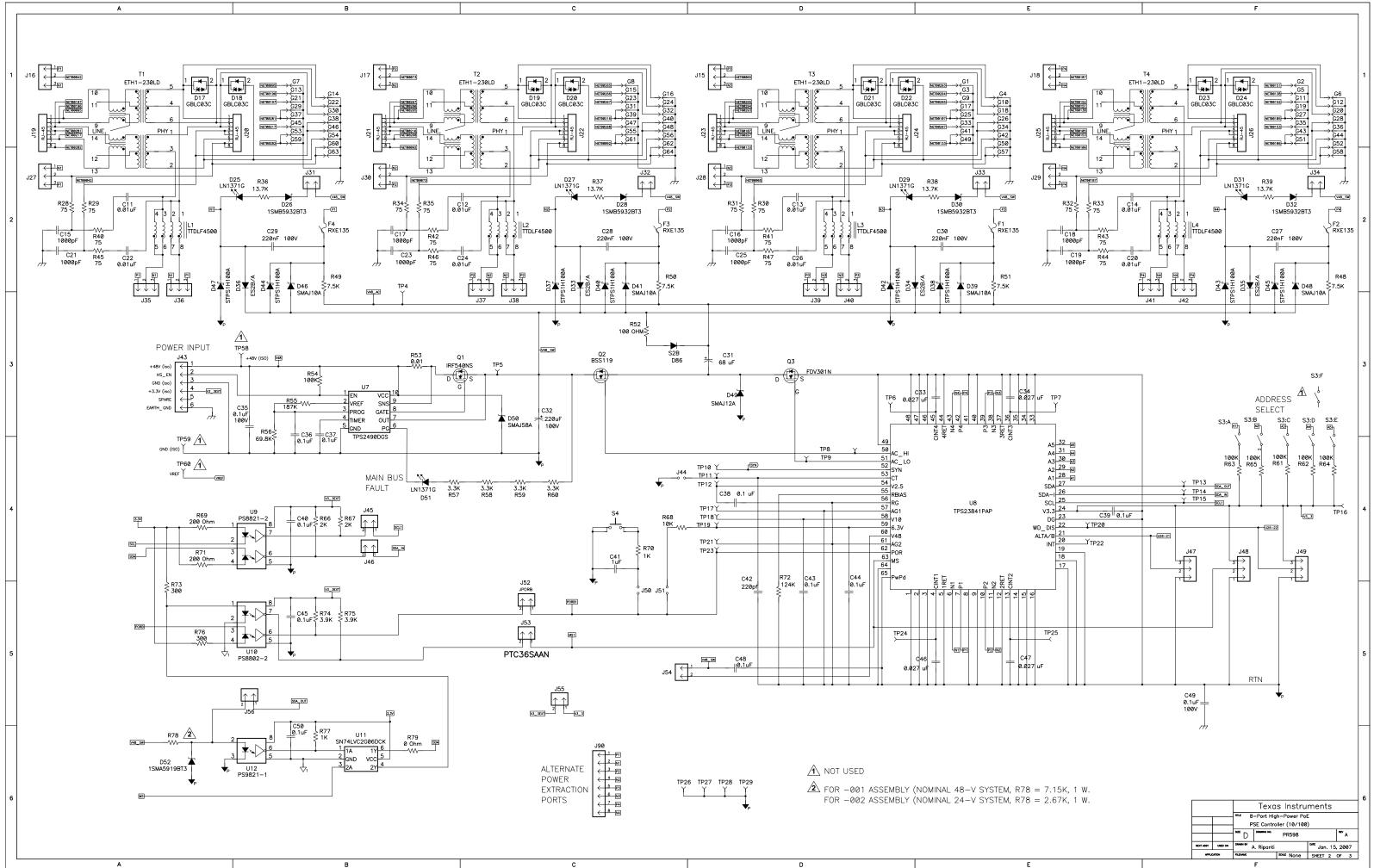


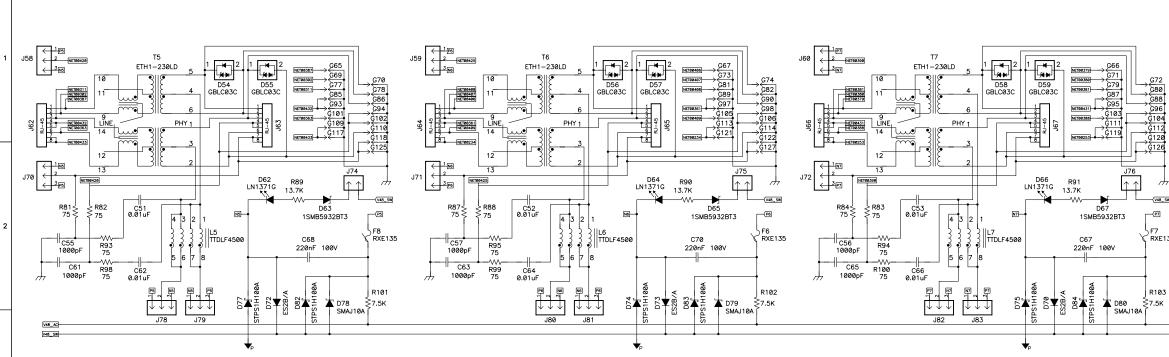
Table 14. List of Materials (continued)

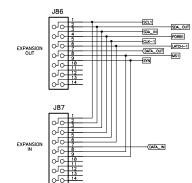
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R4, R15, R17, R19, R20, R54, R61 - R65, R106 - R110, R112, R113	18	18	Resistor, chip, 100 k Ω , 1/10 W, 5%	Std	Std
R36 - R39, R89 - R92	8	8	Resistor, chip, 13.7 kΩ, 1/10 W, 1%	Std	Std
R16	1	1	Resistor, chip, 68.1 kΩ, 1/10 W, 1%	Std	Std
R56	1	1	Resistor, chip, 69.8 kΩ, 1/10 W, 1%	Std	Std
R55	1	1	Resistor, chip, 187 k Ω , 1/10 W, 1%	Std	Std
R72, R111	2	2	Resistor, chip, 124 k Ω , 1/10 W, 0.1%	KOA Speer	RN732ALxx1243B 25
			OR	Susumu	RR1220P-1243- BMxx
R78	1	-	Resistor, chip, 2.67 kΩ, 1 W, 1%	Std	Std
R78	-	1	Resistor, chip, 7.15 kΩ, 1 W, 1%	Std	Std
R53	1	1	Resistor, metal strip, 0.01 Ω , 2 W, 1%	IRC	LRC-LRF2512-01- R010-F
S1, S2, S7	3	3	Switch, 1P2T, slide, PC-mount, 200 mA	E-Switch	EG1218
S3, S5	2	2	Switch, 6 pole, DIP, raised rocker	Grayhill	76SB06S
S4, S6	2	2	Switch, PB momentary, sealed, washable	С&К	KT11P2JM
T1 - T8	8	8	Transformer, center-tapped, high-power PoE	Coilcraft	ETH1-230LD
TP1 - TP25, TP30 - TP49, TP54, TP55	47	47	Test point, white, 0.062" hole	Keystone	5012
TP26 - TP29, TP50 - TP53	8	8	Test point, SM, 0.150" x 0.090"	Keystone	5016
TP56 - TP60	-	-	Header, 1 pin, 0.040" Dia.	Sullins	PTC36SAAN
U1	1	1	Device, RS-232 transceivers with auto-shutdown	Maxim	MAX3221ECAE
U2	1	1	Device, Mixed Signal Microcontroller	Texas Instruments	MSP430F169IPM
U3, U5	2	2	Device, Octal Transparent D-Type Latch, Tri-state outputs	Texas Instruments	SN74ALVCH373D GVR
U4, U6	2	2	Device, 8-Bit Parallel-Out Serial Shift Register	Texas Instruments	SN74HC164PW
U7	1	1	Device, Positive High-Voltage Hot Swap Ctlr	Texas Instruments	TPS2490DGS
U8, U13	2	2	Device, High-Power Quad PSE Controller	Texas Instruments	TPS23841PAP
U9	1	1	Device, optocoupler, dual open collector output	NEC	PS8821-2-A
U10	1	1	Device, optocoupler, dual open collector output	NEC	PS8802-2-A
U11	1	1	Device, logic, Dual Inverter w/open-drain outputs	Texas Instruments	SN74LVC2G06D CK
U12	1	1	Device, optocoupler, single open collector output	NEC	PS9821-1-A
U14	1	1	Device, logic, dual bffr/driverr w/open-drain outputs	Texas Instruments	SN74LVC2G07D CK
X1	1	1	Crystal, 8.00 MHz	ECS	ZTT8.00MT
N/A	1	1	PCB, FR-4, 4 layer, SMOBC, 12.25" x 7.25" x .062"		PR598A
N/A	44	44	Shunt	Sullins	STC02SYAN
N/A	9	9	Rubber bumper	SPC Technology	2563











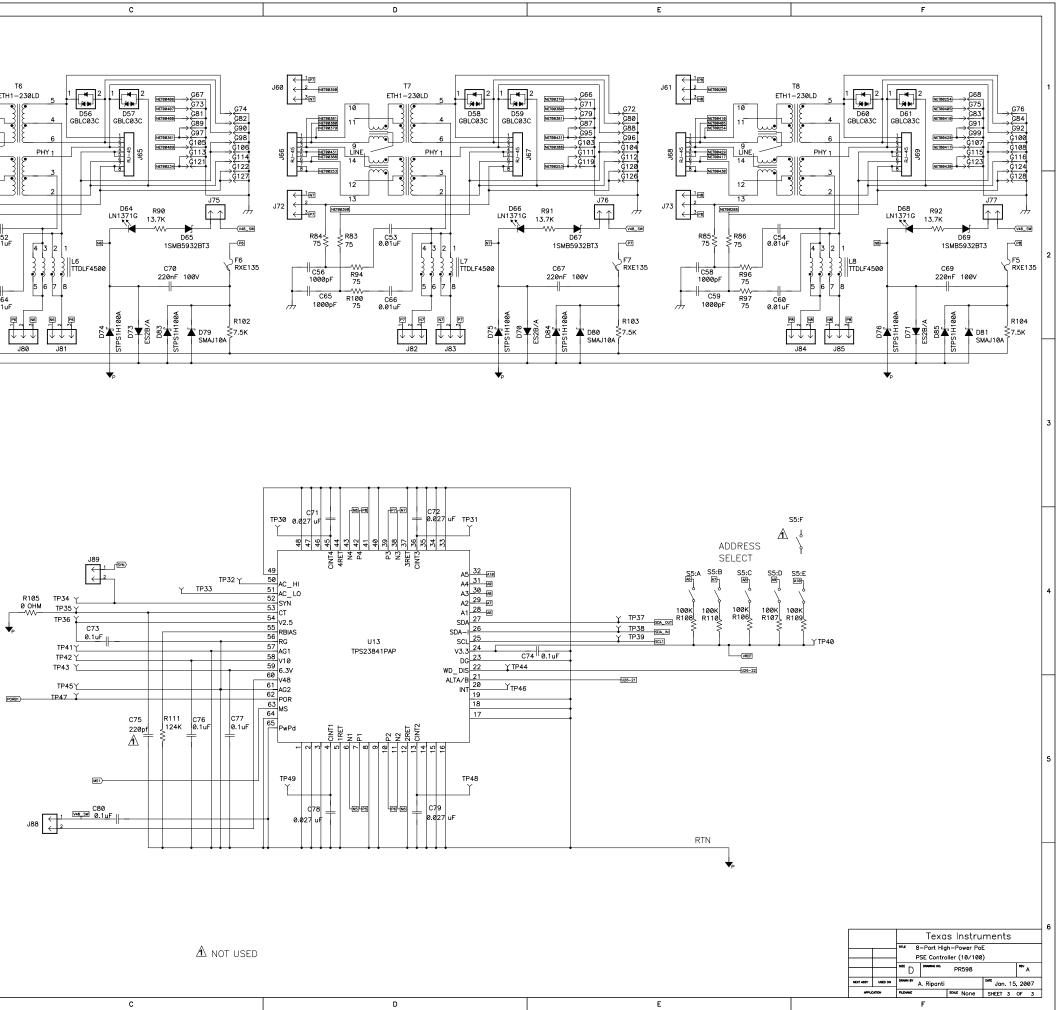
TP50 TP51 TP52 TP53

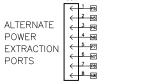
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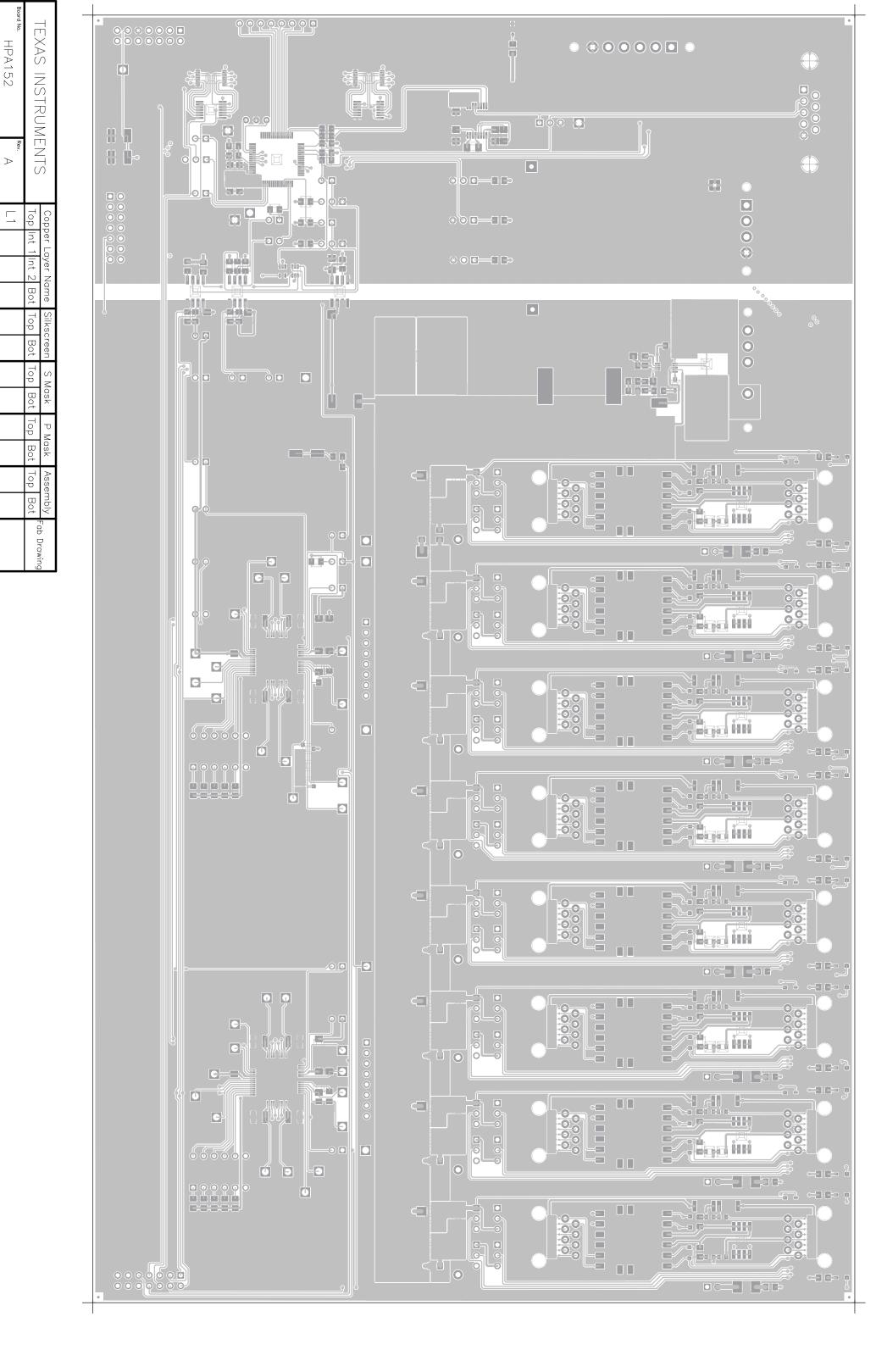




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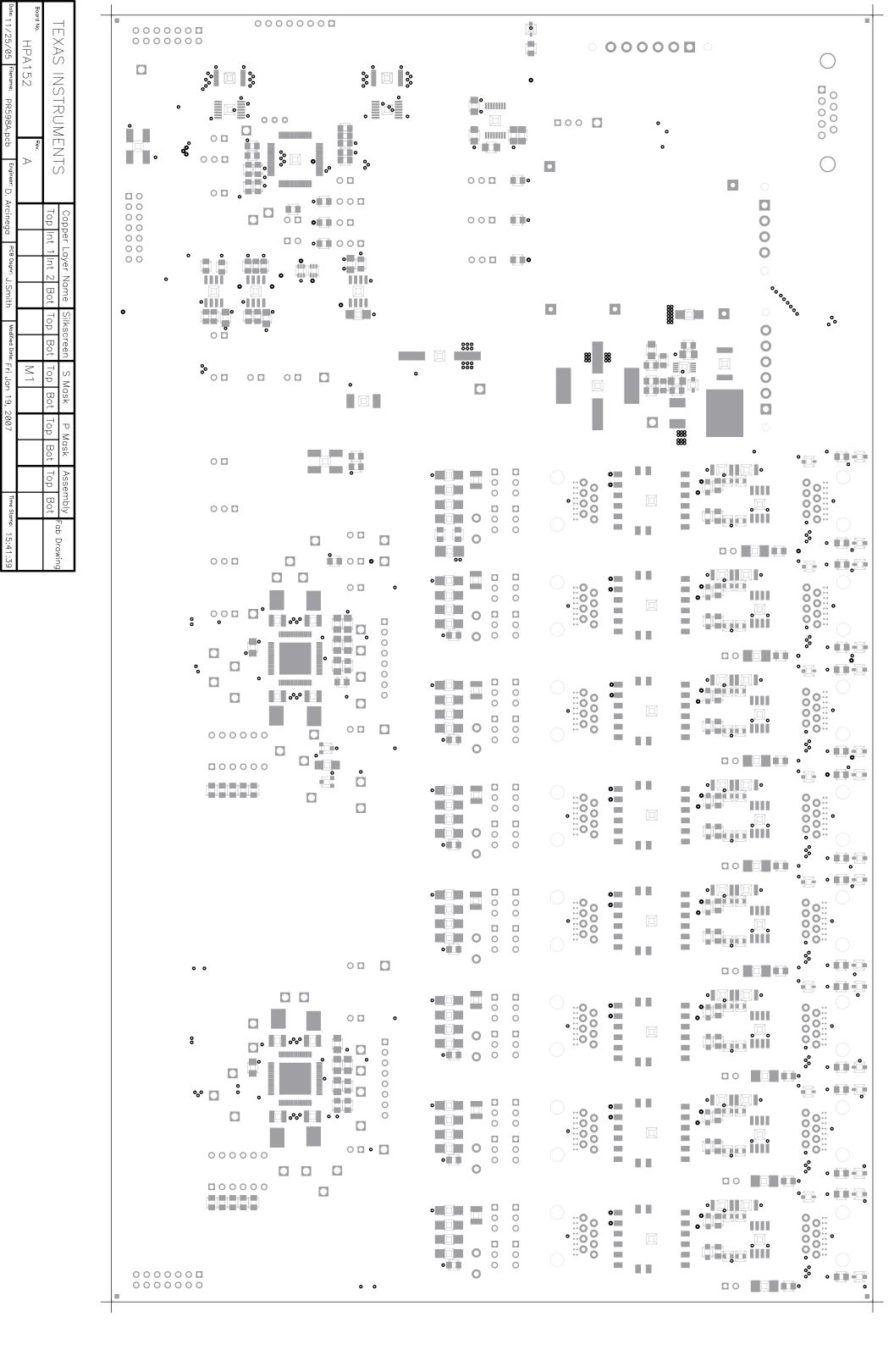
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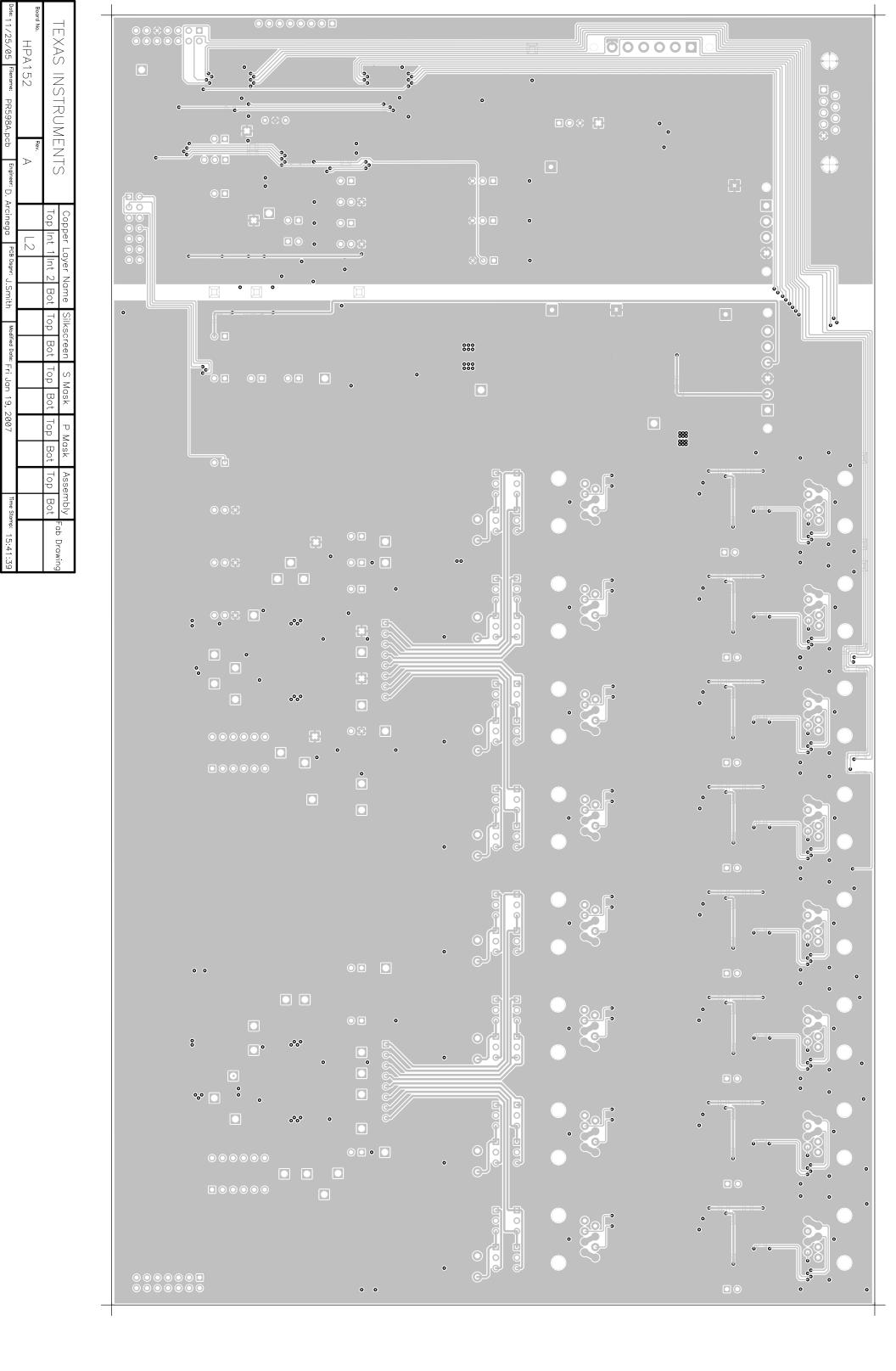
Engineer: D. Arcinega

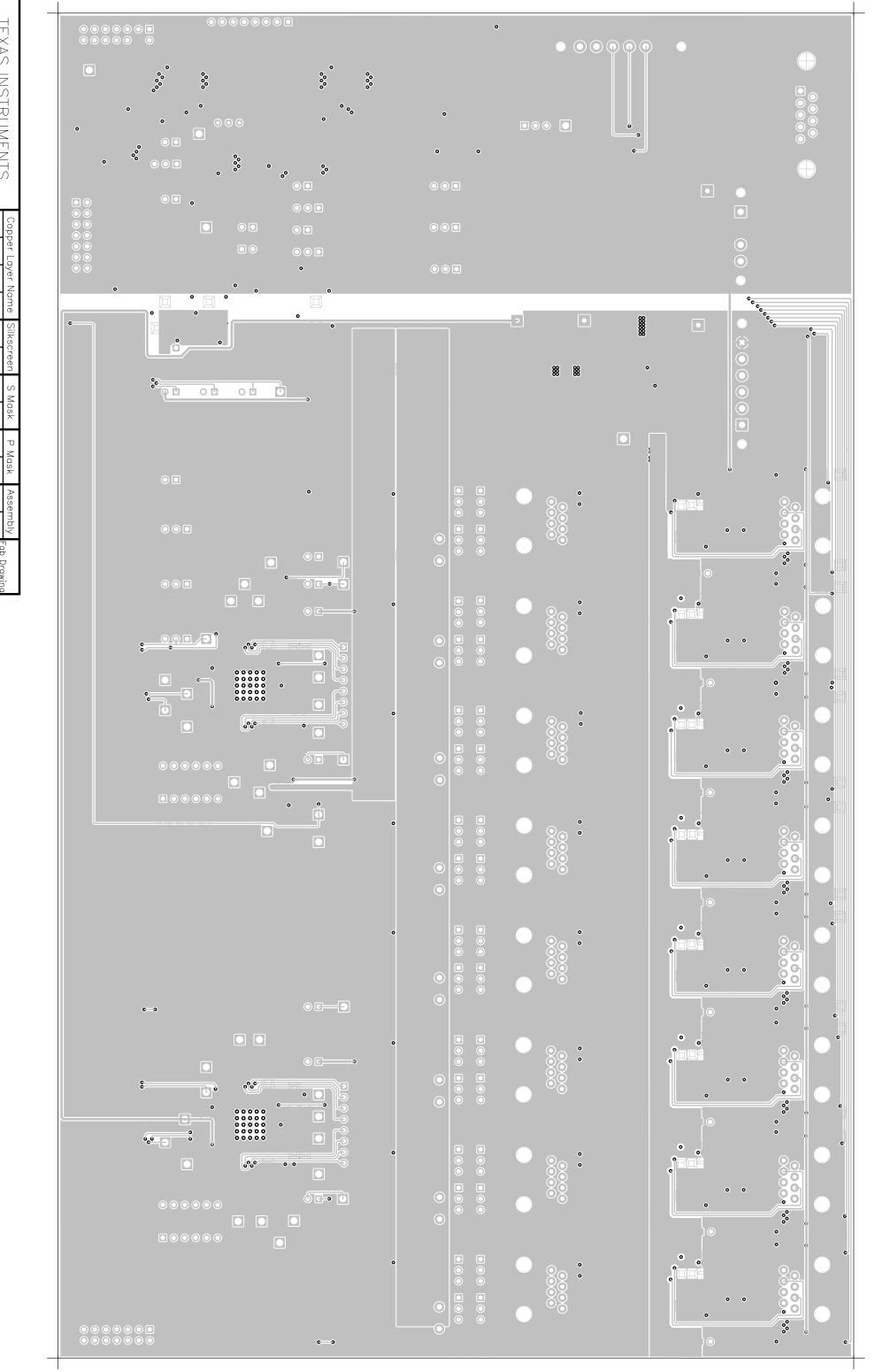
PCB Dsgnr: J.Smith

Modified Date: Fri Jan 19, 2007

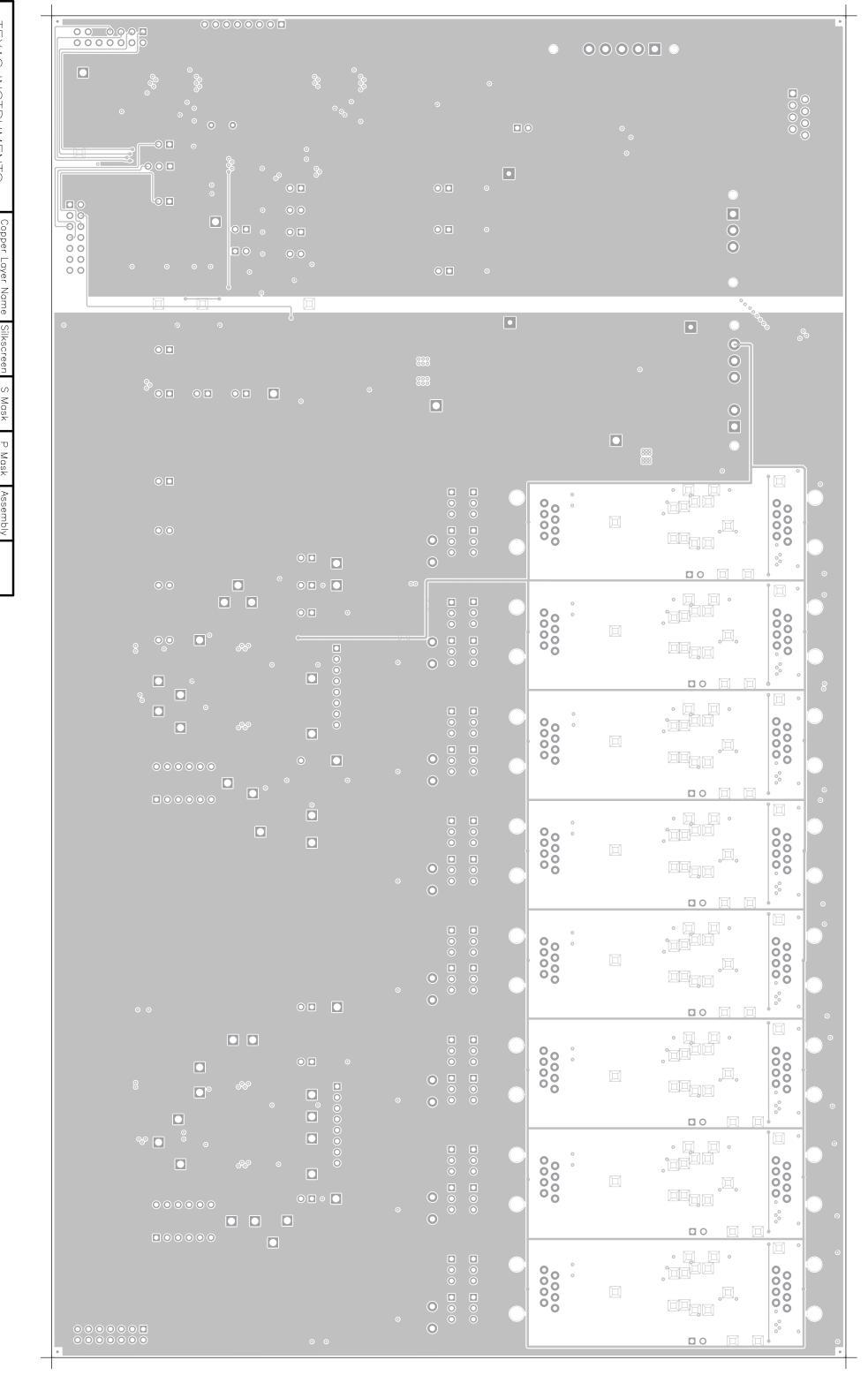
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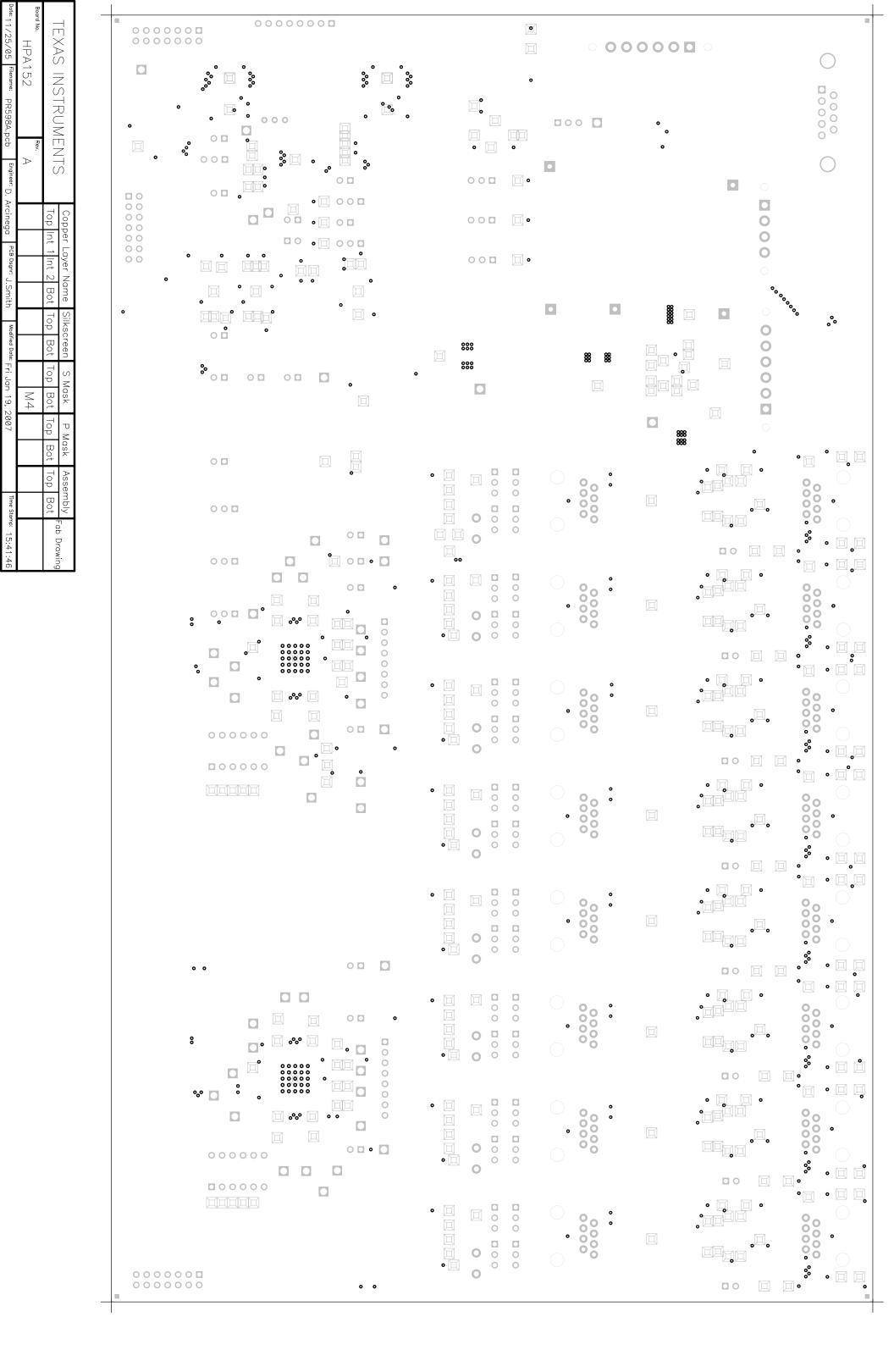


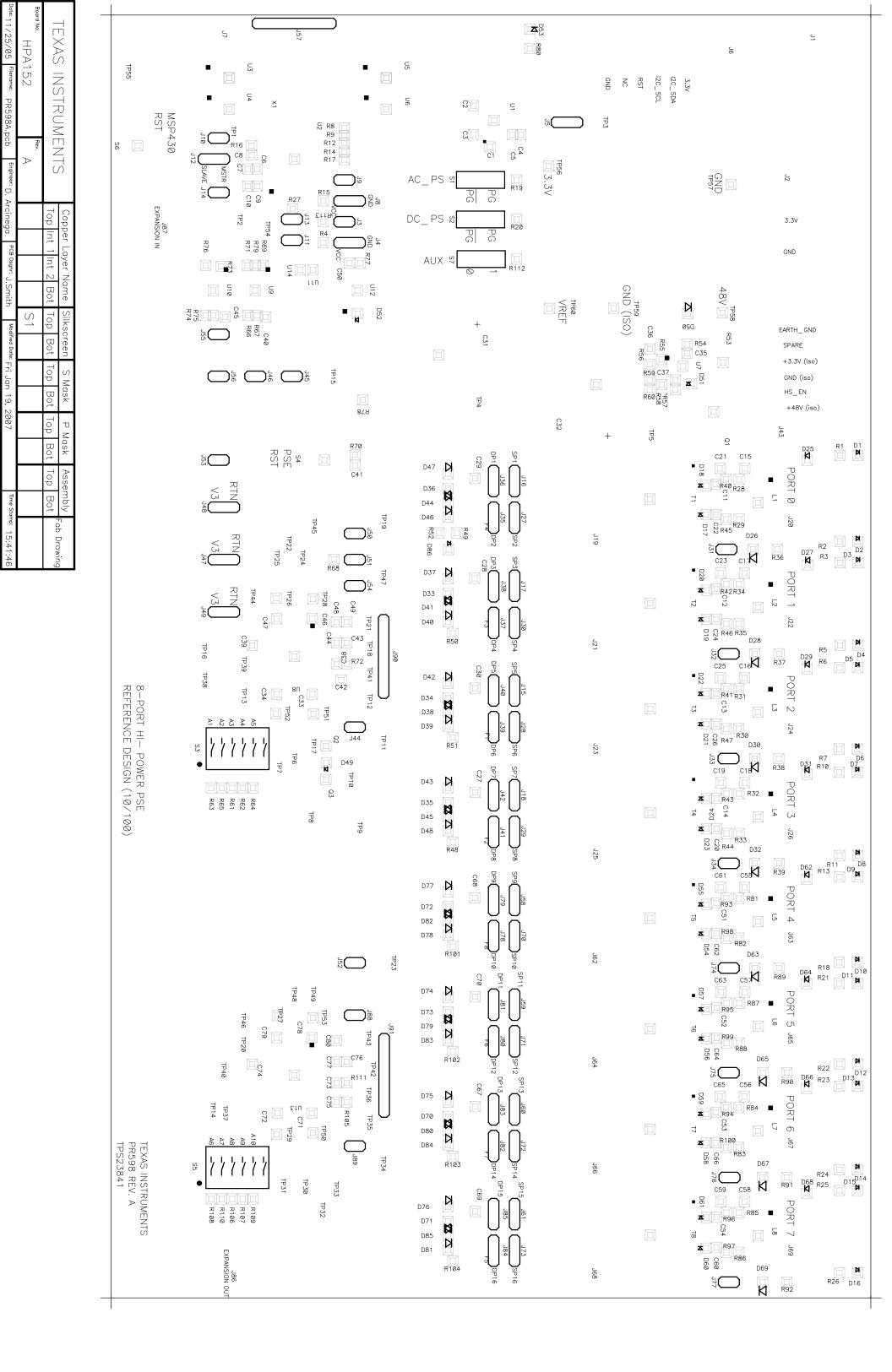


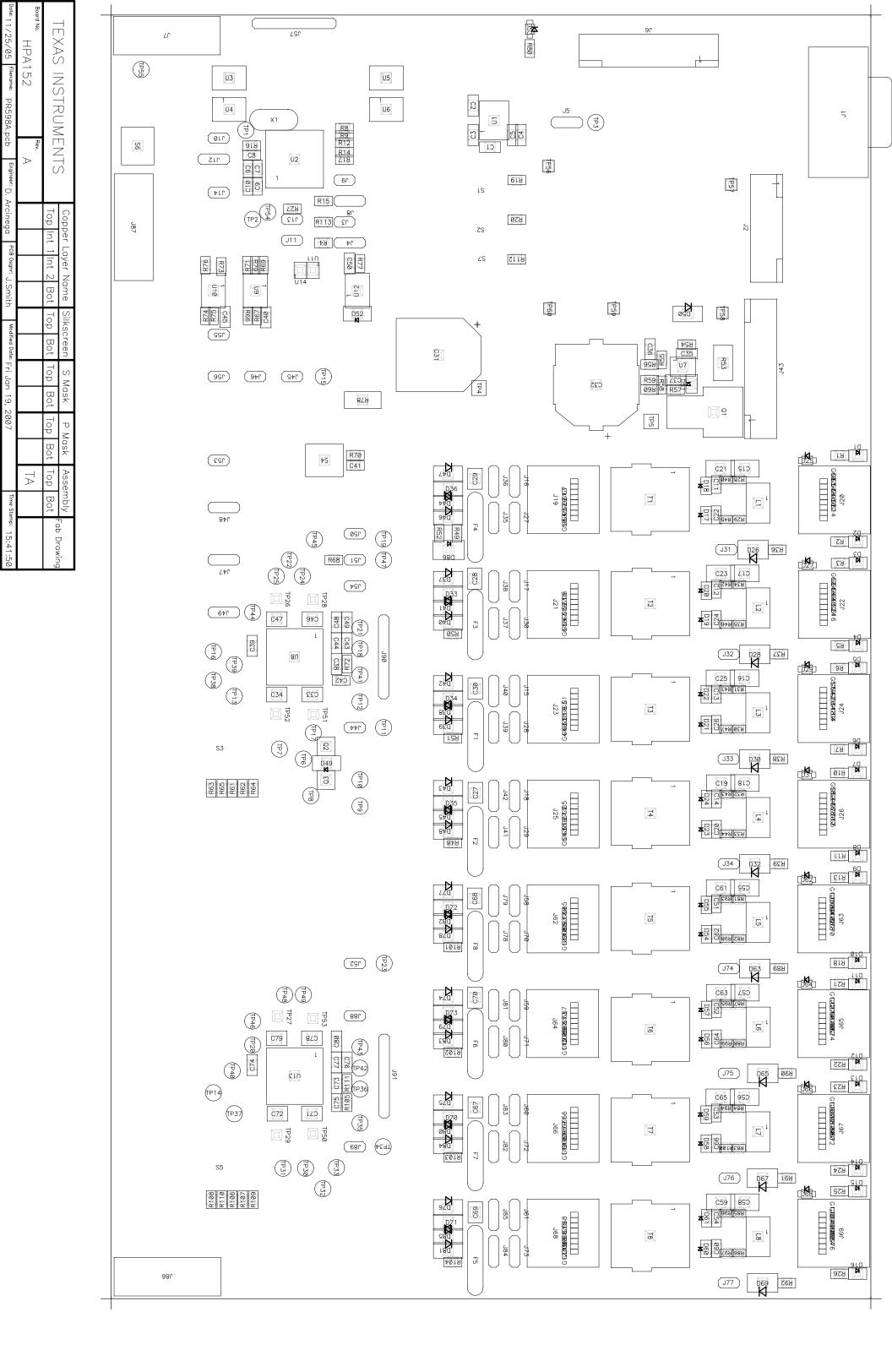
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