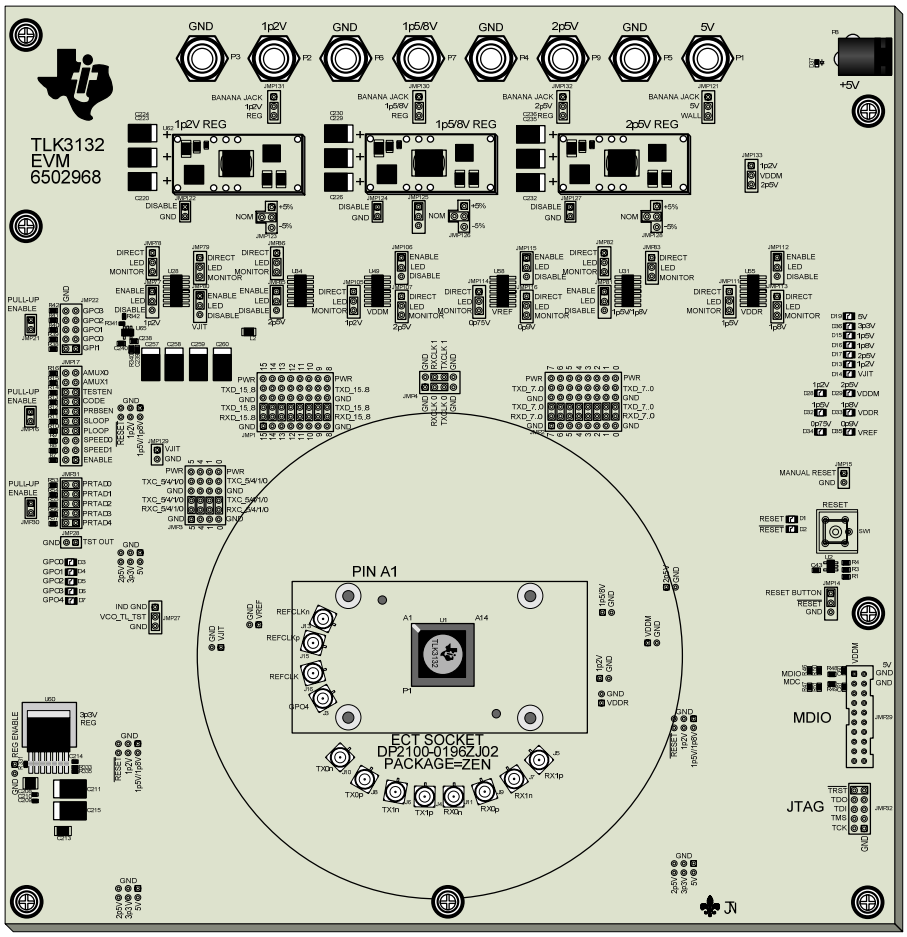
TLK3132 2-Channel Multi-Rate Transceiver Evaluation Module (EVM) Users' Guide

ABSTRACT

This User's Guide describes the usage and construction of the TLK3132 evaluation module (EVM). This document provides guidance on proper use by showing some device configurations and test modes. In addition, design, layout and schematic information is provided to the customer. Information in this guide can be used to assist the customer in choosing the optimal design methods and materials in designing a complete system.



WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at own expense will be required to take whatever measures may be required to correct this interference.

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Introduction

The Texas Instruments (TI™) TLK3132 SerDes evaluation module (EVM) board is used to evaluate the functionality and the performance of TLK3132 2-Channel Multi-Rate Transceiver device (196-ball BGA). The TLK3132 is a flexible two channel independently configurable serial transceiver that can be configured to be compliant with the 1000Base-X 1Gbps Ethernet Specification and will also support 1X/2X/10X Fibre Channel (FC), CPRI (x1/x2/x4), OBSAI (x1/x2/x4) data rates. Many common applications may be enabled by way of externally available control pins and detailed control of the TLK3132 on a per channel basis is available by way of accessing a register space of control bits available through a two-wire access port called the Management Data Input/Output (MDIO) interface.[1]

EVM PCB and High-speed Design Considerations

The board can be used to evaluate device parameters in addition to acting as a guide for high-speed board layout. As the frequency of operation increases, the board designer must take special care to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled to 50 Ω for both the high-speed differential serial and low-speed parallel data and clock connections. Vias are minimized and, when necessary, are designed to minimize impedance discontinuities along the transmission line. Since the board contains both, serial and parallel transmission lines, care was taken also to control trace length mismatch (board skew) to less than +/- 0.5MIL.

Overall, the board layout is designed and optimized to support high-speed operation. Thus, understanding impedance control and transmission line effects are crucial when designing high-speed boards. Some of the advanced features offered by this board include:

- PCB (printed circuit board) is designed for optimal high-speed signal integrity.
- SMP and parallel header fixtures are easily connected to test equipment.
- All input/output signals are accessible for rapid prototyping.
- The entire board can be powered from a single 5V power supply where the power planes can be supplied through on-board regulators or through separate banana jacks for isolation.
- On-board capacitors provide AC coupling of high-speed transmit and receive signals.
- External parallel loop-back function can be achieved easily using simple 0.1 inch jumpers.
- Entire Board can operate from a single 5V power supply, or from individual power supplies.
- Voltage Monitoring LED circuits provide quick indication that the voltage is within specification.

[1]The MDIO register map is located within the *TLK3132 2 Channel Multi-Rate Transceiver datasheet*.

TLK3132 EVM Kit Contents

The TLK3132 EVM kit contains the following:

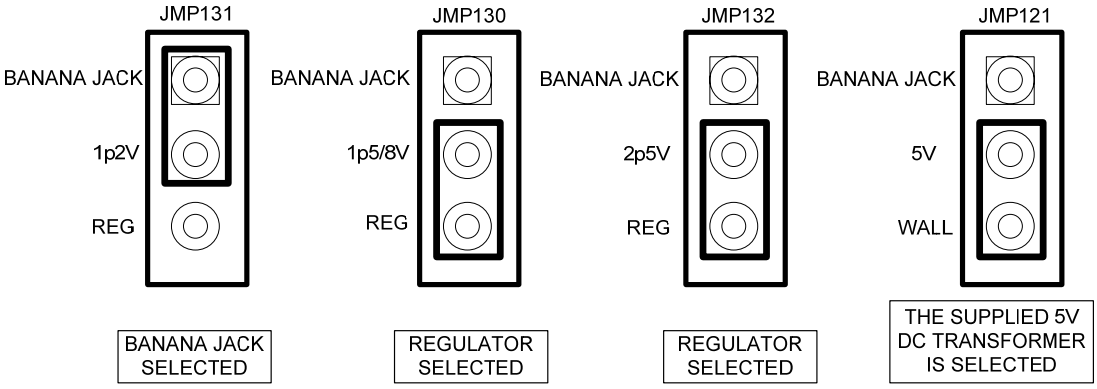
- TLK3132 EVM board
- TLK3132 EVM User's Guide (this document)
- TLK3132 2-Channel Multi-Rate Transceiver datasheet
- MDIO Interface EVM
- MDIO Interface EVM Documentation
- RS-232 Cable
- 20-conductor MDIO Ribbon Cable
- CD-ROM Containing MDIO Software
- 10 3-Foot SMA to SMP cables
- 4 1-Foot SMP to SMP cables
- 5V DC Transformer Power Supply

Power

The TLK3132 EVM can be operated off of a single 5V Power Supply utilizing the on-board voltage regulators to generate the voltages required to correctly operate the TLK3132, off of individual 1.2V, 1.5V or 1.8V, 2.5V, and 5V Power supplies, or a combination of both regulators and separate individual supplies.

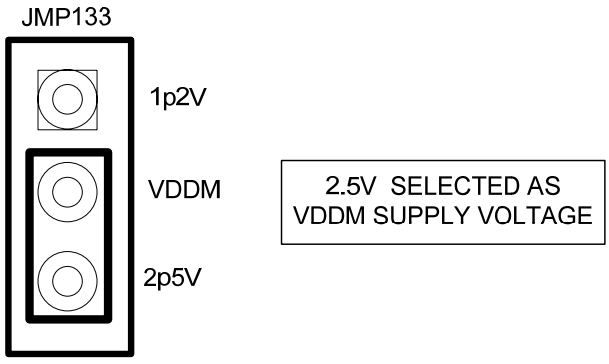
To modify your power supply configuration between either all Individual Supplies, all on-board regulators, or a combination of both, simply change the jumper position on the appropriate power supply headers (JMP130, JMP131, and JMP132) selecting either the “BANANA JACK” or the “REG” pin in combination with the center pin. The following figure shows how to use the on-board regulators for the 1.5V or 1.8V and 2.5V supply rails, and an individual power supply connected to the 1.2V Banana Jack (P2). The 5V power supply is required for operation of the LEDs on this board even if you are not using the on-board voltage regulators and can be provided from a lab power supply through the Banana Jack (P1) or through the supplied 5V DC Transformer. Changing the jumper location on JMP121 will change the 5V power supply source.

Figure 1. TLK3132 EVM Power Source Selection Example



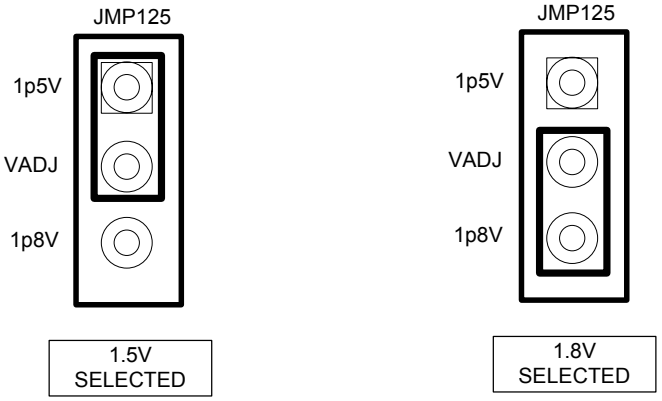
The MDIO power supply VDDM can be operated off of either 1.2V or 2.5V depending upon your specific setup. **If you are using the supplied MDIO controller board that came with this EVM kit, the 2.5V setting must be selected on the VDDM Power Select Header (JMP133).**

Figure 2. TLK3132 EVM VDDM Voltage Source Selection



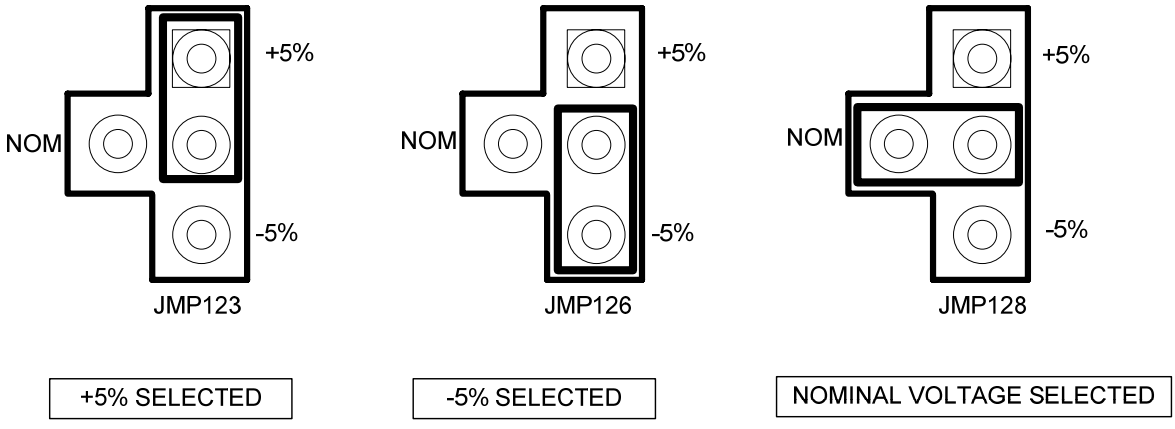
The PTH05010WAS voltage regulators included on the TLK3132 EVM are adjustable and are set with a single external resistor. Separate regulators have been provided and set to output 1.2V and 2.5V because both voltages are required simultaneously. However, since 1.5V and 1.8V are not necessarily required simultaneously, a single regulator has been configured to provide both of those voltages, although not at the same time depending upon the jumper position on JMP115 shown in the following figure. JMP125 selects between the 1.5V set resistor and the 1.8V set resistor and connects one or the other to the Voltage Adjust pin of regulator U63.

Figure 3. TLK3132 EVM VDDM Voltage Source Selection



The PTH05010WAS voltage regulators are also equipped with a +/- 5% selectable Margin Control allowing easy testing of the device near the min/max voltage limits specified in the datasheet. Place the jumper position to either the “+5%”, “-5%”, or “NOM” positions keeping the center pin in common as demonstrated in the following figure.

Figure 4. TLK3132 EVM Regulator Margin Selection



When the on-board regulators are not being used and independent power supplies are being used instead, i.e. the case of a voltage tolerance test, the on-board regulators should be disabled to prevent the regulator's voltage sense line from trying to regulate the voltage supplied through the banana jack and not from its own output. This is accomplished by placing a short on the headers (JMP122, JMP124, and JMP127) labeled "DISABLE". The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator. A large 0 ohm resistor has been installed at the voltage entrance point of each power plane and can be replaced with a ferrite bead of desired. In this situation, the 0 ohm resistors on the sense lines can be interchanged to connect the sense line directly to its output and eliminate the additional components that could otherwise create instability on the regulator's output. For the 1.2V regulator, the R350 0 ohm resistor should be removed and the R351 populated with a 0 ohm resistor. For the 1.5V or 1.8V regulator, R343 should be removed and placed on R345, and similarly R353 should be moved to R355 for the 2.5V regulator.

The VREF plane is sourced through a Voltage Divider providing half of the voltage on the 1p5/8V plane. The VDDQ and VDDR power pins of the TLK3132 can both be operated off of either 1.5V or 1.8V with VREF being half of whatever voltage is on the VDDQ pins. The VREF plane can be powered through the plane monitoring header (JMP7) and removing the 0 ohm resistor (R347) although this is not recommended. A separate VDDR plane has been added as there is no relationship between the VDDR pin and the VDDQ pins, however, the VDDR plane is sourced through a 0 ohm resistor (R344) from the voltage on the 1p5/8V plane that provides power to the VDDQ pins. This resistor can be replaced with a ferrite bead or removed completely and an external supply can be connected to the VDDR Header (JMP9) in the case different voltages are desired on the two planes.

Furthermore, for more accurate current readings the PULLUP_EN Jumpers on all control pin headers can be removed quickly disconnecting the pullup resistors from the voltage plane. However, the removal of the PULLUP_EN jumpers will also require manual high/low control of every control pins

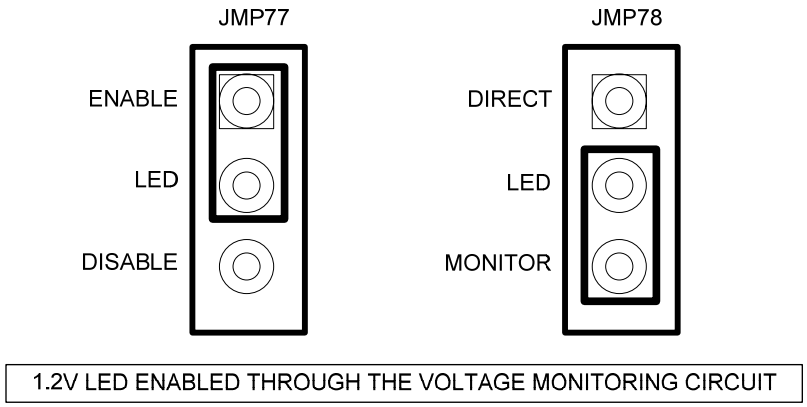
A dedicated LDO 1.2V Regulator (U65) is used to power the Jitter Cleaner Power Plane and should be considered for the end application. Due to the nature of the PLL circuitry, poor performance could result from noise on the VDDA_VCO, VDDA_CP, VDD_CML, VDD_PLL power and VSSA_VCO, VSSA_CP, VSS_CML, VSS_PLL ground pins. Separating the source and using an Low Dropout Regulator instead of a switching regulator will provide the best performance of the Jitter Cleaner Circuit. However, the performance of the device without this LDO can be observed by removing the R340 0 ohm resistor and installing a Ferrite Bead or Inductor of your choice on either of the L2 and L3 place holder footprints. When using a switching regulator and/or trying to share a common source for the Jitter Cleaner Power pins and the other 1.2V Digital Core power pins, noise filtering and suppression is crucial because all digital and switching noise below the PLL cutoff frequency will be passed directly through to the chip providing additional unwanted jitter. Additional de-coupling capacitors have been supplied on this plane to facilitate the evaluation of this device with the power sources that may require more or less bulk plane capacitance in order to achieve the desired level of performance.

Power Monitoring LEDs

Each plane of the TLK3132 EVM has been equipped with a Voltage Monitoring circuit that will monitor the voltage on the plane and light the LEDs when the voltage is within the min/max datasheet limits for that power supply. A precision TI Voltage Reference chip is used along with 0.1% precision resistors setting min and max reference levels providing a detection circuit that is accurate to approximately +/- 10mV. The LEDs should be used as a basic indication of the status of power on the board being within the acceptable min/max limits given in the datasheet, and not as a precise measurement tool as some LED circuits may turn off at slightly different voltages when approaching the limits due to the manufacturing tolerances and available component values.

The voltage monitor circuits can also be bypassed and the LEDs driven directly from the voltage on the individual planes such as when performing voltage tolerance tests. Instead of being lit only when the voltage on the plane is within the min/max range, the LED will be lit when the voltage is greater than the voltage needed to turn on the LED drive circuit's NPN transistor, allowing current to flow, and the LED to be lit from the 5V source. In the Direct Connect mode, the base resistors has been given extra margin to allow the LEDs to light when the voltage on the plane is a little below the minimum limit of that supply in order to provide a LED indicator of power on the plane during voltage tolerance tests near the lower supply limits.

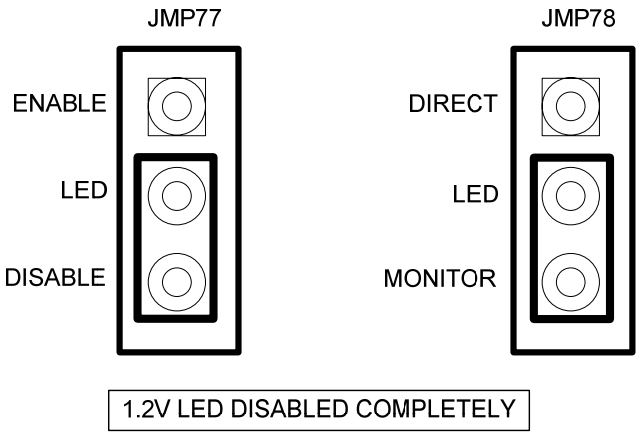
Figure 5. TLK3132 EVM Voltage Monitor LED Enabled Example



Placing the jumper on the ENABLE side of the Voltage Monitor Enable/Disable header connects the power plane to the input of the voltage monitoring circuit. This input is high impedance and will not load down the power source providing the voltage to the plane.

Placing the header on the MONITOR side of the LED Monitor/Direct Connect selection header connects the LED drive circuit to the output of the Voltage Monitor circuit causing the LED to be lit only when the voltage is within the acceptable range.

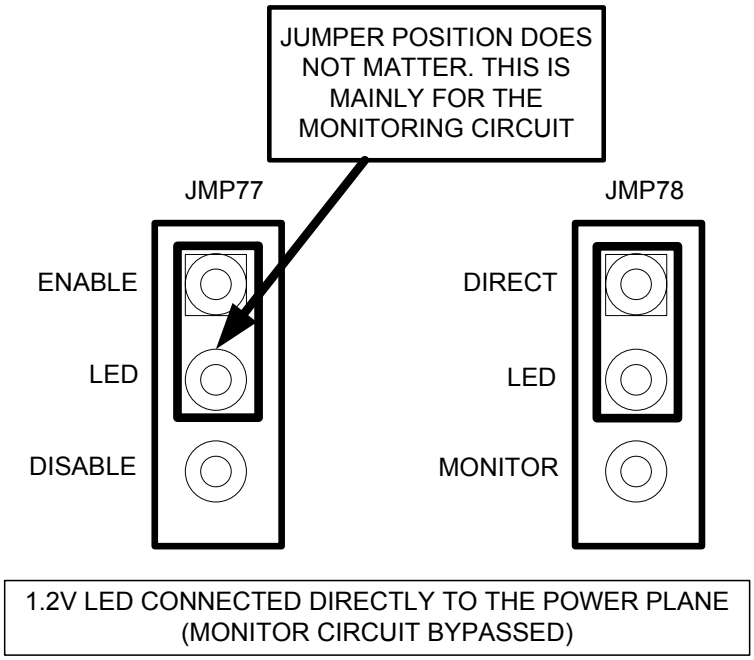
Figure 6. TLK3132 EVM Voltage Monitor LED Disabled Example



Placing the jumper on the DISABLE side of the Voltage Monitor Enable/Disable header disconnects the power plane to the input of the voltage monitoring circuit and instead ties the input to GND. This prevents the output of the Voltage Monitoring Circuit from floating and possibly causing the LED to flicker during contact with the board.

Placing the jumper on the MONITOR side of the LED Monitor/Direct Connect selection header connects the LED drive circuit to the output of the Voltage Monitor circuit causing the LED to be off since the voltage monitor circuit will sense that the plane voltage is GND which is less than the acceptable plane voltage.

Figure 7. TLK3132 EVM Voltage Monitor LED Connected Directly to Plane Example



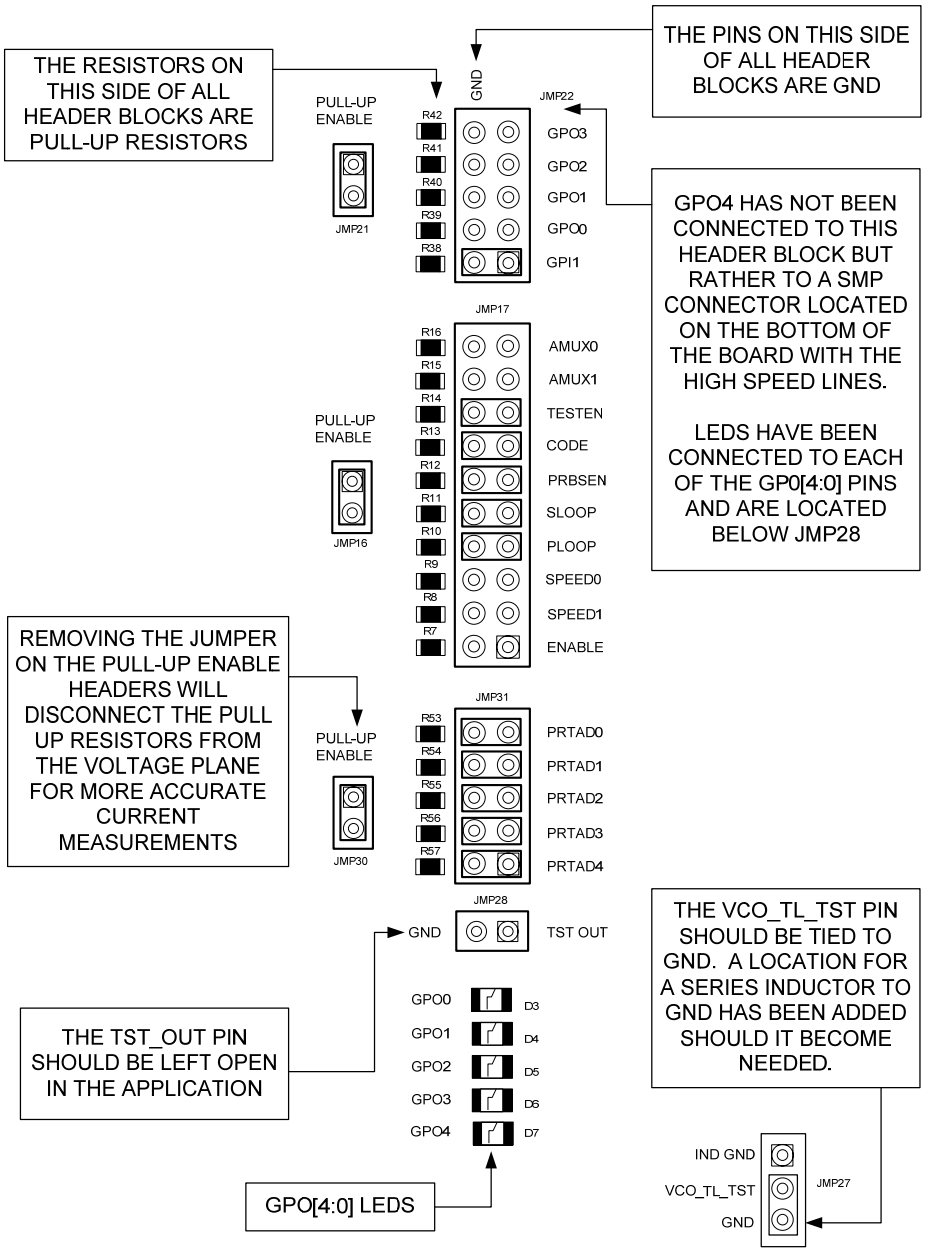
Placing the jumper on the DIRECT side of the LED Monitor/Direct Connect selection header connects the LED drive circuit to the power plane itself causing the LED to be lit when the voltage is great enough to cause current to flow through the LED drive circuit. This LED configuration has been designed to be used when pushing the lower limits of the acceptable voltage range to continue to provide an indicator that power is on the plane, however without regards to what that voltage may actually be.

The jumper on the Voltage Monitor Enable/Disable header does not matter as this is only the input to the voltage monitor circuit which has been bypassed when the LED drive circuit is connected directly to the power plane itself.

Control Signals

All of the external control pins on the TLK3132 EVM have been consolidated to a single location on the board and broken out into several header blocks for easier reference. LEDs have been added to the GPO[0:4] lines in addition to the headers for scope probes, to allow easy monitoring of the High/Low value on the line. The LED will be ON when the line is a Logic High, and the LED will be OFF when the line is a Logic Low.

Figure 8. Control Connectors (JMP16, JMP17, JMP21, JMP22, JMP27, JMP28, JMP30, JMP31)



Control Signal Pin Description:

VCO_TL_TST: This pin is the VCO Testability Input and should be grounded in the application.

TST_OUT: This is the Jitter Cleaner Testability Pin. This signal should be left open (unconnected) in the System Application.

GPO[4:0]: These are General Purpose Outputs and must be left open (unconnected) in the System Application.

GPI1: This is the General Purpose Input and must be Grounded in the System Application.

AMUX0: This is the SERDES Analog Mux 0 TX pin and must be open (unconnected) in the System Application.

AMUX1: This is the SERDES Analog Mux 1 RX pin and must be open (unconnected) in the System Application.

TESTEN: This is the Test Mode Enable Input pin and must be Grounded in the System Application.

CODE: This signal is logically OR'd with the PCS_EN register bit (Register Bit 17.3). RGMII/GMII applications can either tie this input signal high which is preferred, or tie this signal low and program the PCS_EN 17.3 register bit after a device reset to high if CODE is tied off low. Non RGMII/GMII applications must tie this input signal low.

PRBS_EN: This is the PRBS Enable Pin. When this pin is asserted HIGH, the internal PRBS generator and comparator circuits are enabled on the transmit and receive data paths of all channels. The PRBS results for each channel can be read through MDIO counters. Primary chip output signals GPO1/GPO0 remain low during PRBS testing when the input serial stream PRBS pattern is correct, and pulse high when PRBS errors are detected on the input serial stream on a per channel basis.

> **GPO1:** Contains the Channel 1 PRBS currently passing (when low) indication.
>
> **GPO0:** Contains the Channel 0 PRBS currently passing (when low) indication.
>
> An external loopback connection (via external cables) is required during PRBS testing.
>
> PRBS 2^7-1 is transmitted on each transmit channel serial output, and compared on each receive channel serial input.

SLOOP: This pin is the Serial Loop Enable pin. When SLOOP is asserted HIGH, the serial input from each channel is internally looped back to that channel's serial output, making that channel a serial repeater. In device configurations where clock tolerance compensation is not performed in the transmit direction, there are two options for error free serial loopback operation:

1) Frequency lock (0 ppm) the incoming serial data rate to the local reference clock device input.
2) Provision the TX SERDES REFCLK to run from a jitter cleaned version of the RX SERDES RXBCLK (Receive Byte Clock).

PLOOP: This pin is the Parallel Loop Enable pin. When PLOOP is asserted HIGH, the serial output for each channel is internally looped back to its serial input so that the transmit parallel interface input data is output onto the receive parallel interface.

SPEED[1:0]: These are the Speed Selection Pins and put both channels of the TLK3132 into one of the three supported (full/half/quarter) channel operation speeds.

00 – BothChannels in Full Rate mode

01 – BothChannels in Half Rate mode

10 – Both Channels in Quarter Rate mode

11 – Software Selectable Rate

In the Software selectable rate mode, the rate for each channel may be configured independently by the MDIO interface.

The SPEED[1:0] inputs control both RX and TX directions for both channels.

Please see Appendix A of the TLK3132 Datasheet for further information on speed selection (full/half/quarter) for proper settings as a function of the application mode and reference clock frequency.

Please note that if these pins are not configured on the application board to select "Software Selectable Rate", then the internal speed register bits cannot be used to control the rate settings, and the full/half/quarter rate selection is fixed.

ENABLE: This is the Device Enable pin. When ENABLE is held low, the device is in a low power state. When ENABLE is high the device operates normally. **A hard or soft reset must be applied after a change of state occurs on this input signal.**

PRTAD[4:0]: These are the Port Address Assignment Pins and are used to select the Device ID/Port ID in Clause 22 MDIO mode.

PRTAD[4:1] selects a block of two sequential Clause 22 port addresses. Each channel is implemented as a different port address, and can be accessed by setting the appropriate port address field within the Clause 22 MDIO transaction.

PRTAD[0] is not used functionally, but is needed for device testability with other devices in the family of products.

Channel 0 responds to port address 0 within the block of two port addresses.

Channel 1 responds to port address 1 within the block of two port addresses.

MDIO

The TLK3132 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 22 of the IEEE 802.3 Ethernet Specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK3132 is possible without the use of this interface, however, some additional features are accessible only through this interface.

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The device ID and port address are determined by control pins PRTAD[4:0

In Clause 22, the top 4 control pins PRTAD[4:1] determine the device port address. In this mode the 2 individual channels in TLK3132 are classified as 2 different ports. So for any PRTAD[4:1] value there will be 2 ports per TLK3132. The TLK3132 will respond if the 4 MSB's of PHY address field on MDIO protocol (PA[4:1]) matches PRTAD[4:1]. The LSB of PHY address field (PA[0]) will determine which channel/port within the TLK3132 to respond to.

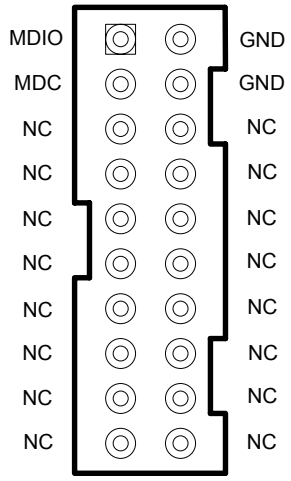
If PA[0] = 1'b0, TLK3132's Channel 0 will respond.

If PA[0] = 1'b1, TLK3132's Channel 1 will respond.

Write transactions which address an invalid register or read only registers will be ignored. Read transactions of invalid registers will return a "0".

The bi-directional MDIO pin is pulled up to 1.2V or 2.5V (VDDM) with a 1.5k Ω resistor as per the MDIO Standard.

Figure 9. TLK3132 EVM MDIO Connector (JMP29)



JMP29

JTAG

The EVM also provides a separate connector to support the full five-pin JTAG interface of the TLK3132 as defined in IEEE 1149.1 for manufacturing tests.

TDI: This pin is the JTAG Input Data pin and is used to serially shift test data and test instructions into the device during the operation of the test port.

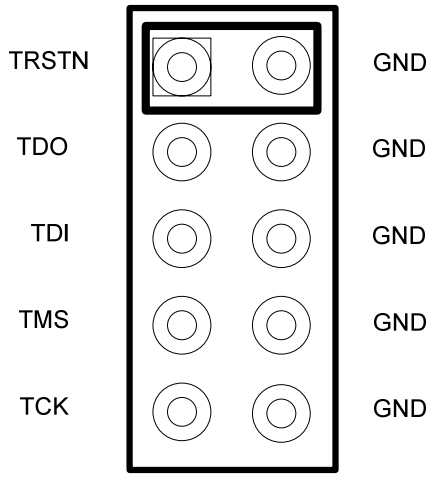
TDO: This pin is the JTAG Output Data pin and is used to serially shift test data and test instructions out of the device during operation of the test port. When the JTAG port is not in use, TDO is in a high impedance state.

TMS: This pin is the JTAG Mode Select pin and is used to control the state of the internal test-port controller.

TCK: This is the JTAG Clock pin and is used to clock state information and test data into and out of the device during the operation of the test port.

TRST_N: This is the JTAG Test Reset pin and is used to reset the JTAG logic into system operational mode. **NOTE: TRST_N should be tied low when the JTAG port is not in use and during normal operation of the port as shown in the following figure.**

Figure 10. TLK3132 EVM JTAG Connector (JMP32)



JMP32

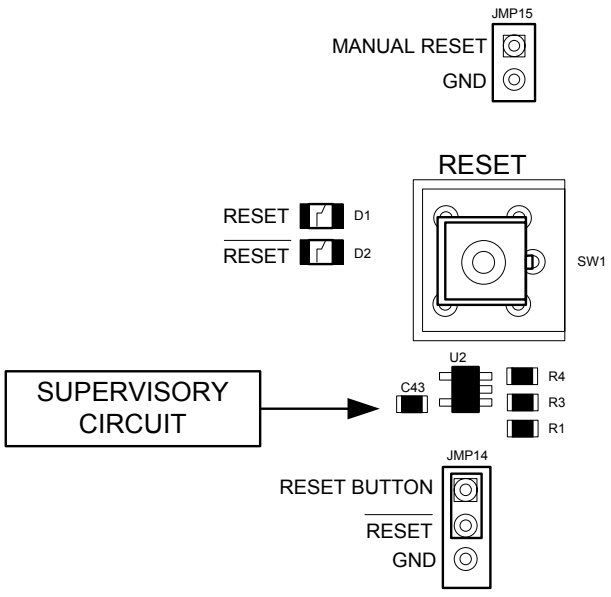
Reset

The TLK3132 EVM comes configured for Manual Reset operations involving the Pushbutton Reset Switch (SW1). When switch SW1 is pressed, the TLK3132 device RESET pin (RST_N) goes LOW and the entire TLK3132 device is reinitialized. A TI TPS3125J18 Ultra Low Voltage Processor Supervisory Circuit is used to control the Reset line. During power-on, /RESET pin of U2 is asserted when the supply voltage becomes higher than 0.75V. Thereafter, the supply voltage supervisor monitors the voltage and keeps /RESET output active as long as the Voltage remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_d=180ms, starts after the voltage has risen above the threshold voltage (V_{IT}).

There is also a manual reset input to the supervisory circuit, /MR, which accepts the input from the pushbutton switch SW1. A low level at /MR causes /RESET to become active, thus resetting the TLK3132 device whenever the pushbutton RESET is pressed. By placing a jumper on JMP15, the Manual Reset (/MR) is tied hard to ground causing the TLK3132 to be held in a constant state of Reset without the need to continually hold the Reset Pushbutton SW1. The Supervisory circuit will release the Reset line to a HIGH 180mS (t_d) from the time the /MR line becomes greater than the threshold voltage (V_{IT}).

By removing the jumper from JMP14, the Supervised Reset Circuit is disconnected from the RST_N line. Reset control from an external controller or piece of equipment can be connected directly to pin 2 (RST_N) of JMP14 and a ground pin GND has been added to the JMP14 header next to the RST_N pin to allow easy access for the return current on that cable.

Figure 11. RESET Switch (SW1, JMP10, or JMP11)

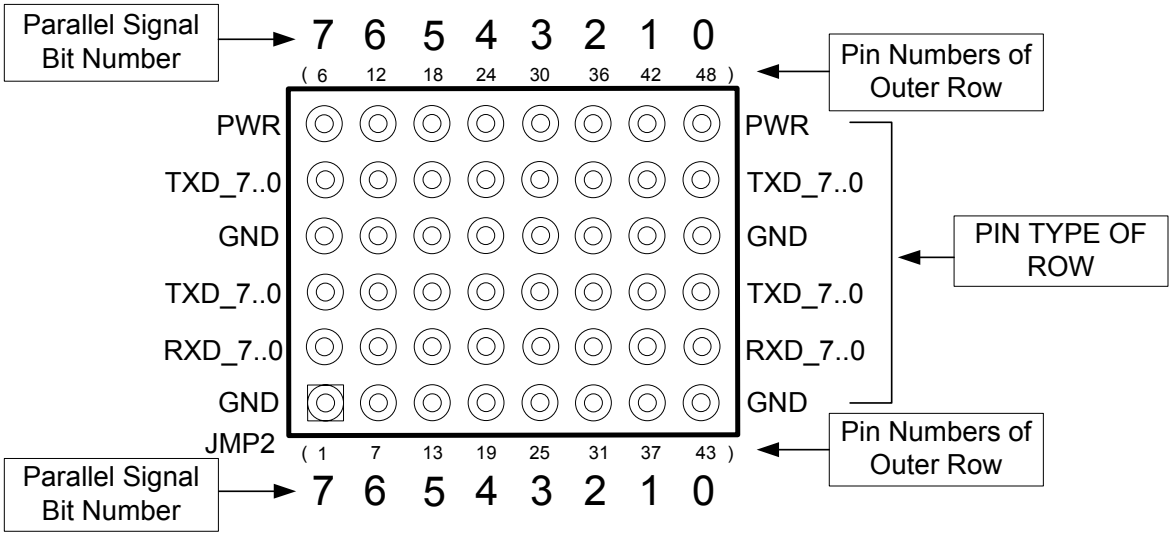


NOTE: The Jumper on JMP14 connecting RESET SW to RST_N must be connected as shown in order to cause the TLK3132 to be reset and reinitialized If switch SW1 is pressed, the device RESET pin (RST_N) goes LOW, the entire TLK3132 device is reinitialized.

Parallel Signals

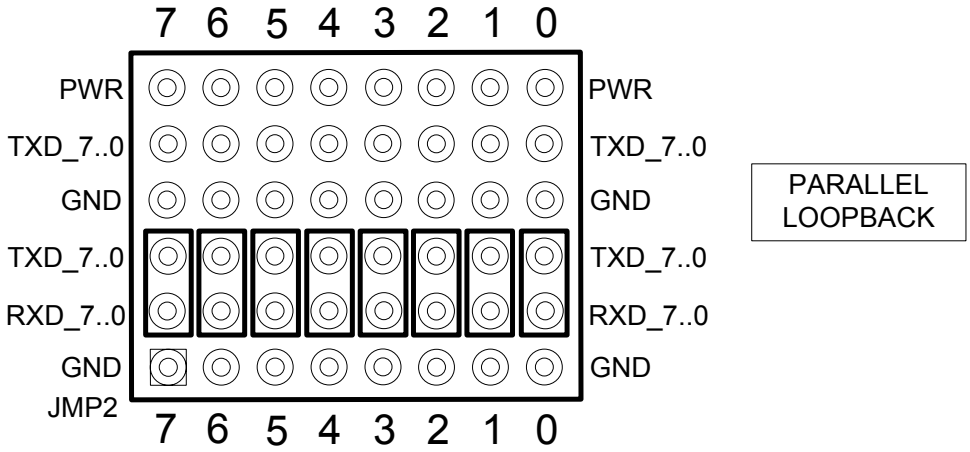
The parallel signals on the TLK3132 EVM have been routed to a 0.1” header block that is configured like the following figure. All RXD pins on header blocks RXD[7:0], RXD[15:8], as well as all TXD pins on header blocks TXD[7:0], TXD[15:8], have matched trace lengths to themselves +/- 0.5MIL.

Figure 12. Parallel Signal Header Block Diagram



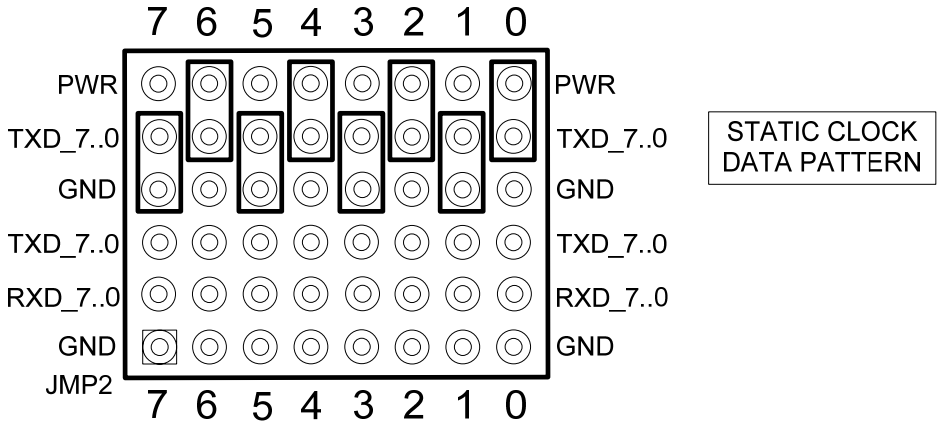
Parallel Loop back, shown in the following figure, can be easily implemented by placing Jumpers on the RXD/TXD pins of the header. For example, placing a jumper on pins 2 and 3 of JMP2 will loop back TXD7 to RXD7.

Figure 13. Parallel Loopback Example



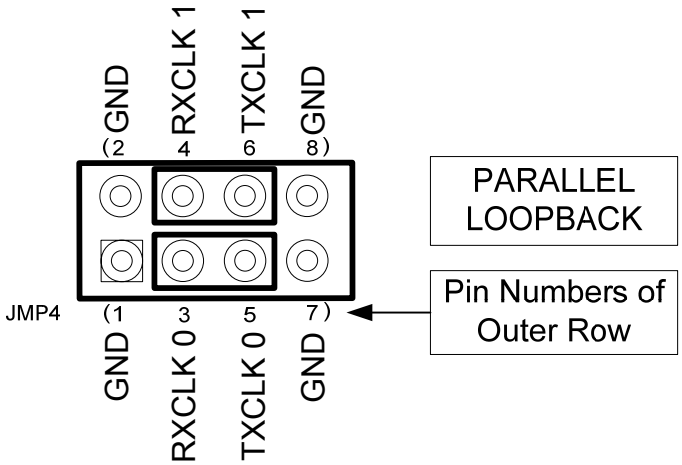
Additional GND and VDD pins have been added into the header block for several reasons. The GND pins next to the RXD and TXD pins provide a convenient ground reference for a scope probe or coax cables. The additional TXD row and VDD pins allow a static pattern to be driven into the TXD bus by placing jumpers across either the TXD and VDD pins for a HIGH, or TXD and GND pins for a LOW eliminating the need for cables during quick tests. The extra row of TXD can also be used to monitor the signals on the TXD pins. The following figure shows a clock pattern (01010101) on TXD[7:0].

Figure 14. TXD Static Clock Data Pattern Example



The Transmit Data Clocks and Receive Data Clocks are located in header block JMP4 with the clock pins next to each other. These signals are the parallel side input and output clocks per channel. During Parallel Loopback, the clocks can be jumpered together as shown in the following diagram.

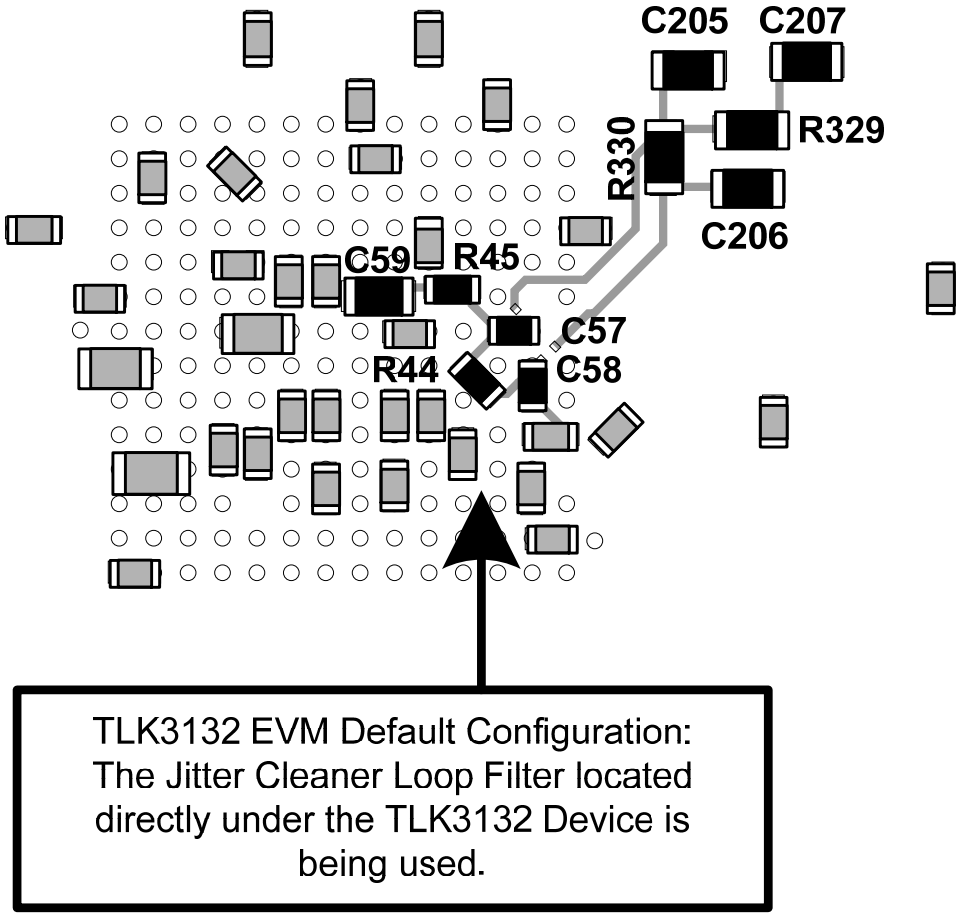
Figure 15. RXCLK Parallel Loop Back with Static Data Pattern Example



Jitter Cleaner External Loop Filter

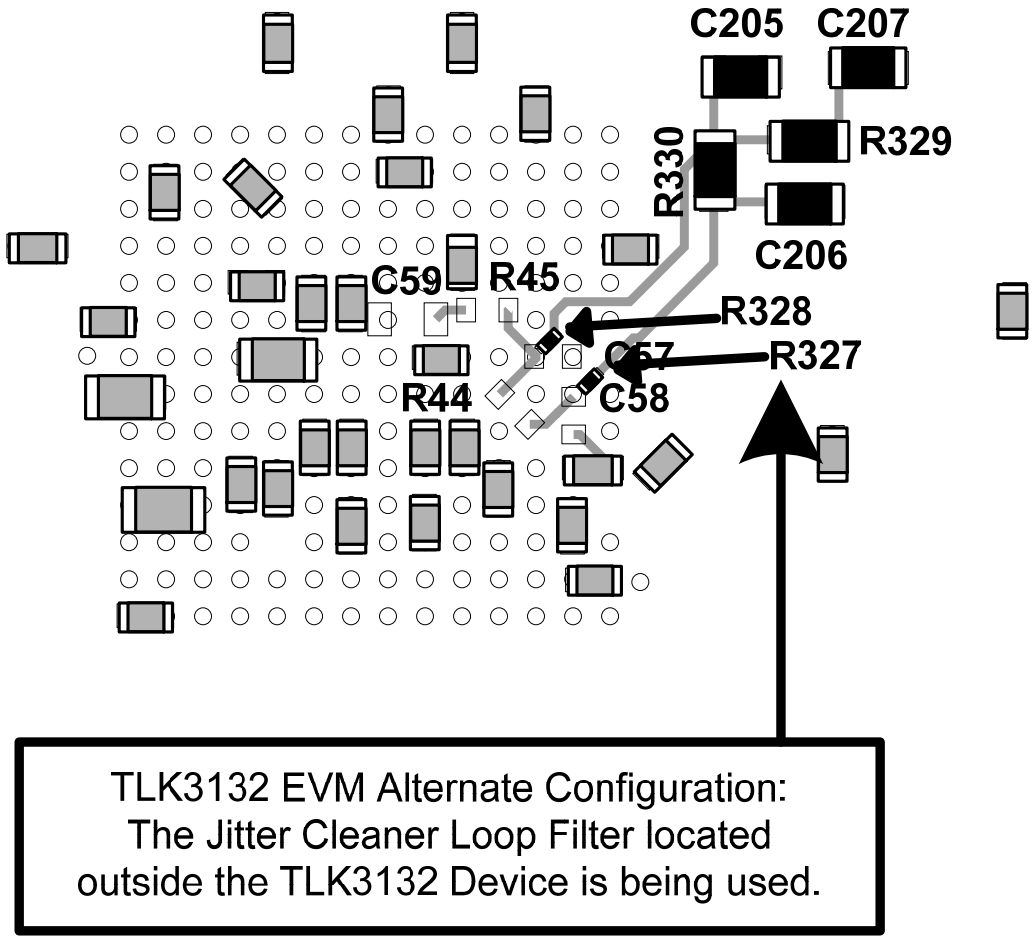
The TLK3132 Jitter Cleaner requires an external loop filter be added to the board as described in the TLK3132 Datasheet. Package size and placement of these 5 resistor and capacitor components is critical and can affect the performance of the Jitter Cleaner circuit. These 5 components have been carefully placed directly under the TLK3132 Device using 0402 packages in order to minimize the trace length and size of the loop filter circuit, as well as reduce the exposure to other signals that will couple unwanted noise into this circuit.

Figure 16. Jitter Cleaner Loop Filter Default Configuration



However, due to cost and manufacturing requirements, an external placement of these components relative to the TLK3132 Ball Field as well as an increase in package size to 0603 devices may be required. For this reason, a second Loop Filter circuit has been installed on this EVM, though not connected by default, to allow for the evaluation of the TLK3132 under these requirements. To engage the 0603 sized loop filter that has been placed outside the TLK3132 ball field instead of the 0402 sized loop filter that is placed inside the ball field, simply remove the following components (R44, R45, C57, C58, and C59) and install a 0-ohm 0201 resistor (or create a solder short) on R327 and R328. Refer to sheet 5 of the TLK3132 EVM Schematics located in the Schematics section of this document.

Figure 17. Jitter Cleaner Loop Filter Alternative Configuration



Peripheral Ports

The TLK3132 EVM can support 3 small peripheral boards which could contain any sort of additional circuitry required for effective evaluation of the TLK3132 device. Examples of additional circuitry that could be implemented would include a clock source such as an oscillator with multiplier/divider chip, FPGA, CPLD, or even an optical module just to name a few. All of the power rails (1.2V, 1.5/8V, 2.5V, 3.3V and 5V) have been provided to allow for minimal power circuitry on the peripheral board itself as well as the global reset signal which is connected to the TLK3132 Reset Pin. TI is developing a clock multiplier and divider peripheral board specifically for use with the TLk3132 EVM which would be capable of providing practically any clock frequency needed for operation of the TLK3132 device. However, it is not complete and ready for distribution with the TLk3132 EVM. Refer to sheet 17 of the TLK3132 EVM Schematic located in the Schematics section as well as the line item in the BOM for connector Part Number information.

Gigabit Ethernet Mode (RGMII) Test and Setup Configuration

The device reset requirements and setup procedure to configure the TLK3132 for Gigabit Ethernet Mode (RGMII) is as follows:

*Note: All global registers must be accessed indirectly through Clause 22.
REFCLK frequency = 125 MHz, Serdes Data Rate = Half Rate, Mode = Transceiver, Edge Mode = Source Centered Mode, RX_CLK[n] out = TXBCLK[n], Jitter Cleaner PLL Multiplier Ratio = 1X or Off

- Device Pin Setting(s) – Pin settings allow for maximum software configurability.
  - Ensure CODE input pin is Low.
  - Ensure PLOOP input pin is Low.
  - Ensure SLOOP input pin is Low.
  - Ensure SPEED [1:0] input pins are both High.
  - Ensure ENABLE input pin is High.
  - Ensure PRBS_EN input pin is Low.
- Reset Device
  - Issue a hard or soft reset (RST_N asserted for at least 10 us -or- Write 1'b1 to 0.15)
- Clock Configuration
  - If using JCPLL (JCPLL 1X)
    JCPLL Mux Settings (Figure 2 on page 3 of the TLK3132 Datasheet rev 0.19)
    - Select REFCLK input (Default = Differential)
      - If Single Ended REFCLK used – Write 2'b01 to 37120.15:14
      - If Differential REFCLK used – Write 2'b00 to 37120.15:14
    - Write 2'b11 to 37120.13:12 to select differential REFCLKP/N as RXBYTECLK
    - Write 4'b0000 to 37120.11:8 to select jitter cleaned clock for SERDES TX/RX.
    - Write 2'b11 to 37120.7:6 to select differential REFCLKP/N as Delay Stopwatch clock input
    - Write 2'b00 to 37120.5:4 to select jitter cleaned clock for HSTL VTP 2x
    - Write 2'b00 to 16.10:9 to select SERDES TX clock as RX_CLK output (per channel)
    - Write 16'h0081 to 37126 to set Charge pump control
    - Write 16'h00A0 to 37128 to set TXRX output divider

    Clock Divide Settings (Table 132 on page 114 of the TLK3132 Datasheet rev 0.19)
    - Write 7'b1000000 to 37124.14:8 to set REF_DIV to value of 1
    - Write 1'b1 to 37124.15 REFDIV_EN to enable reference clock divider
    - Write 7'h18 to 37124.6:0 to set FB_DIV to value of 24
    - Write 1'b1 to 37124.7 FBDIV_EN to enable feedback divider
    - Write 7'h18 to 37125.6:0 to set RXTX_DIV to value of 24
    - Write 1'b1 to 37125.7 OUTDIV_EN to enable RXTX_DIV output divider
    - Write 7'h0D to 37121.14:8 to set HSTL_DIV to value of 13
    - Write 7'h06 to 37121.6:0 to set HSTL_DIV2 to value of 6
    - Write 2'b11 to 36864.14:13 to set RX Loop Bandwidth
    - Write 2'b11 to 36864.6:5 to set TX Loop Bandwidth
    - Write 4'h0101 to 36864.11:8 to set MPY RX multiplier factor to 10
    - Write 4'h0101 to 36864.3:0 to set MPY TX multiplier factor to 10
    - Write 16'h5050 to 36865 SERDES_RATE_CONFIG_TX_RX to set Half Rate
    - Write 3'b000 to 37127.14:2 to set control bits for VCO tail current to 0
    - Write 1'b1 to 37127.15 to enable Jitter Cleaner
    - Wait 50 ms in order for JCPLL to lock

  - Else if using clock bypass mode (JCPLL Off)
    JCPLL Mux Settings (Figure 2 on page 3 of the TLK3132 Datasheet rev 0.19)
    - Select REFCLK input (Default = Differential)
      - If Single Ended REFCLK used – Write 2'b01 to 37120.15:14
      - If Differential REFCLK used – Write 2'b00 to 37120.15:14
    - Select RXBYTE_CLK (Default = Differential)
      - If Single Ended REFCLK used – Write 2'b10 to 37120.13:12
      - If Differential REFCLK used – Write 2'b11 to 37120.13:12
    - Select SERDES TX Reference Clock Input (Default = Differential)
      - If Single Ended REFCLK used – Write 2'b10 to 37120.11:10

        - If Differential REFCLK used – Write 2'b11 to 4/5.37120.11:10
    - Select SERDES RX Reference Clock Input (Default = Differential)
        - If Single Ended REFCLK used – Write 2'b10 to 37120.9:8
        - If Differential REFCLK used – Write 2'b11 to 37120.9:8
    - Select DELAY_CLK (Default = Differential)
        - If Single Ended REFCLK used – Write 2'b10 to 37120.7:6
        - If Differential REFCLK used – Write 2'b11 to 37120.7:6
    - Select HSTL_2X_CLK (Default = Differential)
        - If Single Ended REFCLK used – Write 2'b10 to 37120.5:4
        - If Differential REFCLK used – Write 2'b11 to 37120.5:4
    - Write 2'b00 to 16.10:9 to select SERDES TX clock as RX_CLK output (per channel)
    - Write 7'h04 to 37121.6:0 to set HSTL_DIV2 to value of 4.
    - Write 15'h1515 to 36864.14:0 SERDES_PLL_CONFIG to set MPY RX/TX multiplier factor to 10
    - Write 16'h5050 to 36865 SERDES_RATE_CONFIG_TX_RX to set Half Rate
- Mode Control (Table 2 on page 16 of the TLK3132 Datasheet rev 0.19)
    - Write 1'b0 to 17.0 for RX source centered mode (per channel)
    - Write 1'b0 to 17.1 for TX source centered mode (per channel)
    - Write 1'b1 to 17.2 to enable 8B/10B encode decode functions (per channel)
    - Write 1'b1 to 17.3 to enable 1000Base-X PCS TX & PCS RX functions (per channel)
    - Write 1'b1 to 17.4 to set nibble order, LSB on rising edge, MSB on falling edge (per channel)
    - Write 1'b1 to 17.5 to enable DDR data on TX/RX directions (per channel)
    - Write 1'b0 to 17.6 to disable FC_PH overlay detection (per channel)
    - Write 1'b1 to 17.7 to enable comma detection (per channel)
    - Write 1'b0 to 17.9 to disable full DDR mode (per channel)
    - Write 1'b0 to 16.8 to disable Farend Loop back (per channel)
    - Write 1'b0 to 0.14 to disable loop back mode (per channel)
    - Write 3'b111 to 36874.11:9 to set channel 0 TX swing setting amplitude to 1375 mVdfpp
    - Write 1'b1 to 36874.8 to set channel 0 TX CM bit
    - Write 3'b111 to 36876.11:9 to set channel 1 TX swing setting amplitude to 1375 mVdfpp
    - Write 1'b1 to 36876.8 to set channel 1 TX CM bit
- RX equalization settings
    - Write 4'b0001 to 36866.15:12 to turn on adaptive equalization (4'b0000 is off)
    - Write 4'b0001 to 36868.15:12 to turn on adaptive equalization (4'b0000 is off)
    - Write 2'b01 to 36866,3:2 for AC coupled mode (2'b00 is DC coupled mode)
    - Write 2'b01 to 36868.3:2 for AC coupled mode (2'b00 is DC coupled mode)
- TX DLL offset
    - Write 16'h0028 to 37888 TX0_DLL_CONTROL
    - Write 16'h0028 to 37889 TX1_DLL_CONTROL
- Poll Serdes PLL Status for Locked State
    - Read 36891.4,0 SERDES_PLL_STATUS – PLL_LOCK_TX/RX
    - Keep polling until both bits are high.
- Issue Data path Reset
    - Write 1'b1 to 16.11 (per channel)
- Clear Latched Registers
    - Read 1 PHY_STATUS_1 to clear (per channel)
    - Read 18 PHY_RX_CTC_FIFO_STATUS to clear (per channel)
    - Read 19 PHY_TX_CTC_FIFO_STATUS to clear (per channel)
    - Read 28 PHY_CHANNEL_STATUS to clear (per channel)
    - Read 36891 SERDES_PLL_STATUS to clear

- Operational Mode Status
    - Read Verify 1.2 PHY_STATUS_1 – Link Status (1'b1) (per channel)
    - Read Verify 18.15 PHY_RX_CTC_FIFO_STATUS – RX_CTC_Reset (1'b0) (per channel)
    - Read Verify 19.15 PHY_TX_CTC_FIFO_STATUS – TX_FIFO_Reset_1Gx (1'b0) (per channel)
    - Read Verify 28.13:12 PHY_CHANNEL_STATUS – Enc/Dec Invalid Code Word (2'b00) (per channel)
    - Read Verify 36891.4 SERDES_PLL_STATUS – PLL_LOCK_RX (1'b1)
    - Read Verify 36891.0 SERDES_PLL_STATUS – PLL_LOCK_TX (1'b1)

Figure 18. Example TLK3132 EVM Test Configuration – Gigabit Ethernet Mode (RGMII) Serial Loopback

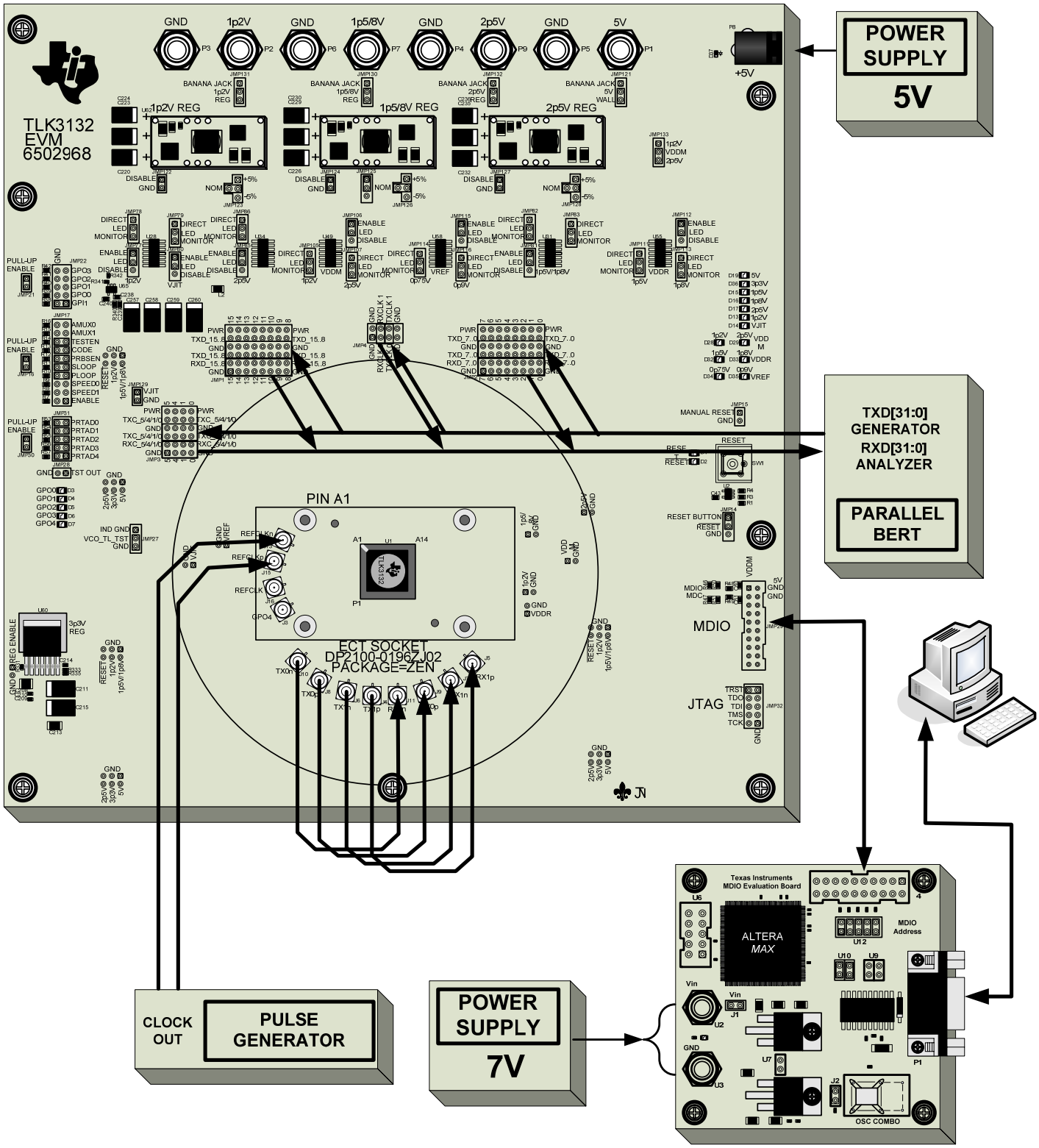
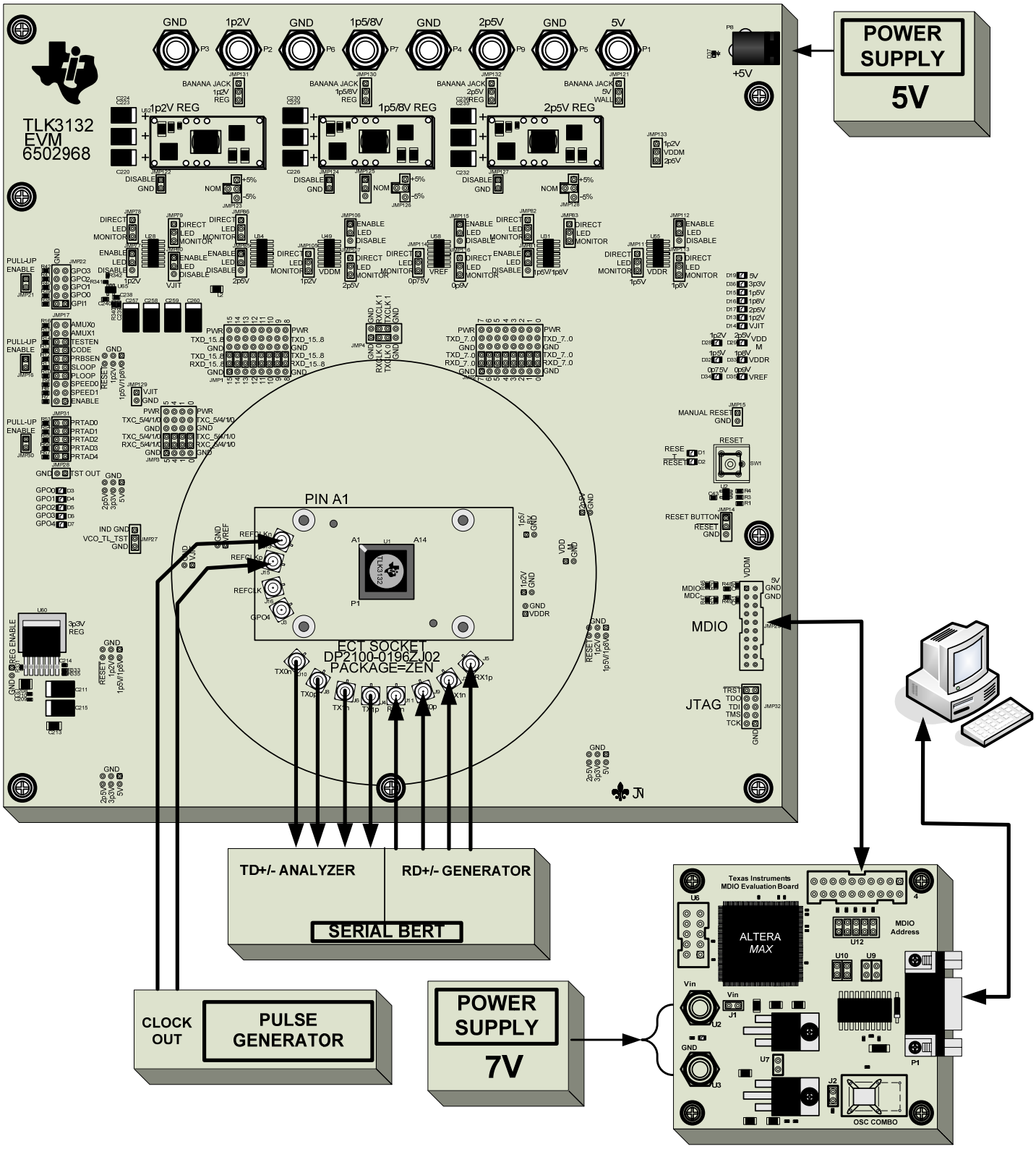


Figure 19. Example TLK3132 EVM Test Configuration – Gigabit Ethernet Mode (RGMII) Parallel Loopback



Schematics

Figure 20. TLK3132 EVM Schematic, Sheet 1 Cover Page and Index

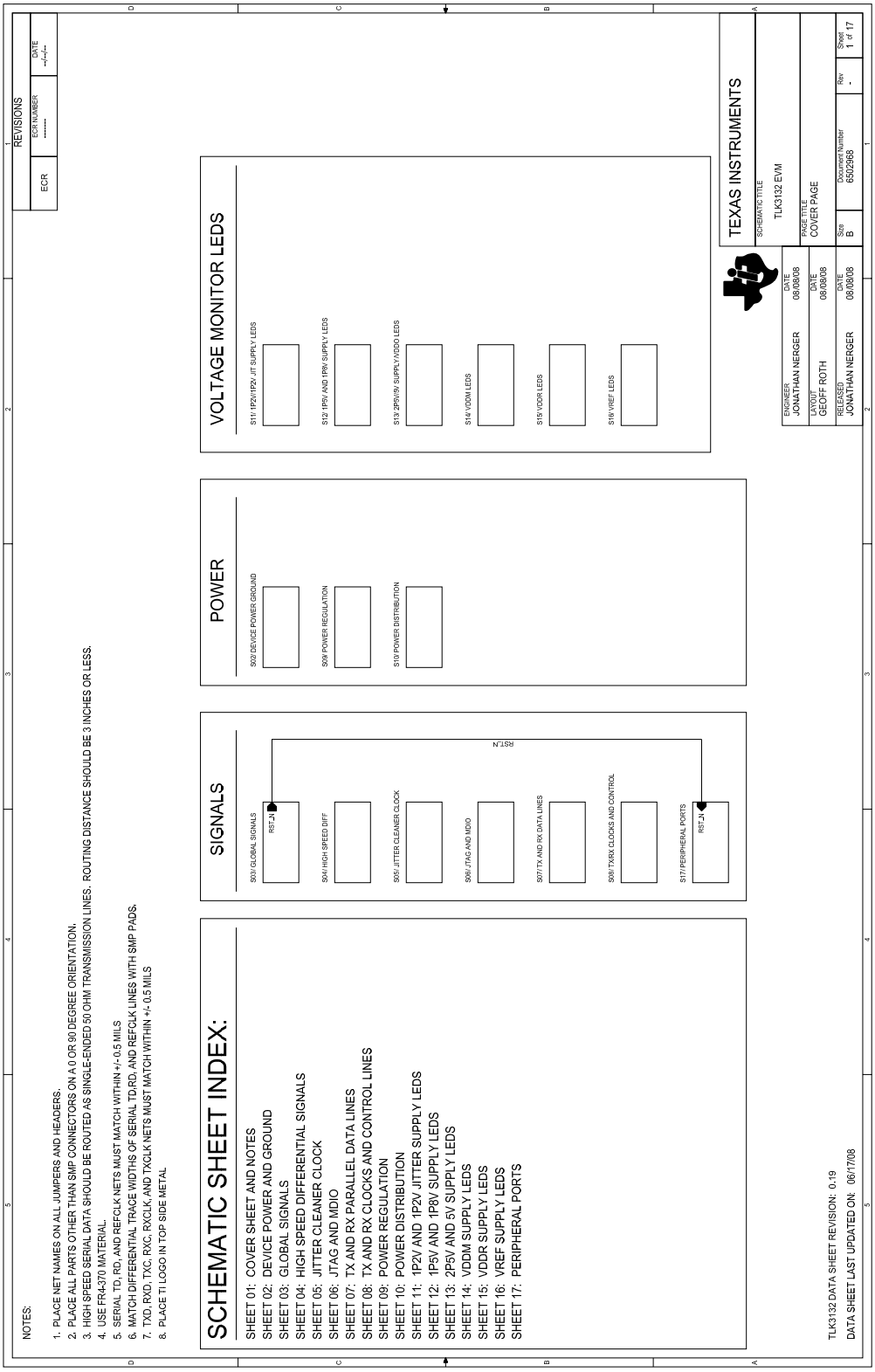


Figure 21. TLK3132 EVM Schematic, Sheet 2 Device Power and Ground

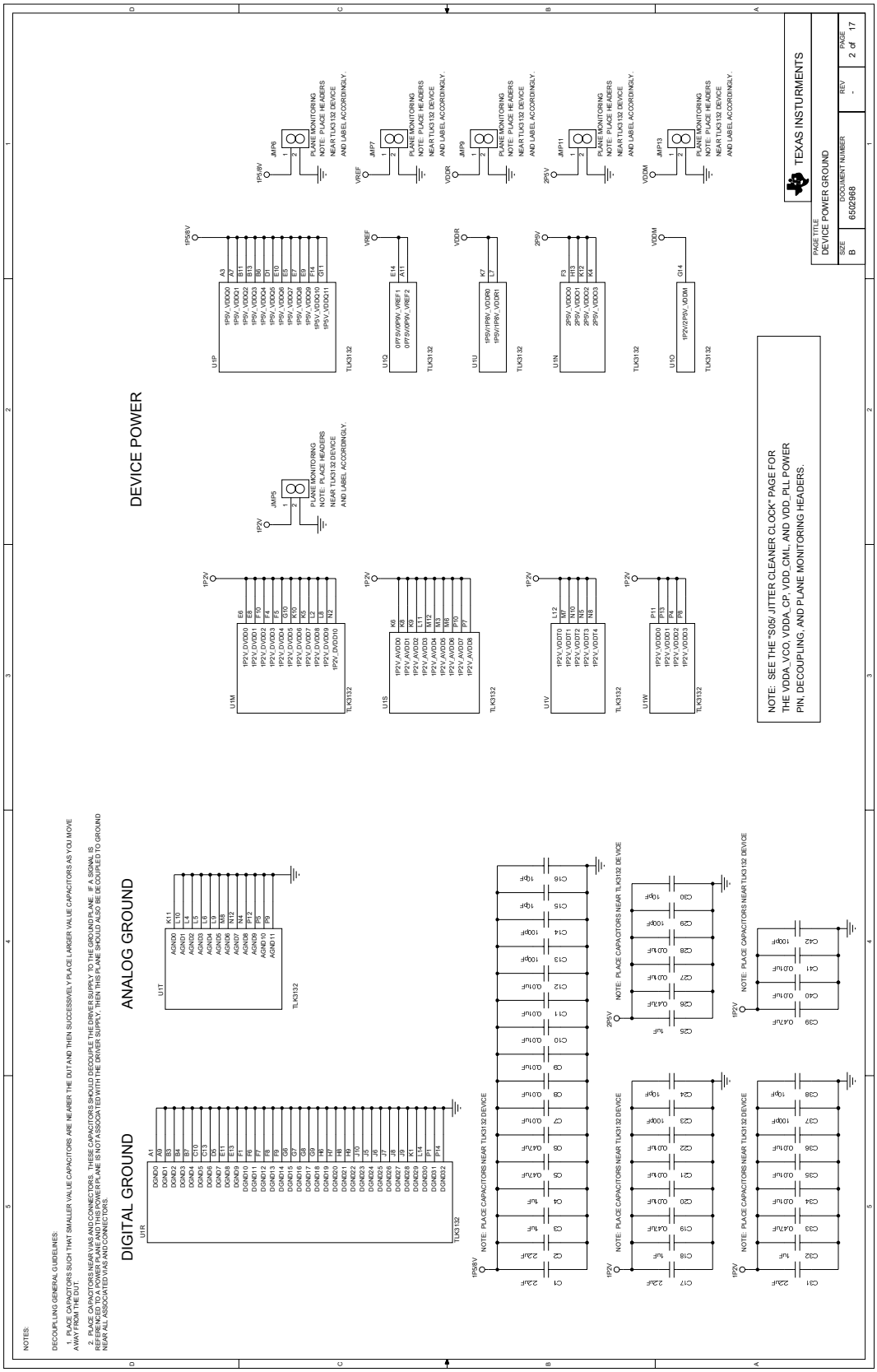


Figure 22. TLK3132 EVM Schematic, Sheet 3 Global Signals

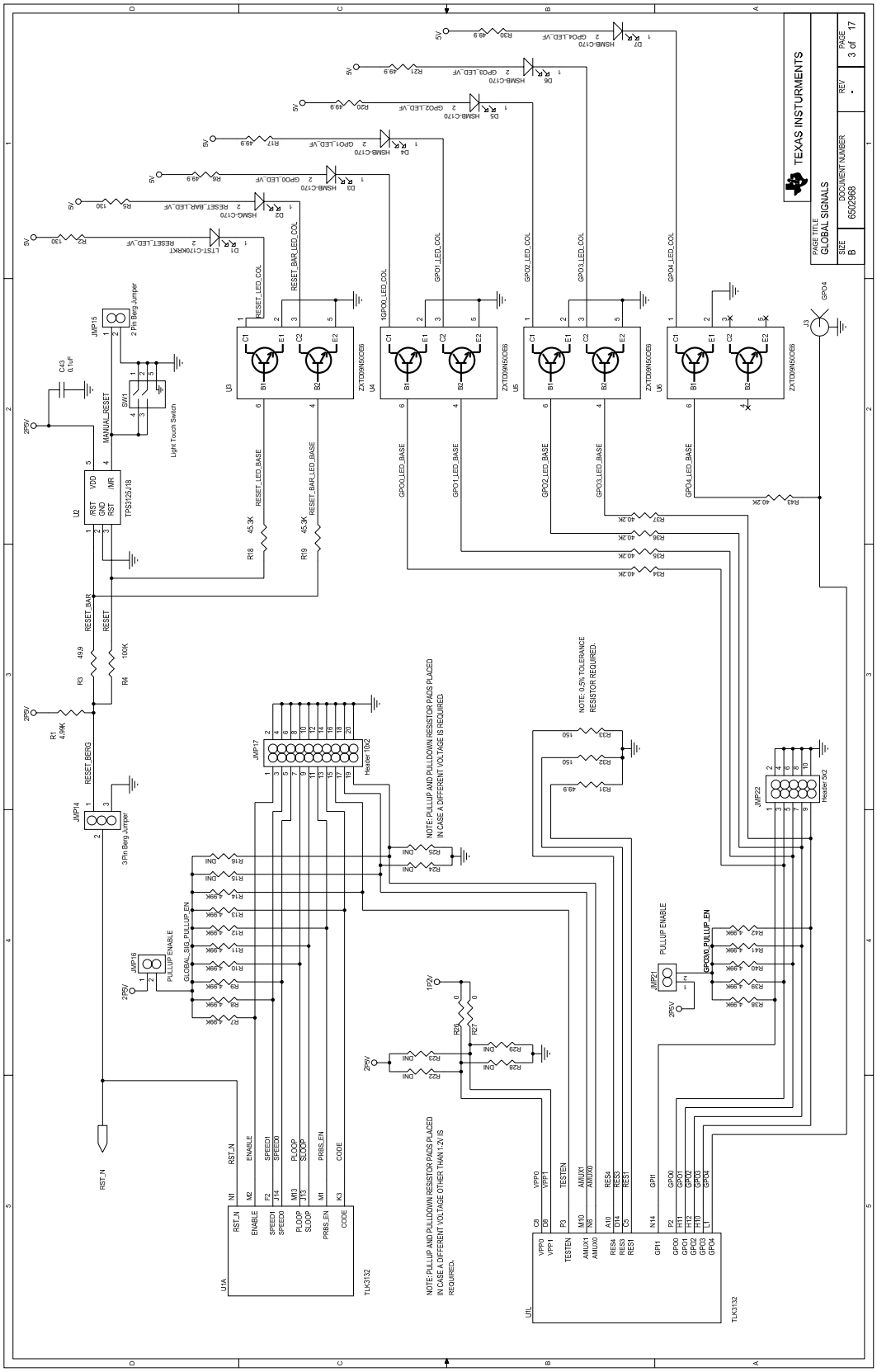


Figure 23. TLK3132 EVM Schematic, Sheet 4 High Speed Differential

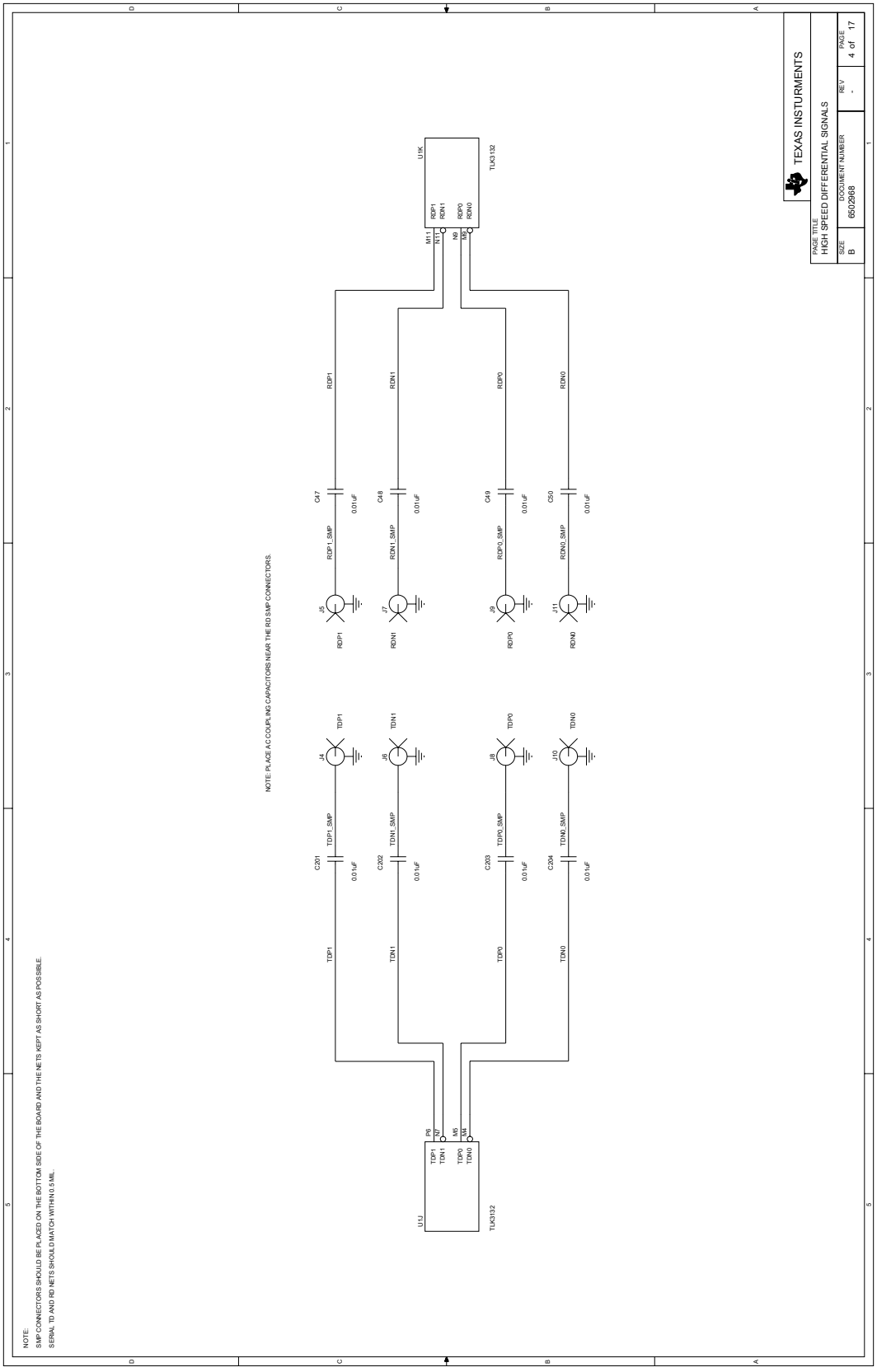


Figure 24. TLK3132 EVM Schematic, Sheet 5 Jitter Cleaner Clock

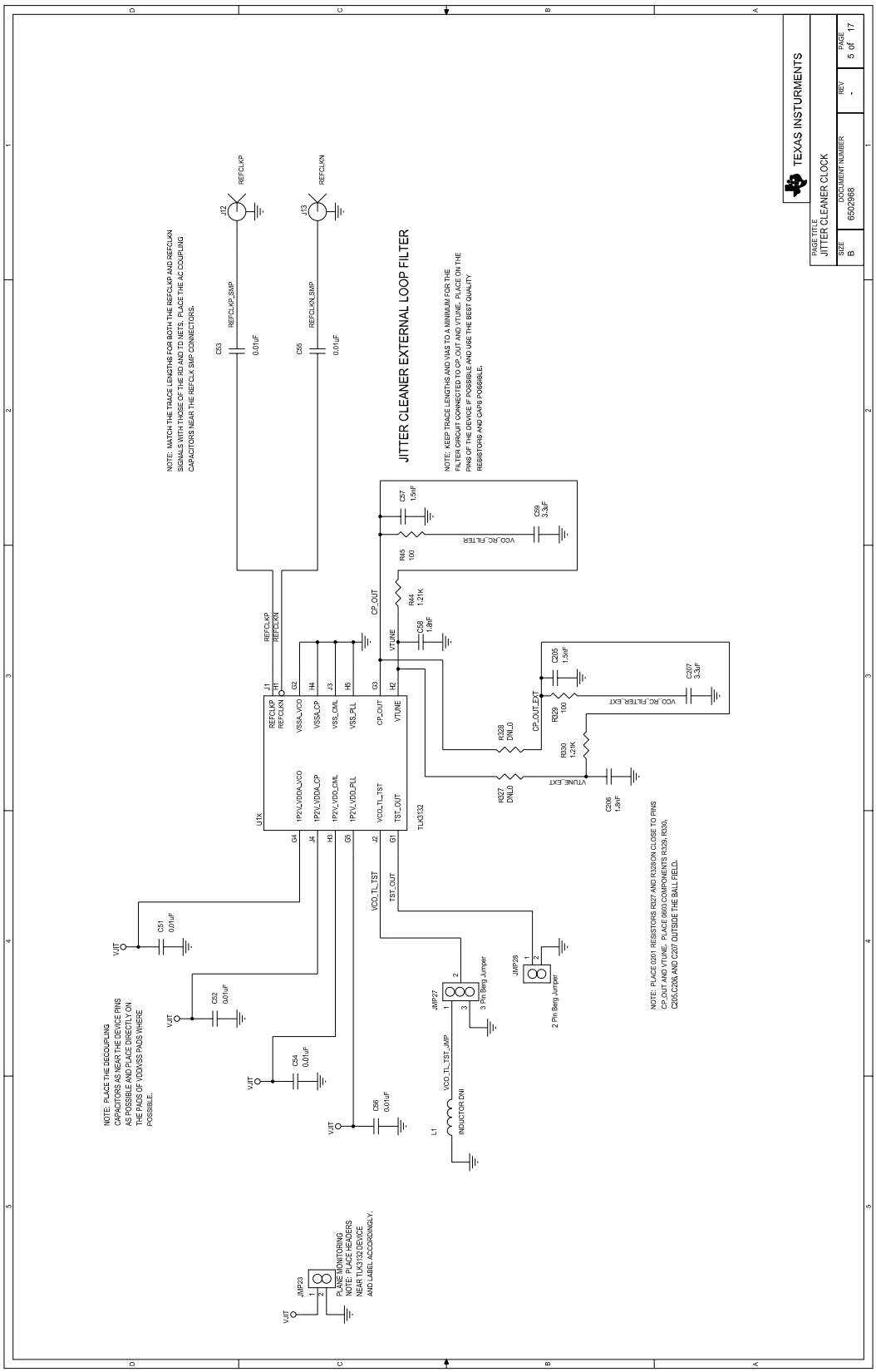


Figure 25. TLK3132 EVM Schematic, Sheet 6 JTAG and MDIO

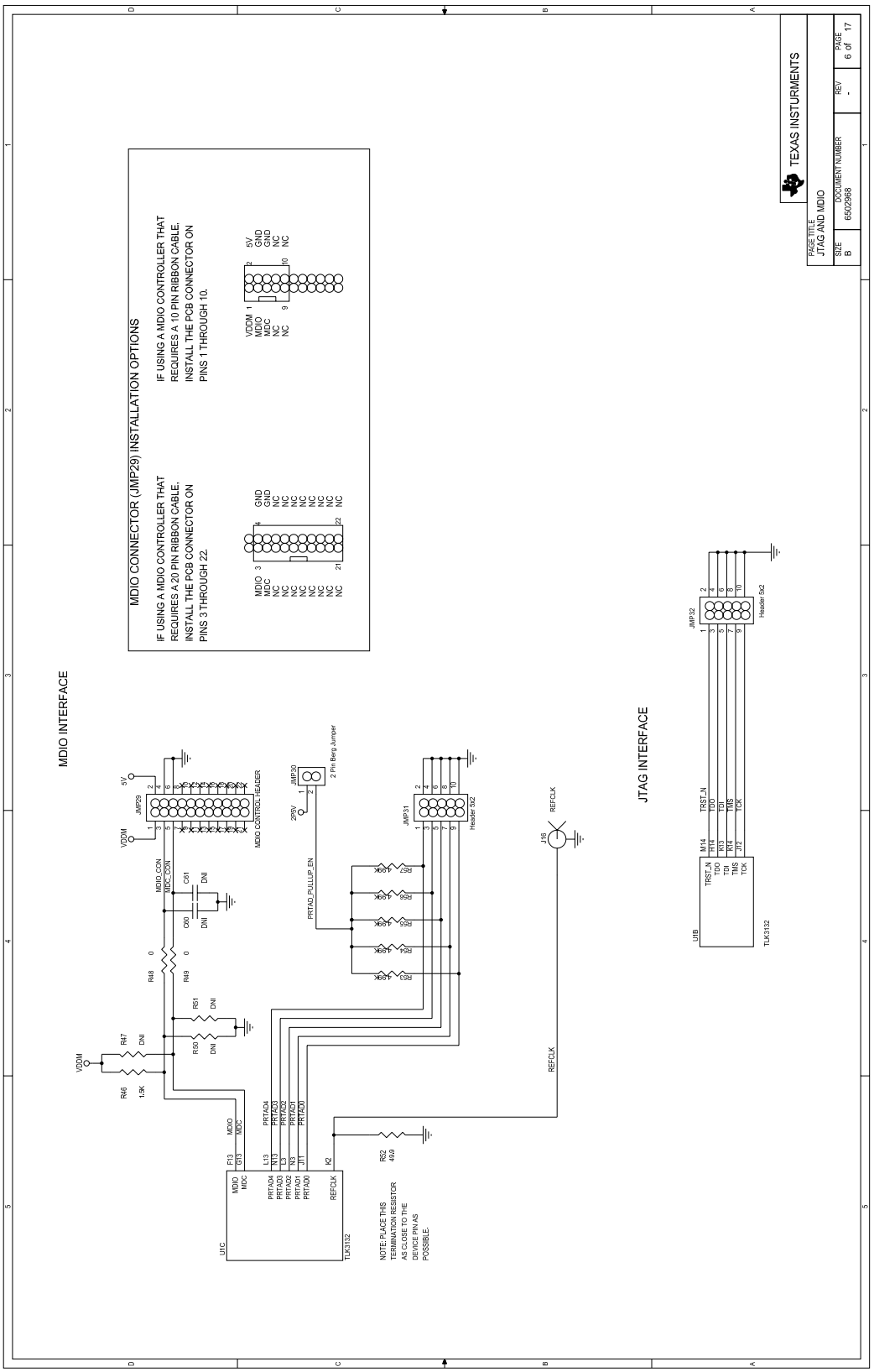


Figure 26. TLK3132 EVM Schematic, Sheet 7 TX and RX Data Lines

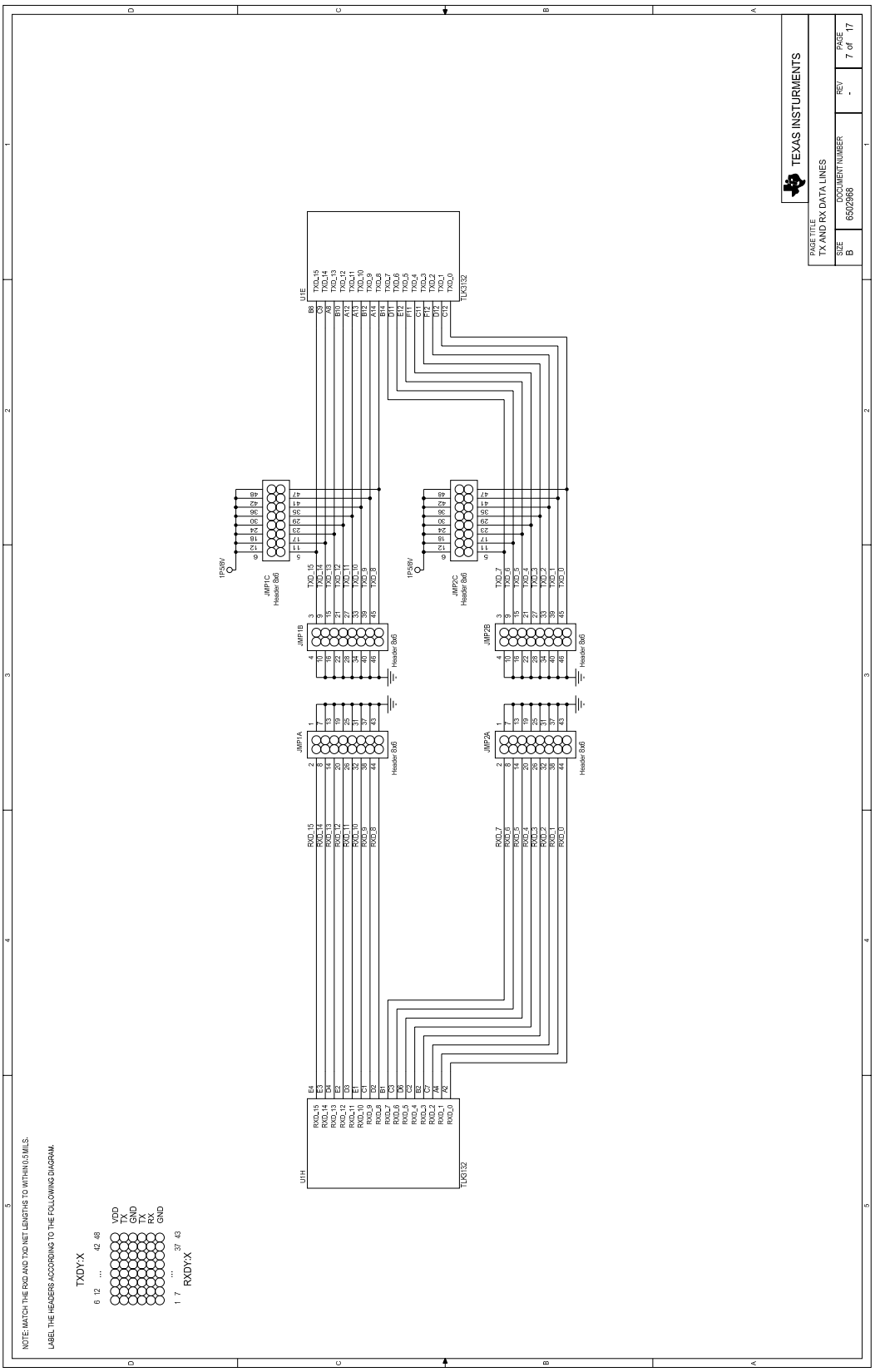


Figure 27. TLK3132 EVM Schematic, Sheet 8 TX/RX Clocks and Control

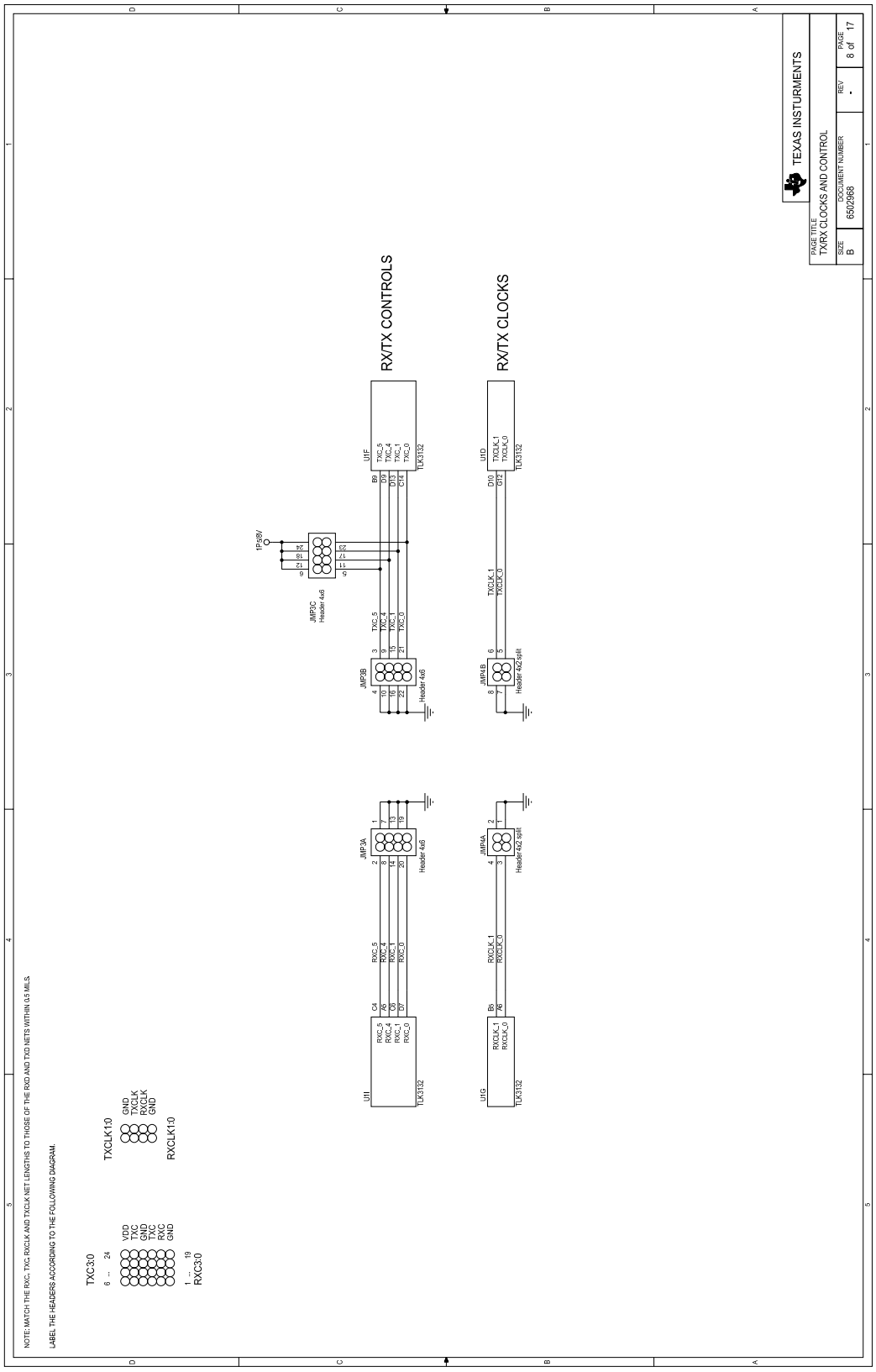


Figure 28. TLK3132 EVM Schematic, Sheet 9 Power Regulation

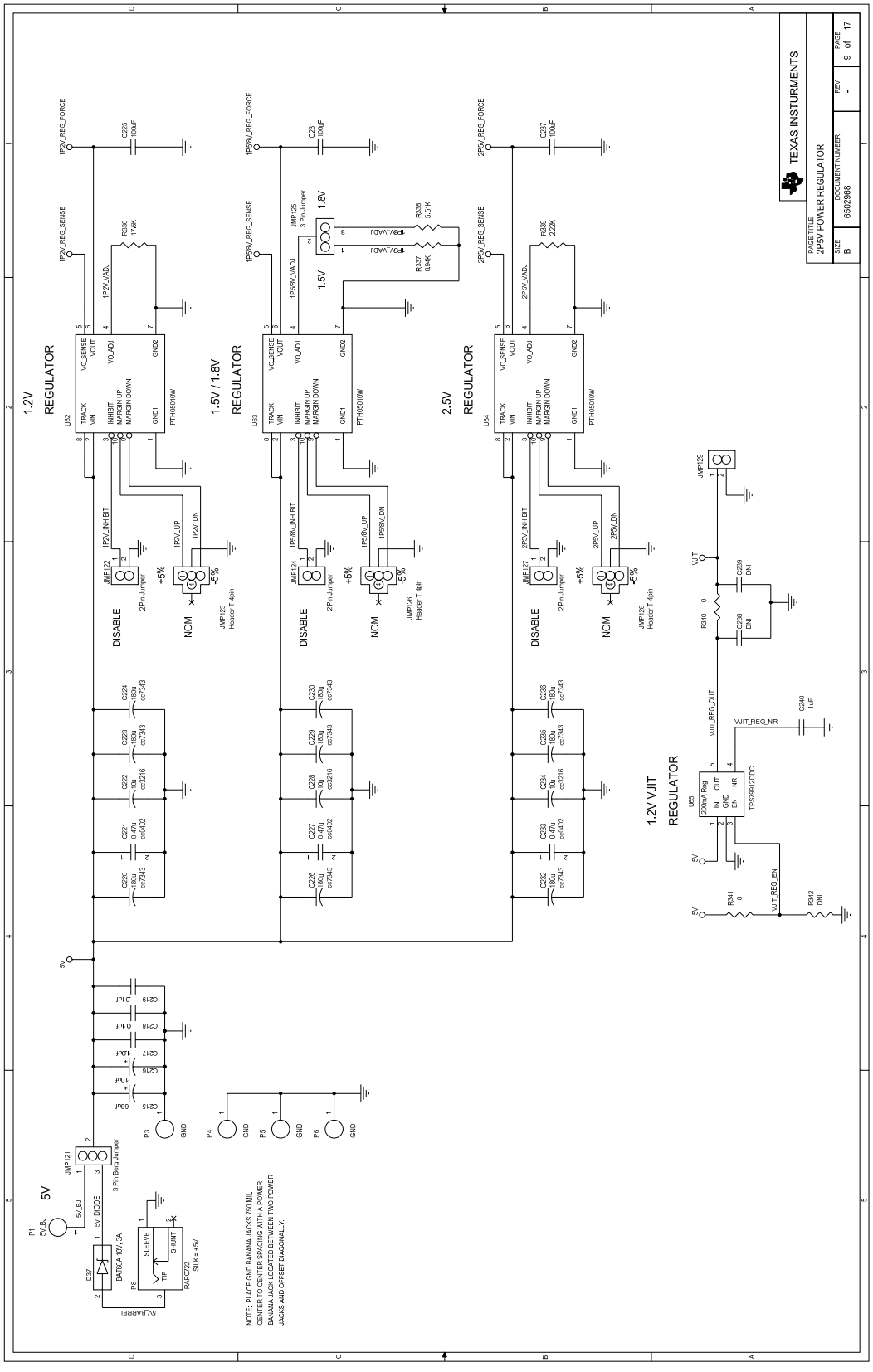


Figure 29. TLK3132 EVM Schematic, Sheet 10 Power Distribution

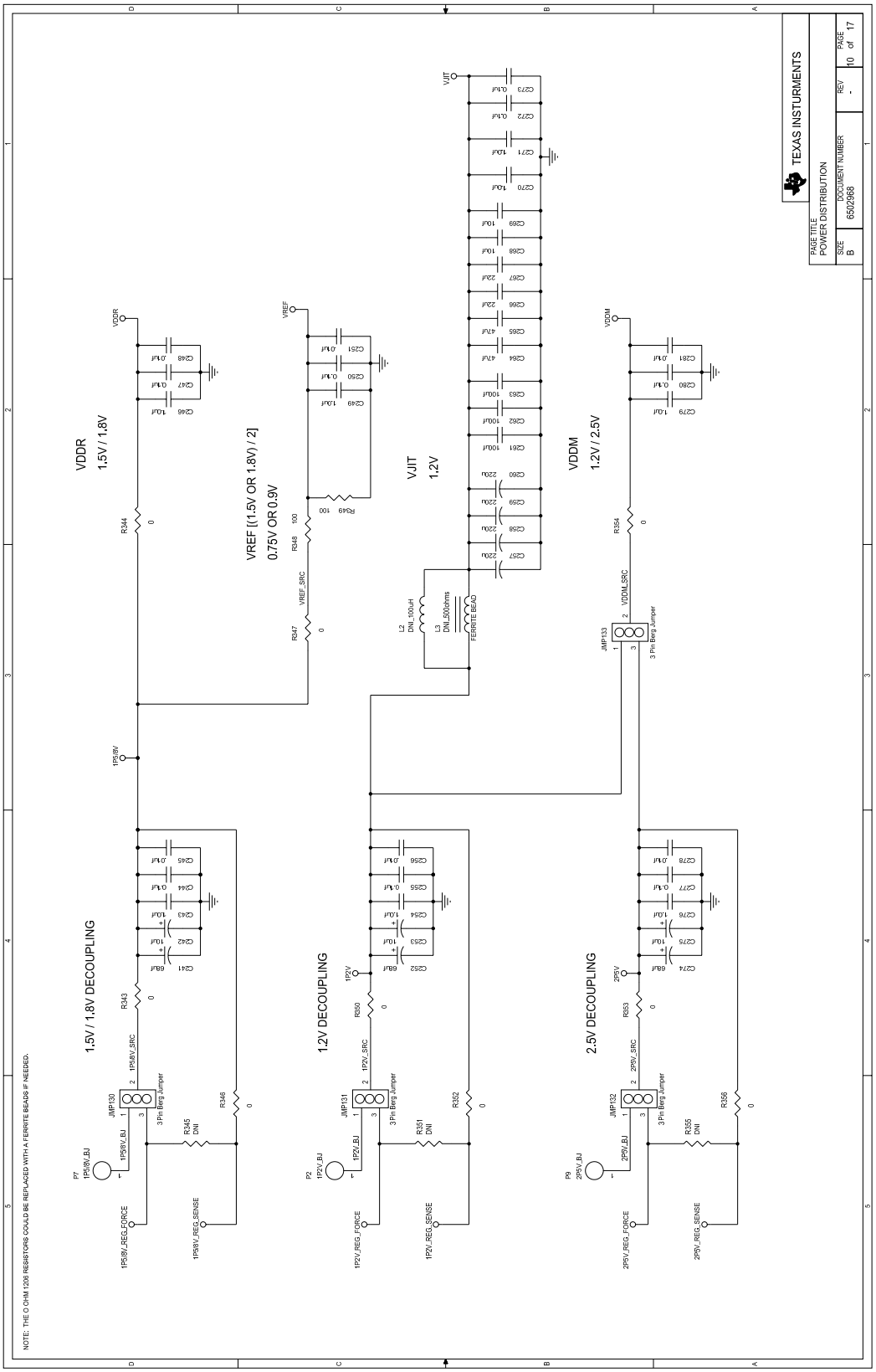


Figure 30. TLK3132 EVM Schematic, Sheet 11 1P2V and VJIT Supply LEDs

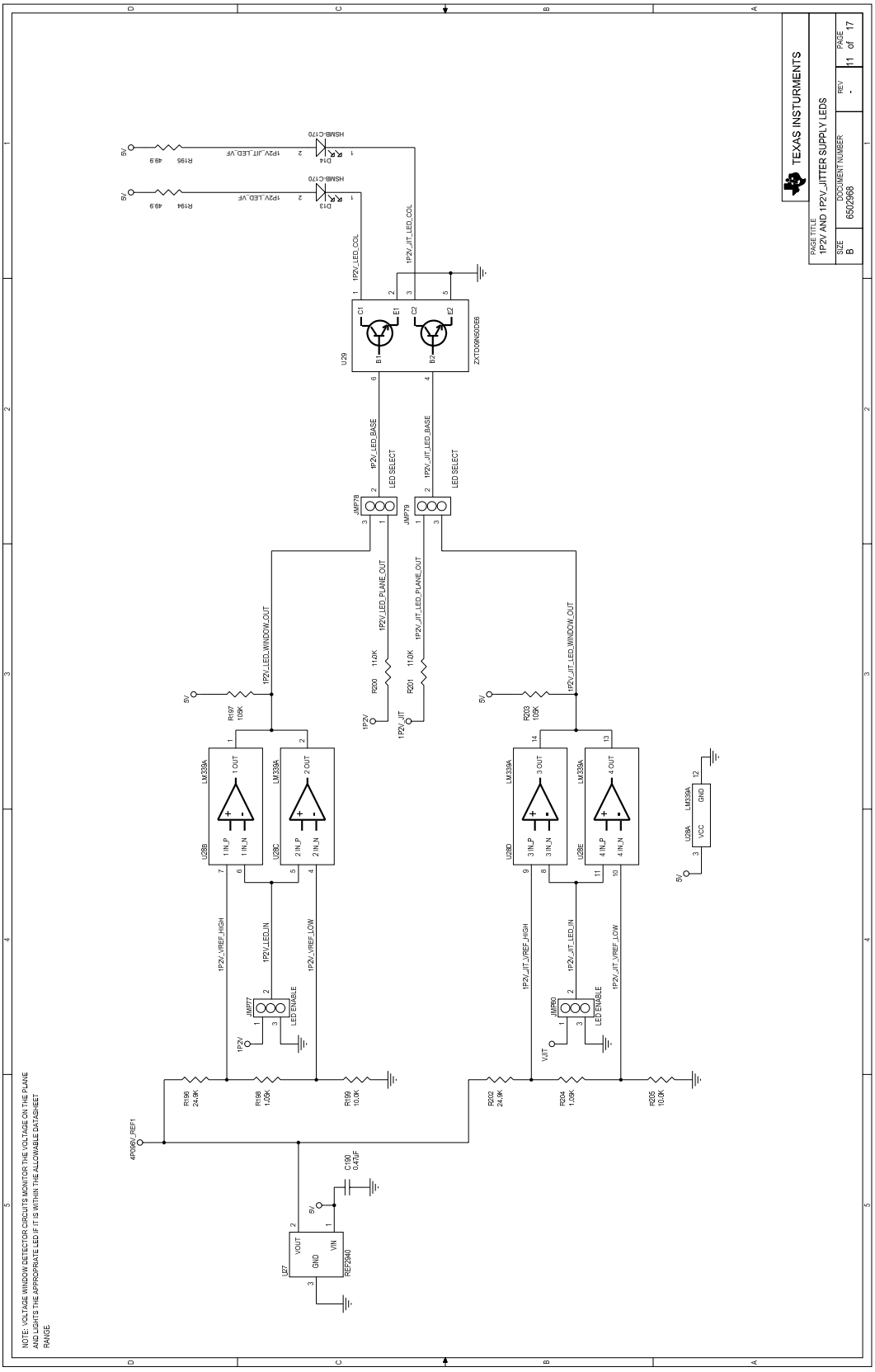


Figure 31. TLK3132 EVM Schematic, Sheet 12 1P5V and 1P8V Supply LEDs

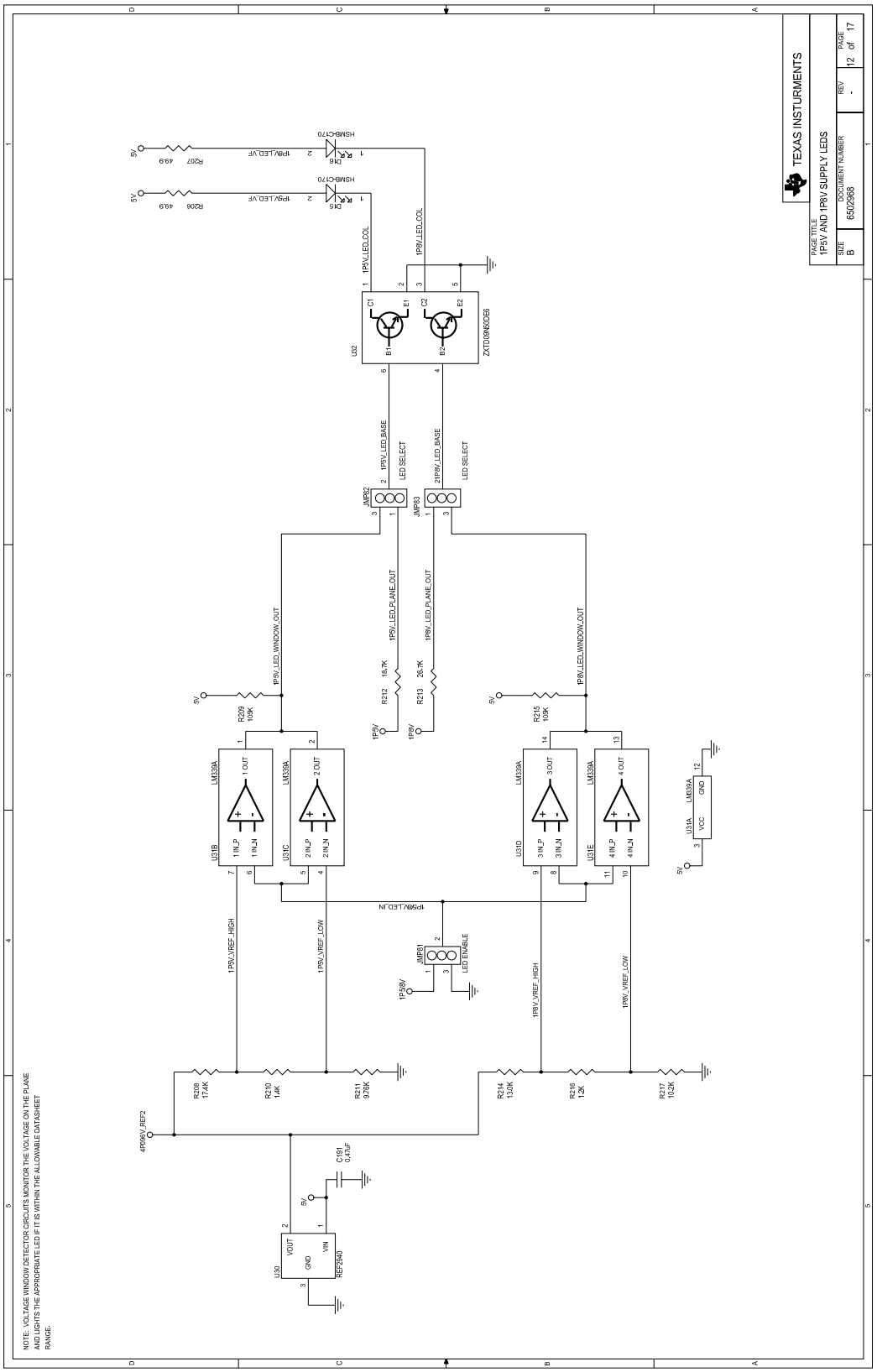


Figure 32. TLK3132 EVM Schematic, Sheet 13 2P5V and 5V Supply LEDs

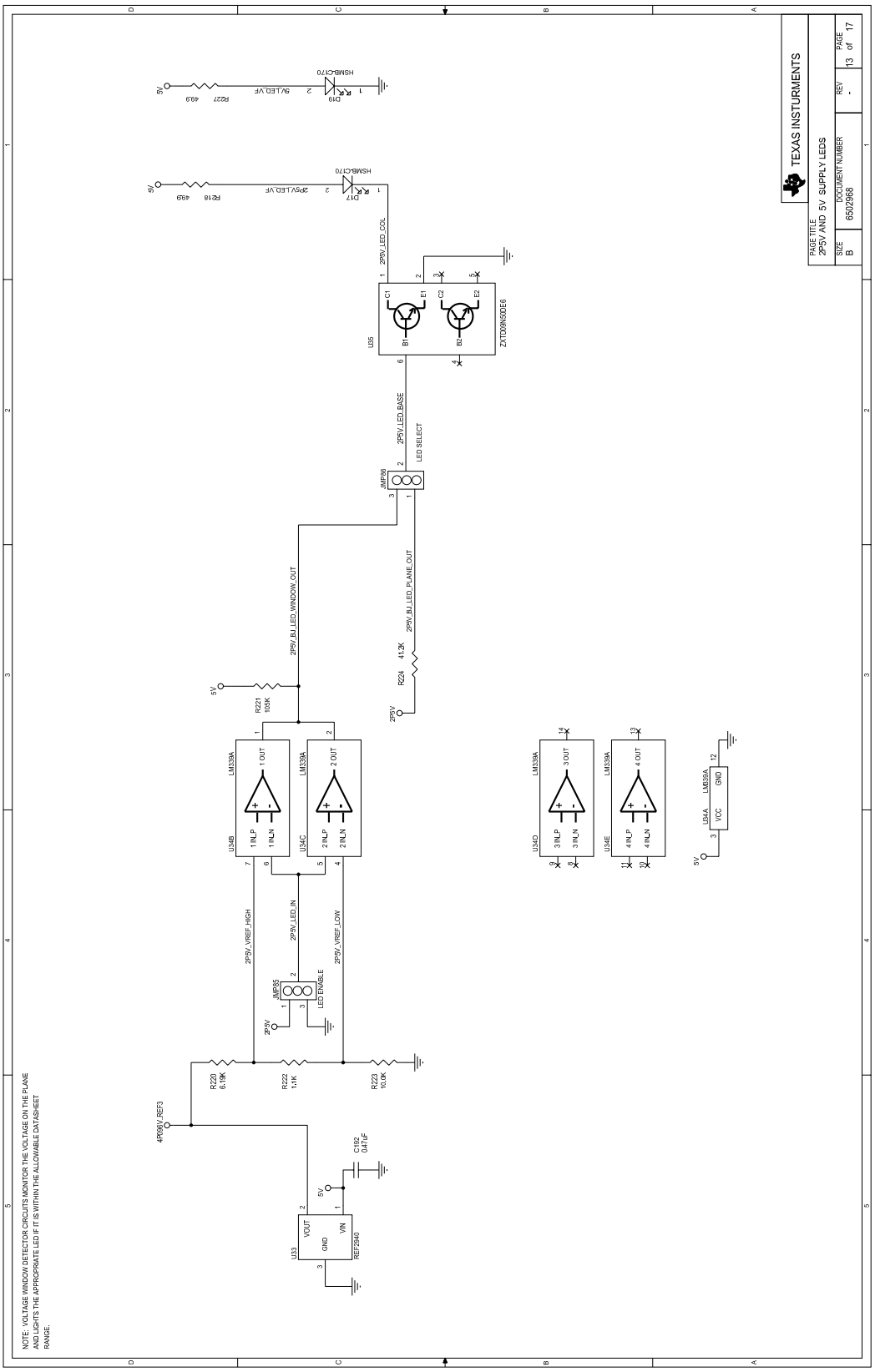


Figure 33. TLK3132 EVM Schematic, Sheet 14 VDDM Supply LEDs

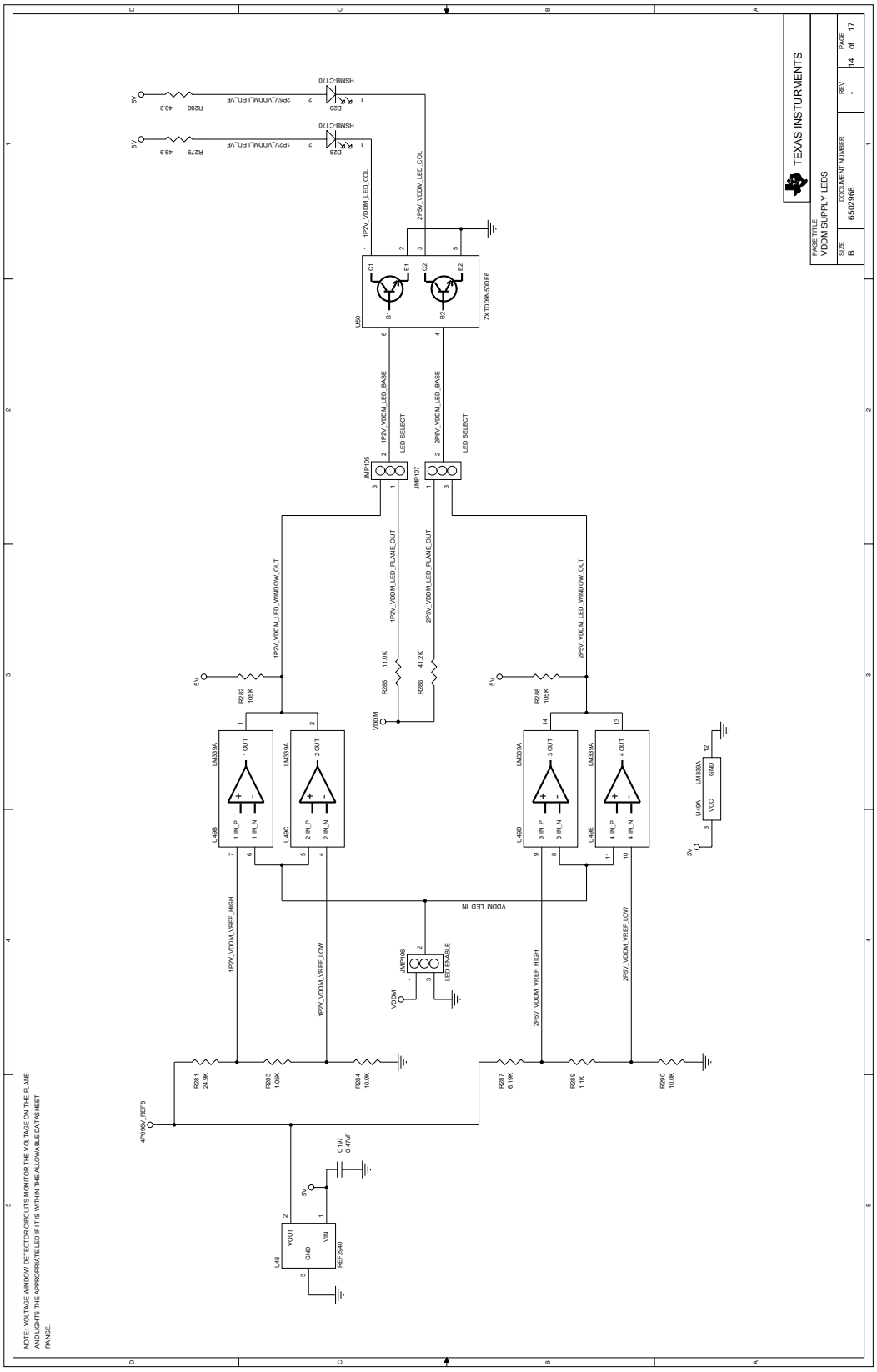


Figure 34. TLK3132 EVM Schematic, Sheet 15 VDDR Supply LEDs

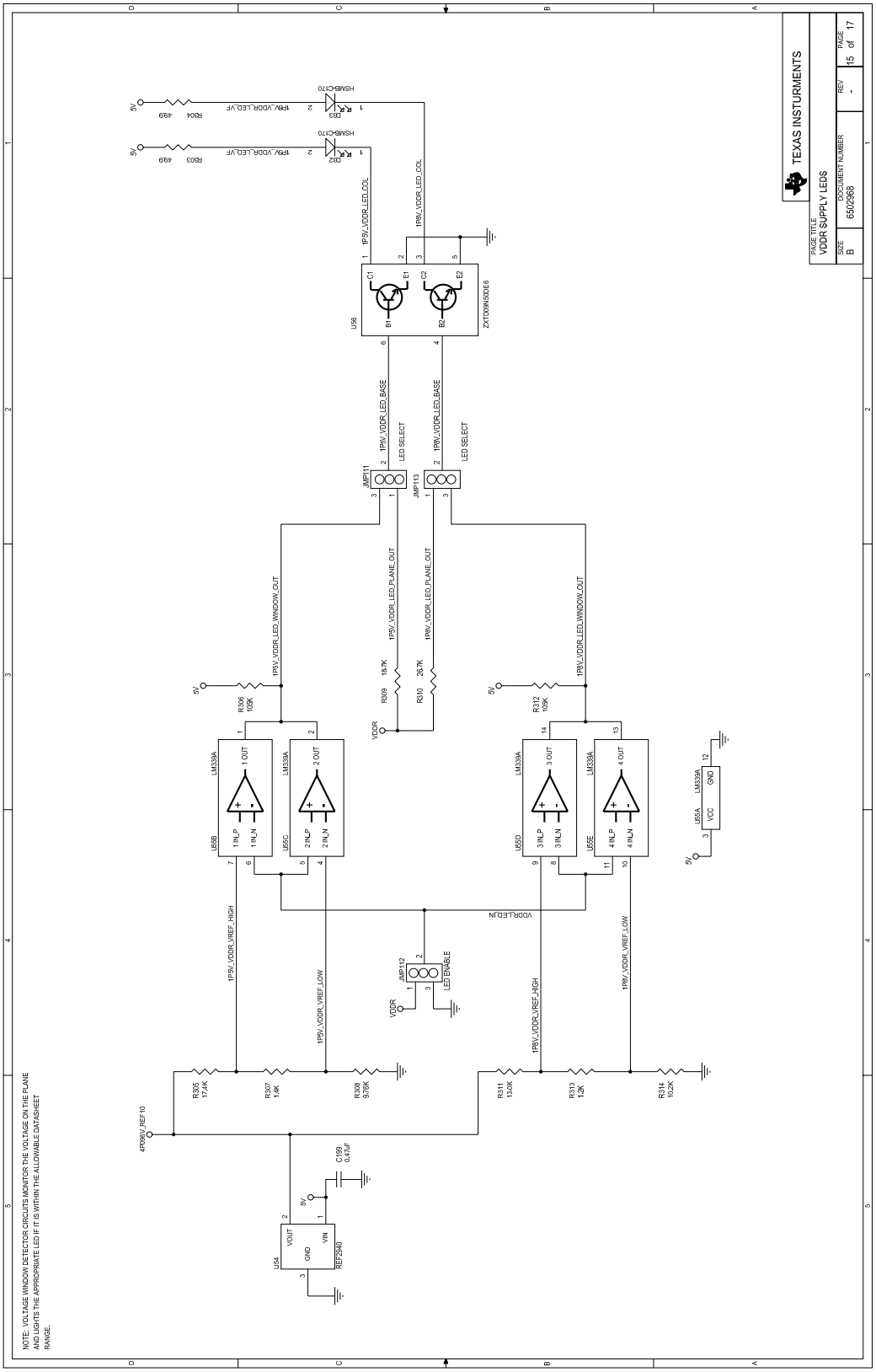


Figure 35. TLK3132 EVM Schematic, Sheet 16 VREF Supply LEDs

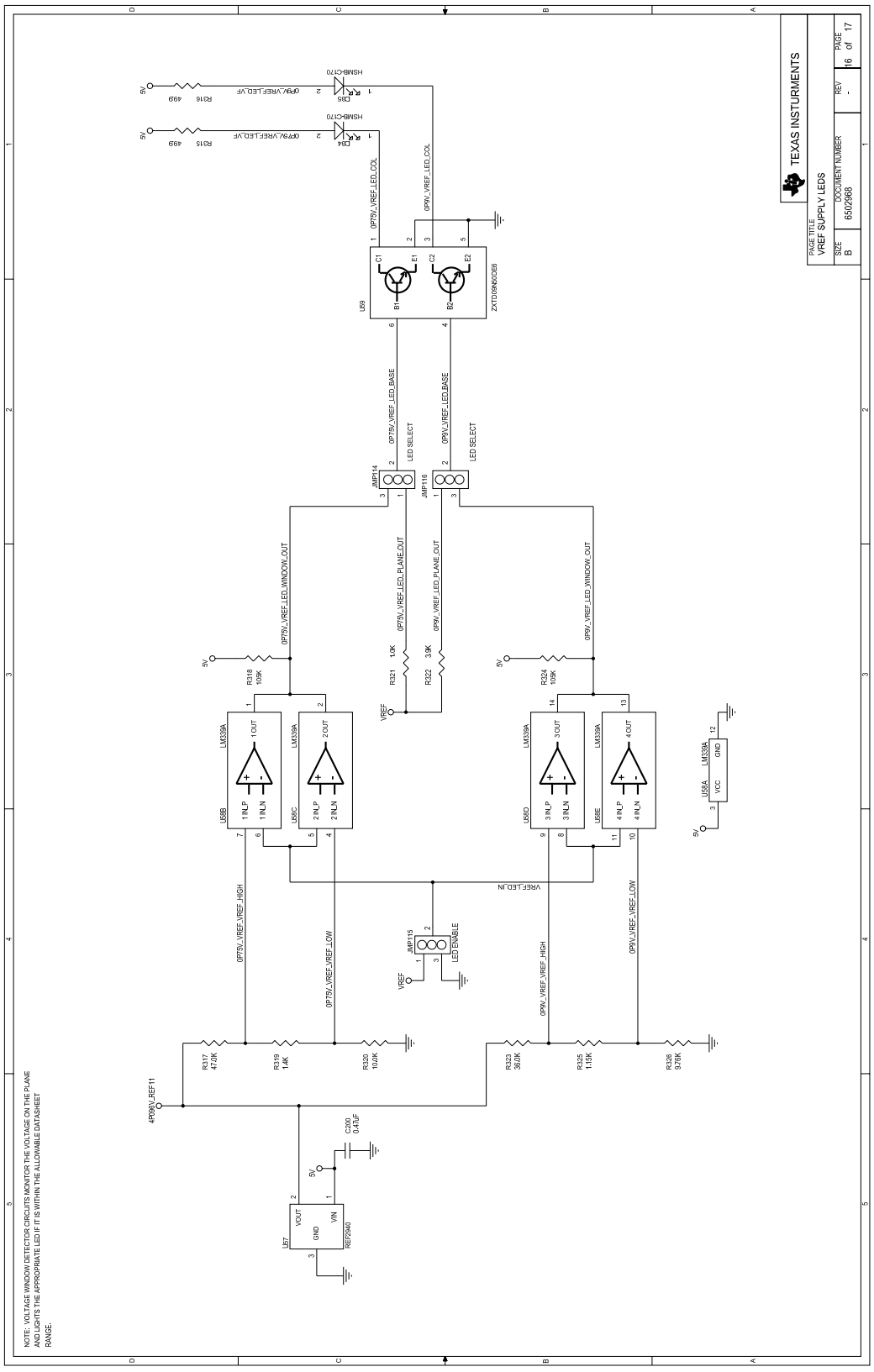


Figure 36. TLK3132 EVM Schematic, Sheet 17 Peripheral Ports

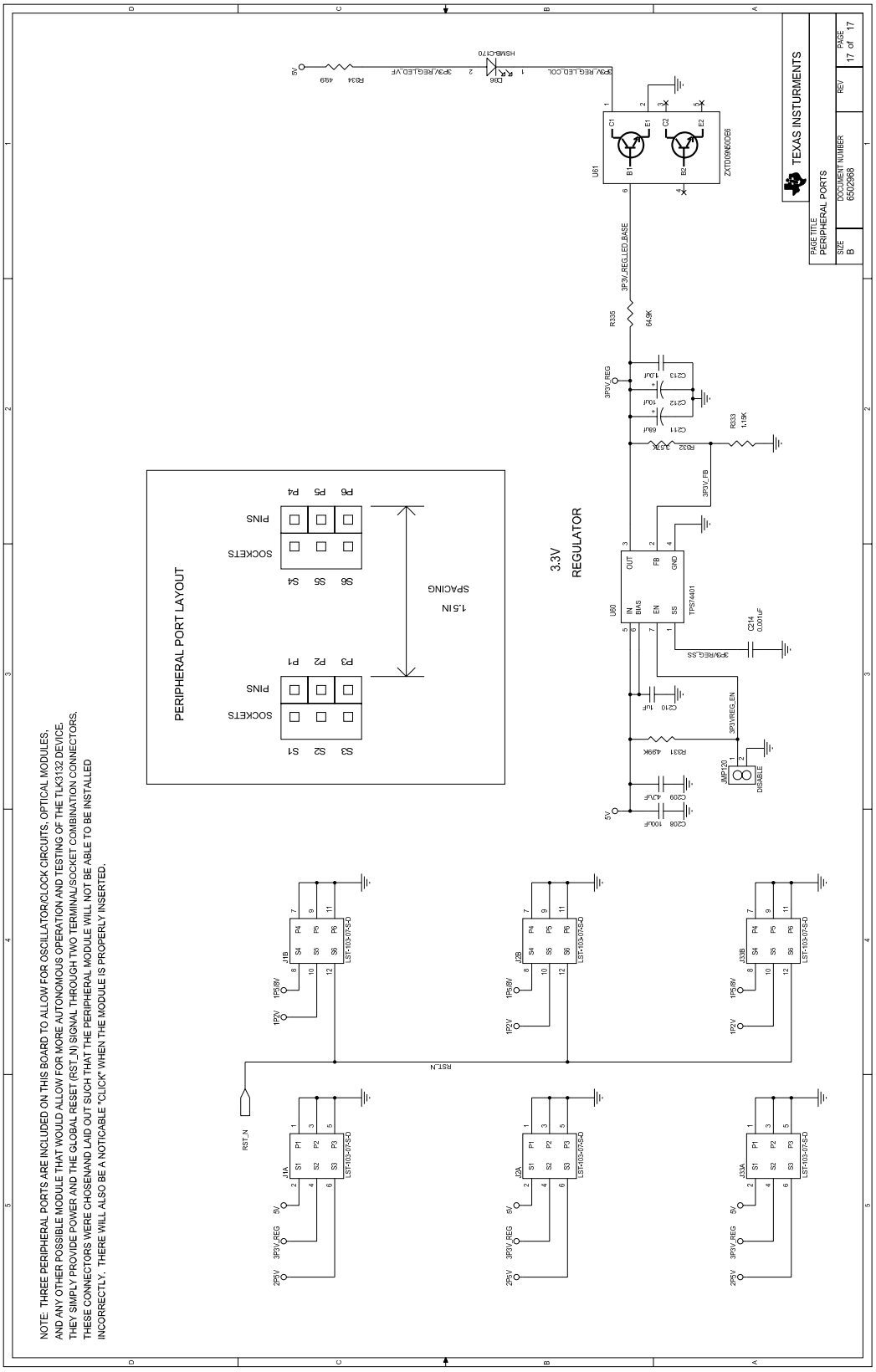


Table 1. TLK3132 EVM Bill of Materials

Item	Qty	Reference	Value	Part	Part_Number	Manufacturer
1	29	C7, C8, C9, C10, C11, C20, C21, C22,C27, C28, C34, C35, C36, C40, C41, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C201, C202, C203, C204	0.01µF	0402 CAP	C0402X7R500-103KNE	Venkel
2	8	C5, C6, C19, C26, C39, C221, C227, C233	0.47µF	0402 CAP	GRM155R61A474KE15D	Murata Electronics
3	4	C3, C4, C18, C32	1.0µF	0402 CAP	GRM155R61A105KE15D	Murata Electronics
4	6	C13, C14, C23, C29, C37, C42	100pF	0402 CAP	C0402COG500-101JNE	Venkel
5	5	C15, C16, C24, C30, C38	10pF	0402 CAP	C0402COG500-100JNE	Venkel
6	1	C57	1500pF	0402 CAP	C0402X7R500-152KNE	Venkel
7	1	C58	1800pF	0402 CAP	04025C182KAT2A	Avx Corporation
8	4	C1, C2, C17, C31	2.2µF	0402 CAP	GRM155R60J225ME15D	Murata Electronics
9	1	C43	0.1uF	0603 CAP	C0603X7R500-104KNE	Venkel
10	7	C33, C190, C191, C192, C197, C199,C200	0.47µF	0603 CAP	C0603X7R160-474KNE	Venkel
11	3	C25, C210, C240	1.0µF	0603 CAP	C1608X7R1C105K	Tdk Corporation
12	1	C12	10000pF	0603 CAP	C0603C103J5RACTU	Kemet
13	1	C214	1000pF	0603 CAP	C0603COG500-102JNE	Venkel
14	1	C205	1500pF	0603 CAP	C0603X7R101-152KNE	Venkel
15	1	C206	1800pF	0603 CAP	ECJ-1VB1H182K	Panasonic
16	2	C59, C207	1.0µF	0603 CAP	C1608X7R1C105K	Tdk Corporation
17	2	C59, C207	2.2µF	0603 CAP	GRM188R71A225KE15D	Murata Electronics
18	1	C209	4.7µF	0603 CAP	C0603X5R6R3-475KNE	Venkel
19	7	C219, C245, C248, C251, C256, C278, C281	0.01µF	0805 CAP	GRM21BR72A103KA01L	Murata Electronics
20	9	C218, C244, C247, C250, C255, C272, C273, C277, C280	0.1uF	1206 CAP	GRM319R71H104KA01D	Murata Electronics
21	10	C213, C217, C243, C246, C249, C254, C270, C271, C276, C279	1.0µF	1206 CAP	C1206X7R500-105KNE	Murata Electronics
22	3	C261, C262, C263	100µF	1206 CAP	C1206X5R6R3-107MNE	Venkel
23	2	C268, C269	10µF	1206 CAP	C1206X7R160-106KNE	Venkel
24	2	C266, C267	22uF	1206 CAP	C1206X5R6R3-226KNE	Venkel
25	2	C264, C265	47µF	1206 CAP	C1206X5R6R3-476MNE	Venkel
26	4	C208, C225, C231, C237	100µF	1812 CAP	GRM43SR60J107ME20L	Murata Electronics
27	3	C222, C228, C234	10µF	3216-18 (EIA) CAP	B45196H3106K109	Epcos Inc
28	5	C212, C216, C242, C253, C275	10µF	7343-31 (EIA) CAP	TA025TCM106KDR	Venkel
29	13	C220, C223, C224, C226, C229, C230, C232, C235, C236, C257, C258, C259, C260	220µF	7343-31 (EIA) CAP	B45197A3227K509	Kemet
30	5	C211, C215, C241, C252, C274	68µF - LESR	7361-38 (EIA)CAP	TA020TCR686KER	Venkel
31	3	R26, R27, R341	0.0 (Zero Ohm)	0402 RES	ERJ-2GE0R00X	Panasonic - Ecg
32	1	R44	1.21K	0402 RES	RR0510P-1211-D	Susumu Co
33	1	R45	100	0402 RES	RG1005P-101-B-T5	Susumu Co
34	2	R32, R33	150	0402 RES	RG1005P-151-D-T10	Susumu Co
35	5	R34, R35, R36, R37, R43	40.2K	0402 RES	RG1005P-4022-B-T5	Susumu Co
36	2	R18, R19	45.3K	0402 RES	ERJ-2RKF4532X	Panasonic - Ecg
37	2	R31, R52	49.9	0402 RES	RR0510R-49R9-D	Susumu Co
38	6	R48, R49, R340, R346, R352, R356	0.0 (Zero Ohm)	0603 RES	ERJ-3GEY0R00V	Panasonic - Ecg
39	1	R321	1.00K	0603 RES	RR0816P-102-B-T5	Susumu Co
40	3	R198, R204, R283	1.05K	0603 RES	RR0816P-1051-B-T5-03H	Susumu Co
41	2	R222, R289	1.10K	0603 RES	RG1608P-112-B-T5	Susumu Co
42	2	R325, R333	1.15K	0603 RES	RG1608P-1151-B-T5	Susumu Co
43	2	R216, R313	1.20K	0603 RES	RG1608P-122-B-T5	Susumu Co
44	1	R330	1.21K	0603 RES	RG1608P-1211-B-T5	Susumu Co
45	3	R210, R307, R319	1.40K	0603 RES	RG1608P-1401-B-T5	Susumu Co

46	1	R46	1.50K	0603 RES	RG1608P-152-B-T5	Susumu Co
47	6	R199, R205, R223, R284, R290, R320	10.0K	0603 RES	ERA-3AEB103V	Panasonic - Ecg
48	2	R217, R314	10.2K	0603 RES	RG1608P-1022-B-T5	Susumu Co.
49	1	R329	100	0603 RES	RG1608P-101-B-T5	Susumu Co.
50	1	R4	100K	0603 RES	TNPW06031003BT9	Vishay/Dale
51	11	R197, R203, R209, R215, R221, R282, R288, R306, R312, R318, R324	105K	0603 RES	RR0816P-1053-B-T5-03D	Susumu Co.
52	3	R200, R201, R285	11K	0603 RES	RG1608P-113-B-T5	Susumu Co.
53	2	R214, R311	13.0K	0603 RES	RG1608P-133-B-T5	Susumu Co.
54	2	R2, R5	130	0603 RES	RG1608P-131-B-T5	Susumu Co.
55	3	R208, R305, R336	17.4K	0603 RES	RR0816P-1742-B-T5-24C	Susumu Co.
56	2	R212, R309	18.7K	0603 RES	RG1608P-1872-B-T5	Susumu Co.
57	1	R339	2.21K	0603 RES	CR0603-16W-2211FT	Venkel
58	3	R196, R202, R281	24.9K	0603 RES	RG1608P-2492-B-T5	Susumu Co.
59	2	R213, R310	26.7K	0603 RES	RR0816P-2672-B-T5-42C	Susumu Co.
60	1	R332	3.57K	0603 RES	RG1608P-3571-B-T5	Susumu Co.
61	1	R322	3.90K	0603 RES	RG1608P-392-B-T5	Susumu Co.
62	1	R323	36.0K	0603 RES	RR0816P-363-B-T5	Susumu Co.
63	20	R1, R7, R8, R9, R10, R11, R12, R13, R14, R38, R39, R40, R41, R42, R53, R54, R55, R56, R57, R331	4.99K	0603 RES	RG1608P-4991-B-T5	Susumu Co.
64	2	R224, R286	41.2K	0603 RES	RG1608P-4122-B-T5	Susumu Co.
65	1	R317	47.0K	0603 RES	RG1608P-473-B-T5	Susumu Co.
66	19	R3, R6, R17, R20, R21, R30, R194, R195, R206, R207, R218, R227, R279, R280, R303, R304, R315, R316, R334	49.9	0603 RES	ERJ-3EKF49R9V	Panasonic - Ecg
67	1	R338	5.49K	0603 RES	CR0603-10W-5491FT	Venkel
68	2	R220, R287	6.19K	0603 RES	RR0816P-6191-B-T5-77H	Susumu Co.
69	1	R335	64.9K	0603 RES	ERJ-3EKF6492V	Panasonic - Ecg
70	1	R337	8.87K	0603 RES	CR0603-10W-8871FT	Venkel
71	3	R211, R308, R326	9.76K	0603 RES	RR0816P-9761-B-T5-96H	Susumu Co.
72	2	R348, R349	100	0805 RES	RG2012P-101-B-T5	Susumu Co.
73	6	R343, R344, R347, R350, R353, R354	0.0 (Zero Ohm)	1210 RES	RK73Z2ETTE	Koa Speer
74	1	D37	Zener Diode	SOD-323	BAT 60A E6327	Infineon Technologies
75	11	U3, U4, U5, U6, U29, U32, U35, U50, U56, U59, U61	ZXTD09N50DE6TA	SOT-23-6	ZXTD09N50DE6TA	Zetex Inc
76	6	U28, U31, U34, U49, U55, U58	LM339AD	14-SOIC	LM339AD	Texas Instruments
77	1	U1	TLK3132	196-BGA	TLK3132	Texas Instruments
78	1	U65	TPS79912DDCR	5-TSOT	TPS79912DDCR	Texas Instruments
79	1	U60	TPS74401KTWT	7-DD	TPS74401KTWT	Texas Instruments
80	6	U27, U30, U33, U48, U54, U57	REF2940AIDBZT	SOT-23	REF2940AIDBZT	Texas Instruments
81	1	U2	TPS3125J18DBVR	SOT-23-5	TPS3125J18DBVR	Texas Instruments
82	3	U62, U63, U64	PTH05010WAS	SMT PCB	PTH05010WAS	Texas Instruments
83	18	D3, D4, D5, D6, D7, D13, D14, D15, D16, D17, D19, D28, D29, D32, D33, D34, D35, D36	LED - Blue Diffused	0805 LED	HSMB-C170	Avago Technologies Us Inc
84	1	D2	LED - Green Diffused	0805 LED	HSMG-C170	Avago Technologies Us Inc
85	1	D1	LED - SUPER RED CLEAR	0805 LED	LTST-C170KRKT	Lite-On Inc
86	1	SW1	EVQ-PBE05R	6mm	EVQ-PBE05R	Panasonic - Ecg
87	6	J1, J2, J33	LST-103-07-S-D	0.1x0.1"	LST-103-07-S-D	Samtec
88	1	JMP29	20 Pin - Shrouded	0.1" SP	5103308-5	Tyco Electronics/Amp
89	75		Shunt	0.1" SP	382811-6	Amp/Tyco
90	1	JMP4	2 X 4	0.1x0.1"	HTSW-150-08-G-D	Samtec
91	3	JMP22, JMP31, JMP32	2 X 5	0.1x0.1"	HTSW-150-08-G-D	Samtec

92	1	JMP17	2 X 10	0.1x0.1"	HTSW-150-08-G-D	Samtec
93	8	JMP1, JMP2	2 X 6	0.1x0.1"	HTSW-150-08-G-D	Samtec
94	2	JMP3	2 X 6	0.1x0.1"	HTSW-150-08-G-D	Samtec
95	17	JMP5, JMP6, JMP7, JMP9, JMP11, JMP13, JMP23, JMP129, JMP15, JMP28, JMP30, JMP16, JMP21, JMP120, JMP122, JMP124, JMP127	1 X 2	0.1x0.1"	HTSW-150-08-G-S	Samtec
96	26	JMP14, JMP27, JMP121, JMP130, JMP131, JMP132, JMP133, JMP77, JMP80, JMP81, JMP85, JMP106, JMP112, JMP115, JMP78, JMP79, JMP82, JMP83, JMP86, JMP105, JMP107, JMP111, JMP113, JMP114, JMP116, JMP125	1 X 3	0.1x0.1"	HTSW-150-08-G-S	Samtec
97	3	JMP123, JMP126, JMP128	1 X 4	0.1x0.1"	HTSW-150-08-G-S	Samtec
98	1	P8	Power Jack	2.1mm	PJ-002AH	Cui Inc
99	8	P1, P2, P3, P4, P5, P6, P7, P9	Banana Plug - Metal	4mm	108-0740-001	Emerson Network Power Co
100	12	J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J16	19S101-40ML5	SMP	19S101-40ML5	Rosenberger
101	7	Screws	4-40/0.25"		PMSSS 440 0025 PH	Building Fasteners
102	7	Standoff	Round Threaded		2029	Keystone Electronics
103	4	C60, C61, C238, C239	DNI	0603 CAP		
104	1	L1	DNI	0603 IND		
105	1	L2	DNI	1210 IND		
106	1	L3	DNI	1210 IND		
107	7	R15, R16, R24, R25, R47, R50, R51	DNI	0603 RES		
108	5	R22, R23, R28, R29, R342	DNI	0402 RES		
109	2	R327, R328	DNI	0201 RES		
110	3	R345, R351, R355	DNI	0603 RES		

Board Layouts

Figure 37. TLK3132 EVM Layout, Top Signal (Layer 1)

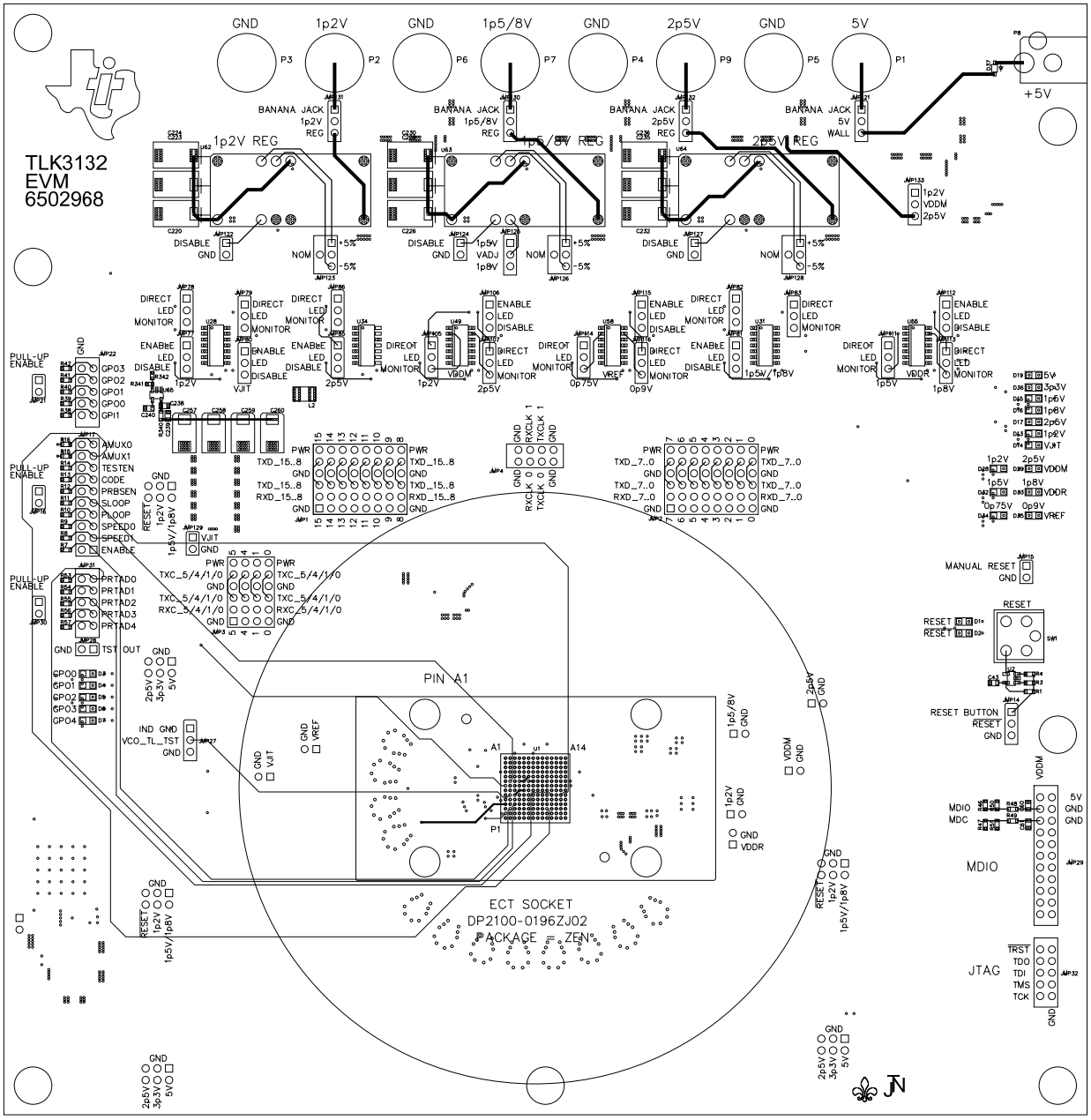


Figure 38. TLK3132 EVM Layout, Internal Ground (Layers 2,4,6,8,10)

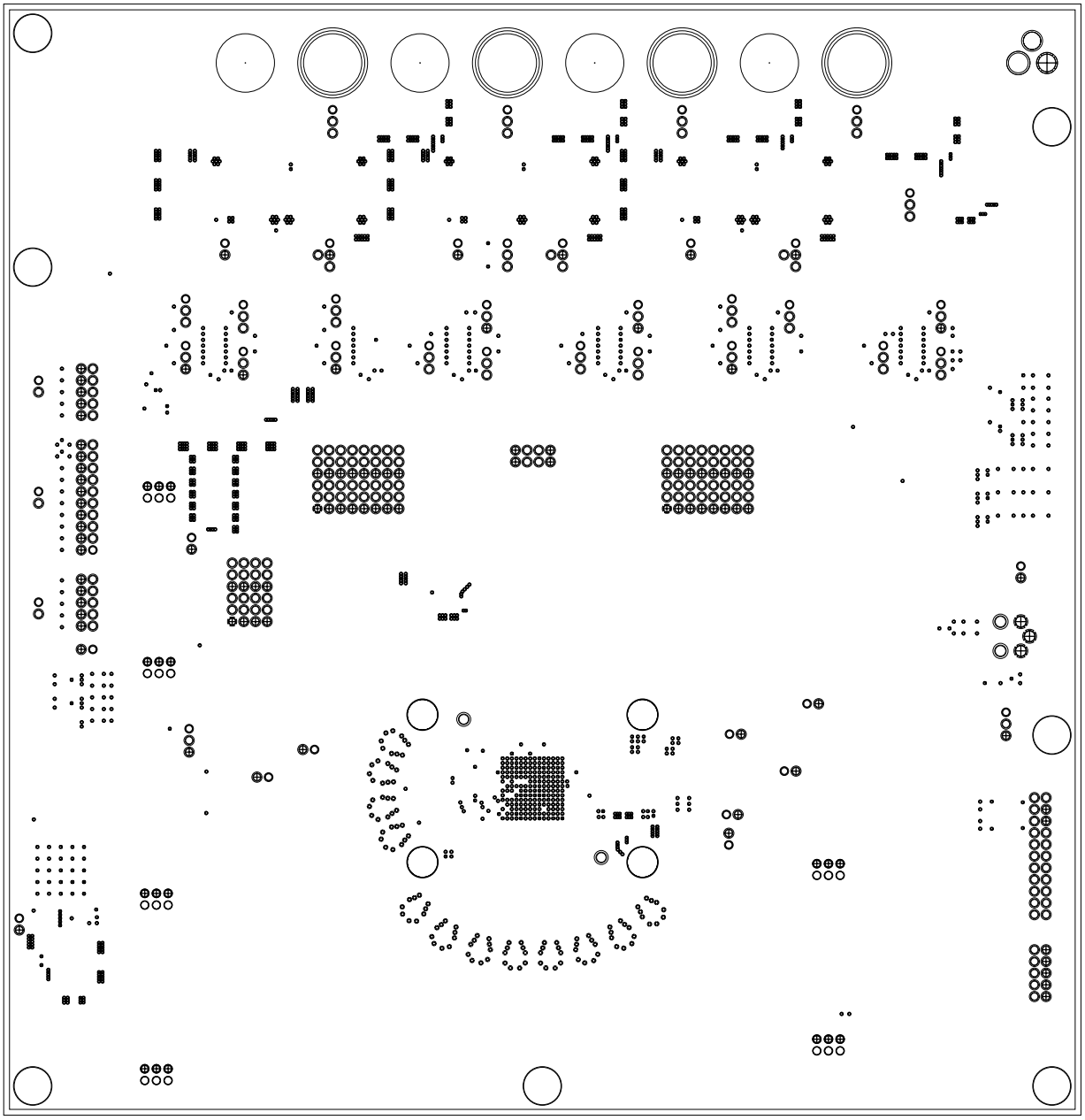


Figure 39. TLK3132 EVM Layout, Internal Power (Layer 3)

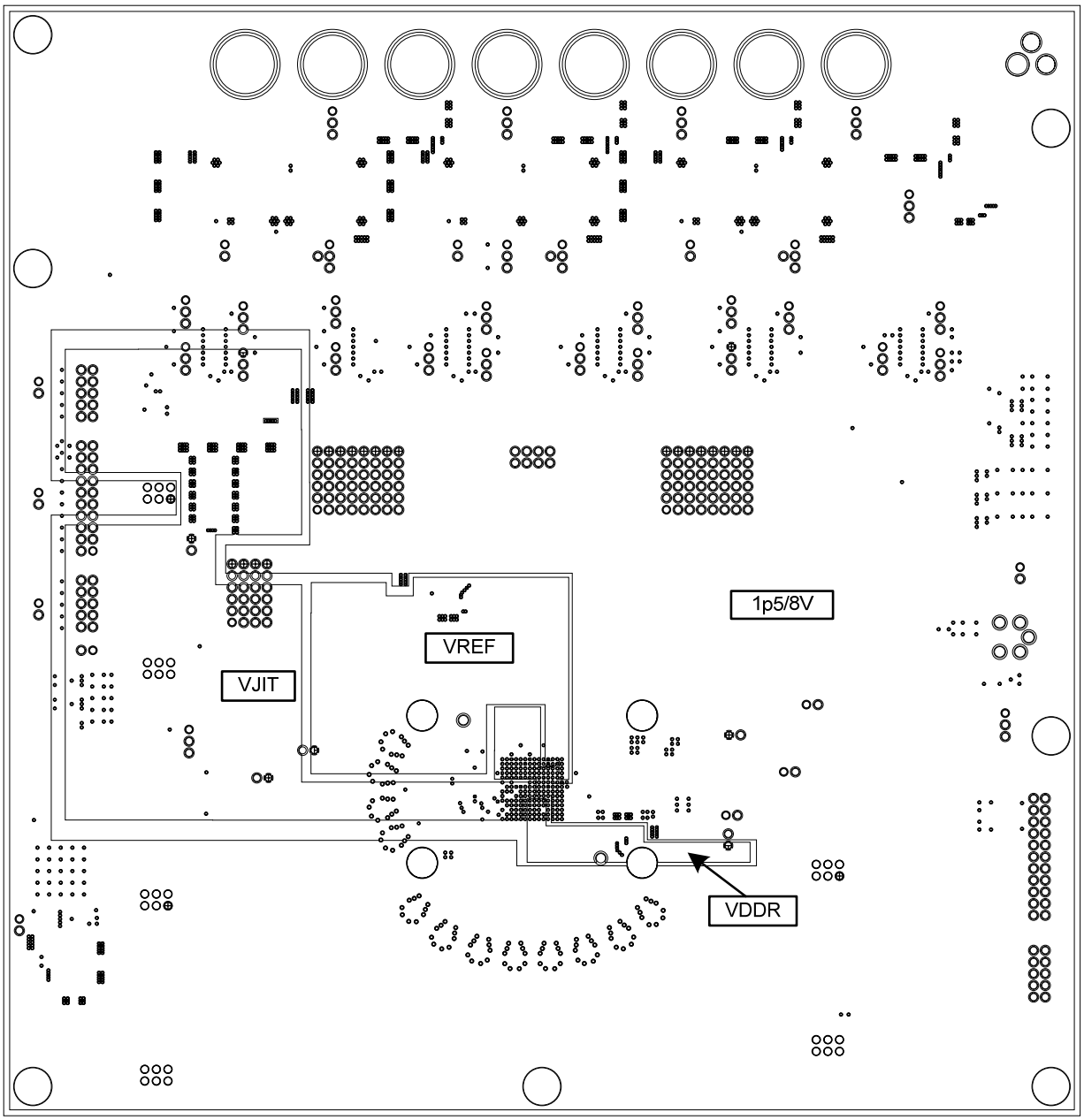


Figure 40. TLK3132 EVM Layout, Internal Signal (Layer 5)

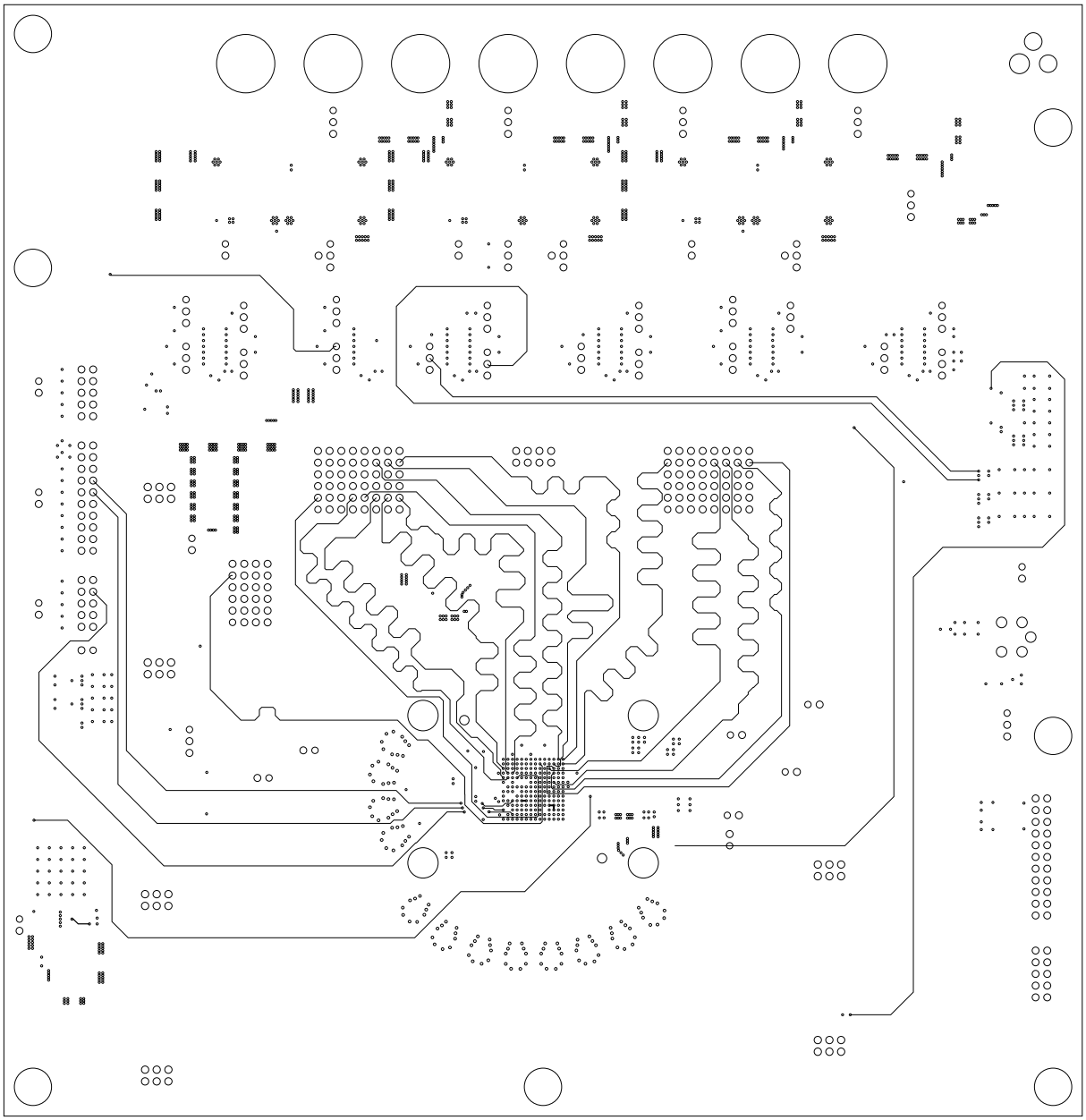


Figure 41. TLK3132 EVM Layout, Internal Signal (Layer 7)

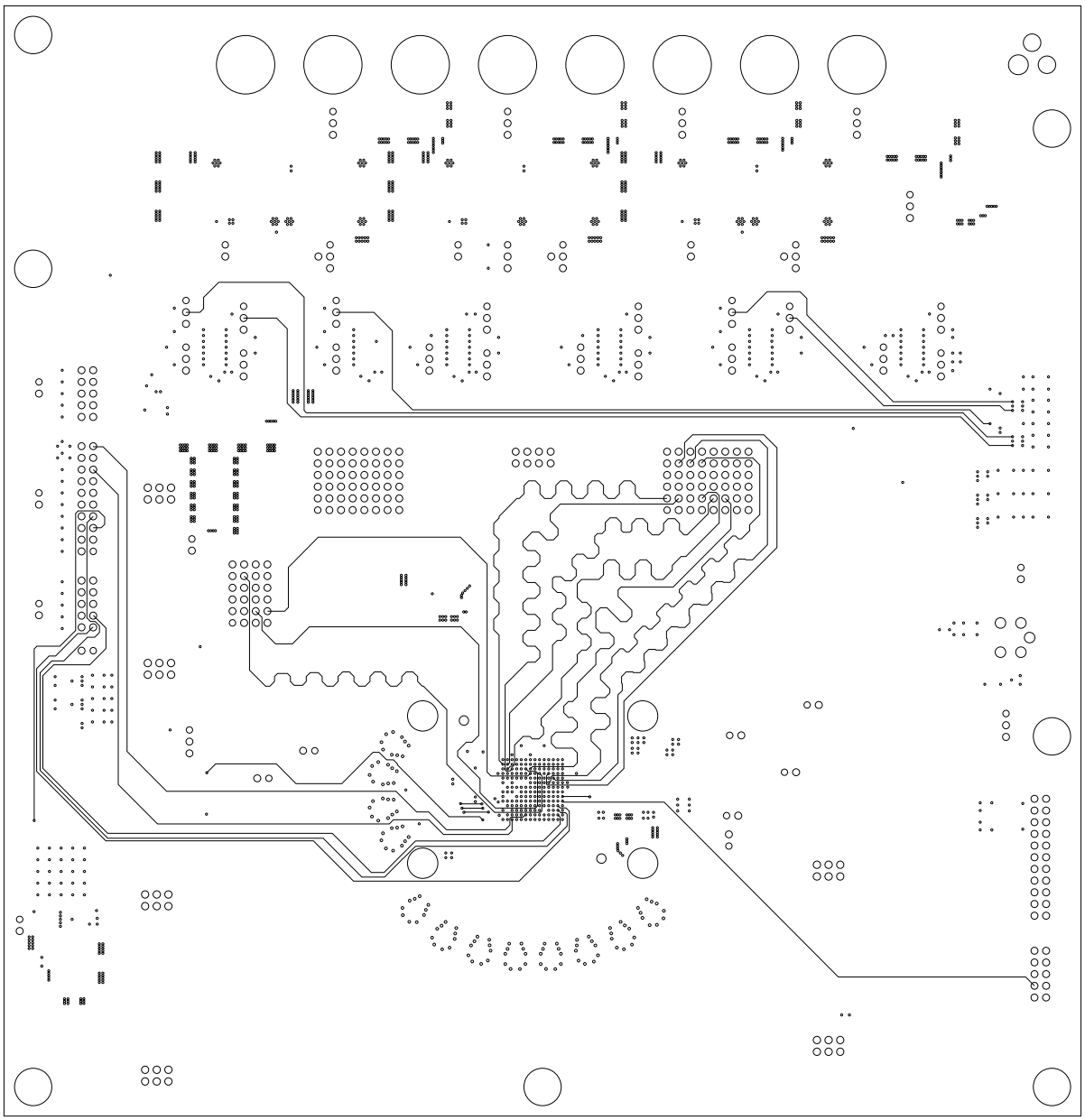


Figure 42. TLK3132 EVM Layout, Internal Power (Layer 9)

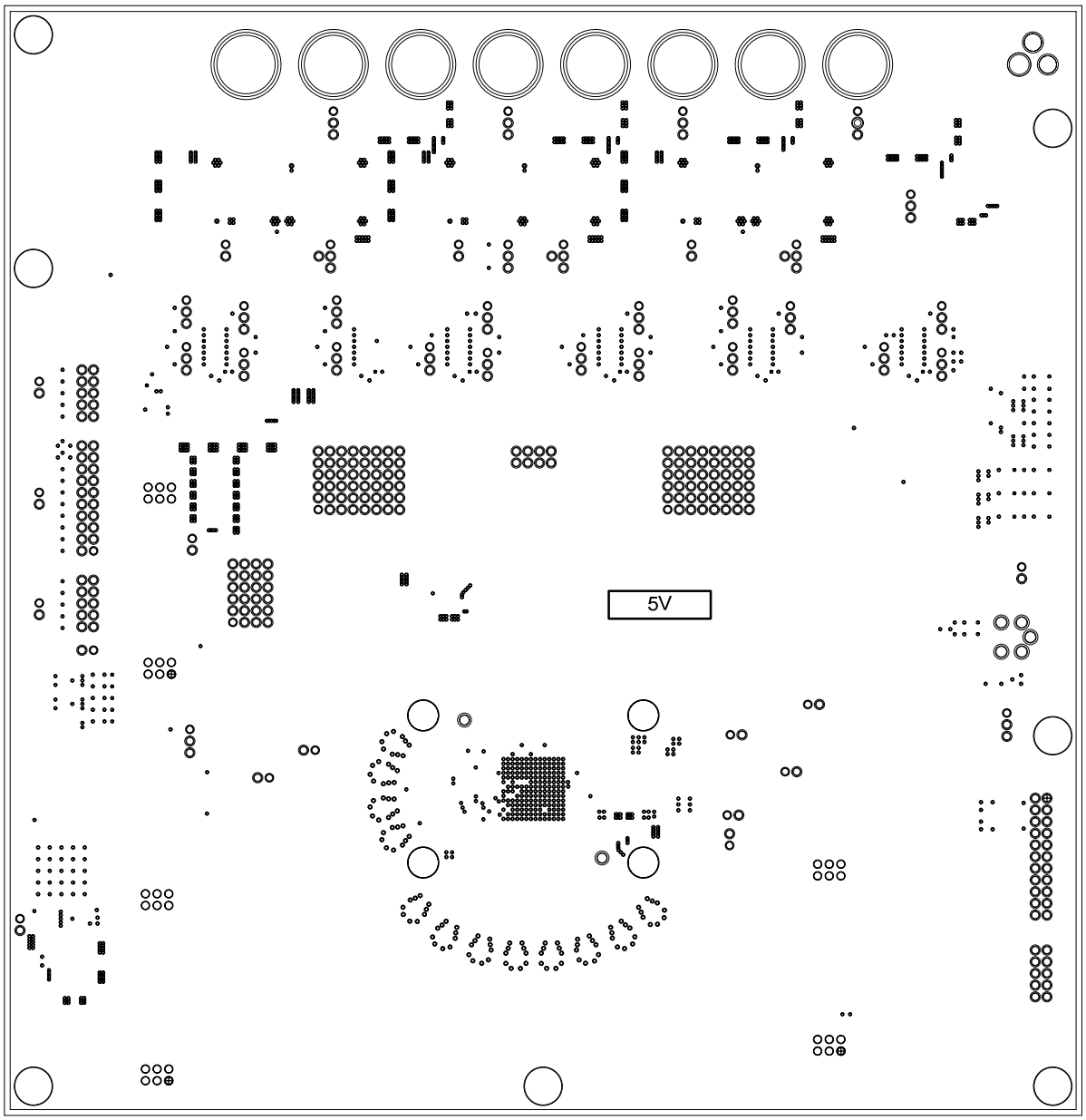


Figure 43. TLK3132 EVM Layout, Internal Ground and Power (Layer 11)

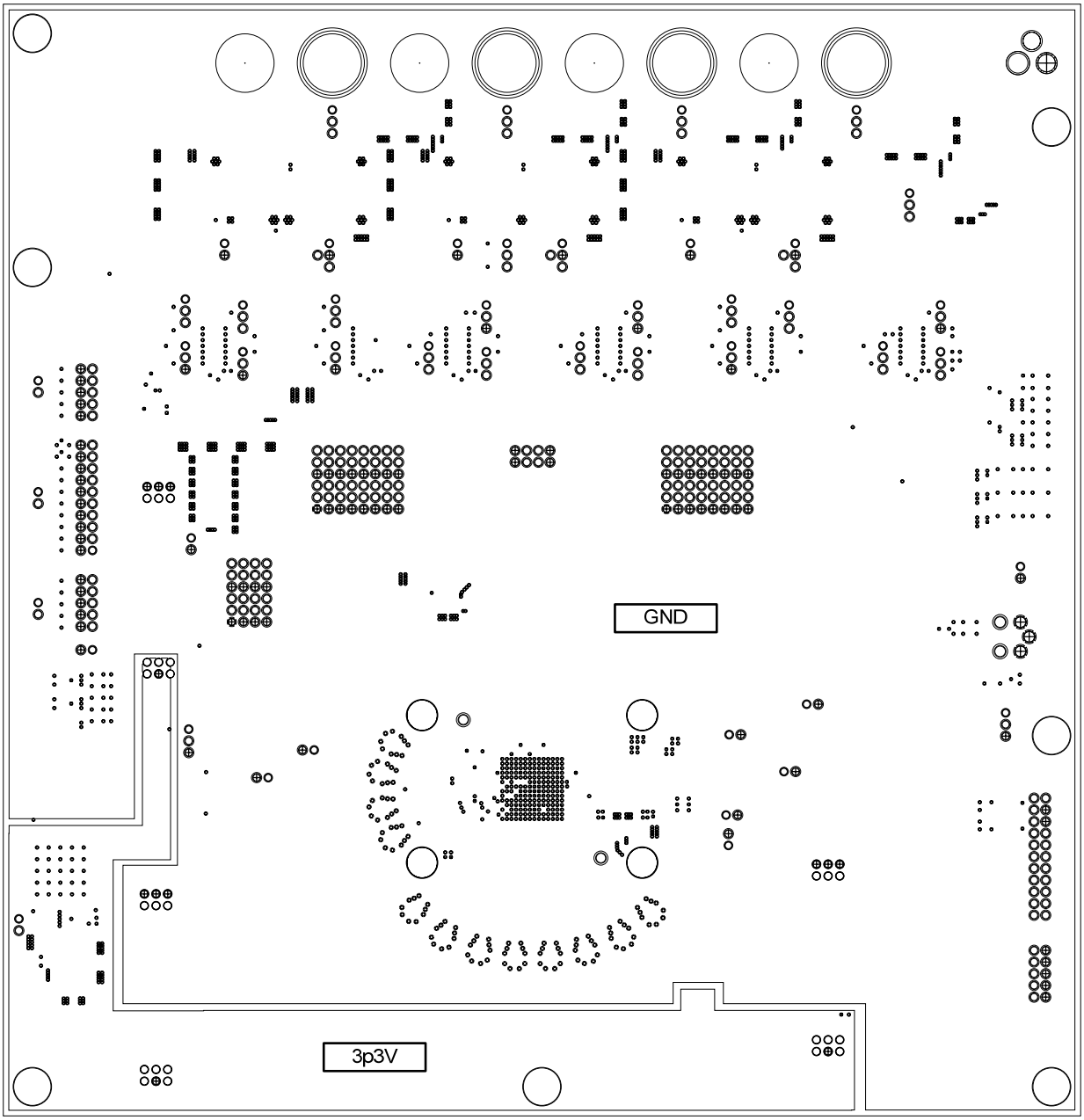


Figure 44. TLK3132 EVM Layout, Internal Signal (Layer 12)

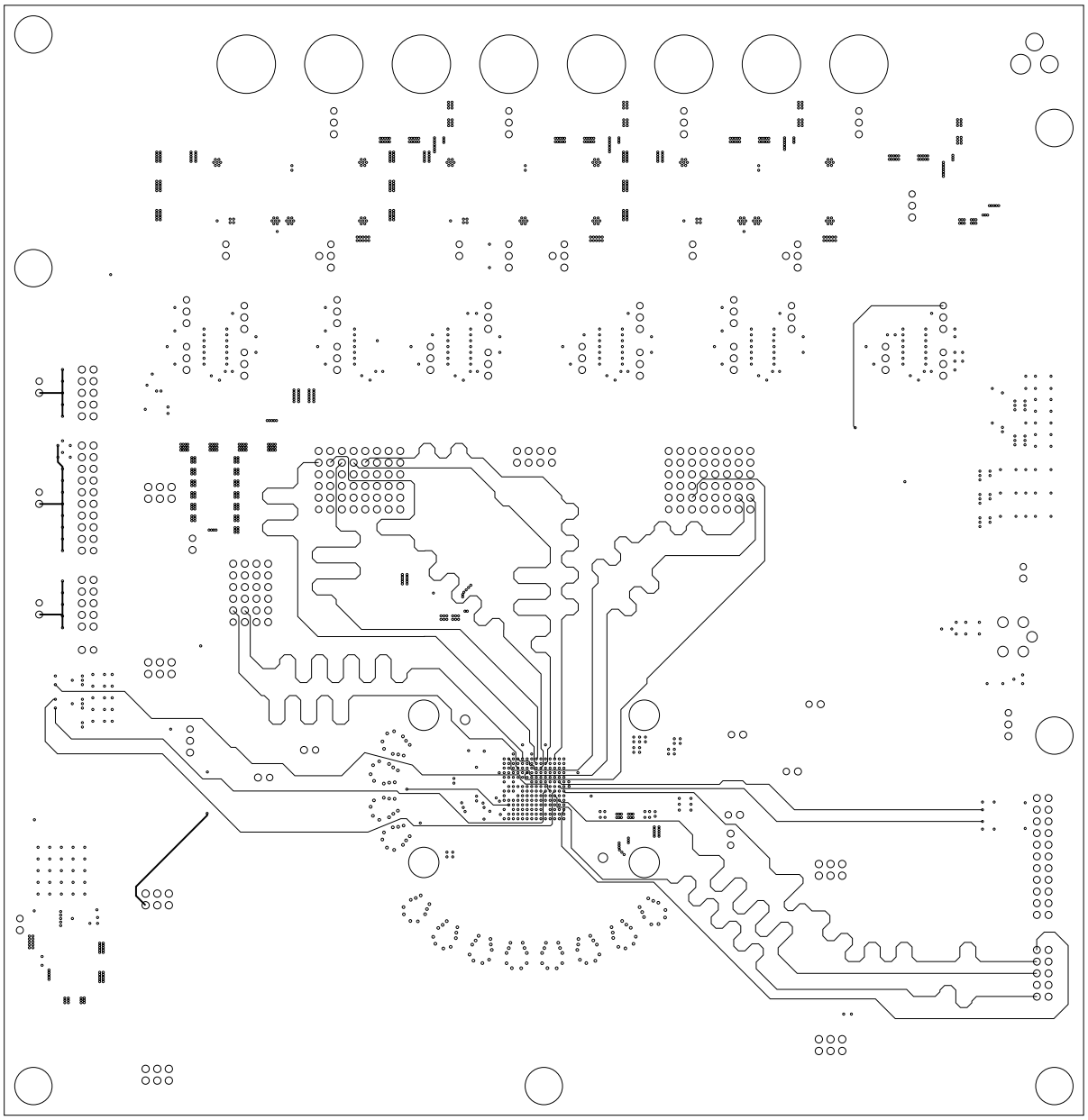


Figure 45. TLK3132 EVM Layout, Internal Ground (Layers 13,15,17)

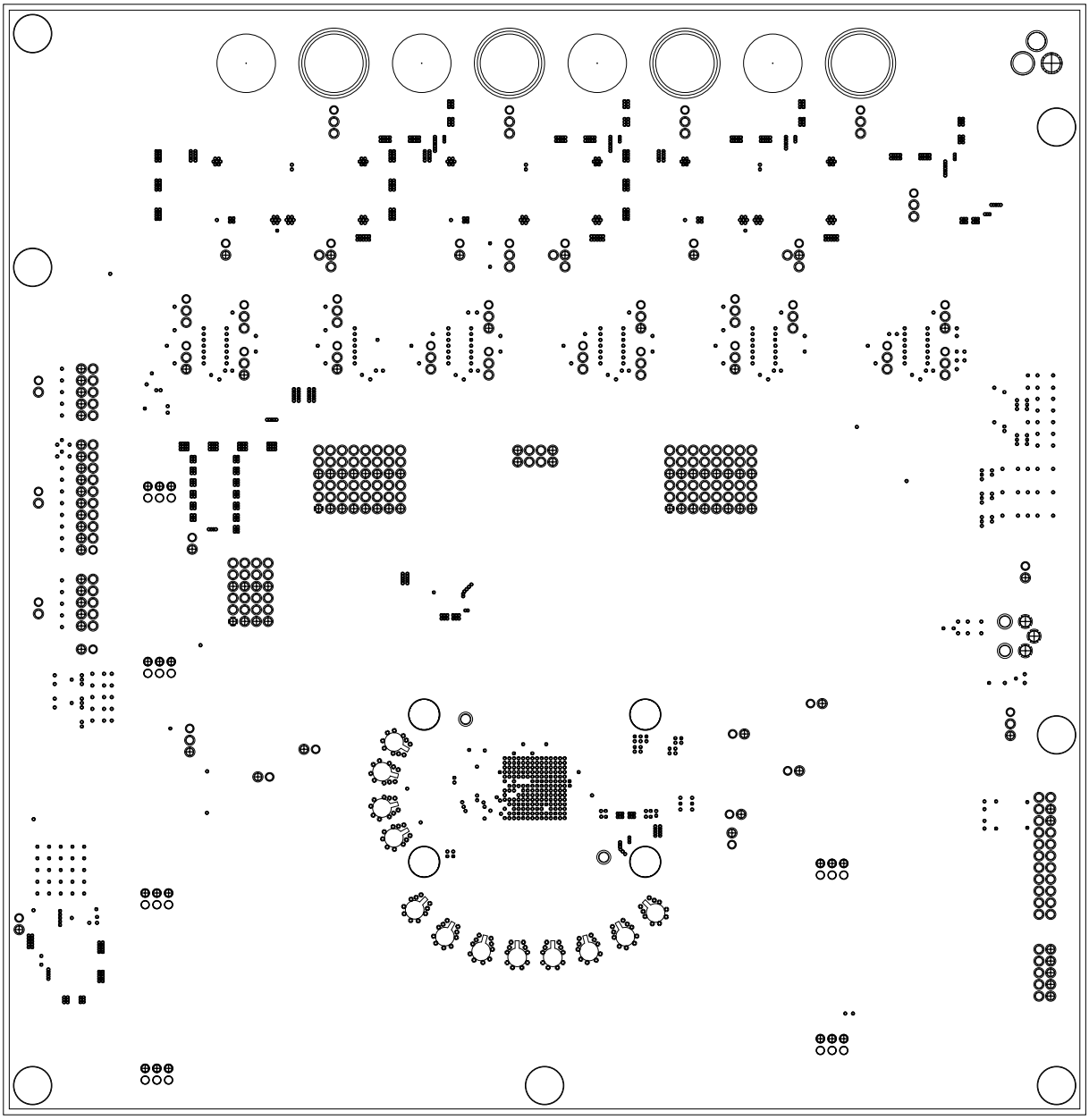


Figure 46. TLK3132 EVM Layout, Internal Signal (Layer 14)

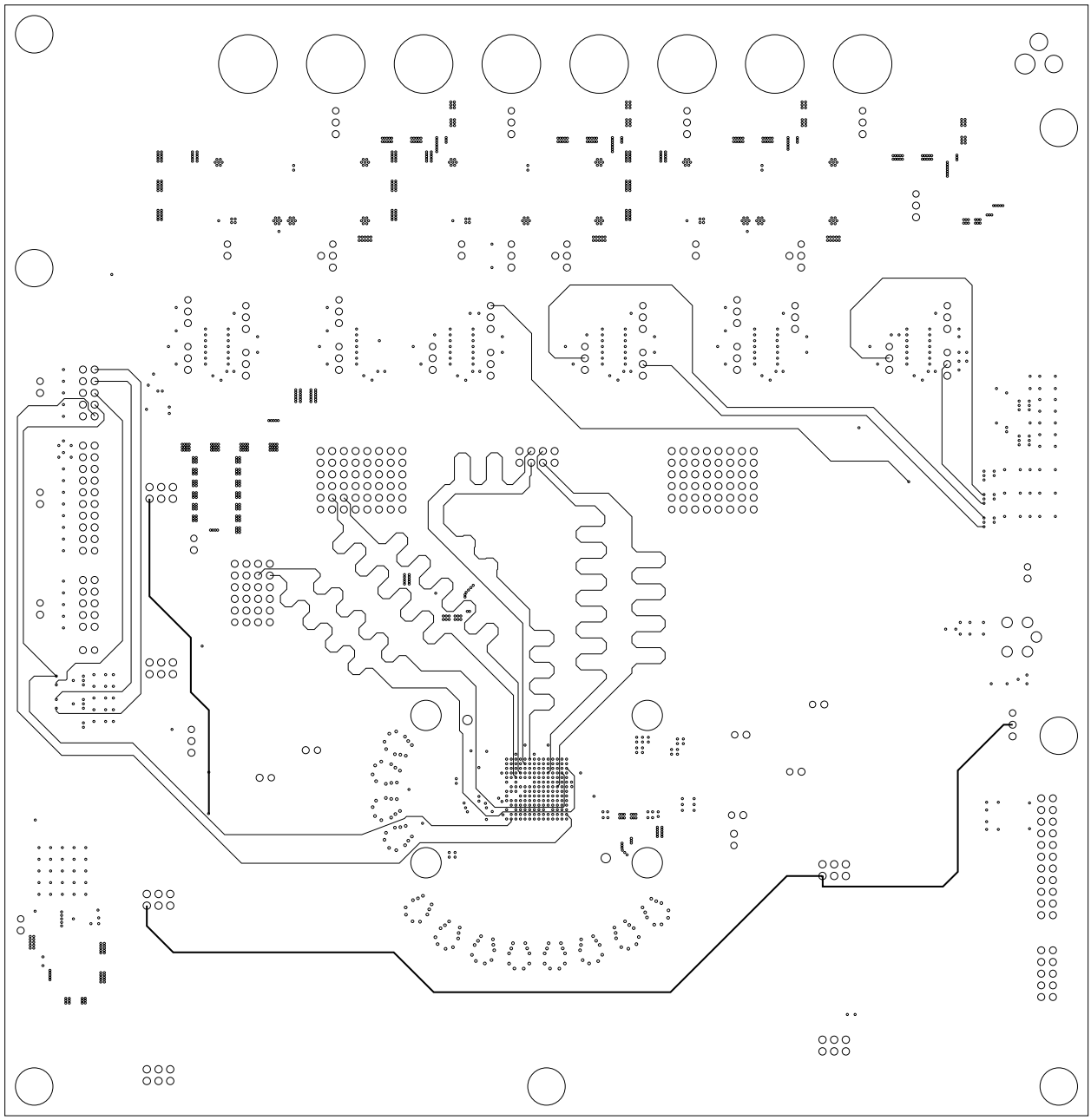
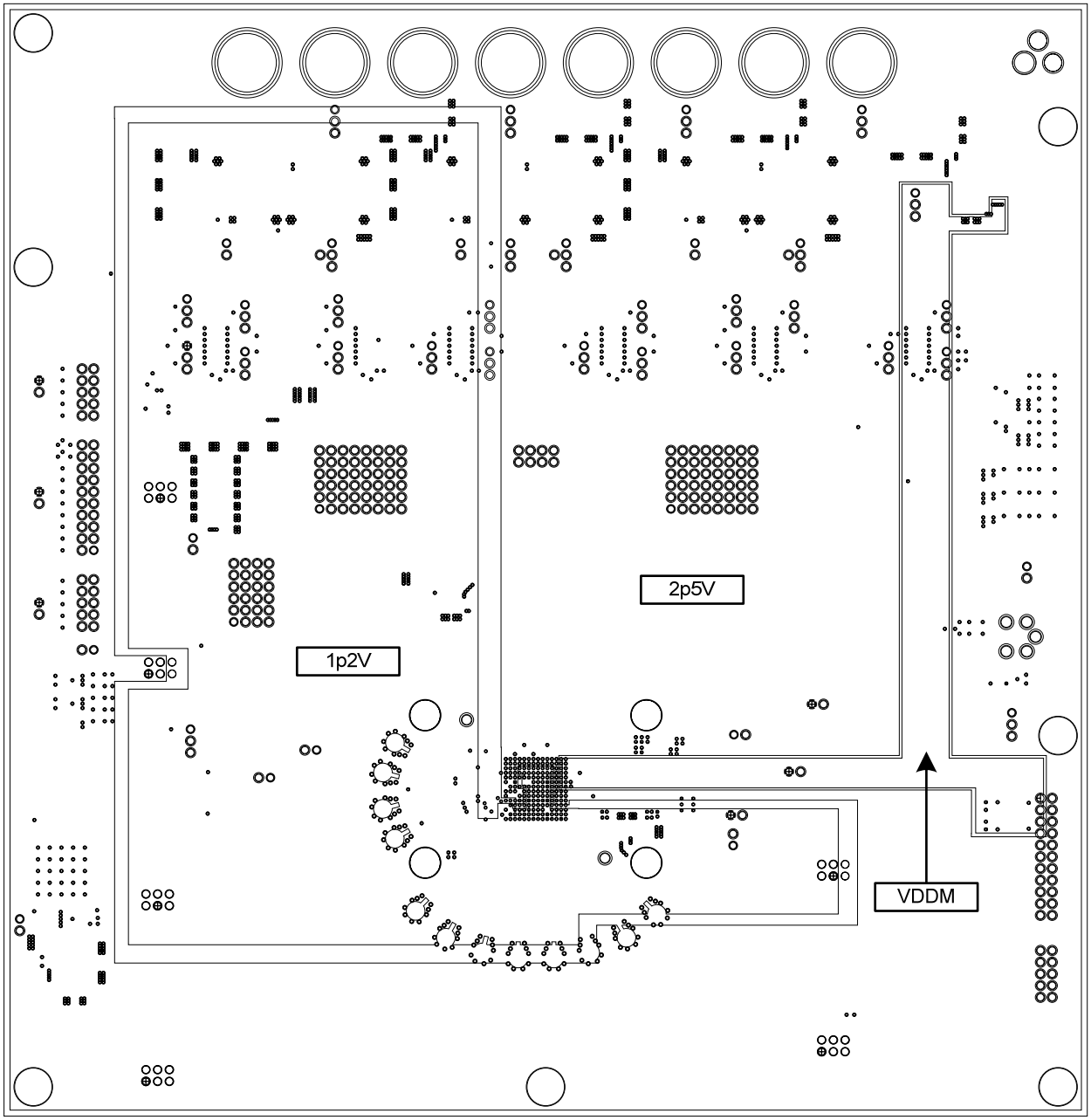
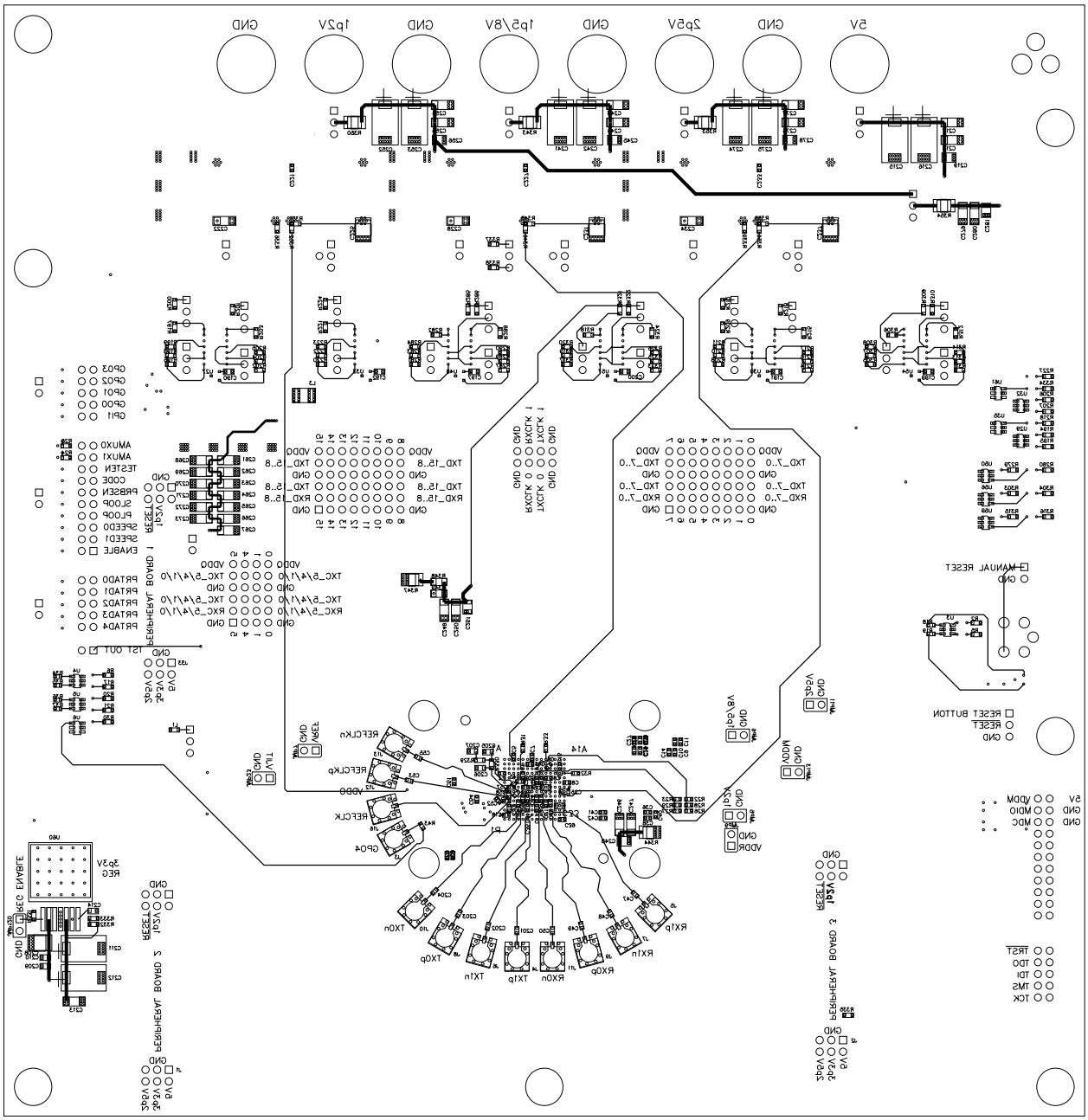


Figure 47. TLK3132 EVM Layout, Internal Power (Layer 16)



TLK3132 EVM Layout, Bottom Signal (Layer 18)



TLK3132 EVM Layer Construction

Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Artwork	Width (MIL)	Impedance (ohm)
	SURFACE	AIR							
TOP	CONDUCTOR	COPPER	2.4	595900	1	0	POSITIVE	9.5	47.917
	DIELECTRIC	FR-4	5	0	4.1	0.035			
L2_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	3	0	4.1	0.035			
L3_VCC	CONDUCTOR	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	3	0	4.1	0.035			
L4_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	6.5	0	4.1	0.035			
L5_SIG	CONDUCTOR	COPPER	1.2	595900	1	0	POSITIVE	6.5	46.469
	DIELECTRIC	FR-4	6.5	0	4.1	0.035			
L6_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	6.5	0	4.1	0.035			
L7_SIG	PLANE	COPPER	1.2	595900	1	0	POSITIVE	6.5	46.469
	DIELECTRIC	FR-4	6.5	0	4.1	0.035			
L8_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	3	0	4.1	0.035			
L9_VCC	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	3	0	4.1	0.035			
L10_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	3	0	4.1	0.035			
L11_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	6.5	0	4.1	0.035			
L12_SIG	CONDUCTOR	COPPER	1.2	595900	1	0	POSITIVE	6.5	46.469
	DIELECTRIC	FR-4	6.5	0	4.1	0.035			
L13_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	6.5	0	4.1	0.035			
L14_SIG	CONDUCTOR	COPPER	1.2	595900	1	0	POSITIVE	6.5	46.469
	DIELECTRIC	FR-4	6.5	0	4.1	0.035			
L15_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	3	0	4.1	0.035			
L16_VCC	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	3	0	4.1	0.035			
L17_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	3	0	4.1	0.035			
BOTTOM	CONDUCTOR	COPPER	2.4	595900	1	0	POSITIVE	9.5	47.917
	SURFACE	AIR							

****NOTE: The Impedance is set to be slightly less than 50 ohms on the traces in order to compensate for slight over-etching during the manufacturing process. The end impedance after etching should result in a 50 ohm Impedance. Always consult with your board manufacturer for their process/design requirements to ensure the desired impedance is achieved.**

Revision History

Initial Creation (09/09/08 – JN)

Rev 0.1 Added (09/16/08 – JN)

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

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As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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本開発キットは技術基準適合証明を受けておりません。

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EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI’s recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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