

TLK6002 Board Design Guide

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ICP-Communications Interface

ABSTRACT

The TLK6002 is a multi-gigabit transceiver intended for use in ultra-high-speed, bidirectional, point-to-point, data transmission systems such as base station Remote Radio Head (RRH) applications as well as any other high-speed applications. All CPRI and OBSAI data rates of 0.6144, 0.768, 1.2288, 1.536, 2.4576, 3.072, 4.9152, and 6.144Gbps are supported using a single, fixed reference clock frequency of either 122.88 MHz or 153.6 MHz and non-CPRI or OBSAI serial data rates between 0.470 and 6.25 Gbps are also supported. Each channel of the TLK6002 can be operated from a single, shared reference clock or independently from separate reference clocks at different frequencies.

This document provides recommendations on successful integration of the TLK6002 in customer systems. It discusses power supplies, high-speed interfaces, as well as various control interfaces and the associated peripheral components.

Contents

1	TLK6002 Power Supply	2
1.1	Generating the 1-V Power Supply	2
1.2	1-V Power Supply Filtering and Decoupling	2
1.3	Generating the 1.5-V/1.8-V Power Supply	3
1.4	1.5-V/1.8-V Power Supply Filtering and Decoupling	3
1.5	Power Supply Ramp Order	4
1.6	AGND and DGND	4
2	TLK6002 High-Speed Data Path	4
2.1	Layout Recommendations for High-Speed Signals	4
2.2	AC-Coupling	7
3	TLK6002 Low-Speed Data Path	7
3.1	Layout Recommendations for Low-Speed Signals	7
4	TLK6002 Clocks: REFCLK, CLK_OUT, TXCLK, and RXCLK	8
4.1	General Information	8
4.2	External Clock Connections	8
5	TLK6002 Control Pins and Interfaces	9
5.1	MDIO Interface	9
5.2	JTAG Interface	9
5.3	SPI Interface	9
5.4	Provisioning for System Debug	9
5.5	Unused Pins	9
6	Summary	9
7	References	9

List of Figures

1	1-V Power Supply Filtering and Decoupling Connections	2
2	1.5-V/1.8-V Power Supply Filtering and Decoupling Connections	4
3	Differential Microstrip PCB Trace Geometry Example	5
4	High-Speed PCB Traces With Vias Having no Via Stubs and no Via Pads on Internal Layers	6
5	Differential PCB via Structure, Top View	6
6	Reference Plane Cutout Under SFP/SFP+ Module Connector Pads	7

7	HSTL Output and Input Schematic	8
8	External Clock Jitter Cleaner Connection Example for Channel A	8

List of Tables

1	TLK6002 Device 1-V Supply Specifications	2
2	TLK6002 Device 1.5-V/1.8-V Supply Specifications	3

1 TLK6002 Power Supply

The TLK6002 operates from two basic power supplies: 1 V and 1.5 V or 1.8 V. Either a linear low-dropout (LDO) regulator or a switching regulator can be used for any of those power supplies.

1.1 Generating the 1-V Power Supply

The TLK6002 device 1-V power supply specifications are highlighted in [Table 1](#).

Table 1. TLK6002 Device 1-V Supply Specifications

PARAMETER		SPECIFICATION		
		MIN	NOM	MAX
Power Supply Voltage	VDDD, AVDD, DVDD, VDDT, VPP	0.95 V	1 V	1.05 V
Power Supply Current	VDDD			75 mA
	AVDD			250 mA
	DVDD+VPP			200 mA
	VDDT			15 mA

1.2 1-V Power Supply Filtering and Decoupling

A recommended power supply filtering and decoupling network is shown in [Figure 1](#). The 0.1- μ F decoupling capacitors in 0201 (preferred) or 0402 size must be placed as close as possible to the respective power supply pins. Package sizes for the remaining capacitors must be chosen as small as possible. For high-frequency filtering, any ferrite bead can be used as long as it has less than 5% dc voltage drop at the maximum respective power supply current as provided in the [Table 1](#). The AVDD_VDDT node shown in [Figure 1](#) must be connected to all AVDD and VDDT pins.

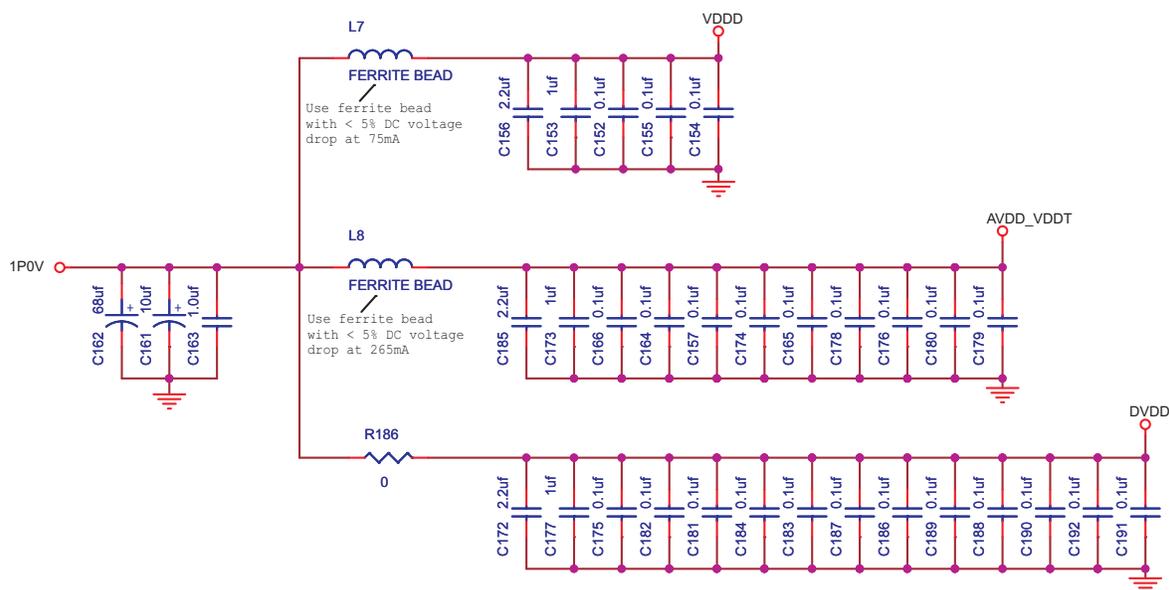


Figure 1. 1-V Power Supply Filtering and Decoupling Connections

1.3 Generating the 1.5-V/1.8-V Power Supply

The TLK6002 device 1.5-V/1.8-V power supply specifications are highlighted in [Table 2](#).

Table 2. TLK6002 Device 1.5-V/1.8-V Supply Specifications

Parameter		Specification		
		Min	Nom	Max
Power Supply Voltage	VDDQA/B	1.4 V/1.7 V	1.5 V/1.8 V	1.6 V/1.9 V
	VDDRA/B,VDDO1/2/3	1.425 V/1.71 V	1.5 V/1.8 V	1.575 V/1.89 V
	VREFTA/B	-1%	0.75 V/0.9 V	+1%
Power Supply Current	VDDQA/B			800 mA
	VDDRA/B			40 mA
	VDDO1/2/3			10 mA
	VREFTA/B			0.5 mA

1.4 1.5-V/1.8-V Power Supply Filtering and Decoupling

A recommended power supply filtering and decoupling network is shown in [Figure 2](#). The 0.1- μ F decoupling capacitors in 0201 (preferred) or 0402 size must be placed as close as possible to the respective power supply pins. Package sizes for the remaining capacitors must be chosen as small as possible. For high-frequency filtering, any ferrite bead can be used as long as it has less than 5% dc voltage drop at the maximum respective power supply current as provided in the [Table 2](#). The VDDQ_VDDO node shown in [Figure 2](#) must be connected to all VDDQA, VDDQB, VDDO1, VDDO2, and VDDO3 pins. The VREF node must be connected to VREFTA and VREFTB pins. The VREF supply is derived from the VDDQ_VDDO supply using a resistive voltage divider.

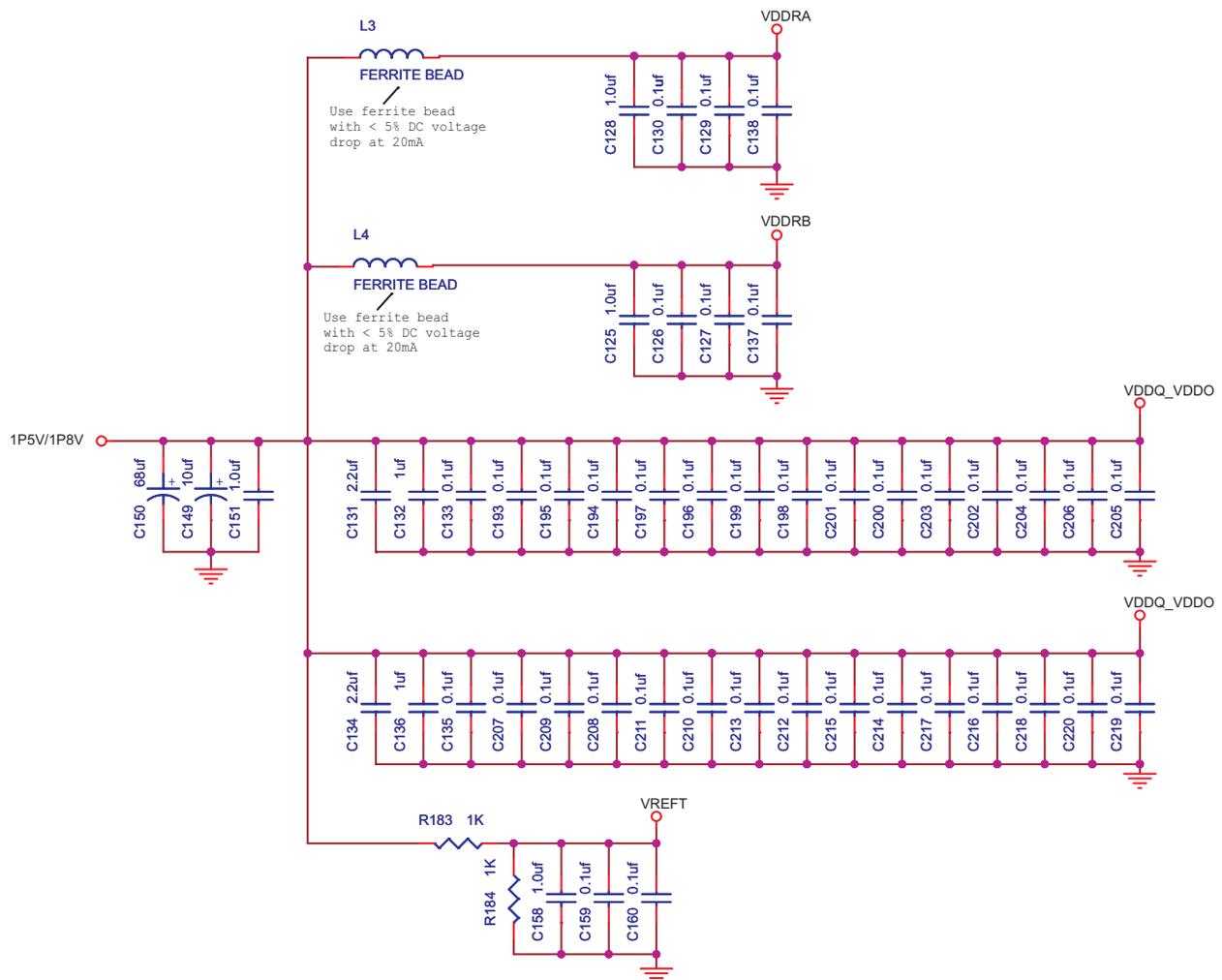


Figure 2. 1.5-V/1.8-V Power Supply Filtering and Decoupling Connections

1.5 Power Supply Ramp Order

No specific 1-V and 1.5-V/1.8-V power supply ramp order needs to be observed as long as the device provisioning includes the setting of register 28, bit 14 to enable normal CLK_OUT_P/N operation. However, it is generally recommended to ramp up DVDD before VDDQA/B.

1.6 AGND and DGND

AGND and DGND pins must be tied together on the application board.

2 TLK6002 High-Speed Data Path

2.1 Layout Recommendations for High-Speed Signals

The high-speed data path CML input pins RXAP/RXAN and RXBP/RXBN, and the CML output pins TXAP/TXAN and TXBP/TXBN have to be connected with loosely coupled, 100- Ω differential transmission lines. Differential intra-pair skew needs to be minimized as much as possible to within ± 1 mil. An example of FR-4 printed-circuit board (PCB) realization of such differential transmission lines in microstrip format is shown in Figure 3.

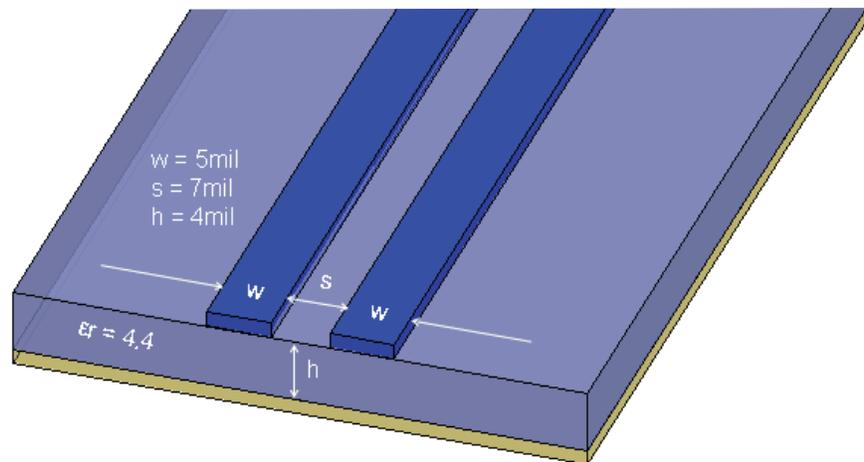


Figure 3. Differential Microstrip PCB Trace Geometry Example

To avoid impedance discontinuities, the high-speed serial signals must be routed on a PCB on either the top or bottom PCB layers in microstrip format with no vias. If vias are unavoidable, an absolute minimum number of vias need to be used. The vias must be made to stretch through the entire PCB thickness (as shown in [Figure 4](#)) to connect microstrip traces on the top and bottom layers of the PCB so as to leave no via stubs that can severely impact the performance. If stripline traces are absolutely necessary, then the routing layers must only be one layer below the top layer and one layer above the bottom layer so as to minimize via stub length.

All unused internal layer via pads on high-speed signal vias must be removed to further improve impedance matching. RXAP/RXAN and RXBP/RXBN signals are more sensitive to impedance discontinuities introduced by vias than TXAP/TXAN and TXBP/TXBN signals. For that reason, if only some of those signals need to be routed with vias, then the latter must be routed with vias and the former with no vias.

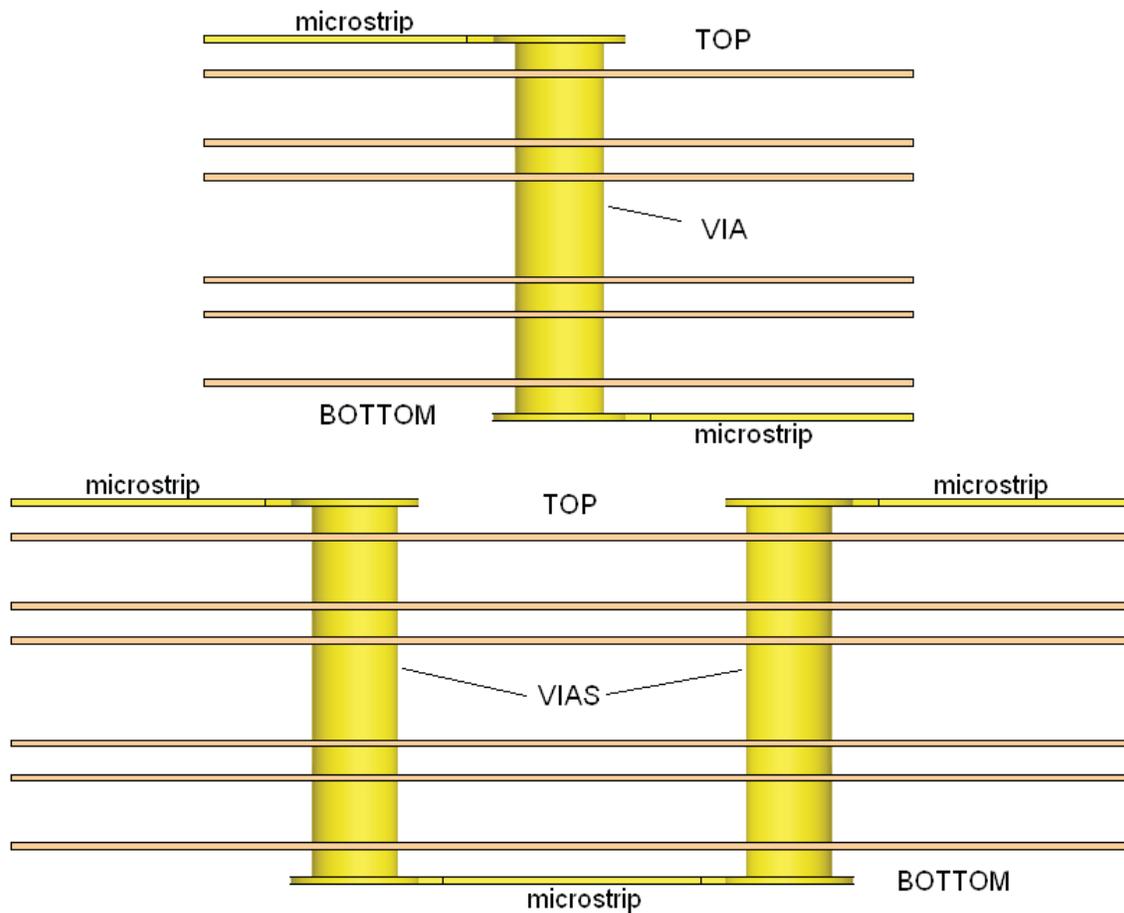


Figure 4. High-Speed PCB Traces With Vias Having no Via Stubs and no Via Pads on Internal Layers

To further improve on impedance matching, differential vias with neighboring ground vias can be used as shown in [Figure 5](#). The optimum dimensions of such a differential via structure depend on various parameters such as the trace geometry, dielectric material, as well as the PCB layer stack-up. A 3D electromagnetic field solver can be used to find the optimum via dimensions.

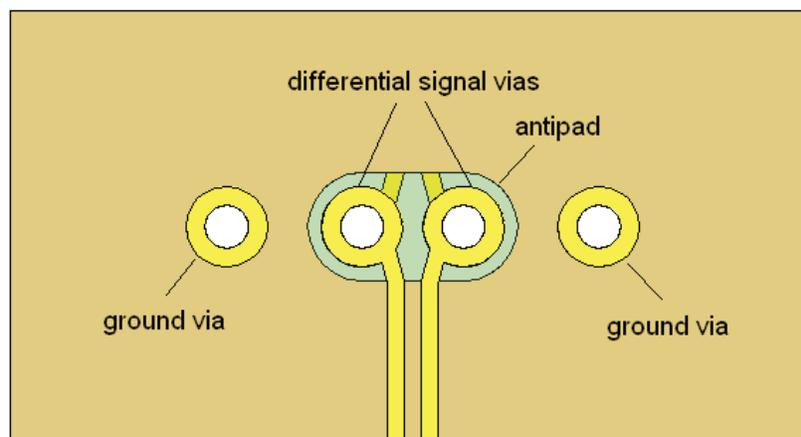


Figure 5. Differential PCB via Structure, Top View

PCB traces connected to the RXAP/RXAN and RXBP/RXBN pins must have at least 4 dB of differential insertion loss at 3 GHz. For the FR-4 material and 5-mil trace width, the PCB microstrip trace that meets that condition is at least 6 inches long.

Surface-mount connector pads such as those used with the SFP/SFP+ module connectors are wider and hence have characteristic impedance that is lower than the regular high-speed PCB traces. If the pads are more than 2 times wider than the PCB traces, the pads' impedance needs to be increased to minimize impedance discontinuities. The easy way of increasing the pads' impedance is to cut out the reference plane immediately under those pads as shown in Figure 6 so as to have the pads refer to a reference plane on lower layers while maintaining 100-Ω differential characteristic impedance.

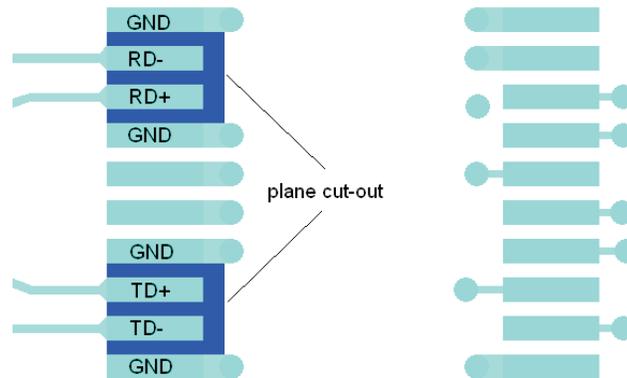


Figure 6. Reference Plane Cutout Under SFP/SFP+ Module Connector Pads

2.2 AC-Coupling

A 0.1-μF series ac-coupling capacitor must be connected to each of the high-speed data path pins RXAP, RXAN, RXBP, RXBN, TXAP, TXAN, TXBP, and TXBN. If the TLK6002 high-speed data path pins are connected to SFP/SFP+ optical modules, then no external ac-coupling capacitors must be used because the modules already have the required capacitors. Adding additional series capacitors may severely impact the performance.

To avoid impedance discontinuities, it is strongly recommended where possible to make the transmission line trace width closely match the ac-coupling capacitor pad size. Smaller capacitor packages such as 0201 make it easy to meet that condition.

3 TLK6002 Low-Speed Data Path

3.1 Layout Recommendations for Low-Speed Signals

The low-speed data path HSTL input pins TDA_[19:0] and TDB_[19:0] and the HSTL output pins RDA_[19:0] and RDB_[19:0] have to be routed on a PCB as 50-Ω, single-ended transmission lines. The HSTL inputs and outputs can operate at 1.5 V or 1.8 V.

All TDA and TDB signals need to be length-matched with the respective TXCLK signals to within ±1 mil. All RDA and RDB signals need to be length-matched with the respective RXCLK signals to within ±1 mil.

The HSTL inputs and outputs have internal terminations that are dynamically calibrated to compensate for process, voltage, and temperature using four external reference resistors: RESRA, RESTA, RESRB, and RESTB. Each of those resistors needs to be 50 Ω with 0.5% tolerance. The internal terminations are as shown in Figure 7. While the 50-Ω series output termination is fixed, the parallel input terminations are selectable: 50 Ω or 100 Ω to (VDDQA/B)/2. The termination also can be disabled for lower power consumption but care has to be taken to maintain signal integrity. Because internal terminations are provided, external terminations on TDA, TDB, RDA, and RDB signals are not needed.

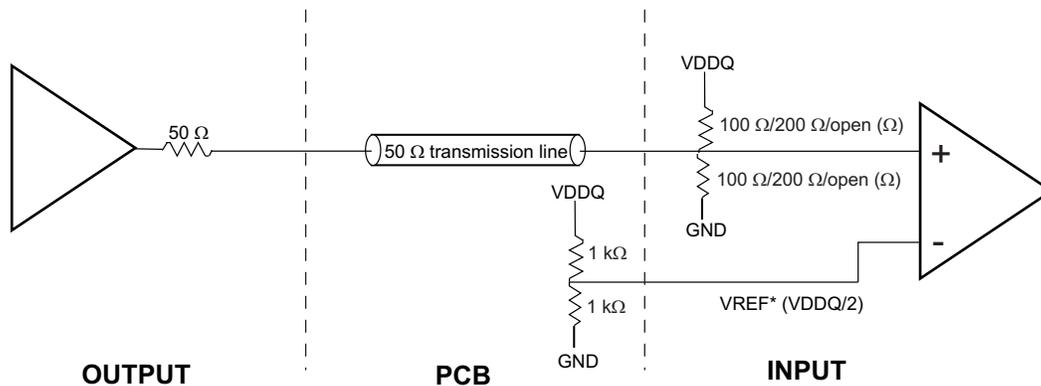


Figure 7. HSTL Output and Input Schematic

4 TLK6002 Clocks: REFCLK, CLK_OUT, TXCLK, and RXCLK

4.1 General Information

The TLK6002 device requires a low-jitter reference clock to work. The reference clock can be provided on the REFCLK_0_P/N or REFCLK_1_P/N pins. Both reference clock input pins have internal 100- Ω differential terminations, so they do not need any external terminations. Both reference clock inputs must be ac-coupled with preferably 0.1- μ F capacitors. The two channels (A and B) can have same or different reference clocks. Refer to the TLK6002 data sheet for more information on reference clock selection.

The TLK6002 serial receiver recovers clock and data from the incoming serial data. The recovered byte clock is made available on the RXCLK_A/B pins and can optionally be made available on the CLK_OUT_P/N pins. The CLK_OUT_P/N CML output pins must be ac-coupled with 0.1- μ F, ac-coupling capacitors.

4.2 External Clock Connections

An external clock jitter cleaner, such as Texas Instruments CDCE72010 or CDCM7005, may be used when needed to provide a low-jitter reference clock. An example external clock jitter cleaner connection for channel A is shown in Figure 8.

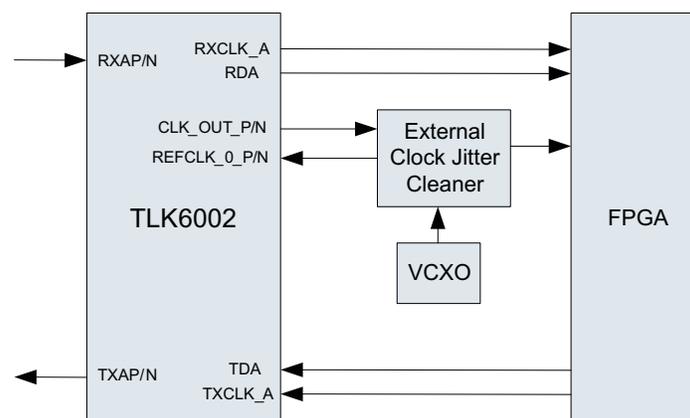


Figure 8. External Clock Jitter Cleaner Connection Example for Channel A

Note that TXCLK_A/B must be synchronous with REFCLK_0/1_P/N. The TXCLK_A/B HSTL input pins (as well as all other HSTL input pins) already have selectable internal 50- Ω or 100- Ω to (VDDQA/B)/2 terminations; so, no external terminations are needed. The termination can also be disabled for lower power consumption but care has to be taken to maintain signal integrity.

RXCLK_A/B HSTL output pins have internal 50-Ω series terminations, so external series terminations are not needed on those pins.

5 TLK6002 Control Pins and Interfaces

The TLK6002 device features a number of control pins and interfaces, some of which are described in the following paragraphs.

5.1 MDIO Interface

The TLK6002 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 22 of the IEEE 802.3 Ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK6002 is possible without use of this interface. However, some features are accessible only through the MDIO.

The MDIO Management Interface consists of a bidirectional data path (MDIO) and a clock reference (MDC). The port address is determined by the PRTAD[4:0] control pins (see Table 2-10 of the TLK6002 data sheet).

The MDIO pin requires a pullup to VDDO3. No pullup is needed on the MDC pin.

5.2 JTAG Interface

The JTAG interface is mostly used for device test. The JTAG interface operates through the TDI, TDO, TMS, TCK, and TRST_N pins. If not used, all the pins can be left unconnected except TDI and TCK which have to be grounded.

5.3 SPI Interface

The SPI interface is not really used to control the TLK6002 device. It is provided only for compatibility with other devices in the same family as the TLK6002. The SPI interface operates through the SCL, SDO, SDI, and CS_N pins. If not used, all the pins can be left unconnected except SDO, which has to be grounded.

5.4 Provisioning for System Debug

To allow easy system debug, PRBS_EN, RATE_B2, LOSA, RATE_A2, and CODEA_EN pins must each have a placeholder for a pullup resistor to VDDO (1.5 V/1.8 V) and a 0-Ω series resistor to physically isolate the pin from an external controller when needed. Additionally, GPIO and TESTEN pins must have placeholders for pullup resistors to VDDO.

5.5 Unused Pins

As a general guideline, any unused HSTL or LVCMOS input pin needs to be grounded and any unused HSTL or LVCMOS output pin can be left unconnected. Unused CML differential output pins can be left unconnected. Unused CML differential input pins must be tied to ground through a shared 100-Ω resistor.

6 Summary

This document provides an overview of recommended board design considerations for successful integration of the TLK6002 device on system boards. See the TLK6002 data sheet for more information on device features and control.

7 References

TLK6002, *Dual Channel 0.47Gbps to 6.25Gbps Multi-Rate Transceiver* data sheet ([SLLSE34](#))

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