Support HDMI 1.3 12-Bit Deep Color With the TMDS341A

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The compatibility of the 3:1 HDMI-switch, TMDS341A, with the HDMI1.3 standard is questioned frequently because the device was originally designed to support version 1.2 of the standard. Hence, its release to production occurred almost two months before HDMI 1.3 was published. To remove any remaining concerns, this application brief explains why the TMDS341A is HDMI 1.3 compatible.

The functional principles of a HDMI system are reviewed with regards to video data processing, followed by the identification of challenges the new standard presents to the device. A comparison between maximum device bandwidth and the required signaling rate to support the video formats specified by HDMI 1.3 concludes this brief.

Figure 1 shows a HDMI system comprising a HDMI source, a data link and a HDMI sink. The entire signal chain, (from source to sink), consists of three data channels and a clock channel. Each data channel carries the video data for one of the primary color components Red, Green or Blue, as well as corresponding control and auxiliary data, such as audio samples or packet headers.

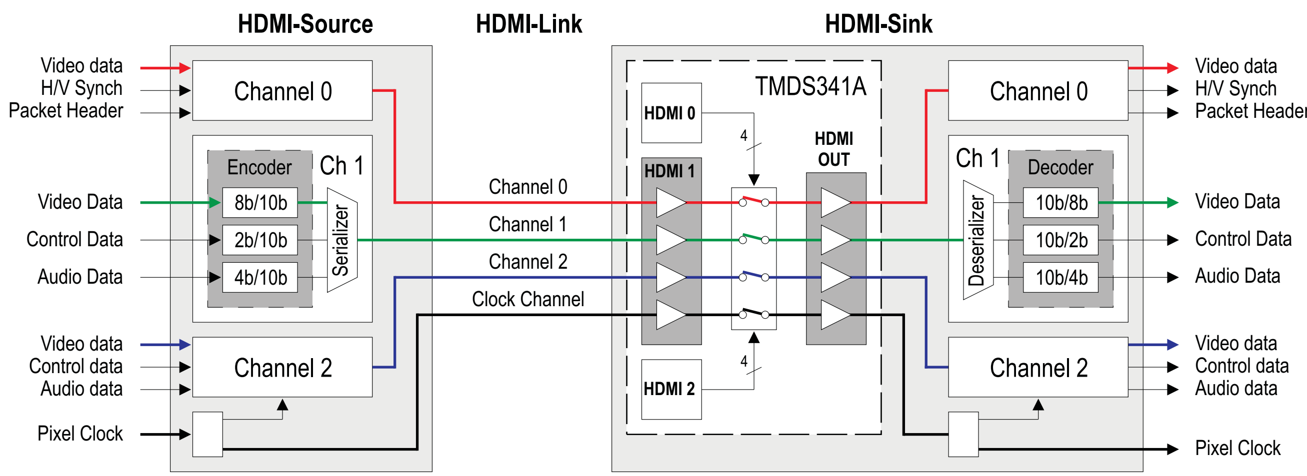


Figure 1. HDMI System Overview

Video data enters the transmitter inputs in an 8-bit parallel format and is then encoded into a 10-bit parallel format by an 8b/10b encoder. Encoding is also applied to the 4-bit audio/auxiliary and 2-bit control data. Each type of input data is converted into a 10-bit parallel format. The following serializer converts the parallel data into serial 10-bit data packets ready for transmission across the transition-minimized-differential-signaling (TMDS™) data link.

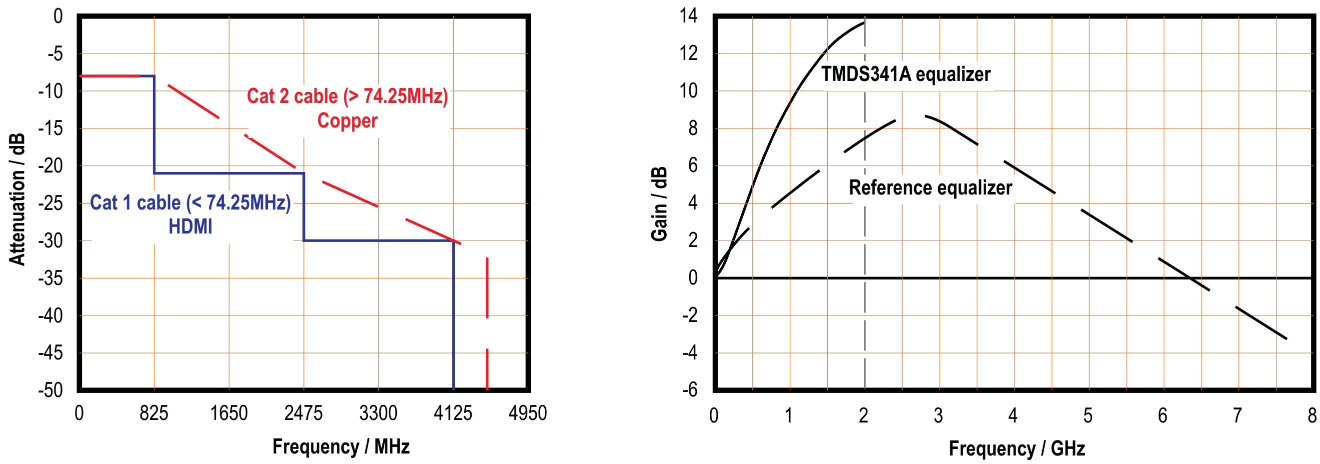
On the data link a 10-bit packet is transmitted during one TMDS clock cycle, thus maintaining a ratio of signaling rate to TMDS clock of 10:1.

The HDMI sink reverses the data processing steps of the source and converts the serial data from the TMDS channel back into the original, parallel format. One additional processing step, the data recovery, is required at the data link-to-source interface. It is here where repeater chips, such as the TMDS341A, find their application.

TMDS is a trademark of Texas Instruments.

Data Recovery

Due to the insertion losses of the data link cables, predominantly at high frequencies, the input stages of the TMDS341A consists of four high-speed amplifiers with high-pass characteristics. This equalization function (EQ) compensates for the high-frequency cables losses, thus equalizing the overall frequency response. The left diagram in Figure 2 presents the specified loss profiles for HDMI cable and low-cost copper cable.



NOTE: The terms Cat1 and Cat2 distinguish between the low- and high frequency cabling described by HDMI1.3 and do not represent the grade of UTP cabling described by EIA/TIA 568B.

Figure 2. Specified Cable Loss Profiles

The HDMI standard also specifies the gain response of a reference equalizer, which should be approximated by any type of repeater IC with internal equalization. The right diagram in Figure 2 compares the EQ-response of the TMDS341A with the one of the reference equalizer. The TMDS341A is providing significant higher gain than the reference equalizer and well exceeds HDMI 1.3.

Color Depth and Display Formats

Determining a repeater's data signaling rate compatibility, (DSR), with HDMI 1.3 requires knowledge of the color depths and display formats to be supported. The standard progression in Table 1 mentions everything from improved compatibility testing and added audio support to CEC implementation and new test requirements for specific cables, but little on the available color depths and nothing on display formats.

Table 1. Standard Progression HDMI 1.0 to 1.3

December-02	June-04	August-05	December-05	June-06
HDMI1.0	HDMI1.1	HDMI1.2	HDMI1.2a	HDMI1.3
Initial Specification	Added support for DVD-Audio	Added support for SACD	CEC Functionality fully specified	Supports 24, 30, 36 and 48-bit color depth for RGB and YCbCr
	Improvement to compatibility Testing	Permits use of RGB color space for monitor application	Testing required for specific cable lengths	Supports next-generation "xvYCC" color space
		Supports low-voltage (AC-coupled sources) in PCs	Certified Connector List – required to pass ATC testing	Adds new Mini-HDMI connector for mobile applications
				Adds automatic video/audio synching capability
				Adds Dolby TrueHD and DTS-HD Audio formats

In contrast the lesser known diagrams in Figure 3 are very specific on the supported color depths and display formats. According to these diagrams 24-bit had already been specified as the mandatory standard color depth in HDMI 1.0, while the higher color depths of 30, 36 and 48-bits were added in HDMI 1.3 as optional deep-color modes only. The standard states, however, that if a new system design is intended to support one or more of the optional deep color modes, it must at least support the 36-bit mode as well as the 24-bit mode.

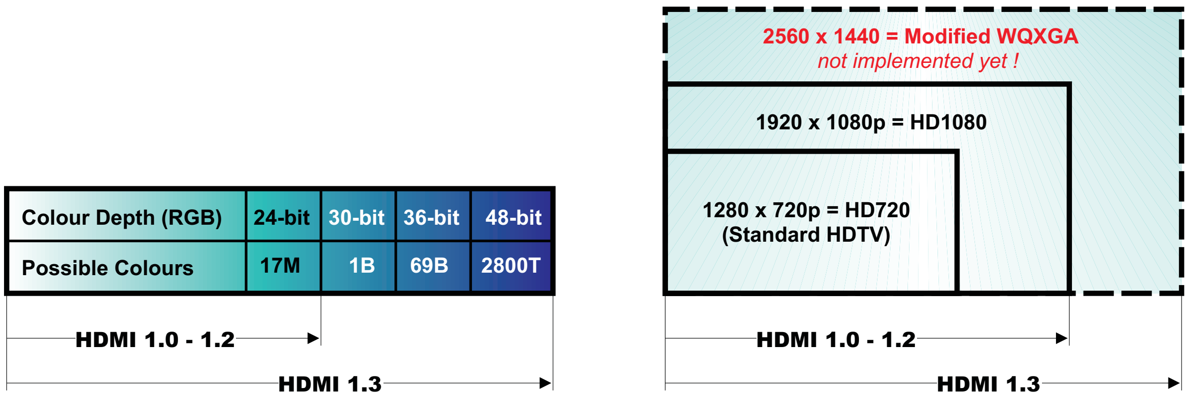


Figure 3. HDMI Progression of Color Depths and Monitor Formats

With regards to display formats, both the standard HDTV format HD720 with 1280 x 720 pixels, and the larger HD1080 format with 1920 x 1080 pixels have been supported all along since version 1.0. The modified WQXGA format, (2560 x 1440 pixels), however, is not yet listed in HDMI's supported video formats.

Figure 4 shows the pixel allocation of a 1920 × 1080 display. While these numbers describe the active video area only, the total pixel count required to scan an entire frame is somewhat higher. This is due to the *retrace* time intervals required between consecutive line scans in horizontal direction and consecutive frame scans in vertical direction. The term *retrace* is taken from the CRT-TV where the steering of the electron beam back to its start position is necessary after each line and frame scan. LCDs do not have to steer electron beams, so they do not have this hardware limitations. They do, however, have memory bandwidth limitations for the screen buffer, not to mention image scaling calculations and noise reduction.

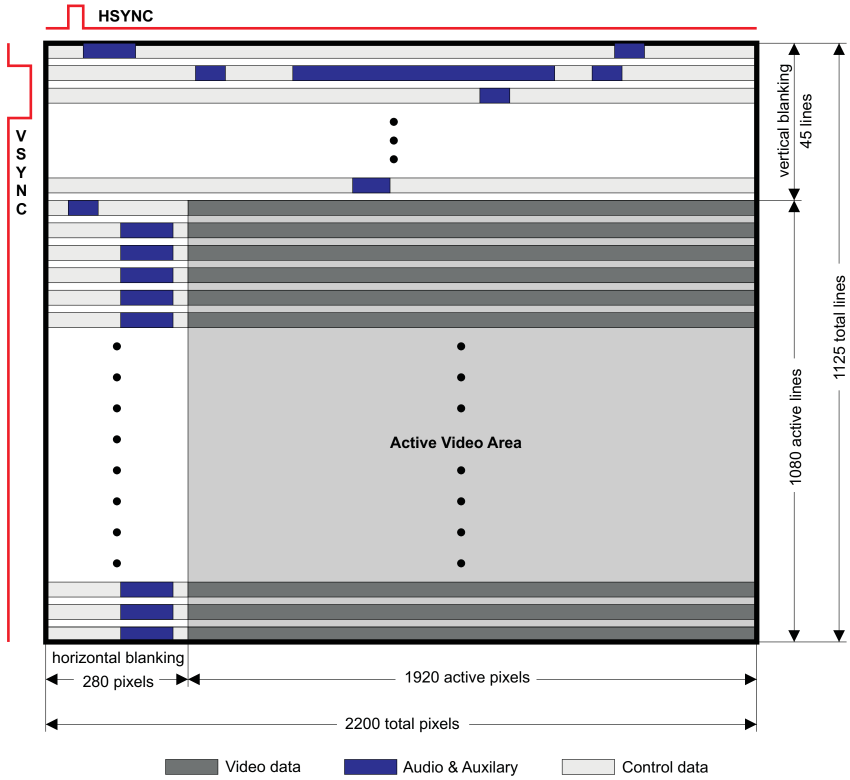


Figure 4. Pixel Allocation of a 1920 × 1080 Display Format

The retrace time intervals, also known as vertical and horizontal blanking, are presented in the form of additional, virtual pixels above and beside the active video area. Again, the term *blanking* is taken from the CRT-TV where the electron-beam is blanked when steered back to its start position. In an LCD, however, during the retrace time intervals, the pixels of the video area maintain their color information, while control and audio data are transmitted across the TMDS channels. Because the retrace intervals reduce the rate at which an LCD is able to accept new frames of video data, their representation in form of virtual pixels must be taken into account when calculating the required signaling rate. For a display format of 1920 × 1080 pixels of active video area, the total pixel.

Data Signaling Rate (DSR)

When determining the DSR one must distinguish between progressive and interlaced scanning. Progressive scanning, (i.e., 1080p), scans all lines of a frame sequentially. Interlaced scanning, (i.e., 1080i), however, only scans the odd-numbered lines during a first field and the even-numbered lines during a second field. For interlaced scanning, the two interlaced fields compose one full frame.

At a typical frame/scan rate of 60Hz, progressive scanning yields 60 frames per second, while interlaced scanning only generates 30 frames per second.

In addition to the display and scanning formats, the color depth also affects the signaling rate. For a given display and scanning format, the time to scan a pixel is fixed. For color depths higher than 24-bit/pixel, more data bits must be transmitted within the same time frame, thus requiring an increase in data rate and TMDS clock. The factor by how much the TMDS clock must increase is given by the ratio of deep color mode (n-bit/pixel) to standard color mode (24-bit/pixel). Table 2 lists the various color depths and their corresponding multiplying factors.

Table 2. Color Depth Versus TMDS Clock

COLOR DEPTH		INCREASE IN TMDS CLOCK (multiplying factor)
BITS PER PIXEL	BITS PER SUB-PIXEL	
24	8	1.00
30	10	125
36	12	150
48	16	200

Distinguishing between the signaling rate of an entire HDMI link, (three TMDS channels = 1 pixel), and the signaling rate per TMDS channel, (per color component or sub-pixel) is required when claiming a certain signaling rate.

Keep in mind that the 8b/10b encoder increases the number of bits per color component by a factor of 1.25 (=10/8). Then the standard color depth of 24-bit/pixel at the transmitter input translates to 30-bit/pixel across the HDMI link, or 10-bit per sub-pixel across one TMDS channel.

Equation 1 calculates the data signaling rate by taking all variables into account, previously discussed in this article:

$$DSR = Y \bullet X \bullet f \bullet 10 \bullet M \quad (1)$$

With:

X = total number of lines per frame

Y = total number or pixels per line

f = frame rate in frames per second

10 = number of encoded bits per sub-pixel for 24-bit standard color depth

M = multiplying factor for deep color modes (see Table 2).

Applying Equation 1 to the video formats 1080i and 1080p yields the signaling rates and TMDS clock frequencies for the various color depths listed in Table 3.

Table 3. DSR and Clock Frequency Versus Color Depth

VIDEO FORMAT	X	Y	f	COLOR DEPTH	M	SIGNALING RATE/TMDS CHANNEL	TMDS-CLK
	[pixels/line]	[lines]	[frames/second]	[bit/pixel]		[Gbps]	[MHz]
1080i	2200	1125	30	24	1	0.74	74.25
				30	1.25	0.93	92.81
				36	1.5	1.11	111.4
				48	2	1.49	148.5
1080p			60	24	1	1.49	148.5
				30	1.25	1.86	185.6
				36	1.5	2.23	222.8
				48	2	2.97	297.0

Conclusion

The criterion whether or not the TMDS341A is compatible with HDMI 1.3 is its data signaling rate, which operates up to 2.25Gbps. Table 3 shows that the TMDS341A supports the 1080i format up to 48-bit color depth and supports the 1080p format up to 36-bit at 60fps.