TSW3XJ8XEVM

The TSW3XJ8XEVM is an evaluation module (EVM) designed to evaluate the DAC3XJ8X family of high-speed, JESD204B interface DACs (DAC37J82, DAC37J84, DAC38J82, DAC38J84) with the TRF3705 quadrature modulator and TRF3722 quadrature modulator with integrated RF synthesizer. The EVM includes an onboard clocking solution (LMK04828), full power solution, and easy-to-use software GUI and USB interface.

The TSW3XJ8XEVM is designed to work seamlessly with the TSW14J56EVM, Texas Instruments' JESD204B pattern generator card, through the High Speed Data Converter Pro (HSDCPro) software tool for high-speed data converter evaluation. The TSW3XJ8XEVM was also designed to work with many of the development kits from leading FPGA vendors that contain an FMC connector.

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1 Functional Description

The TSW3XJ8XEVM is intended for evaluation of the DAC3XJ8X family of high-speed, JESD204B interface DACs with the TRF3705 quadrature modulator and TRF3722 quadrature modulator with integrated RF synthesizer. The digital input signal to the DAC is provided from the FMC connector (J16) on up to eight 12.5-Gbps SerDes lanes using the JESD204B interface standard. The FMC connector is also used for the SYNC signal required to establish the JESD204B link and both device clock and SYSREF signal for the FPGA.

The RF output from the quadrature modulators of the TSW3XJ8X can be monitored through the RF_OUT SMA connectors. Channels A and B of the DAC3XJ8X drive the TRF3722 quadrature modulator with the integrated RF synthesizer. Channels C and D of the DAC3XJ8X drive the TRF3705 quadrature modulator using an external local oscillator (LO) source. Alternatively, the TRF3722 can be configured to drive the TRF3705 for a complete dual transmit solution.

The clocks for the DAC and FPGA are distributed using the LMK04828 ultra low-noise clock jitter cleaner for JESD204B applications. The LMK04828 can be setup in a variety of configurations including clock distribution mode and dual-loop jitter cleaning mode. In clock distribution mode, the desired DAC output rate is provided to the CLKIN connector and the LMK04828 divides and distributes the device clocks and SYSREF signals. In dual-loop mode, the CLKIN connector can be used to provide a reference to the LMK04828, but the clocks are generated on board using the LMK04828 PLL and onboard 122.88 MHz VCXO. The LMK04828 is also used to source the reference clock for the TRF3722's integrated RF synthesizer.

Figure 1 shows a simplified block diagram of the TSW3XJ8XEVM. See the schematics and bill of materials (BOM) located in the TSW3XJ8X Design Package (SLAC646) for detailed information. Table 1 contains descriptions of many of the connectors and jumpers available on the TSW3XJ8XEVM.

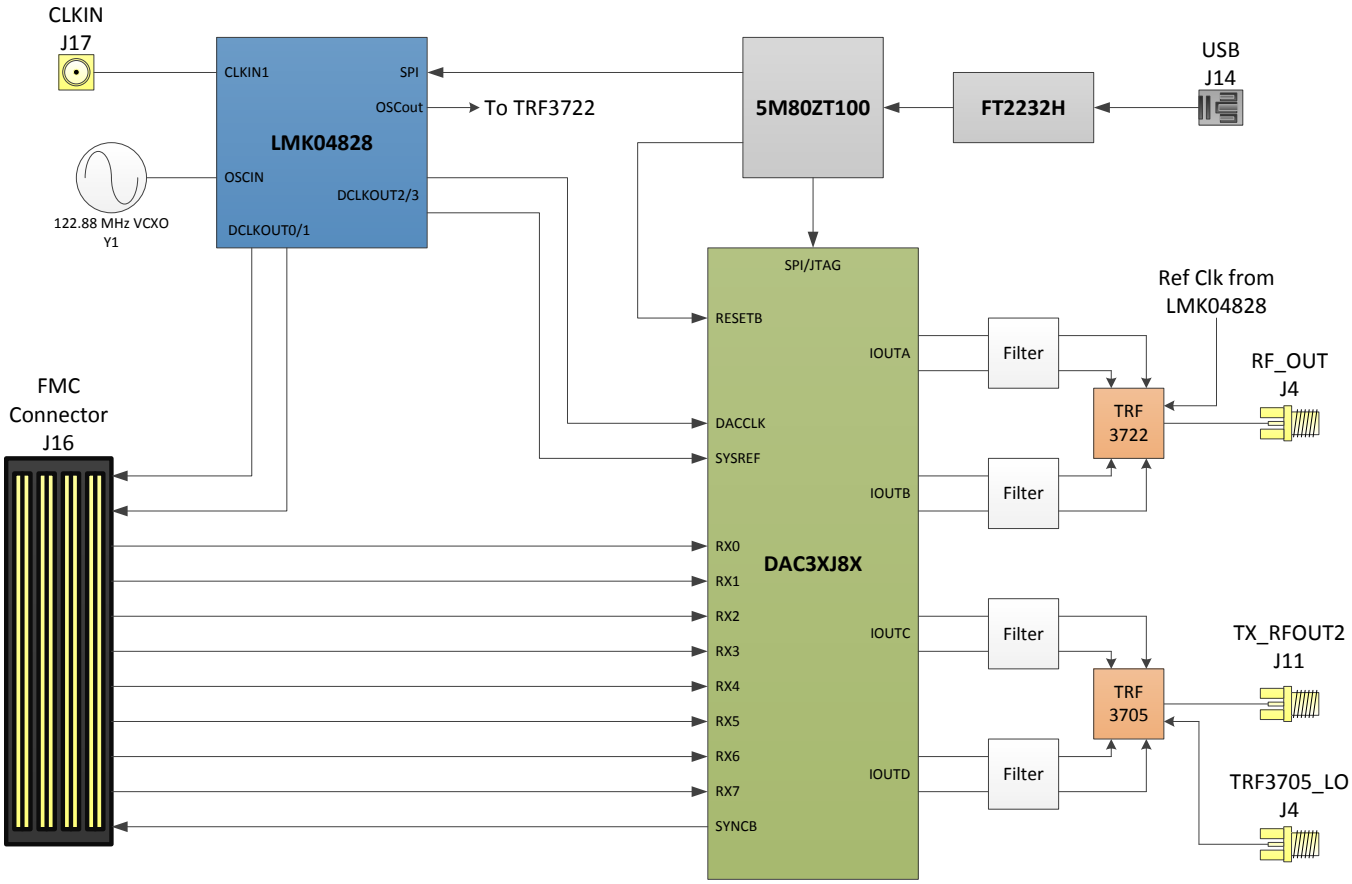


Figure 1. TSW3XJ8XEVM Simplified Block Diagram

Table 1. Input and Output Connectors and Jumper Descriptions

Connector/Jumper Label	Reference Designator	Purpose
RF_OUT	J4	TRF3722 RF output
TX_RFOUT2	J11	TRF3705 RF output
RF_LO_IN	J8	TRF3722 external LO input
TRF3705_LO	J2	TRF3705 external LO input
SPI_SELECTOR	JP3	Select SPI Signal Source. Short 1-2 for FMC connector, 2-3 for USB.
1.8V_SEL	JP7	Select 1.8-V supply source for CPLD. Short 1-2 for board supply, 2-3 for USB power.
3.3V_SEL	JP9	Select 3.3-V supply source for CPLD. Short 1-2 for board supply, 2-3 for USB power.
CLKIN	J17	Clock input for LMK04828. Default setup provides clock to CLKIN1, but can be configured to provide a clock to OSCIN pins.
XO_PWR	JP2	Short jumper to provide power to onboard 122.88 MHz VCXO for PLL mode of the LMK04828. If not using the VCXO, disconnect power to prevent unwanted spurs from showing up.
TXENABLE	JP1	Controls the TXENABLE pin of the DAC3XJ8X. Short 1-2 to enable transmission.
SLEEP	JP4	Controls the SLEEP pin of the DAC3XJ8X. Short 1-2 to put DAC to sleep.
TRF3722 PWR SAVE	JP10	Power down control for TRF3722. Short 1-2 to put TRF3722 to sleep.
TANK_SEL	JP6	VCO tank supply voltage selection for TRF3722. Default is 3.3 V but 5 V can be selected by moving this jumper to short 1-2.
PWR DOWN	JP5	TRF3705 power down control. Short 1-2 to put TRF3705 to sleep.
GAIN CNTL	JP8	TRF3705 gain control. Short 1-2 for "high gain" mode.
FMC_CONNECTOR	J16	Connection to TSW14J56 or FPGA development board
USB	J14	USB cable port
+5V_IN	J6	5-V power supply barrel jack

2 Schematics, Layout, and BOM

For the EVM schematics, layout, and BOM, please see the TSW3XJ8X Design Package (SLAC646).

3 Software Control

The TSW3XJ8XEVM is controlled through an easy-to-use graphical user interface (GUI) to provide access to the DAC3XJ8X, TRF3722, and LMK04828 SPI interfaces.

3.1 Installation Instructions

Use the following instructions to install the TSW3XJ8X GUI:

1. The software can be downloaded from the TSW38J84EVM product page on www.ti.com. Find the page by searching for TSW38J84EVM.
2. Extract the files from the zip file named *TSW3XJ8X GUI vXpY* installer.zip where “XpY” represents the version number.
3. Run *setup.exe* and follow the installation prompts.
4. Start the GUI by going to **Start Menu → All Programs → Texas Instruments DACs → TSW3XJ8X GUI.**
5. Connect the EVM board to the computer with the supplied USB cable. A prompt to install the USB drivers is shown after the initial connection.
   - Microsoft® Windows® XP: If Windows XP does not automatically install the drivers, follow the prompts on the screen to do so. Do not let Windows XP search Microsoft update for the drivers, but do let Windows XP install the drivers automatically.
   - Windows 7: After installing the GUI, Windows 7 should automatically install the drivers for the ADS42LBx9EVM with no user input.

3.2 Software Operation

The following sections detail the operation of the TSW3XJ8XEVM GUI.

3.2.1 Quick Start Page

The *Quick Start* page should be the starting point for all TSW3XJ8XEVM evaluation. Simply follow the steps to set the clocking mode, data rate, number of SerDes lanes, interpolation and TRF3722 LO frequency. Before moving forward, the FPGA (TSW14J56 or FPGA development kit) should be programmed and waiting to establish the JESD204B link. After configuring the settings and FPGA, verify the correct settings in the *DAC Calculated Results* and *LO Calculated Results* sections. Click *1. Program LMK04828 and DAC3XJ8X* to program the registers of both the DAC and clock chip. Next, program the TRF3722 by clicking *2. Program TRF3722*. Once the DAC3XJ8X and TRF3722 are programmed, clicking the *3. Reset DAC JESD Core* button resets the DAC's JESD204B core. Next, trigger the SYSREF signal using the *4. Trigger LMK04828 SYSREF* button. If the FPGA is configured correctly then the DAC should be outputting the digital signal that is sent to it. Figure 2 shows the Quick Start page of the TSW3XJ8X GUI. See the *Basic Test Setup* section of this user's guide for an example setup.

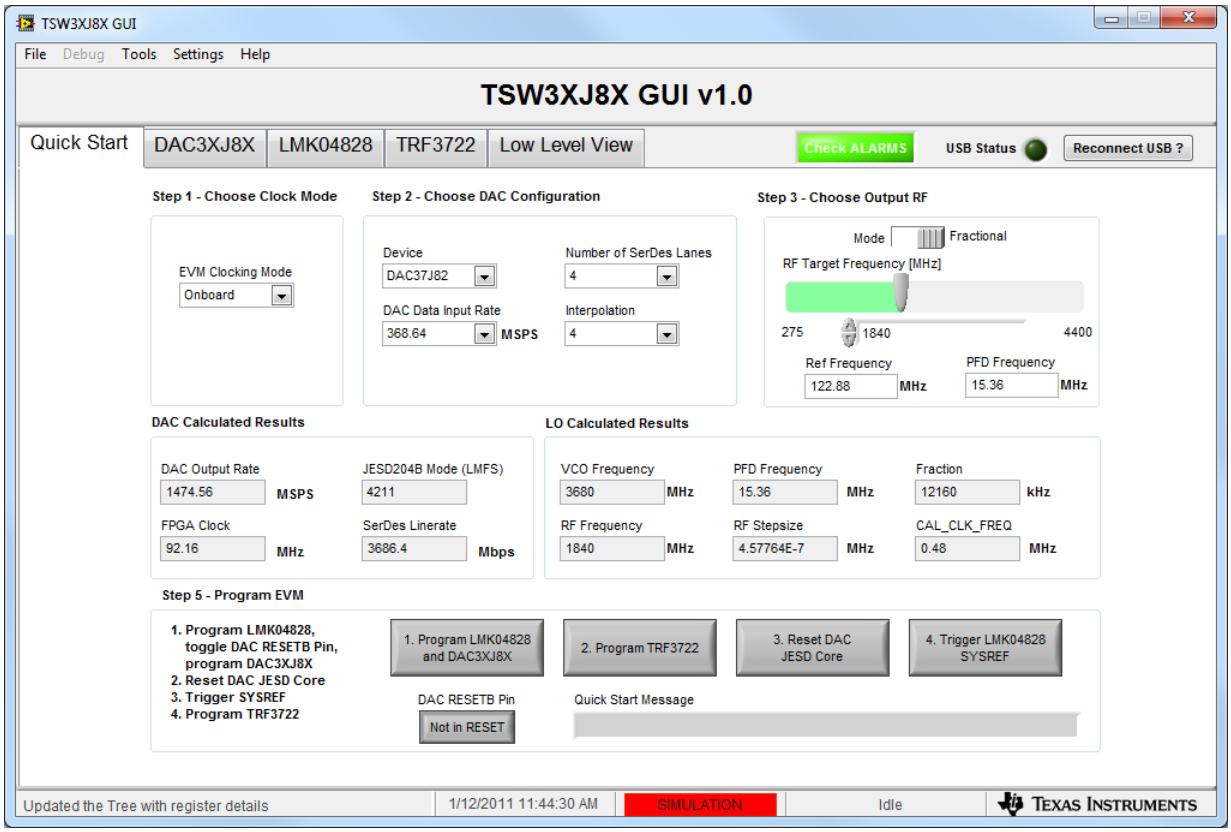


Figure 2. Quick Start Page

3.2.2 DAC3XJ8X

After using the Quick Start page to configure the EVM, the *DAC3XJ8X Controls* tab can be used to access the individual controls of the DAC3XJ8X. Figure 3 shows the Overview page of the *DAC3XJ8X Controls* tab. Table 2 describes each page within the *DAC3XJ8X Controls* tab. The various digital features of the DAC3XJ8X are accessed on the *Dig Block 1* and *Dig Block 2* pages.

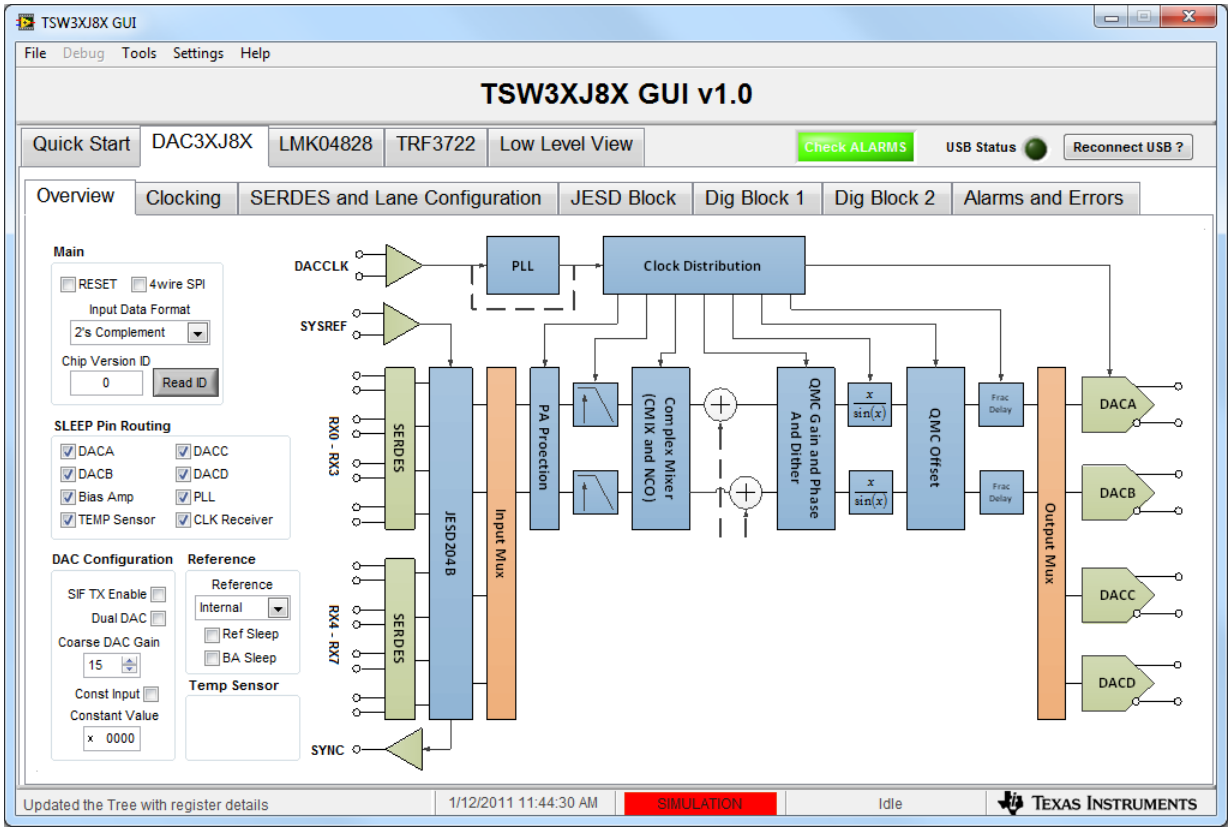


Figure 3. DAC3XJ8X Controls Tab

Table 2. DAC3XJ8X Controls Page Descriptions

DAC3XJ8X Controls Page	Description
Overview	The Overview page shows a block diagram of the TSW3XJ8X and allows access to the input data format, SLEEP pin routing, coarse DAC gain and reference settings.
Clocking	This page shows the basic clocking instruction of the TSW3XJ8X. The Quick Start page sets this up automatically to not use the DAC PLL. The DAC PLL can be enabled using this page. The SERDES block clocking is also configured on this page.
SERDES and Lane Configuration	This page is used to setup the SERDES receivers including enabling lanes, lane routing, and lane IDs. It is not recommended to touch any controls in the *SERDES Configuration* section, since these will be configured using the Quick Start programming.
JESD Block	The JESD Block page is used to configure the JESD core of the TSW3XJ8X. This page will be programmed automatically using the Quick Start page. The page contains the JESD204B link configuration including L, M, F, K, S, RBD, N, N', HD, and so forth.
Dig Block 1	Dig Block 1 allows access to some of the digital features of the TSW3XJ8X including the coarse mixer and NCO, digital block input mux, interpolation, PA protection, and quadrature modulator correction (QMC).
Dig Block 2	Dig Block 1 allows access to some of the digital features of the TSW3XJ8X including the large and small fractional delay blocks, QMC offset, digital dither, and digital block output mux.
Alarms and Errors	The various alarms in the TSW3XJ8X can be viewed on this page. Clicking *Clear All Errors and Read* clears the current DAC errors and checks for new errors. Once the errors have been cleared, the *Read Errors* button can be used to check for new errors during operation.

3.2.3 LMK04828

The *LMK04828 Controls* tab of the TSW3XJ8X GUI allows access to the LMK04828 configuration. Note that the LMK04828 is automatically programmed to the desired configuration using the Quick Start page. Figure 4 shows a screenshot of the LMK04828 tab and Table 3 provides descriptions of the pages within this tab.

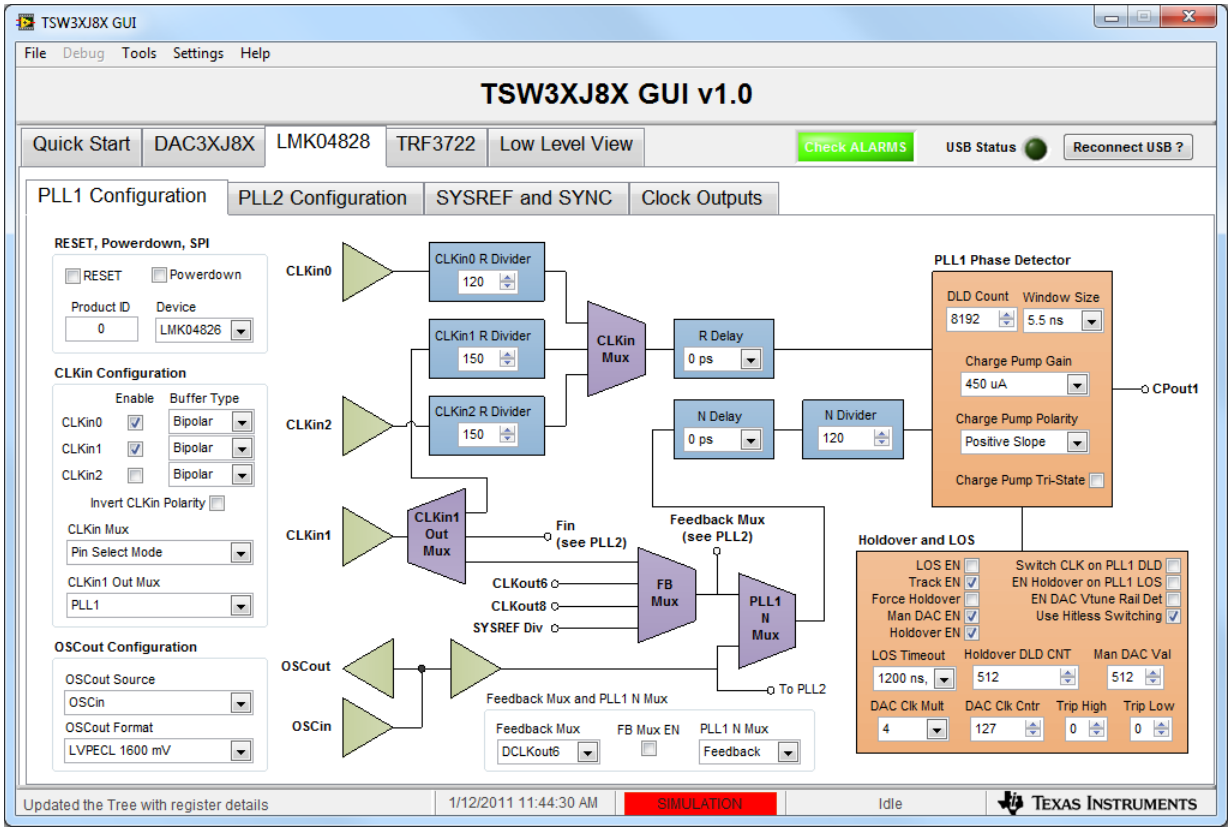


Figure 4. LMK04828 Controls Tab

Table 3. LMK04828 Controls Page Descriptions

LMK04828 Controls Page	Description
PLL1 Configuration	This page shows the block diagram for the first PLL of the LMK04828. This PLL is used to lock a reference provided to the LMK04828 using the CLKIN SMA connector to the onboard 122.88 MHz VCXO. The PLL can be bypassed by setting the "CLKin1 Out Mux" control to "Fin".
PLL2 Configuration	This page shows the block diagram for the second PLL of the LMK04828. The second PLL is used to lock the internal VCO of the LMK04828 to the onboard 122.88 MHz VCXO. PLL2 can be bypassed by setting the "VCO Mux" control to "External VCO". In combination with bypassing PLL1, the LMK04828 can be setup for clock distribution mode.
SYSREF and SYNC	This page allows access to the SYSREF generator block. It also contains the controls required to sync the LMK04828 clock dividers. The dynamic and analog delays for the clock output groups can be accessed from this page.
Clock Outputs	The clock outputs can be configured using this page. Each clock group is labeled with the appropriate signal names for clarity. For use with the TSW14J56, only CLKout0 and 1 and CLKout 2 and 3 are required.

3.2.4 TRF3722

The TRF3722 tab can be used to access the individual controls of the TRF3722. It is recommended to start with the Quick Start tab when working with the TRF3722 and then modifications can be made from the default configuration. Figure 5 shows a screenshot of the TRF3722 tab.

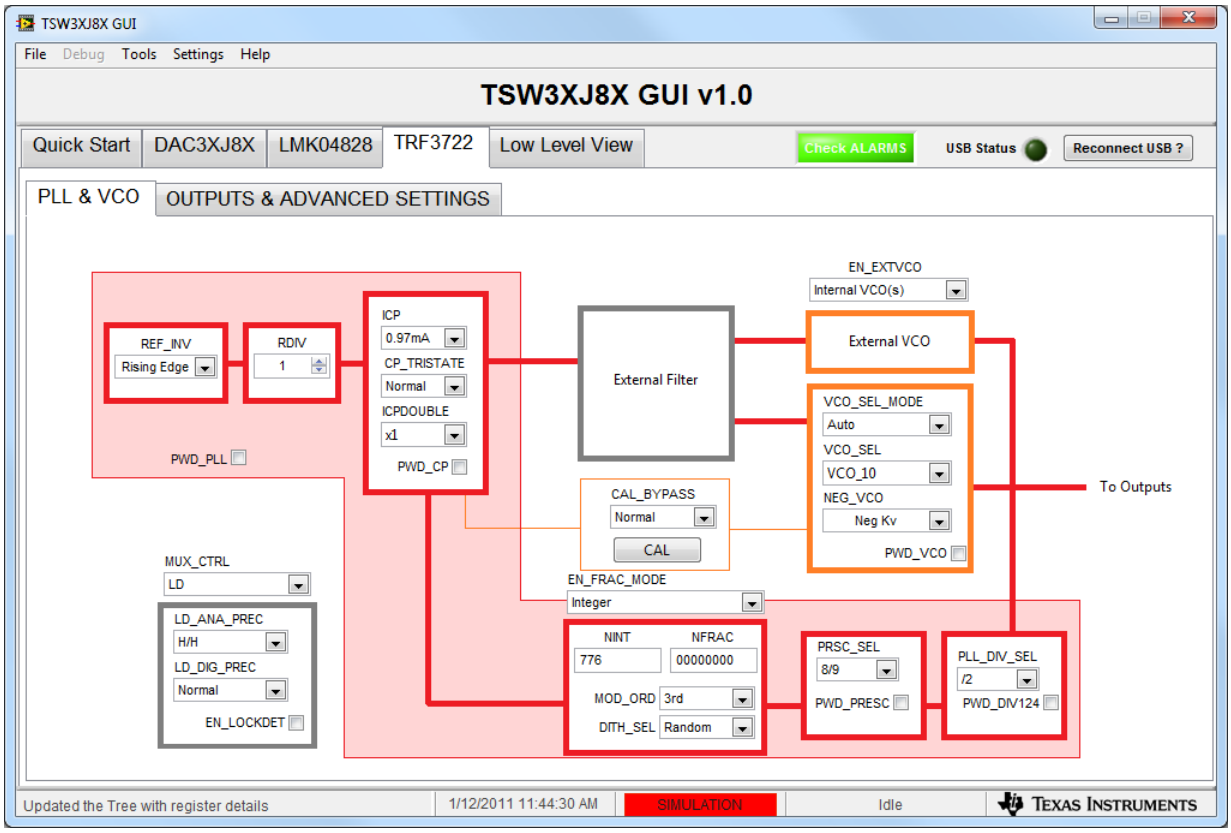


Figure 5. TRF3722 Tab

3.2.5 Low Level View

The *Low Level View* tab can be used to access the various registers of the LMK04828, DAC3XJ8X, and TRF3722. High-level control of most of these registers is accessible in the DAC3XJ8X, LMK04828, and TRF3722 tabs. This page also provides the option of saving a register configuration or loading a previously saved configuration. Figure 6 shows a screenshot of the *Low Level View* tab.

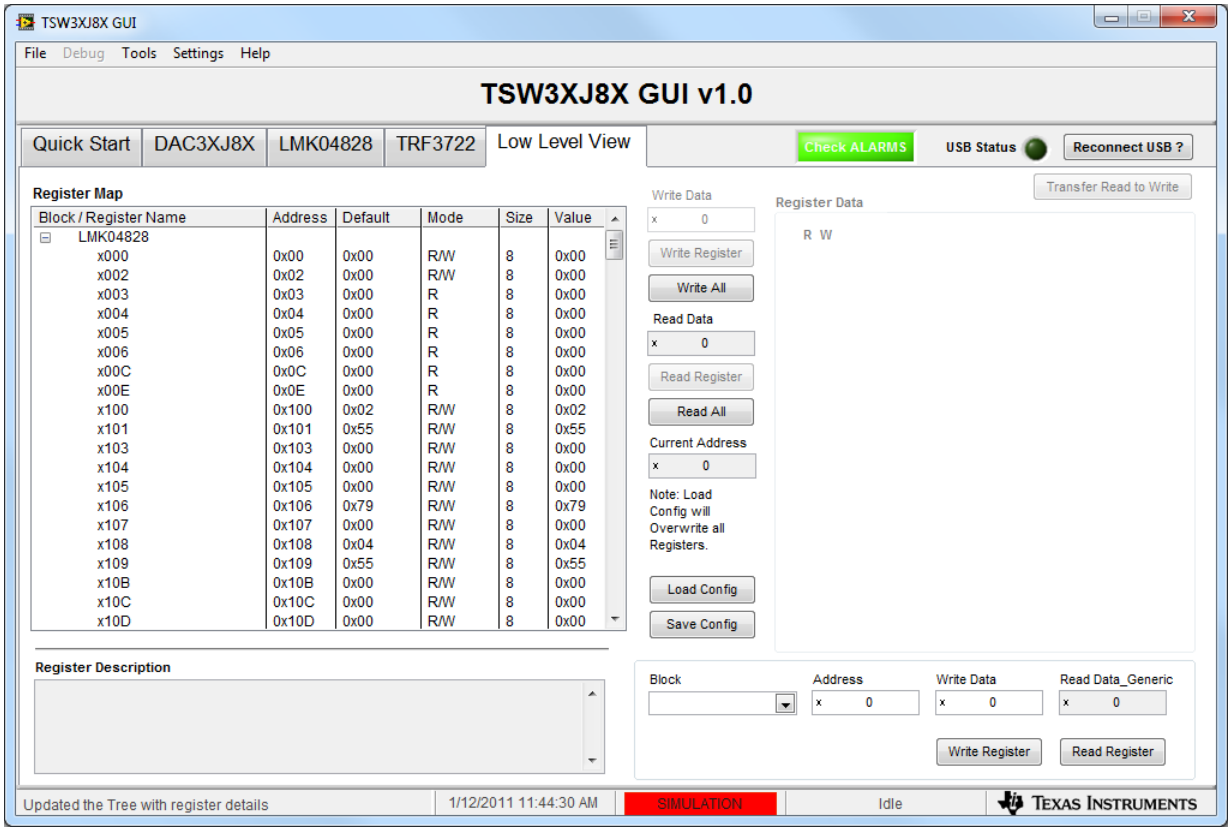


Figure 6. Low Level View Tab

4 Basic Test Setup

4.1 Test Block Diagram

Figure 7 illustrates the test setup block diagram.

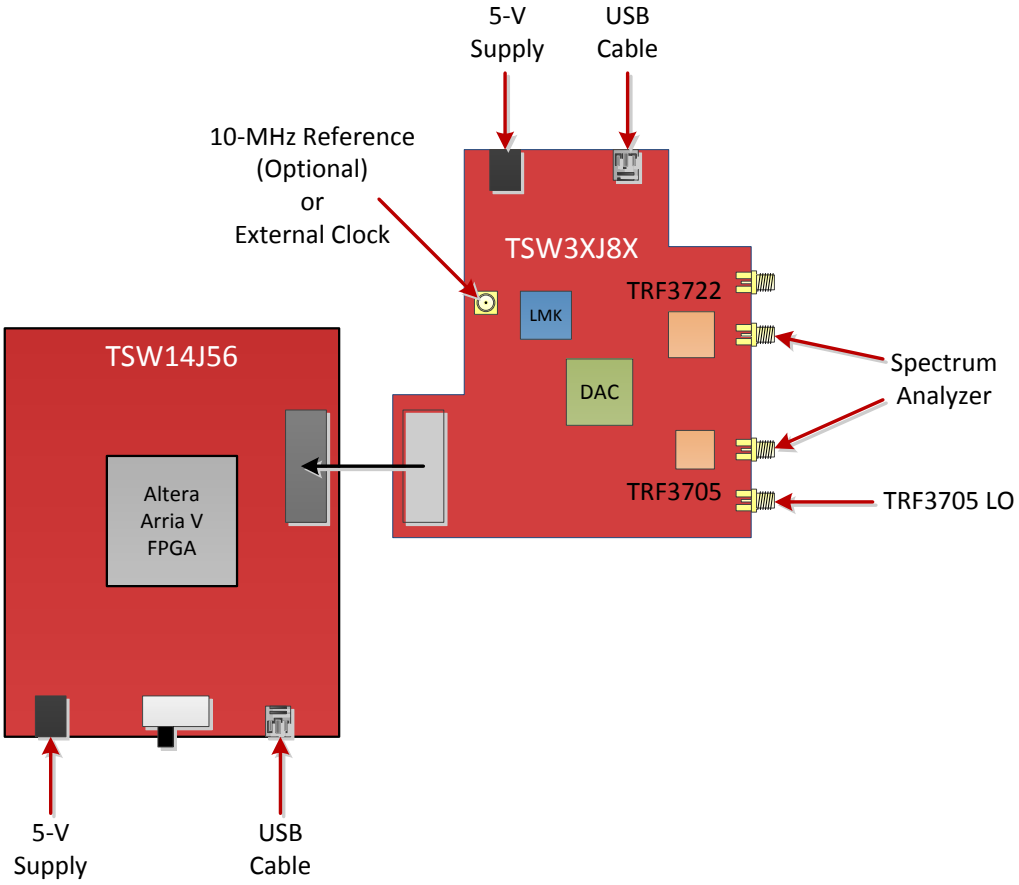


Figure 7. Test Setup

4.2 TSW14J56 Setup

Install High Speed Data Converter Pro (HSDCPro) from the TI website (www.ti.com/tool/dataconverterpro-sw). See the HSDCPro user's guide (SLWU087) for software installation and use information. See the TSW14J56 user's guide (SLWU086) for detailed hardware information.

4.3 TSW3XJ8X Quick-Start Procedure

The following sections provide quick-start procedures for the TSW14J56, TSW3XJ8XEVM, HSDCPro, and the TSW3XJ8X GUI:

4.3.1 TSW14J56

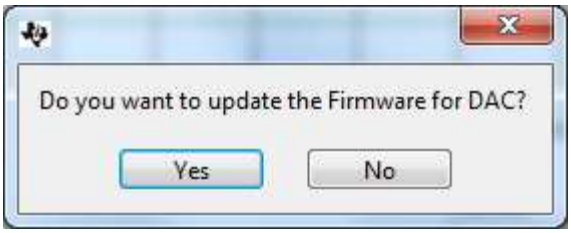
1. Connect TSW14J56 and TSW3XJ8XEVM via the FMC connector.
2. Connect a 5-V power supply to connector J11 (+5V IN).
3. Connect a USB cable to the USB connector (J9).
4. Flip the power switch (SW6) to the “ON” position.

4.3.2 TSW3XJ8XEVM

1. Connect a 5-V power supply to connector J6 (MAIN PWR) on the bottom of the board.
2. Connect a USB cable to the USB connector (J14).
3. Provide a 6-dBm, 10-MHz, reference clock to J17 (CLK_IN). This is optional if synchronization with other test equipment is not required.
4. For TRF3722 evaluation, connect a spectrum analyzer to the RF_OUT SMA connector. For TRF3705 evaluation, connect a spectrum analyzer to the TX_RFOUT2 SMA connector.
5. For TRF3705 evaluation, connect an LO source to the TRF3705_LO SMA connector at 1840 MHz and a power of 0 dBm.

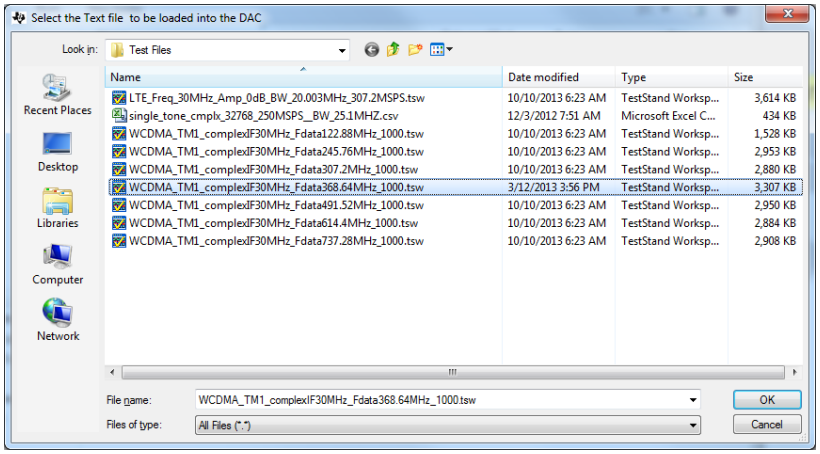
4.3.3 High Speed Data Converter Pro (HSDCPro)

1. Open High Speed Data Converter Pro (v2.4 or later) by going to *Start Menu → All Programs → Texas Instruments → High Speed Data Converter Pro*.
2. Select the *DAC* tab.
3. Use the *Select DAC* drop down menu at the top left corner to select the desired DAC and configuration:
   - DAC3XJ82_LMF_222 for DAC37J82 or DAC38J82
   - DAC3XJ84_LMF_442 for DAC37J84 or DAC38J84
4. When prompted to update the firmware for the DAC, click “Yes” as shown in the following image, and wait for the firmware to download to the TSW14J56.



5. Enter “368.64M” in the *Data Rate (SPS)* field.
6. Choose “2’s Complement” in the *DAC Option* drop down menu.

7. Click "Load File to transfer into TSW1400" and select "WCDMA_TM1_complexIF30MHz_Fdata368.64MHz_1000.tsw" in the "Test Files" folder of the HSDCPro installation directory as illustrated in the following image.



8. Do not send the data until the TSW3XJ8X EVM is configured. Complete the TSW3XJ8X GUI configuration in the next section before clicking the *Send* button.

4.3.4 TSW3XJ8X GUI

1. Open the TSW3XJ8X GUI by going to **Start Menu → All Programs → Texas Instruments DACs → TSW3XJ8X GUI**.
2. Verify that the green USB Status indicator is lit. If it is not, click the *Reconnect USB* button and check the *USB Status* indicator again.
3. On the *Quick Start* tab, setup the controls as shown in Figure 8. For the dual-channel DAC3XJ82 choose "2" for the number of SerDes lanes. This configures the TSW3XJ8X EVM to use clocks generated onboard by the LMK04828 and 122.88 MHz VCXO. The DAC will be programmed for 1 lane per DAC, 4x interpolation, and an input data rate of 368.64 MSPS. The TRF3722 will be configured for an LO frequency of 1840 MHz.

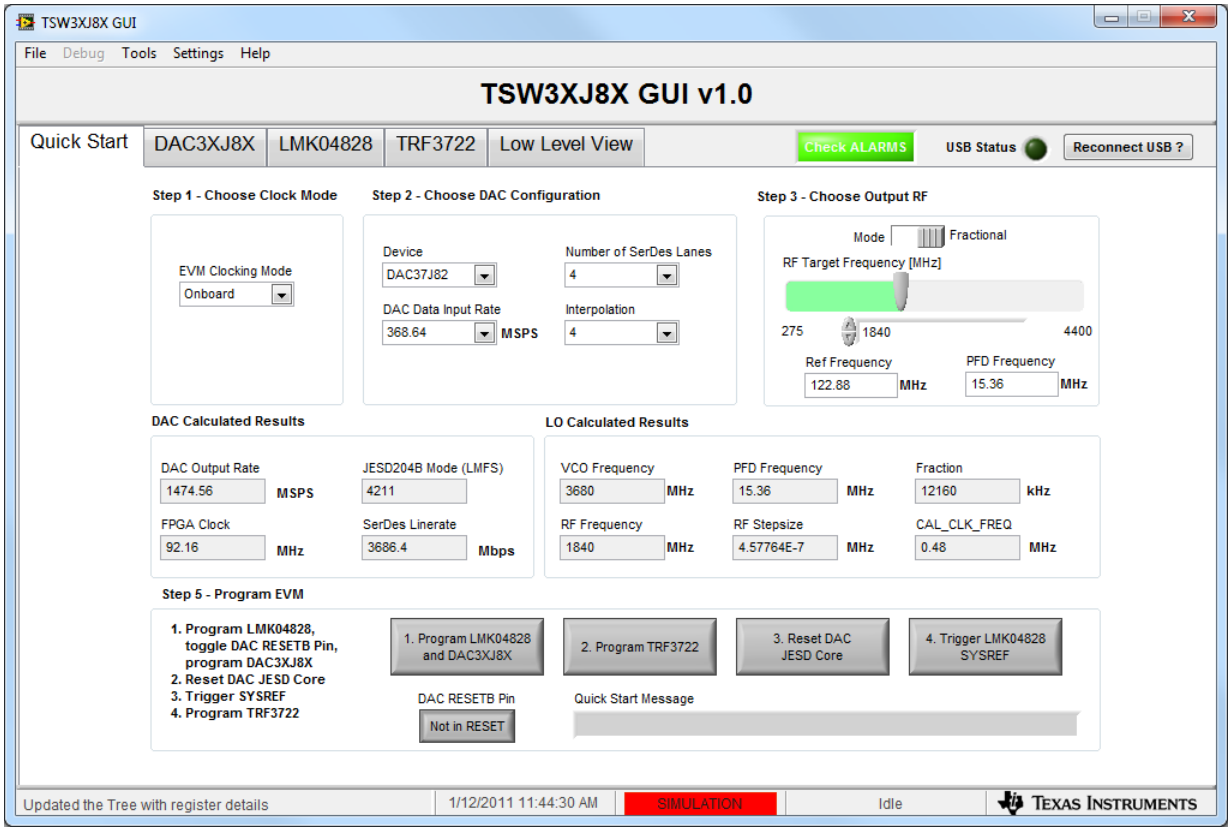


Figure 8. TSW3XJ8X GUI Configuration for DAC37J84 and DAC38J84

4. Click the *1. Program LMK04828 and DAC3XJ8X* button to program the EVM. Wait until programming is completed.
5. Verify that the LMK04828 PLLs are locked by checking that the “PLL1 LOCKED” and “PLL2 LOCKED” LEDs are lit. The “PLL1 LOCKED” LED will only be lit if a 10-MHz reference clock is connected to the CLK_IN SMA connector (J17), which is not required. If these LEDs are not lit, check the hardware setup and make sure that JP2 (XO PWR) has a jumper installed. Then try to reprogram the TSW3XJ8X EVM.
6. Once correct clock operation is verified, switch back to the HSDCPro GUI and click the *Send* button to send the pattern to the TSW14J56.
7. Click the *2. Program TRF3722* button to program the TRF3722 for the chosen LO frequency.
8. Click the *3. Reset DAC JESD Core* button to reset the DAC3XJ8X JESD204B core.
9. Click the *4. Trigger LMK04828 SYSREF* button to trigger the SYSREF signal

10. You should now see a WCDMA signal centered at 1870 MHz on the spectrum analyzer, as shown in Figure 9.

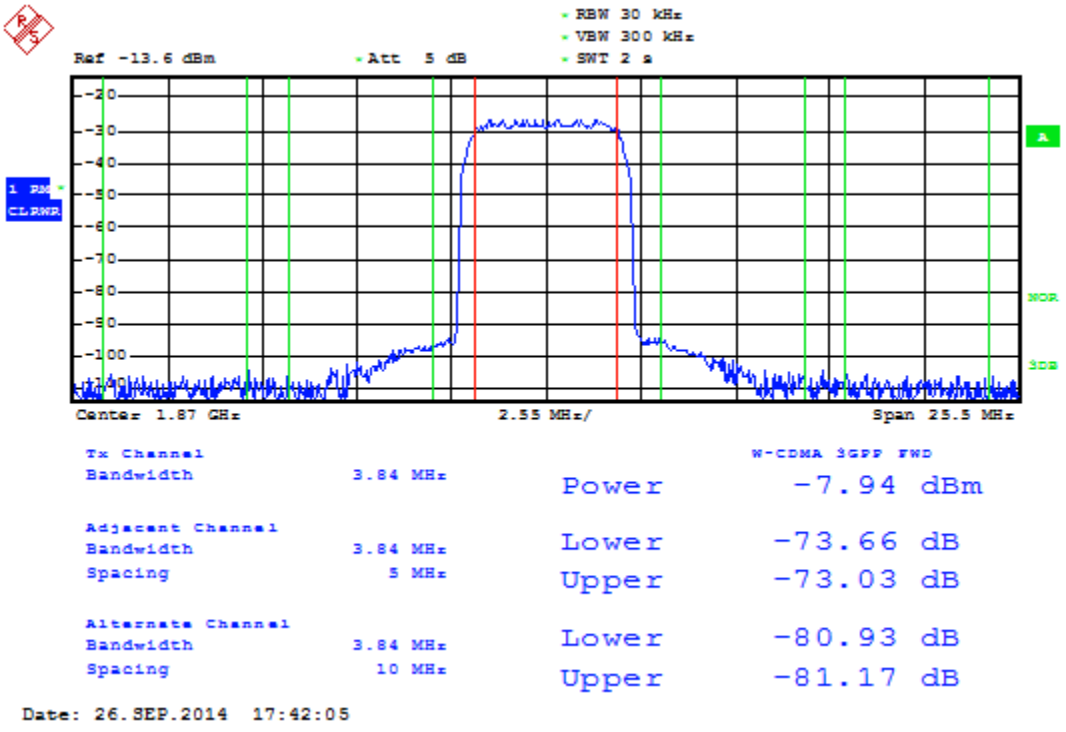


Figure 9. TRF3722 Quick Start Result

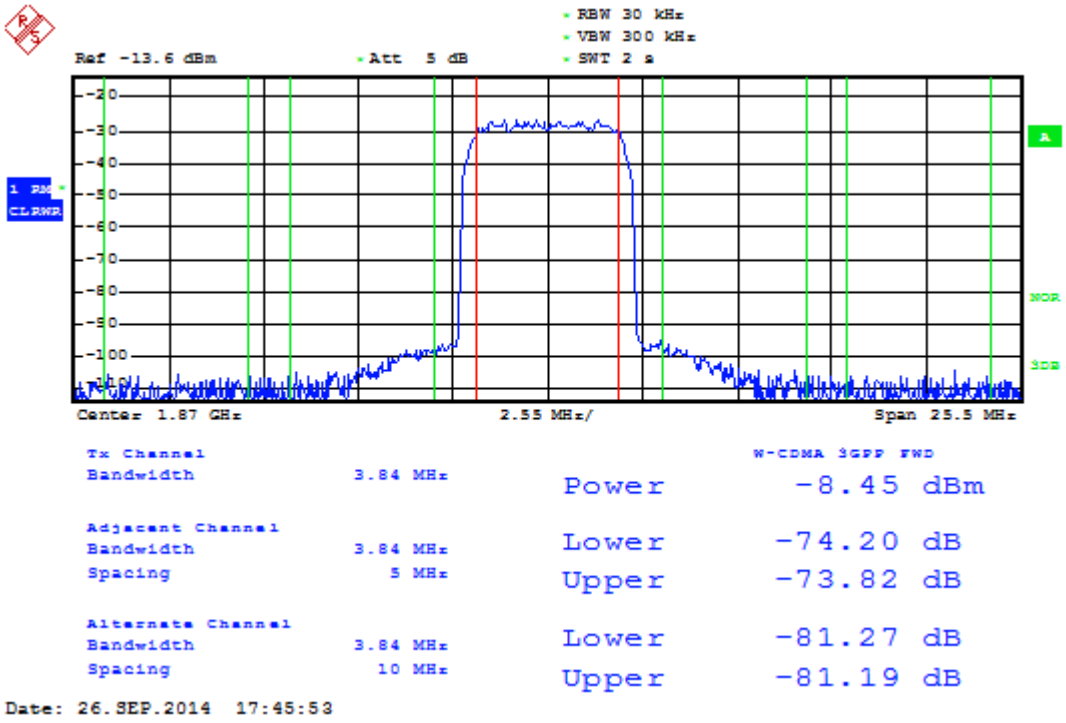


Figure 10. TRF3705 Quick Start Result

5 Clock Configuration

This section includes TSW3XJ8XEVM clocking options, and LMK04828 configuration options.

5.1 TSW3XJ8XEVM Clocking Options

The TSW3XJ8XEVM allows three clocking options for the DAC3XJ8X:

1. *Clocks Generated or Distributed by LMK04828*
   The DAC clocks and FMC clocks come from the onboard LMK04828 clock chip. This is the default option. The device clock for the DAC is DCLKOUT2 and SYSREF is SDCLKOUT3. There are three pairs of clocks sent to the FMC connector meant for the FPGA or other use. The device clock and SYSREF pairs sent to the FMC connector are as follows: DCLKOUT0 and SDCLKOUT1, DCLKOUT6 and SDCLKOUT7, and DCLKOUT8 and SDCLKOUT9. Any of these pairs can be configured as a device clock and SYSREF pair or as two device clocks of the same frequency. Only one clock is needed for use with the TSW14J56 which is DCLKOUT0 and SDCLKOUT1 and the other two FMC clock pairs can be powered off.
2. *FMC Port Provides Clocks to DAC3XJ8X*
   The DAC device clock and SYSREF are provided through the FMC port on the signals FMC_DACCLK_P/N and FMC_SYSREF_P/N. For this option, R16, R18, R4, and R7 must be uninstalled and R187, R188, R189, and R190 need to be installed. If a common-mode voltage of 0.5 V cannot be guaranteed on these signals then it is recommended to install 0.01-µF capacitors instead of 0-Ω resistors for these components. The LMK04828 can still be used to provide clocks to the FMC connector, but the DACCLK and FPGA clocks should share the same time base for proper operation. If the LMK04828 is not used then it should be powered down.
3. *DAC3XJ8X Clocks are Provided through SMP Connectors*
   The DAC device clock and SYSREF are provided through the SMP connectors (J1, J3, J5, J7). For this option, R16, R18, R4, and R7 need to be uninstalled and C12, C16, C1, and C8 need to be installed. DC coupling of these signals is only recommended if a common-mode voltage of 0.5 V can be guaranteed on these signals, in which case, 0-Ω resistors can be installed instead. The LMK04828 can still be used to provide clocks to the FMC connector, but the DACCLK and FPGA clocks should share the same time base for proper operation. If the LMK04828 is not used then it should be powered down.

5.2 LMK04828 Configuration Options

The following list describes three options for using the LMK04828 to provide clocks to the DAC3XJ8X and FMC connector:

1. *Clock Distributor*
   The LMK04828 is used as a clock distributor. This mode is selected by choosing "External" for the EVM Clocking Mode on the Quick Start tab of the GUI. In this case, the fastest required clock, or an integer multiple of it, should be provided to the CLKIN SMA connector (J17) with a maximum frequency of 2.5 GHz. The LMK04828 is used to divide down to the desired clock frequencies. Leave JP2 open to turn off the onboard VCXO to avoid crosstalk.
2. *Clock Generator using Onboard VCXO*
   The LMK04828 is used as a clock generator using the onboard 122.88 MHz VCXO. This mode is selected by choosing "Onboard" for the EVM Clocking Mode on the Quick Start tab of the GUI. JP2 must be shorted to turn on the onboard VCXO. The internal PLLs of the LMK04828 can be used with the onboard VCXO to generate the desired frequencies. The possible LMK04828 VCO frequencies are 2457.6 MHz and 2949.12 MHz with the possible clock outputs being an integer division of those, with a maximum division of 32. The first PLL of the LMK04828 can be used to lock to an external reference provided to the CLKIN SMA connector (J17), but it is not required.
3. *Clock Generator using External Reference*
   The LMK04828 is used a clock generator using an external reference provided to the CLKIN SMA connector (J17). For this option, R177, C206, and C121 should be uninstalled and R23, R24, and C92 should be installed. JP2 can be left open to turn off the onboard VCXO to avoid crosstalk. This option allows a wider frequency range of generated clock frequencies only limited by the VCO frequency ranges of the LMK04828 (see LMK04828 datasheet (SNAS605) for VCO frequency ranges). The possible clock outputs are an integer division of the VCO frequency with a maximum division of 32. PLL1 of the LMK04828 is bypassed in this mode

6 Modulator Configuration

The interface between the DAC3XJ8X and both modulators (TRF3722 and TRF3705) uses 50-Ω pull-down resistors at each DAC output and a second 50-Ω pull-down resistor at each modulator input. The total resistance to ground is 25 Ω and sets the DAC and modulator common mode voltage to approximately 312.5 mV.

A low-pass filter module from Soshin Electric Company performs low-pass filtering of the DAC3XJ8X output to remove high-frequency DAC images. The low-pass filter for the TSW37J82EVM and TSW37J84EVM is set to 400 MHz. The low pass filter for the TSW38J82EVM and TSW38J84EVM is set to 650 MHz. These filters are marked as FLT1, FLT2, FLT3, and FLT4 in the schematic and BOM. There are placeholders for a custom LC filter in which case the filter modules will need to be removed and resistor jumpers will need to be placed across the module pads.

The TRF3722 generates its own LO frequency using its internal RF synthesizer. The reference clock for the synthesizer is sourced from the OSCout port of the LMK04828. By default, the TRF3705 expects an external LO source brought into the TRF3705_LO SMA connector. The LO source should be sourced from a high quality signal generator or an external RF synthesizer. The TSW3XJ8XEVM can be modified so that the TRF3722 sources an LO to the TRF3705. To make this change, remove R12 and C417 and install R219 and R11. The unadjusted sideband suppression will be heavily effected by harmonics of the LO, so filtering should be used between the TRF3722 and TRF3705 to achieve datasheet performance. Some placeholders have been included to allow insertion of a filter in the LO path.

7 References

1. High Speed Data Converter Pro software (SLWC107).
2. *High Speed Data Converter Pro User's Guide* (SLWU087).
3. *TSW14J56 User's Guide* (SLWU086).
4. TSW3XJ8X Design Package (SLACxxx).
5. TSW3XJ8XEVM Software (SLACxxx).
6. DAC38J84 data sheet (SLASE17)
7. LMK04828 data sheet (SNAS605)
8. TRF3722 data sheet (SLWS245)
9. TRF3705 data sheet (SLWS223)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (December 2014) to B Revision	Page
• Changed R185 to R23 and R186 to R24 in option 3 of the *LMK04828 Configuration Options* section.	15

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS AND CONDITIONS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT MADE, CONCEIVED OR ACQUIRED PRIOR TO OR AFTER DELIVERY OF THE EVM.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS ANDCONDITIONS OR THE USE OF THE EVMS PROVIDED HEREUNDER, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY WARRANTY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS AND CONDITIONS, OR ANY USE OF ANY TI EVM PROVIDED HEREUNDER, EXCEED THE TOTAL AMOUNT PAID TO TI FOR THE PARTICULAR UNITS SOLD UNDER THESE TERMS AND CONDITIONS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM AGAINST THE PARTICULAR UNITS SOLD TO USER UNDER THESE TERMS AND CONDITIONS SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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