

Application Report SLAA253–June 2005

Using the Programmable Gain Amplifier Function in TSC210x/AIC26/AIC28/DAC26 Devices

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ABSTRACT

TI's touch screen and audio codec/DAC devices, such as TSC2100, TSC2101, TSC2102, TLV320AIC26 (AIC26), TLV320AIC28, and TLC320DAC26, have one or more audio-band programmable gain amplifiers (PGA) in their input circuitry. This application report describes how to implement this PGA function using the TLV320DAC26 as an example.

The Texas Instruments touch screen and audio codec/DAC devices, such as TSC2100, TSC2101, TSC2102, TLV320AIC26 (AIC26), TLV320AIC28, and TLC320DAC26, have one or more audio-band programmable gain amplifiers (PGA) in their input circuitry. The input signal through the PGA can be mixed with the digital-to-analog converter (DAC) results or can be directly fed to the device's output drivers/amplifiers; the latter can be seen as a separate PGA.

Consider the TLV320DAC26 (DAC26) as an example, and refer to Figure 1, the DAC26 functional block diagram. In this diagram, the PGA-related blocks are enclosed in yellow boxes. The features of the DAC26 PGA include gain ranges from –35.5 dB to 12 dB in 0.5-dB steps with soft-stepping logic. The gain is programmable using a standard SPI bus; input can be fed into the PGA through the MICIN or AUX pin and with single-ended mode; output can drive a 8- Ω /325-mW speaker or headphone. Power supplies range from 2.7-V to 3.6-V, analog and from 1.1-V to 3.6-V, digital. See the TLV320DAC26 data sheet (SLAS428) for details of the audio input/output features.

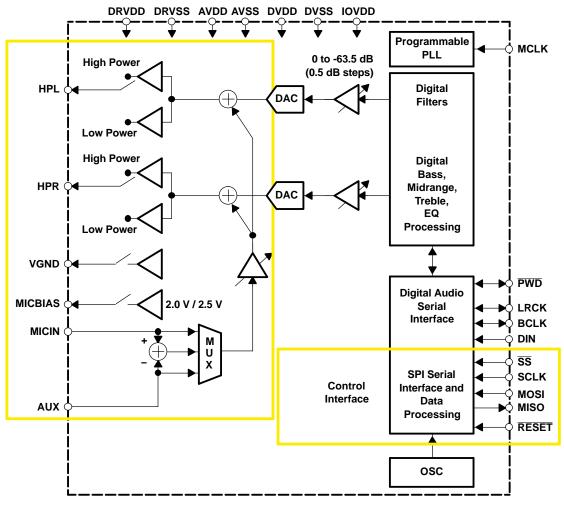


Figure 1. DAC26 Function Block Diagram

The following steps describe the physical connections and setups for using the separate PGA function, with the DAC26 EVM as the tool.

Connections:

- 1. Connect a single-ended audio input signal to the DAC26 MICIN or AUX pin.
- 2. Connect an audio output device to the HPL and/or HPR pins (the other end of the connection can be to VGND if in capacitorless mode or to the analog ground if in capacitor-coupling mode).

DAC26 Control Registers' Settings:

1. Start the DAC26EVM software on your PC, and the graphic user interface (GUI) shown in Figure 2 appears.



Register Reading	DAC Configuration	DAC Output Filters
Image: Section and the section of the secti	Read DAC Registers Read Audio Boost Regs Clear	
	SW Reset	

Figure 2. DAC26 EVM GUI With Page2 Registers Read

- 2. As an example, to connect the AUX to the analog sidetone PGA, set the D13–D12 of Page2/Reg00h to 01b.
- 3. To power up the PGA, set the D13 of Page2/Reg05h to 0b (and if in the capacitorless output mode, also power up the VGND).
- 4. To unmute the PGA, set the D15 of Page2/Reg03h to 0b.

The preceding settings are reflected in the Page2 registers' contents shown in Figure 2. Inside the *Register Reading* box, the right column is the register content, and the left column identifies the register, where the 0 to 6 lines correspond to Page2/Reg00h to 06h and the 7 to 10 lines correspond to Page2/Reg1Bh to 1Eh. Note the settings in registers 00h, 03h, and 05h.

Figure 3 displays the audio input and output signals of the PGA where channel 1 (Ch1) is the input signal, and channel 2 (Ch2) and channel 3 (Ch3) are the outputs from the PGA (HPL and HPR pins of DAC26). In Figure 3-a to Figure 3-d, the PGA gain was set to 9.5 dB, 3 dB, 0 dB, and –9.5 dB, respectively.

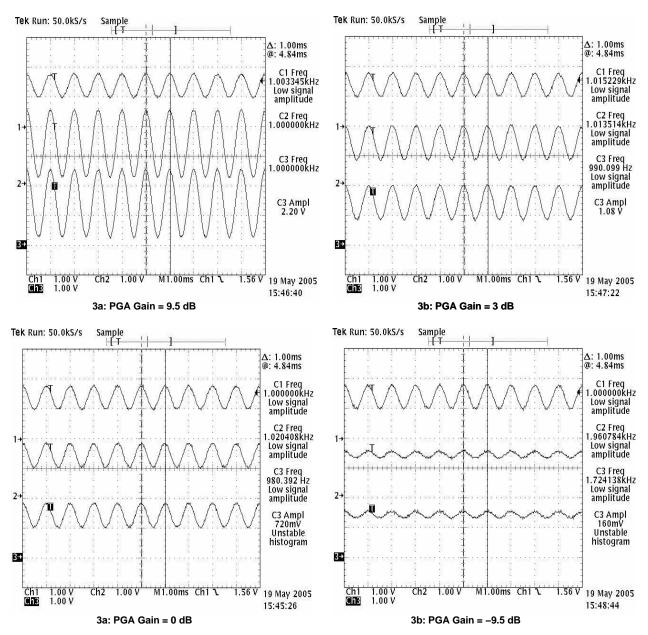


Figure 3. PGA Gains

The PGA function with the same or similar features can also be obtained through TSC2100, TSC2101, TSC2102, TLV320AIC26 (AIC26), and TLC320AIC28 (AIC28), depending on the input circuitry and the output drivers.

Example: Using the CP_IN PGA and output to receiver driver OUT32P/OUT32N of TSC2101 (AIC28). To have the CP_IN route to the OUT32P/N, no ADC, DAC, PLL, or I2S mode needs to be powered or set, because only the bypass route from the CP_IN pin to the OUT32P/N pins are involved.

Therefore, the only control registers that need to be set up for this channel to work are described as follows:

- 1. Keep all registers on page 2 as the power-up/reset default.
- 2. Set Page2/Reg20h to 8200h (to select SPK1 at differential and route CP_IN to the OUT32P/N).
- 3. Set Page2/Reg1Fh to 457Ch (to power up the CP_IN PGA and set it at 0 dB).
- 4. Set Page2/Reg05h to EFFCh (to power up the OUT32 driver).

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5. Set Page2/Reg20h to 8202h (to unmute the OUT32 driver).

In the following illustrations, a single-ended sine wave was input to the CP_IN pin (and another end was wired to the analog ground). In Figure 4, the CELL_IN PGA was set to 0 dB, to –6 dB in Figure 5, and to 4 dB in Figure 6.

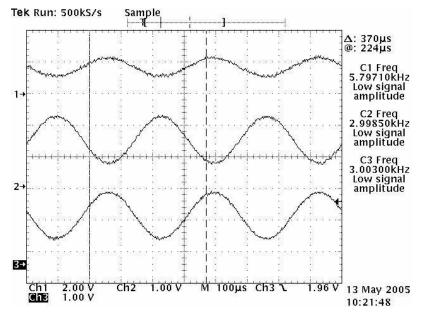


Figure 4. CP_IN to OUT32P/N Path, PGA Gain = 0 dB

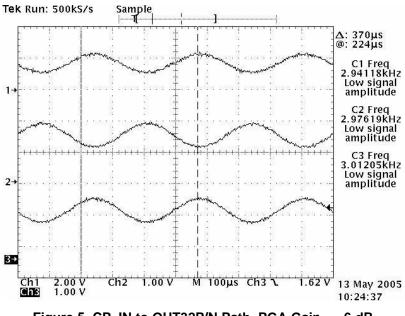


Figure 5. CP_IN to OUT32P/N Path, PGA Gain = -6 dB



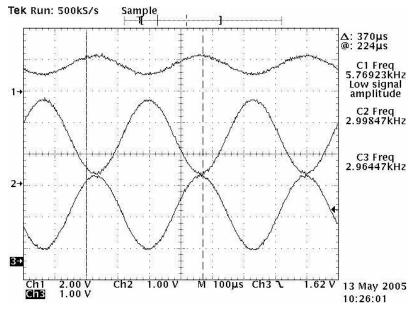


Figure 6. CP_IN to OUT32P/N Path, PGA Gain = 4 dB

References

- 1. TLV320DAC26, Low Power Stereo Audio DAC With Headphone/Speaker Amplifier data sheet (SLAS428)
- TSC2101, Audio CODEC With Integrated Headphone, Speaker Amplifier and Touch Screen Controller data sheet (<u>SLAS392</u>)

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