

10.9-MHz to 1.175-GHz, Low Phase Noise Clock Evaluation Board

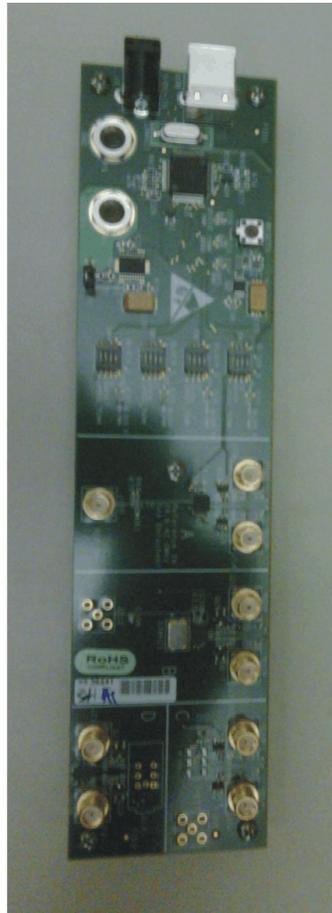


Figure 1. CDCE421A Evaluation Board

Features:

- Easy-to-use evaluation board to generate low phase noise clocks between 10.9 MHz and 1.175 GHz
- Easy device programming via host-powered USB port
- Fast configuration through GUI software interface
- Total board power provided either through USB port or separate 3.3-V and ground connections
- LVCMOS input interface or crystal input
- Standard 6-pin XO package connection available

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1 General Description

The [CDCE421A](#) is a high-performance, low phase noise clock generator. It has two fully integrated, low-noise, LC-based voltage-controlled oscillators (VCOs) that operate in the range of 1.75 GHz to 2.35 GHz.

The CDCE421A has an integrated crystal oscillator circuitry that operates in conjunction with an external AT-cut crystal to produce a stable frequency reference for the PLL-based frequency synthesizer. A 3.3-V LVCMOS level input can also be used instead of a crystal to provide a frequency reference to the PLL.

This evaluation module (EVM) is designed to demonstrate the electrical performance of the CDCE421A. This fully assembled and factory-tested evaluation board allows complete validation of the CDCE421A device functionalities. Throughout this document, the acronym *EVM* and the phrases *evaluation module* and *evaluation board* are synonymous with the CDCE421AEVM. [Figure 1](#) illustrates the CDCE421AEVM.

For optimum performance, the board is equipped with 50-Ω SMA connectors and well-controlled, 50-Ω impedance microstrip transmission lines.

2 Signal Path and Control Circuitry

The CDCE421A can accept a 29-MHz to 44-MHz frequency input from either an LVCMOS source (up to 3.3 V) or a crystal in the same frequency range.

The CDCE421AEVM is divided into four blocks. The programming section and device power for each block can be enabled or disabled through individual switches provided for each block. For example, in order to enable power and programming for Block A, the switch must be in the position shown in [Figure 2](#). The other blocks are disabled with the respective switches as the figure illustrates.

For more information about the CDCE421A, see the [CDCE421A product data sheet](#) available for download from the TI web site (www.ti.com).

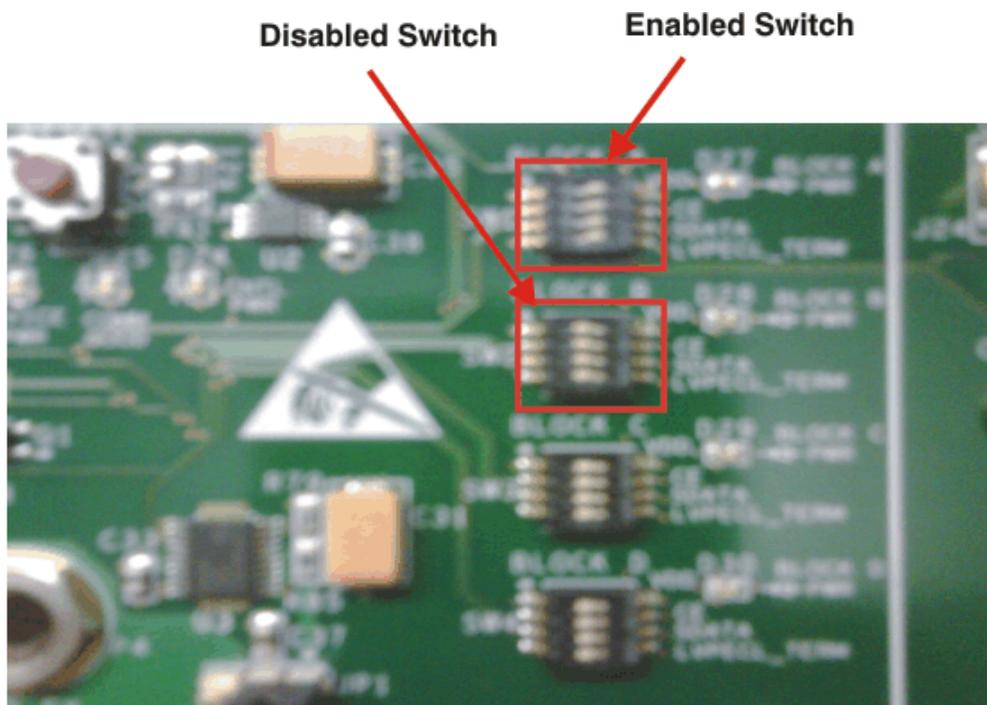


Figure 2. Enabled (Block A) and Disabled (Blocks B, C, D) Switch Positions

3 Block Description

This section summarizes the function of each block.

3.1 Block A

Block A includes a CDCE421A QFN device that accepts an LVCMOS reference input through the vertical SMA input connector (Ref Input), which is already ac-coupled onboard the EVM.

3.2 Block B

This block includes a CDCE421A QFN device that uses an AT crystal. This block can be used as either a crystal oscillator (XO) or a voltage-controlled crystal oscillator (VCXO). For use as an XO or VCXO, the crystal should be mounted on either of the two crystal footprints on the board, and a vertical SMA input connector must be installed on the provided footprint to be used as the control voltage input.

3.3 Block C

Block C can accommodate a 5×7 crystal oscillator. The oscillator package must also include a fixed-frequency crystal with a specified load and range.

3.4 Block D

Block D includes a socket that fits the oscillator part used in block C.

The output frequency of the CDCE421A is always an integer multiple or integer divide of the input frequency. The output frequency is determined through the selection of VCO1 or VCO2 and the appropriate prescaler and output divider based on the values discussed in the [CDCE421A product data sheet](#).

The loop filter selection will affect the output frequency phase noise, and should be considered in conjunction with the type of input used.

In LVDS mode, the device can achieve up to 400 MHz. In LVPECL mode, the device can achieve up to 1.175 GHz. The output signaling level and LVPECL termination are selectable through the software interface.

4 Software-Selectable Options

The provided graphical user interface (GUI) software allows users to easily send commands to the CDCE421A through the host-powered USB interface. The EVM includes a slave USB controller that transmits the commands to the single-pin programming interface located on the CDCE421A. DC power for the USB controller can either be derived from the 5-V power pin in the USB cable or by using an external 5-V ac adapter in the slot available on the EVM.

In addition to writing commands to the CDCE421A SRAM while the board is powered up, commands can also be stored in either the nonvolatile USB microcontroller memory or the EEPROM included within the CDCE421A. This option allows users to start the EVM in the desired state without requiring additional programming at power-up.

Note: The CDCE421A does have a permanent EEPROM lock mode. After this mode, is selected the EEPROM within the CDCE421A cannot be changed. This option is useful when setting final configurations.

5 Installing the GUI Software and USB Driver

To start the software installation, run the *CDCE421A Control GUI v 1.0.msi*, software, available in the [CDCE421A](#) product folder on TI.com. The screen shown in [Figure 3](#) appears.



Figure 3. Software Installation Screen 1

Note the location of the installation folder because the USB driver must be installed to the same folder after setup completes and the USB cable is connected, as indicated in [Figure 4](#).

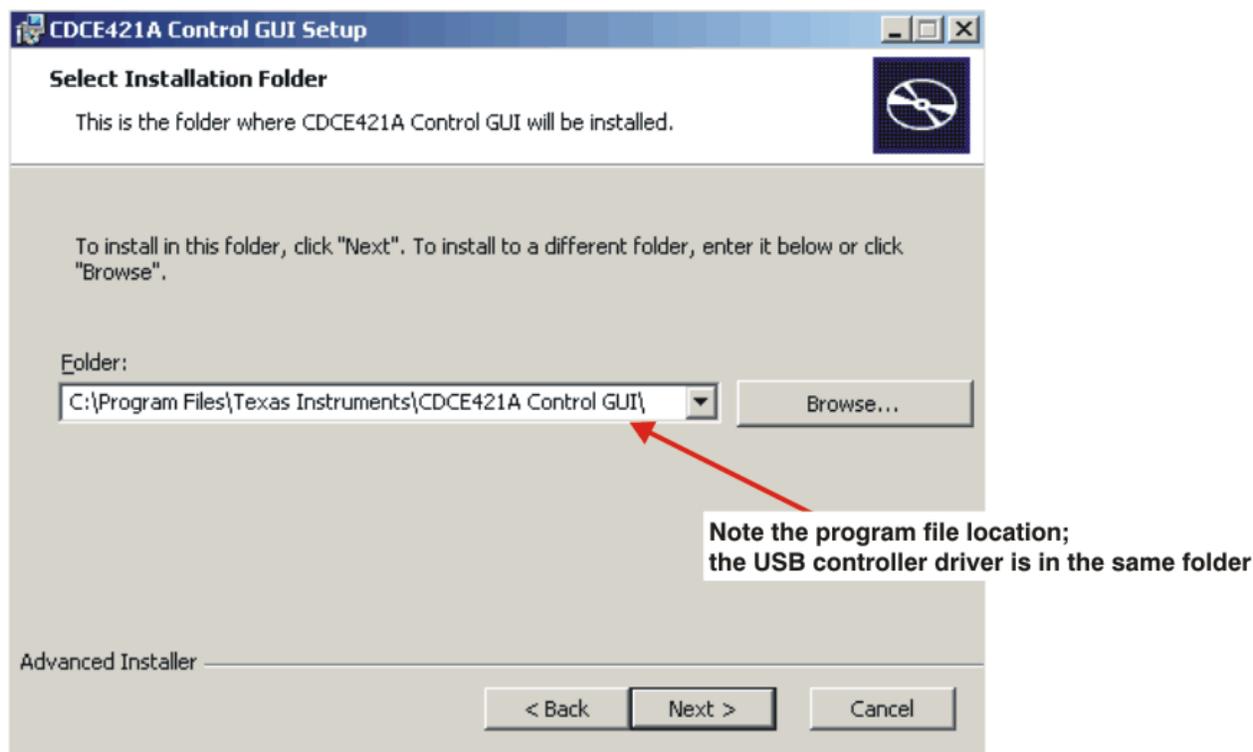


Figure 4. Software Installation Screen 2

After the setup wizard completes, start the GUI interface from the Windows® Start menu (Start→Texas Instruments→Chronos Eval↑TICronosGUI.exe).

Connect the USB cable to the EVM. If Windows prompts you for an appropriate driver, do not use the automatic search option. Instead, select the manual search, and when prompted for the driver location, browse to the Chronos GUI file folder that was used during installation. (No action is needed if Windows does not prompt you for a different driver.)

Once the USB driver installation completes, the GUI software should load properly and be ready for use. A green light in the USB communication box indicates a good USB connection; a red light indicates a faulty USB connection. If you get a red light in the communication box, make sure that the correct USB driver is properly installed and the USB cable is properly connected to the EVM.

6 Chronos GUI Software

Figure 5 illustrates the TI Chronos GUI software display.

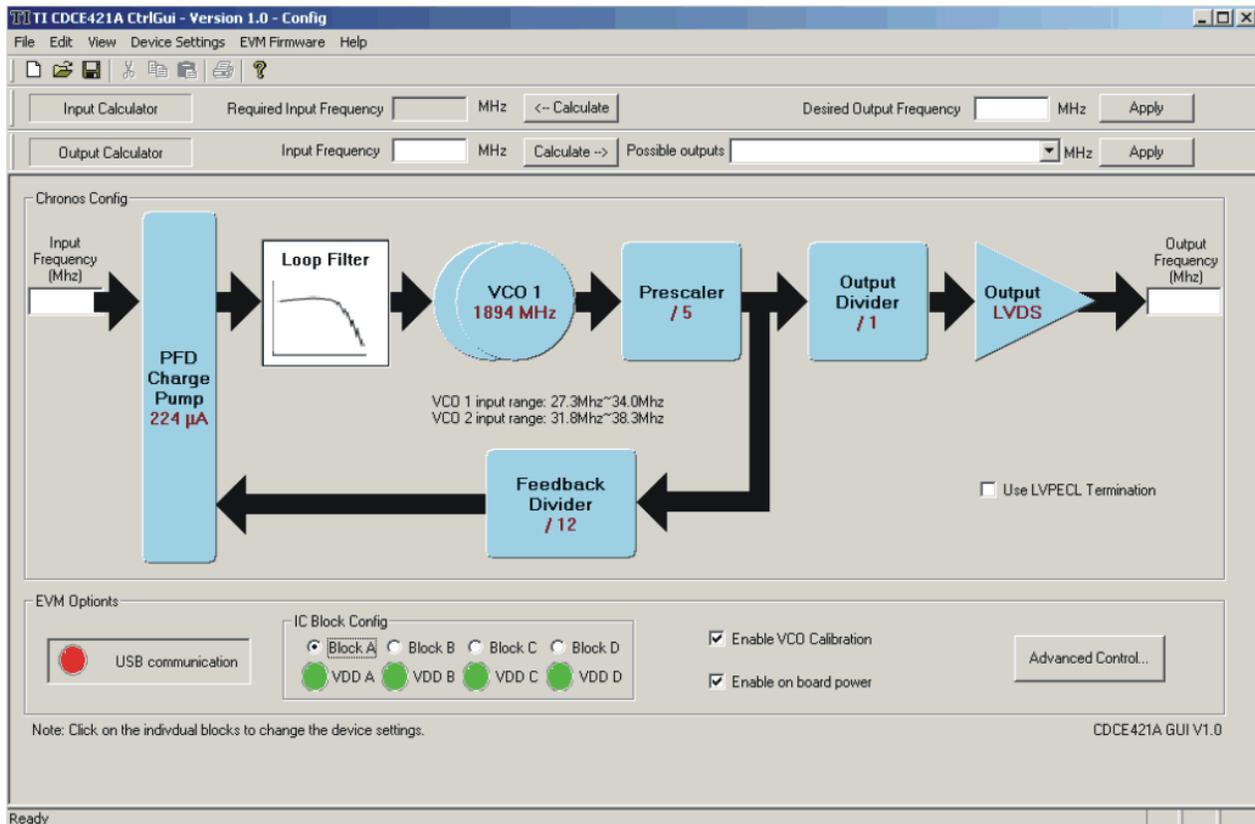


Figure 5. TI Chronos GUI Window

6.1 Using Software-Enabled Automatic PLL Selection

The screenshot displayed in Figure 5 shows the on-chip PLL structure of the CDCE421A. In this display, the user can change the Input Frequency, PFD Charge Pump, Loop Filter, and Output settings. The balance of the settings are selected by the software with user-selectable options as described in the steps below.

Step 1. IC Config and Input Calculator

Before programming the PLL, the EVM block that is being programmed must be selected in the *IC Block Config* section of the GUI. For any block in the EVM that is being used, the first row of calculations is useful when trying to investigate the input frequency to the CDCE421A required in order to obtain a desired output frequency. The input is found by pressing the *Calculate* button.

Step 2. Store Crystal Frequency

If a crystal input is used in Block B of the EVM, the crystal frequency must be entered into the space provided by clicking on the *Device_EEPROM* field found at the top of the software GUI. This action opens a drop-down menu, where the user can click the menu item labeled *Save Block B – XTAL Freq to EEPROM*. In this field, enter the crystal frequency in the format *xx.xxx*, specified in MHz.

Step 3. Output Calculator and Apply PLL Settings

The second row of calculations is used to get the PLL settings required to obtain a particular output frequency provided by a given input frequency to CDCE421A. The input must be entered in the second row as well as the place provided at the input of the PLL block diagram. After the *Calculate* button is pressed, the adjacent drop-down menu is populated with several choices for the given input; the desired output can then be chosen from this list. Choosing an output then sets the divider settings within the PLL. Click on the *Apply* button (next to the drop-down menu) to write the PLL settings to the

device SRAM. If LVPECL output is desired, scroll through the Output type box until *LVPECL* is displayed. This option automatically enables onboard LVPECL termination. If LVDS output is desired, scroll through the Output type box until *LVDS* is displayed.

Step 4. PLL Bandwidth Select

If the user wants to adjust the PLL bandwidth, the *Loop Filter* block must be clicked. Clicking this block brings up a pop-up screen, as shown in [Figure 6](#).

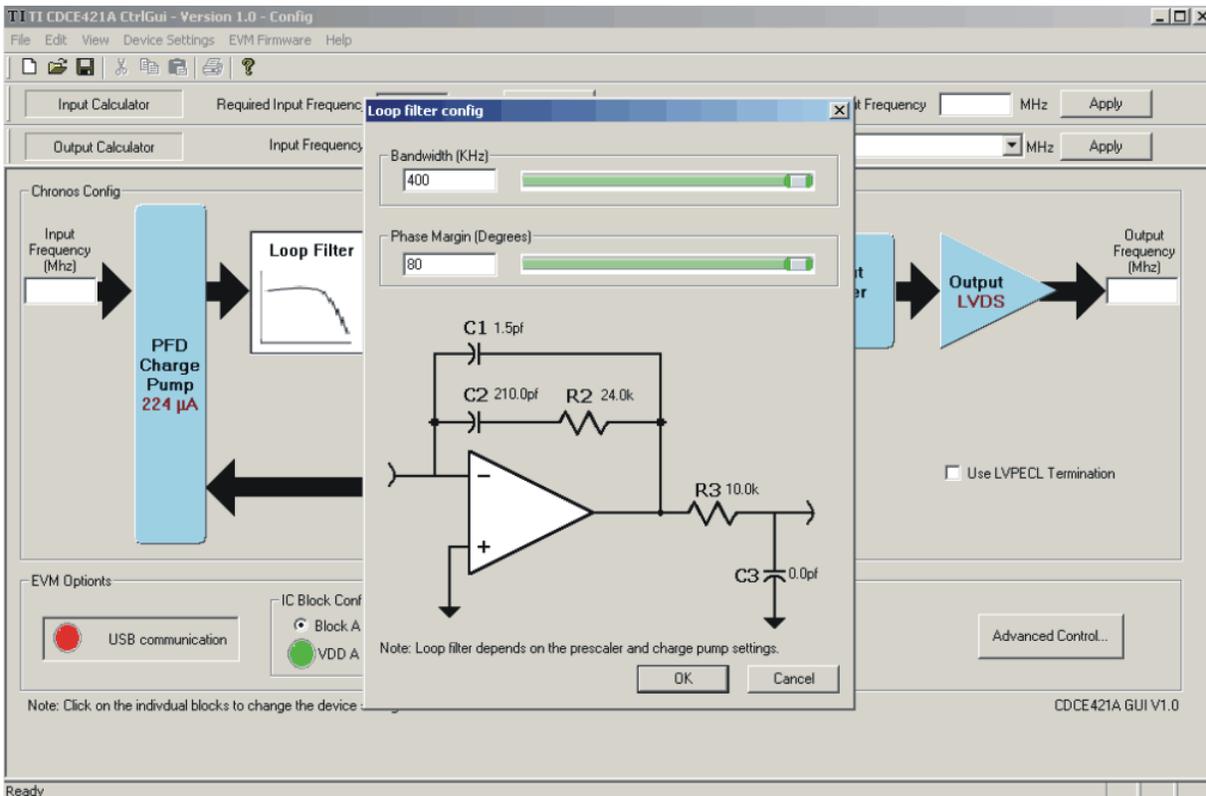


Figure 6. Loop Filter Configuration Pop-Up Dialog

For a clean reference input to CDCE421A (such as from an oscillator or crystal), the maximum bandwidth and phase margin settings must be used, or 400 kHz and 80 degrees, respectively. The PDF charge pump current must be set to its maximum (224 μ A). The PFD charge pump current can be set by clicking on the *PDF Charge Pump* block. This selection then presents a drop-down menu with the various charge pump current settings.

For a dirty reference input to CDCE421A, use the minimum bandwidth setting (50 kHz). Additionally, to reduce the output jitter for a dirty input, the phase margin can be reduced to near-minimum (30 degrees), depending on the integration limits of the jitter that is deemed important for a given application. To reduce the output jitter even further, reduce the charge pump current to near-minimum (56 μ A), depending on the integration limits of the jitter.

Step 5. Write to CDCE421A EEPROM

To write any particular setting to the EEPROM (in locking or no-locking mode), the menu item at the top of the GUI titled *Device_EEPROM* must be clicked. This action highlights the items *Write settings to EEPROM (No locking)* and *Write settings to EEPROM (Locking)* as part of a drop-down menu. Choose the appropriate option after setting the desired PLL configurations in order to write to the EEPROM in the appropriate mode.

6.2 Manual PLL Block Selection (Advanced Control)

This GUI helps users to set the PLL without having to manually alter all the blocks individually within the PLL. If a user is familiar with the general operation of PLLs, one may activate individual control of the PLL blocks by clicking on the *Advanced Control* button. A new window appears, as shown in [Figure 7](#).

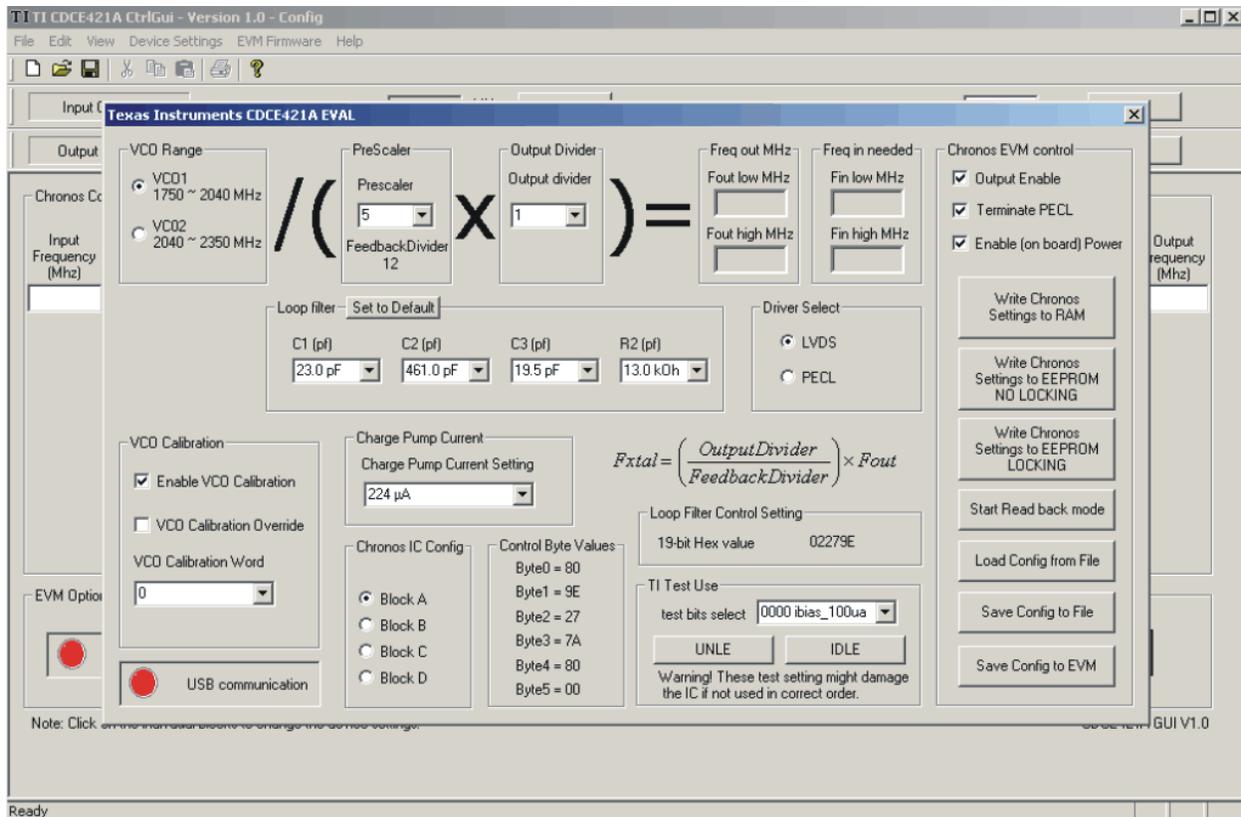


Figure 7. CDCE421A Advanced Controls Pop-Up Dialog

[Table 1](#) summarizes the various menu options available in this dialog window.

Table 1. Advanced Control: Software Setting Options

Section	Function
VCO Select	Selects between VCO1 and VCO2. Only one VCO can be used during operation. See the CDCE421A product data sheet for VCO tuning ranges.
Prescaler	The prescaler selection will be determined in conjunction with the VCO and output divider selection. See the CDCE421A product data sheet to determine the proper setting.
Output Divider.	The output divider will be determined in conjunction with the VCO and prescaler settings. See the CDCE421A product data sheet to determine the proper setting.
Driver Select	Selects between LVPECL or LVDS.
PECL config	This option should be activated with using LVPECL output. When selected, the USB controller will enable onboard LVPECL termination.
Charge Pump Current.	Selects appropriate charge pump current. See screen shotsxx for recommended configurations.
Loop Filter Bias Select	Bias 0 should be used at all times. Bias 1 is a reserved test mode for TI.

Table 1. Advanced Control: Software Setting Options (continued)

Section	Function
Loop Filter	Selects the loop filter C and R values. See screen shotsxx for recommended configurations.
VCO Calibration	When <i>Enable VCO Calibration</i> is selected, the CDCE421A will use its internal calibration circuit to lock the PLL loop. <i>VCO Calibration Override</i> should not be checked. (TI uses manual calibration for test modes.)
TI Test Use	This setting should be kept at <i>0000 ibias_100ua</i> . Other settings are for TI internal use only.
Chronos IC Config	<ul style="list-style-type: none"> • Select <i>Use U13 programming socket</i> for rapid programming of Chronos-enabled devices. • Select <i>Use U8 DIE/U9 QFN socket</i> if the EVM is using a direct-mounted die OR a QFN-mounted device. Note: This setting is the typical configuration. • Select <i>Use U12XTAL EVAL</i> if using the optional 6 pin XO mounting pads (for Chronos-enabled oscillators).
Chronos Control	<ul style="list-style-type: none"> • Select <i>Enable Power</i> to run the entire board from the host USB voltage. In this mode, the EVM will not need an external 3.3-V power supply. If this option is not selected, then a 3.3-V supply and ground connection must be attached. • Select <i>Output Enable</i> to provide a clock output. When not selected, the output will go to a high-Z state. • Push <i>Write Chronos settings to RAM</i> to download settings to the CDCE421A onboard volatile SRAM. These settings will be lost upon power down. • Push <i>Write Chronos settings to EEPROM NO LOCKING</i> when ready to store the configuration in the CDCE421A nonvolatile EEPROM. The settings will be available after power down. The settings can be changed at a later time. • Push <i>Write Chronos settings to EEPROM LOCKING</i> only if the settings are permanent and final. After this selection, the EEPROM will be locked and cannot be altered at a later time.
USB communication	A bright red light indicates that USB is not connected or not communicating properly. A green light indicates a proper USB connection.

7 Configuring the Board

The CDCE421AEVM can be powered from either the USB power supply or from an external source. The CDCE421AEVM only requires a USB cable to be attached for programming purposes; however, for test measurements, it is recommended to also use an external 3.3-V power supply. Test measurements can also be taken with only the USB-supplied power. However, as a result of USB power variances, results may degrade. It is also possible to program the CDCE421A and then disconnect the USB cable with minor board configuration changes. To enable power and programming of any of the four blocks on the CDCE421AEVM, the respective switch must be turned on, as explained earlier (see [Section 2](#)).

7.1 Configuration for Programming and Testing (with USB Cable Attached)—Default Configuration

The CDCE421AEVM is configured by default to operate with the USB cable attached and a 3.3-V power supply added to AUX VDD and GND. In this configuration, the USB microcontroller is powered by the USB port 5-V supply while the CDCE421A is powered by the 3.3-V external supply. This setup is optimal for programming the CDCE421A while also taking measurements. This configuration removes the power variation found in USB power supplies by isolating the CDCE421A from the USB supply.

7.2 Configuration for Programming (with USB Cable Attached)

The CDCE421AEVM can also use power supplied through the USB cable as its sole power source. However, as mentioned earlier, because of power-supply variances in the USB supply, this configuration is not recommended for measurements. This setup is helpful for saving configuration settings to the CDCE421A and then later powering the device from its internal memory (a useful option if there is no USB port available on a PC in a lab or test chamber). In this configuration, JP1 must be moved from its default position to the new position shown in [Figure 8](#). Additionally, the *Enable (onboard) Power* box must be checked on the GUI software, followed by pushing the *Apply* software button.

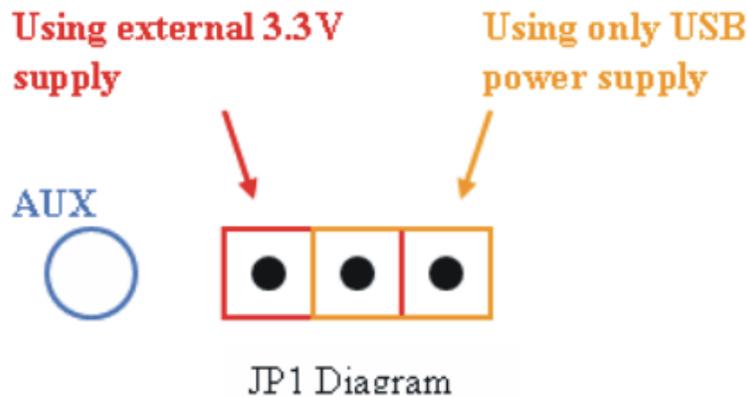


Figure 8. JP1 Settings

7.3 Configuration for Testing from a Saved Configuration (with USB Cable Removed after Programming)

When operating the CDCE421A without the USB programming cable, the CDCE421AEVM must be pre-programmed in one of the configurations discussed in this section and then reconfigured for external power-supply usage.

Before making these board modifications, the CDCE421A settings must be saved with one of the above USB cable attached configurations. Use the *Write Chronos Settings to EEPROM NO LOCKING* software button to save the CDCE421A settings to the device-internal EEPROM. After the settings are saved to the EEPROM, the USB cable can be removed. Once the cable has been disconnected, jumper JP1 should be in the *Using External 3.3-V Supply* position (as shown in [Figure 8](#)). The EVM is now ready for use without the USB cable connected. The CDCE421A will always start from its saved configuration state in this mode.

If the CDCE421A must be isolated from the microcontroller, the switch that corresponds to the block in use should be set to *Off* for CE_x, SDATA_x, and LVPECL_TERM_x (where x represents the block name). The power line switch for that block, however, should be kept on. This sequence also allows for the USB cable to be removed without affecting performance while the CDCE421A is powered up.

8 Schematics and Layout

[Figure 9](#) through [Figure 11](#) show the printed circuit board (PCB) schematics for the CDCE421AEVM.

Note: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing CDCE421AEVM PCBs.

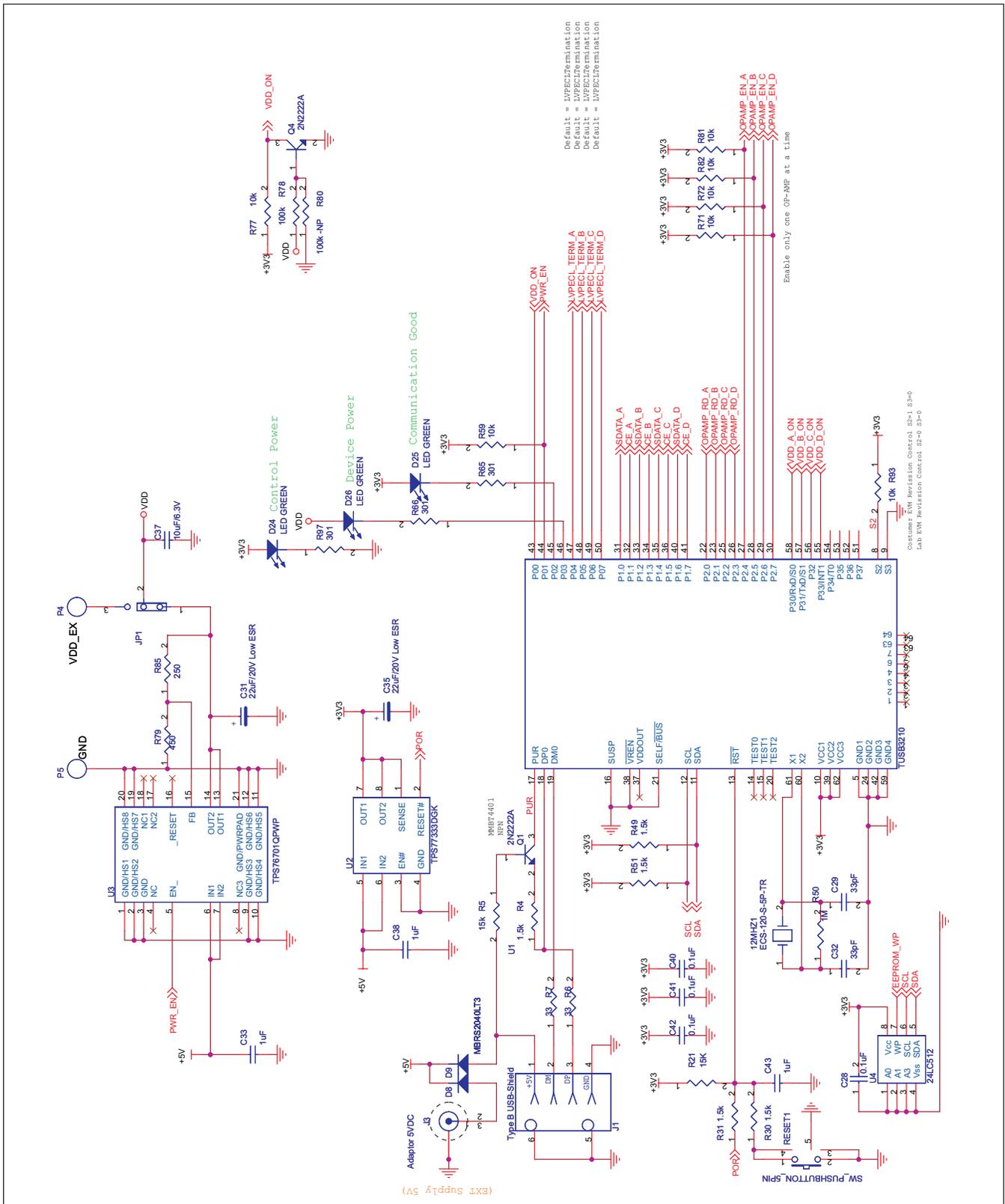


Figure 9. CDCE421AEVM—Schematic

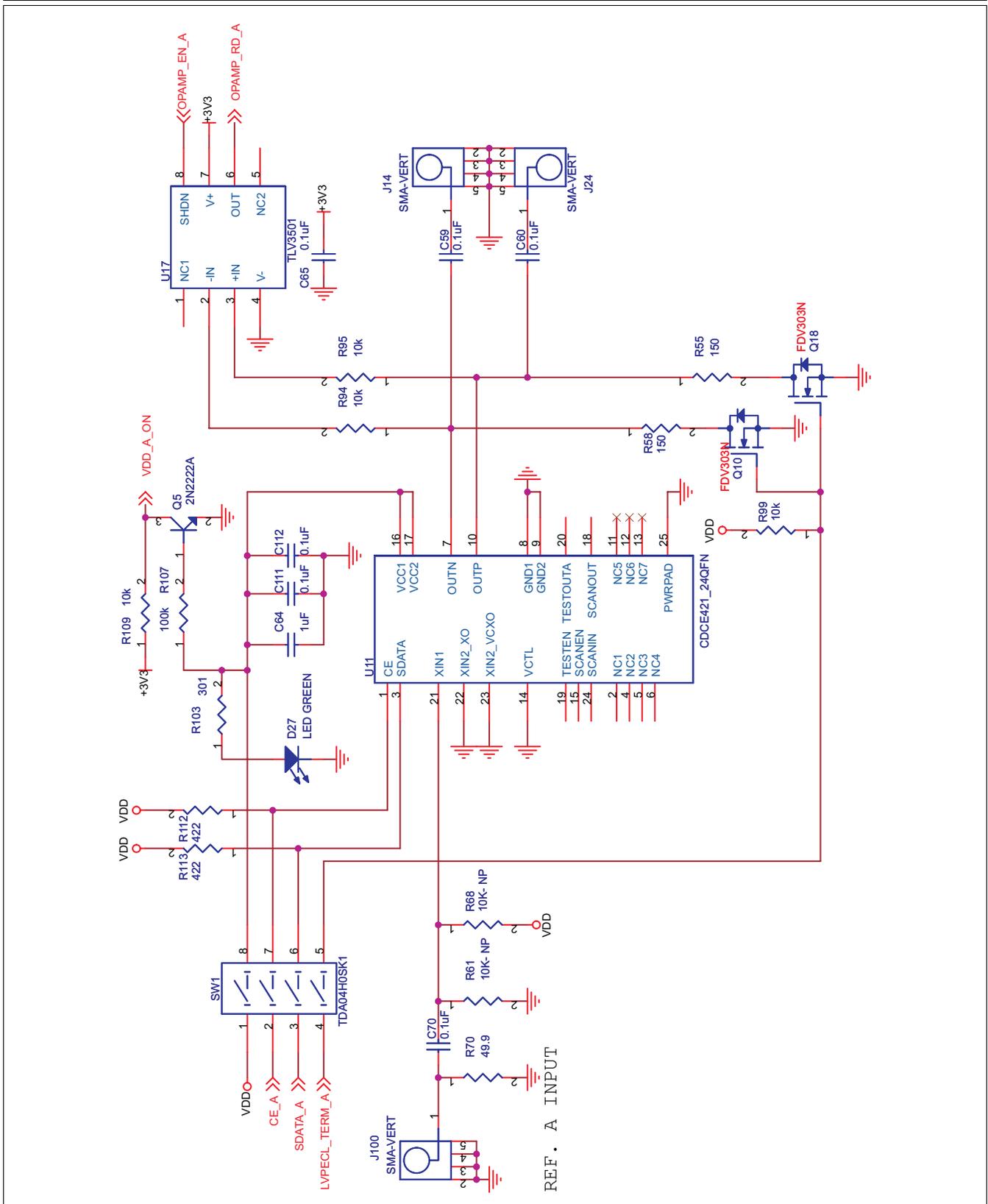


Figure 10. CDCE421AEVM—Schematic

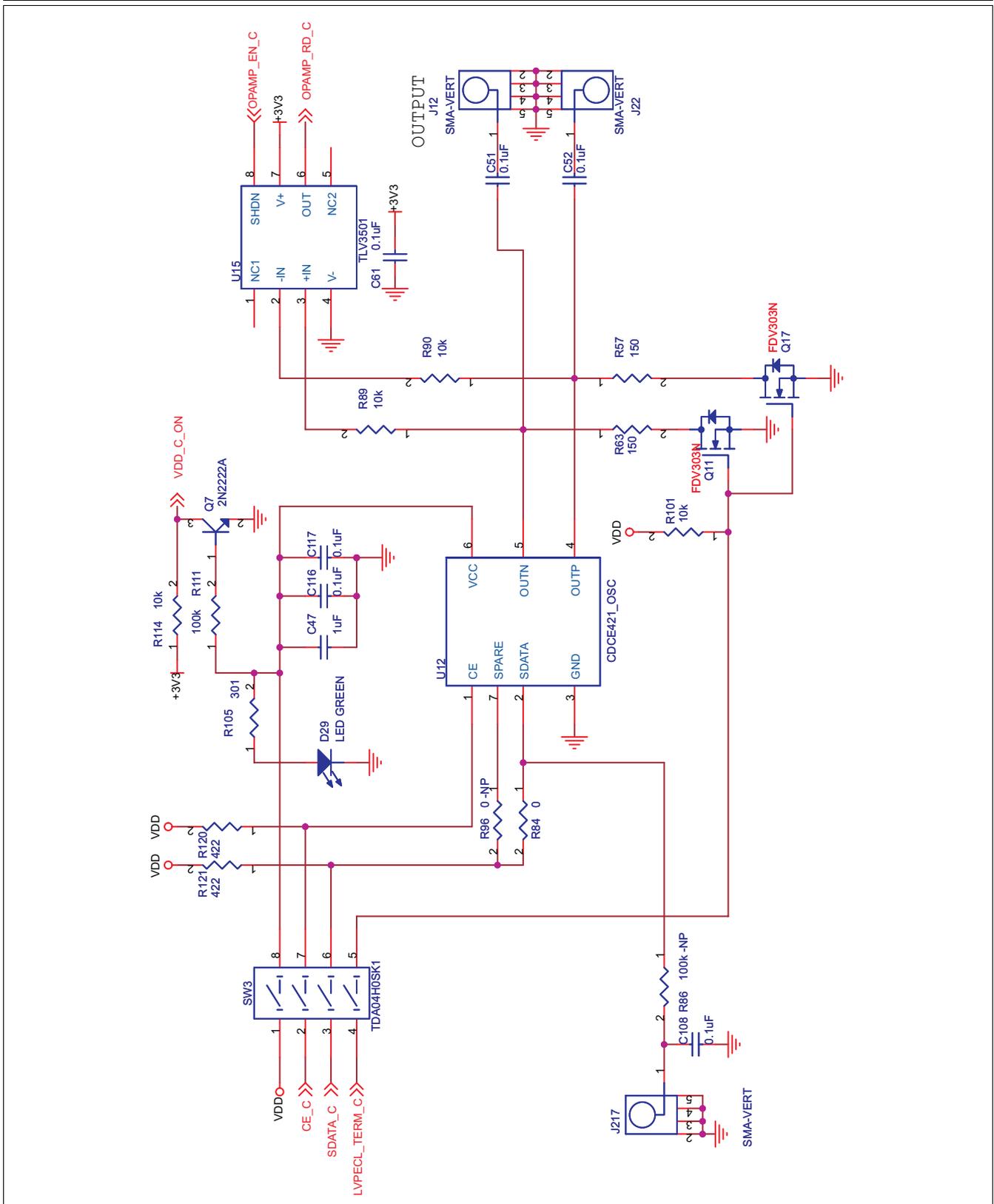


Figure 12. CDCE421AEVM—Schematic

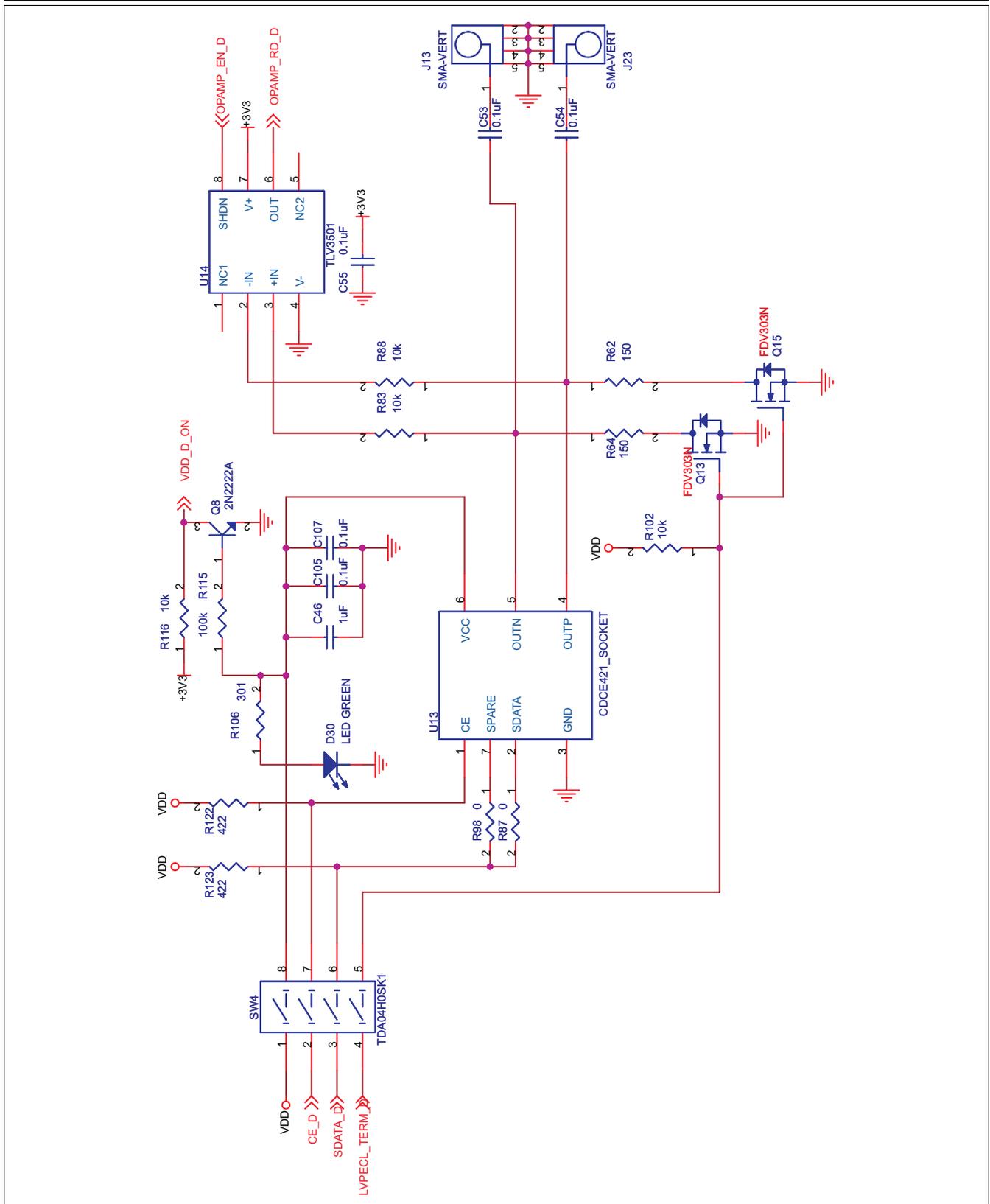


Figure 13. CDCE421AEVM—Schematic

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -0.5 V to $+4.0\text{ V}$ and the output voltage range of 0 to $+3.6\text{ V}$.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than $+120^{\circ}\text{C}$. The EVM is designed to operate properly with certain components above $+85^{\circ}\text{C}$ as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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