Using TI's CDCVF2310 and CDCVF25081 with TLK1501 Serial Transceiver

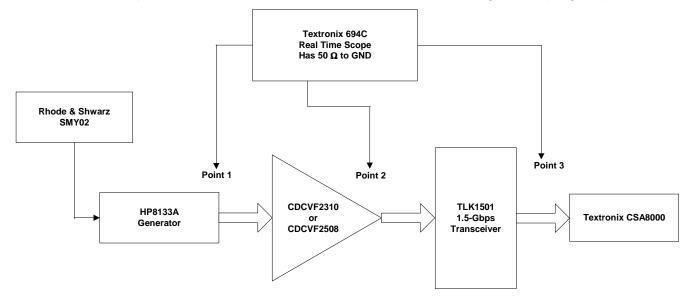*Kal Mustafa/Roger Chan*   *High Performance Analog*

ABSTRACT

This test report discusses jitter transfer of TI's CDCVF2310 and CDCVF25081 clock drivers when driving TI's TLK1501 serial gigabit transceiver at 600 Mbit/sec. This application report summarizes the peak-to-peak and RMS jitter measurements taken during the testing of the clock drivers with the TLK1501. The CDCVF2310 is a high-performance clock buffer that provides 10 low-skew copies of CLK at 2.5 V or 3.3 V. The CDCVF25081 is a phase-lock loop clock driver that provides eight copies of zero-delay CLK. The CDCVF25081 operates from a nominal supply voltage of 3.3 V.

Test Setup

The block diagram of the test setup is shown in Figure 1. The clock source was provided by a HP8133A at 30 MHz. The clock was then driven into TLK1501 by either CDCVF2310 or CDCVF25081. Jitter measurements were taken at point 1, point 2, and point 3. A PRBS 2^7-1 pattern was generated by TLK1501 with the clock provided by the CDCVF2310 clock driver and the transmit jitter was then measured with a Tektronix CSA8000 digital sampling scope.

Figure 1.   Block Diagram of Test Setup With CDCVF2310 and CDCVF25081 Driving TLK1501

Transmission lines usually have 50-Ω characteristic impedance. The transmitted signals should be controlled such that surplus energy is absorbed at either the source or the load end of the line, preventing reflection. The termination method used in this report was a 50-Ω source termination for both clock drivers (CDCVF2310 and CDCVF25081), which are included on-chip and thus no external termination were required.

Test Results

The TLK1501 was tested with the CDCVF2301 clock driver. The jitter at the output of HP8133A, CDCVF2310, and TLK1501 is summarized in Table 1. The total peak-peak jitter at the output of the Tek8133A was ~16 ps at 30 MHz. With the 30-MHz clock from the HP8133A, the CDCVF2310 provides a LVTTL clock with peak-to-peak total jitter of 20 ps, which was below the TLK1501 requirement of ≤40-ps peak-to-peak.

Reference Clock	Period Jitter (ps)			Comments
	PP	RMS	V_Amplitude (V)	
Rohde & Schwarz SMY02 +HP8133A With 6-dB attenuator	16	2.593	1.422	HP8133A set at: V_{IH} = 2 V V_{IL} = 0.8 V (See Figure 2)
Rohde & Schwarz SMY02 +HP8133A + CDCVF2310 Without 6-dB attenuator	20 (rising edge) 20(falling edge)	2.767 2.976	1.422 1.422	HP8133A set at: V_{IH} = 2 V V_{IL} = 0.8 V (See Figure 3, 4)
Rohde & Schwarz SMY02 +HP8133A + CDCVF2310 + TLK1501	112	17.6	1.422	HP8133A set at: V_{IH} = 2 V V_{IL} = 0.8 V (See Figure 5)
Rohde & Schwarz SMY02 +HP8133A + TLK1501	122	18.59	1.422	HP8133A set at: V_{IH} = 2 V V_{IL} = 0.8 V (See Figure 6)
Rohde & Schwarz SMY02 +HP8133A + CDCVF25081 (Zero-Delay PLL) + TLK1501	166	26.6	1.422	HP8133A set at: V_{IH} = 2 V V_{IL} = 0.8 V (See Figure 7)

**Table 1.   Jitter Result With CDCVF2310 Driving TLK1501 at
600 Mbit/sec (30-MHz Clock)**

Figure 2 through Figure 7 show the zero crossings of the eyes captured for each case in Table 1 using the CSA8000. There was no degradation in performance when driving the clock with the CDCVF2310. The following graph shows that the CDCVF2310 is able to drive the TLK1501 with less than the 40-ps peak-to-peak input jitter. The TLK1501 output jitter in PRBS data pattern is below 0.1 UI (166.67 ps), the output specification at 600 Mbit/sec.
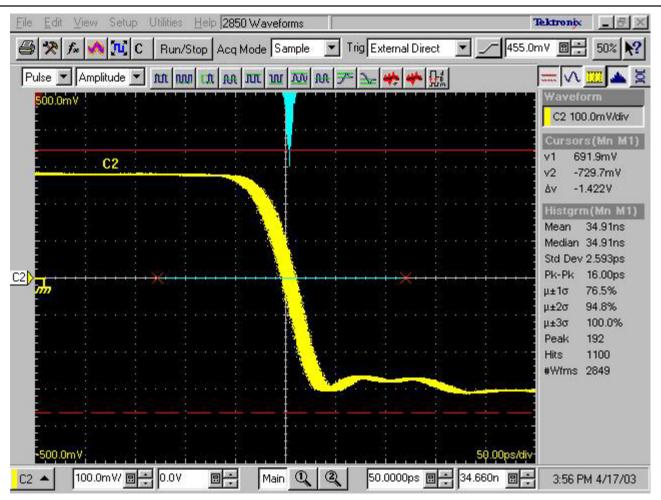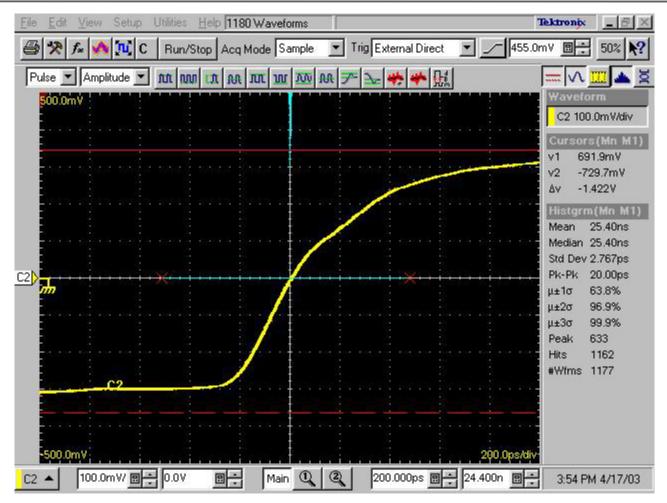
Figure 2.   Zero Crossing of Data Eye at 600 Mbit/sec: R&S SMY02→HP8133A

Figure 3. Zero Crossing of Data Eye at 600 Mbit/sec: R&S SMY02→HP8133A→CDCVF2310 Rising Edge
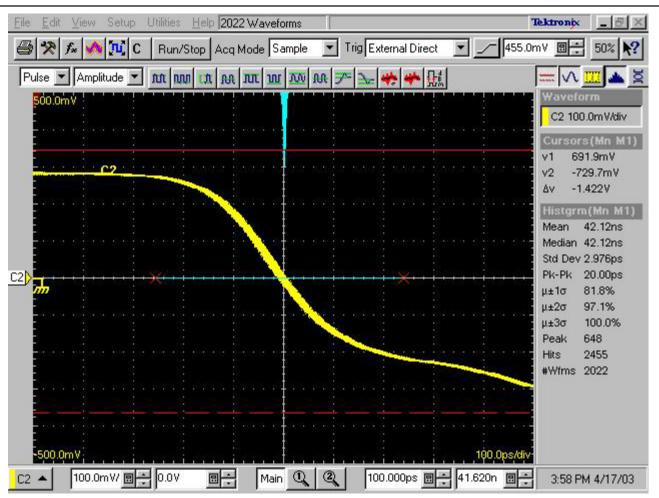
Figure 4.   Zero Crossing of Data Eye at 600 Mbit/sec: R&S
SMY02→HP8133A→CDCVF2310 Falling Edge

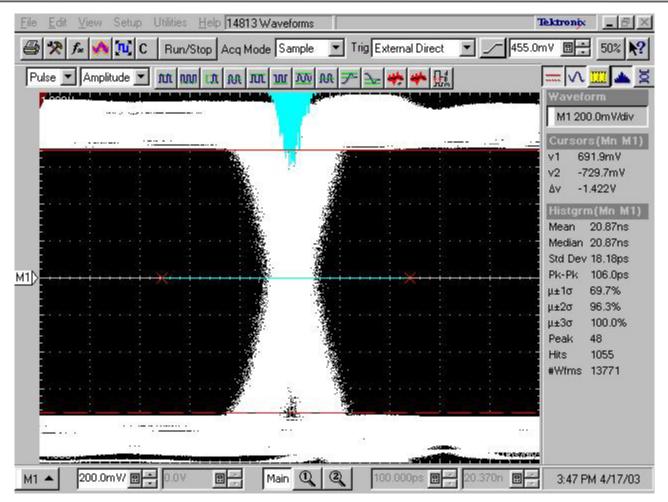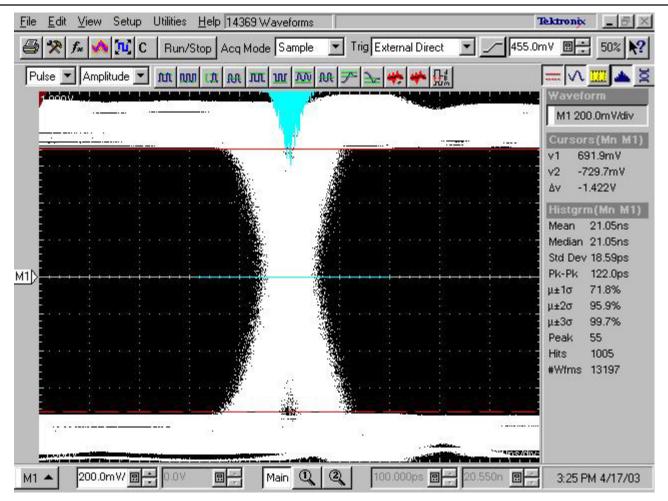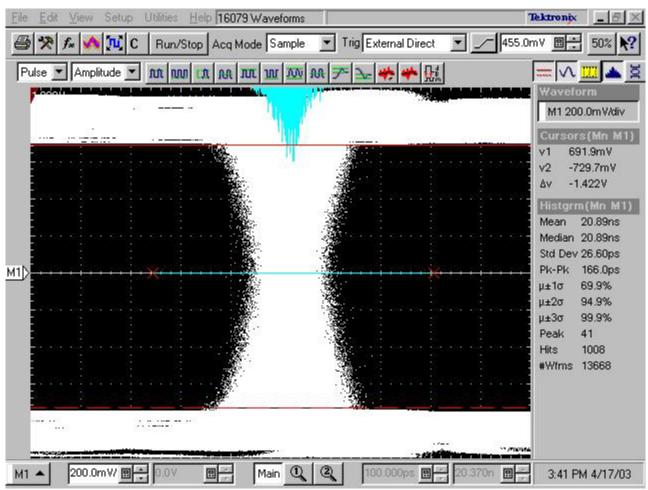**Figure 5.   Zero Crossing of Data Eye at 600 Mbit/sec: R&S
SMY02→HP8133A→CDCVF2310→TLK1501**

Figure 6.   Zero Crossing of Data Eye at 600 Mbit/sec: R&S SMY02→HP8133A→TLK1501

The TLK1501 was then tested with CDCVF25081, a phased-lock loop clock driver. The clock provided by CDCVF25081 had more jitter (166 ps) at 30MHz. Figure 7 was the zero crossings of the eyes captured by the CSA8000 with the CDCVF25081 clock driver. The TLK1501 output jitter increased to 166 ps in this setup.

**Figure 7.   Zero Crossing of Data Eye at 600 Mbit/sec: RS
SMY02→HP8133A→CDCVF25081→ TLK1501**

For testing purpose, we ran a PRBS 2^7-1 data pattern from the TLK1501 driver through 72 inches, 5 mil wide trace and loopback to the TLK1501 with both CDCVF2310 and CDCVF25081. No error was reported in both cases.
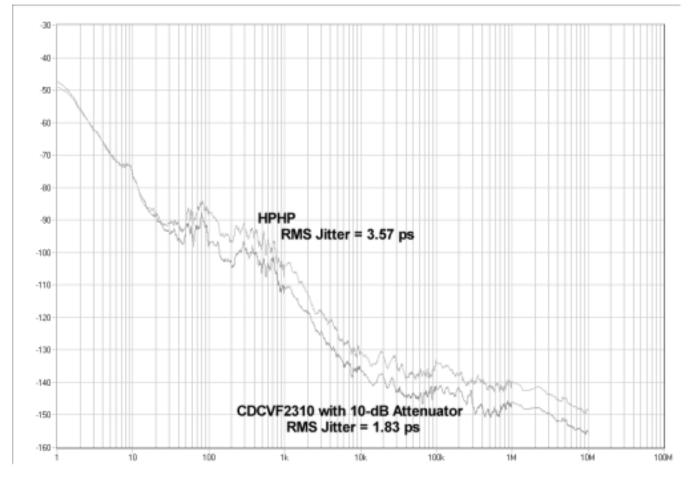
Phase Noise Plots

Figure 8. Phase Noise of HP8133A and CDCVF2310 (12 kHz – 10 MHz)

Conclusion

The CDCVF2310 is able to drive the TLK1501 and meets the jitter requirements without any problem. CDCVF2310 is recommended for applications that need high clock fan out (1:10) but can tolerate a small amount of clock skew (<100 ps). A phase-locked loop-based clock driver like the CDCVF25081 is not recommended as the clock driver for TLK1501.

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