TVS1801 18V 双向平缓钳位浪涌保护器件

1 特性

- 针对工业信号线的 1kV、42Ω IEC 61000-4-5 浪涌测试提供保护
- 双向极性可针对双极信号传输或误接线情形提供保护
- 30A 8/20μs 浪涌电流下的钳位电压为 27.4 V
- 关断电压：±18V
- 3mm × 3mm 小型 SON 封装
- 在 125°C 时，可耐受超过 5,000 次的 30A 8/20μs 浪涌电流的重复冲击
- 强大的浪涌保护
  - IEC61000-4-5 (8/20μs)：30A
  - IEC61643-321 (10/1000μs)：4.5A
- 低泄漏电流
  - 27°C 下为 0.4nA（典型值）
  - 85°C 时的最大值为 280nA
- 低电容：65 pF
- 集成 4 级 IEC 61000-4-2 ESD 保护

2 应用

- 工业传感器 I/O
- PLC I/O 模块
- 固态硬盘
- 电器
- 医疗设备
- 12V 电源线路

3 说明

TVS1801 器件可将高达 30A 的 IEC 61000-4-5 故障电流进行分流，以保护系统免受高功率瞬态冲击或雷击。该器件可通过 42Ω 阻抗进行耦合的方式承受 1kV 的 IEC 61000-4-5 开路电压，满足常见的工业信号线路 EMC 要求。TVS1801 使用反馈机制确保在故障期间发挥精确的平缓钳位能力，使系统接触电压始终低于传统 TVS 二极管。精确的电压调节允许设计人员放心地选择具有较低电压容差的系统组件，从而能够在不影响可靠性的情况下降低系统成本和复杂度。TVS1801 具有 ±18V 的工作范围，可在需要反向接线情形防护的系统中运行。

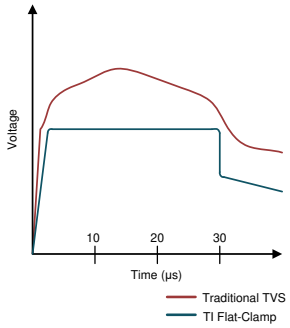
此外，TVS1801 采用小型 SON 封装，专为空间受限的应用而设计，与标准 SMA 和 SMB 封装相比，其尺寸显著减小。低器件泄露电流和电容确保更大限度地降低了对受保护线路的影响。为了确保在产品的整个寿命期间提供可靠保护，TI 在 125°C 的环境下对 TVS1801 进行了 5000 次重复浪涌冲击测试，但器件性能未发生任何变化。

TVS1801 是 TI 的平缓钳位系列浪涌器件中的一款产品。如需深入了解平缓钳位系列，请参阅*用于高效系统保护的平缓钳位浪涌保护技术*白皮书。

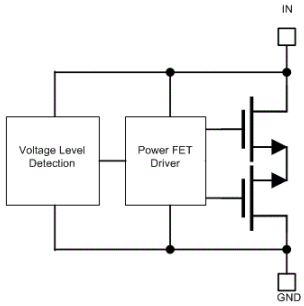
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TVS1801	SON (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



对 8/20μs 浪涌事件的电压钳位响应



功能方框图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 2018) to Revision B (May 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated the *8/20-µs Surge Clamping Response at 30 A* figure	7

Changes from Revision * (September 2018) to Revision A (December 2018)	Page
• 将“预告信息”更改为“量产数据”	1

5 Device Comparison Table

DEVICE	V_{rwm}	V_{clamp} at I_{pp}	I_{pp} (8/20 µs)	Leakage at V_{rwm}	POLARITY	Package
TVS0500	5	9.2 V	43 A	0.07 nA	Unidirectional	DRV (SON-6)
TVS0701	7	11 V	30 A	0.25 nA	Bidirectional	DRB (SON-8)
TVS1400	14	18.6 V	43 A	2 nA	Unidirectional	DRV (SON-6)
TVS1401	14	20.5 V	30 A	1.1 nA	Bidirectional	DRB (SON-8)
TVS1800	18	22.8 V	40 A	0.3 nA	Unidirectional	DRV (SON-6)
TVS1801	18	27.4 V	30 A	0.4 nA	Bidirectional	DRB (SON-8)
TVS2200	22	27.7 V	40 A	3.2 nA	Unidirectional	DRV (SON-6)
TVS2201	22	29.6 V	30 A	2 nA	Bidirectional	DRB (SON-8)
TVS2700	27	32.5 V	40 A	1.7 nA	Unidirectional	DRV (SON-6)
TVS2701	27	34 V	27 A	0.8 nA	Bidirectional	DRB (SON-8)
TVS3300	33	38 V	35 A	19 nA	Unidirectional	DRV (SON-6), YZF (WCSP)
TVS3301	33	40 V	27 A	2.5 nA	Bidirectional	DRB (SON-8)

6 Pin Configuration and Functions

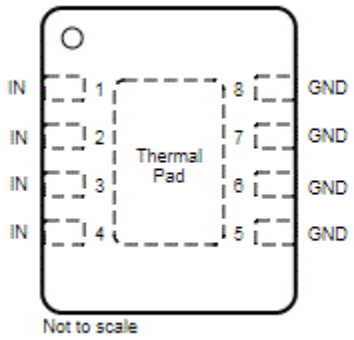


图 6-1. DRB Package, 8-Pin SON (Top View)

表 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DRB		
IN	1, 2, 3, 4	I	Surge Protected Channel
GND	5, 6, 7, 8	GND	Ground
FLOAT	Exposed Thermal Pad	NC	Exposed Thermal Pad Must Be Floating

(1) NC = no connect, GND = ground, I = input

7 Specifications

7.1 Absolute Maximum Ratings

T_A = 27°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20 µs), T_A < 125°C		±30	A
	IEC 61000-4-5 Power (8/20 µs)		825	W
	IEC 61643-321 Current (10/1000 µs)		±4.5	A
	IEC 61643-321 Power (10/1000 µs)		120	W
EFT	IEC 61000-4-4 EFT Protection		80	A
I_{BR}	DC Current		33	mA
T_A	Ambient Operating Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings - JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±8	kV
		IEC 61000-4-2 air-gap discharge	±15	

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{RWM}	Reverse Stand-Off Voltage		±18		V

7.5 Thermal Information

THERMAL METRIC(1)		TVS1801 DRB (SON) 8 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	52	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	56.1	°C/W
R_{qJB}	Junction-to-board thermal resistance	24.9	°C/W
Y_{JT}	Junction-to-top characterization parameter	2.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	24.8	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LEAK}	Leakage Current	Measured at V_{IN} = ±V_{RWM}, T_A = 27°C		0.4	25	nA
		Measured at V_{IN} = ±V_{RWM}, T_A = 85°C			290	
V_{BR}	Break-down Voltage	I_{IN} = ±1 mA	23.35	24.4		V
V_{CLAMP}	Clamp Voltage	±I_{pp} IEC 61000-4-5 Surge (8/20 µs), V_{IN} = 0 V before surge, T_A = 27°C		27.4	28.8	V
		±I_{PP} IEC 61000-4-5 Surge (8/20 µs), V_{IN} =±V_{RWM} before surge, T_A = 125°C			30.4	
R_{DYN}	8/20 µs surge dynamic resistance	Calculated from V_{CLAMP} at .5*I_{PP} and I_{PP} surge current, T_A = 25°C		50		mΩ
C_{IN}	Input pin capacitance	V_{IN} = V_{RWM}, f = 1 MHz, 30 mV_{pp}, IO to GND		65		pF
SR	Maximum Slew Rate	0-±V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PEAK} = 1 mA, T_A = 27°C		2.5		V/µs
		0-±V_{RWM} rising edge, sweep rise time and measure slew rate when I_{PEAK} = 1 mA, T_A = 85°C		1		

7.7 Typical Characteristics

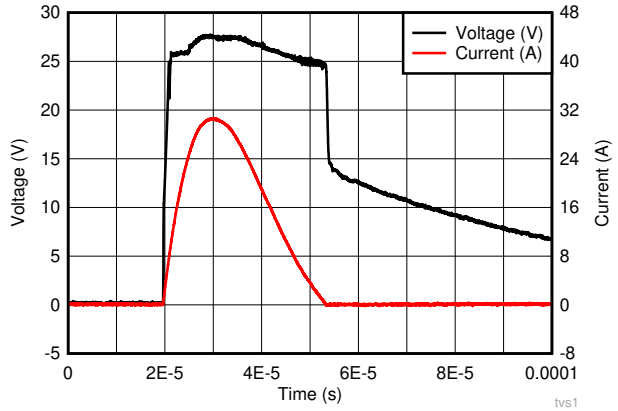


图 7-1. 8/20-µs Surge Response at 30 A

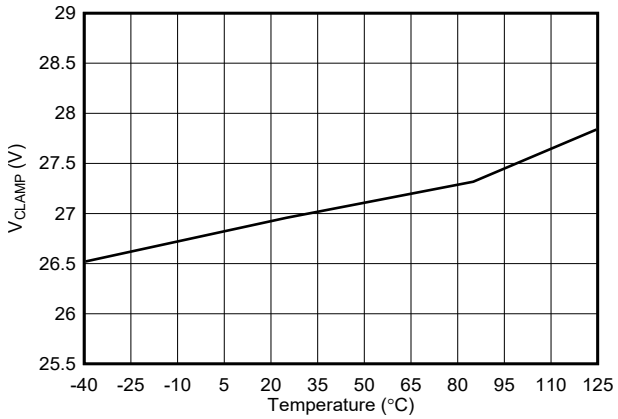
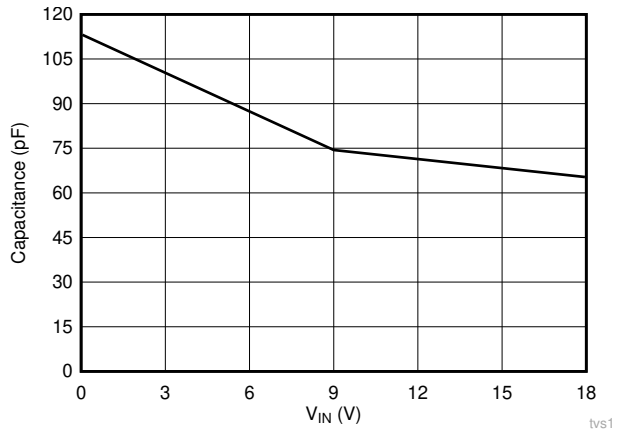


图 7-2. 8/20-µs Surge Clamping Response at 30 A



f = 1 MHz, 30 mVpp, IO to GND

图 7-3. Capacitance vs Voltage Bias

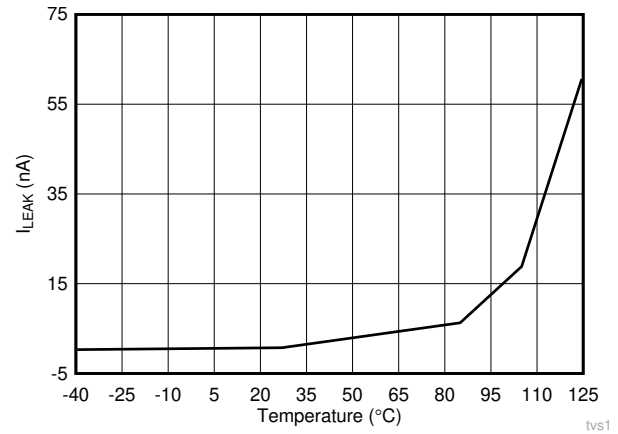


图 7-4. Leakage Current vs Temperature at 18 V

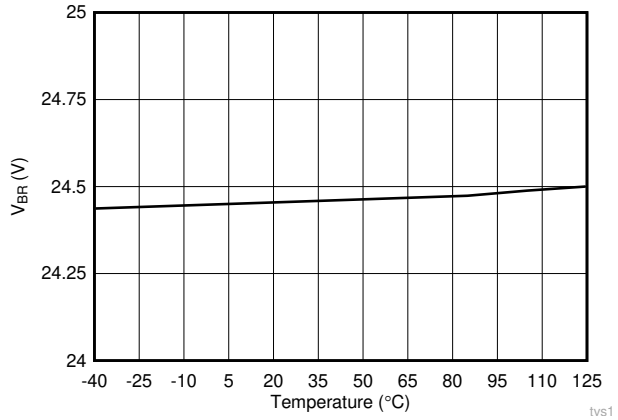


图 7-5. Breakdown Voltage (1 mA) vs Temperature

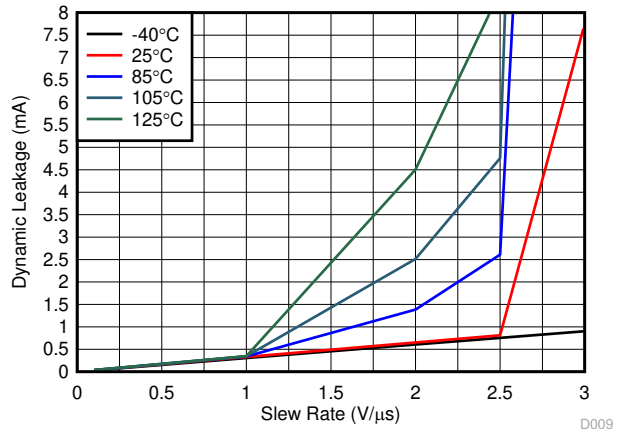


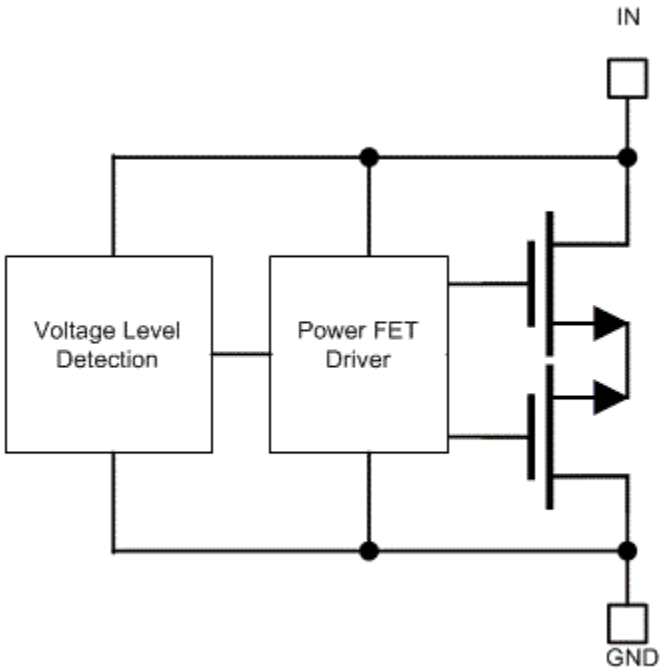
图 7-6. Dynamic Leakage vs Signal Slew Rate Across Temperature

8 Detailed Description

8.1 Overview

The TVS1801 is a bidirectional precision clamp with two integrated FETs driven by a feedback loop to tightly regulate the input voltage during an overvoltage event. This feedback loop leads to a very low dynamic resistance, giving a flat clamping voltage during transient overvoltage events like a surge.

8.2 Functional Block Diagram



8.3 Feature Description

The TVS1801 is a precision clamp that handles 30 A of IEC 61000-4-5 8/20-µs surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost, lower voltage tolerant downstream ICs. This device provides a bidirectional operating range, with a symmetrical V_{RWM} of ±18 V, designed for applications that have bipolar input signals or that must withstand reverse wiring conditions. The TVS1801 has minimal leakage at V_{RWM}, designed for applications where low leakage and power dissipation is a necessity. Built in IEC 61000-4-2 and IEC 61000-4-4 ratings make it a robust protection solution for ESD and EFT events and the TVS1801 wide ambient temperature range of –40°C to +125°C enables usage in harsh industrial environments.

8.4 Device Functional Modes

8.4.1 Protection Specifications

The TVS1801 is specified according to both the IEC 61000-4-5 and IEC 61643-321 standards. This enables usage in systems regardless of which standard is required by relevant product standards or best matches measured fault conditions. The IEC 61000-4-5 standard requires protection against a pulse with a rise time of 8 µs and a half-length of 20 µs, while the IEC 61643-321 standard requires protection against a much longer pulse with a rise time of 10 µs and a half-length of 1000 µs.

The positive and negative surges are imposed to the TVS1801 by a combination wave generator (CWG) with a 2-Ω coupling resistor at different peak voltage levels. For powered-on transient tests that need power supply bias, inductances are used to decouple the transient stress and protect the power supply. The TVS1801 is post-tested by assuring that there is no shift in device breakdown or leakage at V_{RWM}.

In addition, the TVS1801 has been tested according to IEC 61000-4-5 to pass a ±1-kV surge test through a 42-Ω coupling resistor and a 0.5-µF capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS1801 precision clamp can be used in applicationos that have that requirement.

The TVS1801 integrates IEC 61000-4-2 level 4 ESD Protection and 80 A of IEC 61000-4-4 EFT Protection. These combine to ensure that the device can protect against most common transient test requirements.

For more information on TI's test methods for Surge, ESD, and EFT testing, refer to the *TI's IEC 61000-4-x Tests for TI's Protection Devices* application report.

8.4.2 Reliability Testing

To ensure device reliability, the TVS1801 is characterized against 5000 repetitive pulses of 25-A IEC 61000-4-5 8/20-µs surge pulses at 125°C. The test is performed with less than 10 seconds between each pulse at high temperature to simulate worst-case scenarios for fault regulation. After each surge pulse, the TVS1801 clamping voltage, breakdown voltage, and leakage are recorded to ensure that there is no variation or performance degradation. By ensuring robust, reliable, high temperature protection, the TVS1801 enables fault protection in applications that must withstand years of continuous operation with no performance change.

8.4.3 Zero Derating

Unlike traditional diodes, the TVS1801 has zero derating of maximum power dissipation and ensures robust performance up to 125°C. Traditional TVS diodes lose up to 50% of their current carrying capability when at high temperatures, so a surge pulse above 85°C ambient can cause failures that are not seen at room temperature. The TVS1801 prevents this so the designer can see the surge protection regardless of temperature. Because of this, Flat-Clamp devices can provide robust protection against surge pulses that occur at high ambient temperatures, as shown in TI's *TVS Surge Protection in High-Temperature Environments* application report.

8.4.4 Bidirectional Operation

The TVS1801 is a bidirectional TVS with a symmetrical operating region. This allows for operation with positive and negative voltages, rather than just positive voltages like the unidirectional TVS1800. This allows for single chip protection for applications where the signal is expected to operate below 0 V or where there is a need to withstand a large common-mode voltage. In addition, in many cases, there is a system requirement to be able to withstand reverse wiring conditions, in many cases where a high voltage signal is accidentally applied to the system ground and a ground is accidentally applied to the input terminal. This causes a large reverse voltage on the TVS diode that it must be able to withstand. The TVS1801 is designed to not break down or see failures under reverse wiring conditions, for applications that must withstand these miswiring issues.

备注

If the applied signal is not expected to go below 0 V, a unidirectional device will clamp much lower in the reverse direction and should be used. In this case, the recommended device would be the TVS1800.

8.4.5 Transient Performance

During large transient swings, the TVS1801 will begin clamping the input signal to protect downstream conditions. While this prevents damage during fault conditions, it can cause leakage when the intended input signal has a fast slew rate. To keep power dissipation low and remove the chance of signal distortion, TI recommends that the designer keep the slew rate of any input signal on the TVS1801 below 2.5 V/µs at room temperature and below 0.7 V/µs at 125°C shown in 图 7-6. Faster slew rates will cause the device to clamp the input signal and draw current through the device for a few microseconds, increasing the rise time of the signal. This will not cause any harm to the system or to the device; it can, however, cause device overheating if the fast input voltage swings occur regularly.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TVS1801 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

9.2 Typical Application

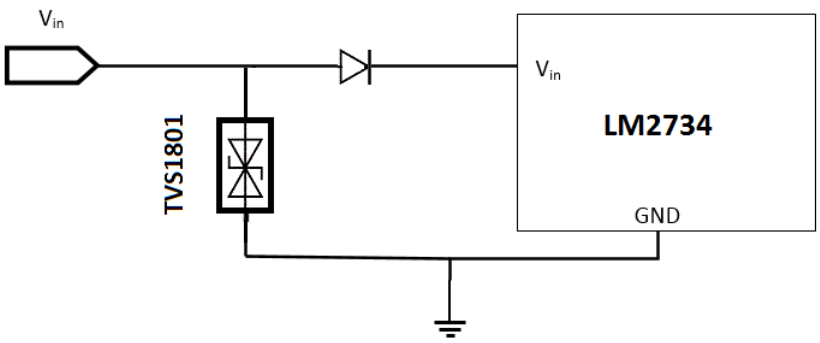


图 9-1. TVS1801 Application Schematic

9.2.1 Design Requirements

A typical operation for the TVS1801 would be protecting a 12-V input voltage line with a wide variance requiring extra standoff from the nominal voltage, up to 18 V, as shown in 图 9-1. In this example, a TVS1801 is protecting the input to a LM2734, a buck converter with an input voltage range of 20 V and an absolute maximum input voltage of 24 V. This input must be protected against transient voltage surge events, and must have protection for reverse applied voltage in case of cable shorts or in case of operator wiring error. Without any input protection, this input voltage will rise to hundreds of volts for multiple microseconds, and violate the absolute maximum input voltage and harm the device if a surge event is caused by lightning, coupling, ringing, or any other fault condition. TI's Flat-Clamp technology provides surge protection diodes that can maximize the useable voltage range and clamp at a safe level for the system.

9.2.2 Detailed Design Procedure

If the TVS1801 is in place to protect the device, the voltage will rise to the breakdown of the diode at 24.4 V during a surge event. The TVS1801 will then turn on to shunt the surge current to ground. With the low dynamic resistance of the TVS1801, even large amounts of surge current will have minimal impact on the clamping voltage. The dynamic resistance of the TVS1801 is around 50 mΩ, which means a 25-A surge current will cause a voltage raise of 25 A × 50 mΩ = 1.25 V. Because the device turns on at 24.4 V, this means the module input will be exposed to a maximum of 24.4 V + 1.25 V = 26.9 V during surge pulses, close to the LM2734 absolute maximum. Because this is a transient pulse, this will likely be safe for the system.

In addition, the TVS1801 provides protection against reverse voltage application that could accidentally be caused by shorts between pins. If – 12 V is applied to the V_{BUS} pin, the LM2734 will not be harmed because the series diode will prevent the voltage from being applied to the input, and the TVS1801 will not shunt current because the reverse working voltage is – 18 V. If the TVS1800 or an unidirectional device is used in this case, a – 12-V short would cause the device to shunt current until it fails.

Finally, the small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS1801 allows the device to be placed extremely close to the input connector, which lowers the length of the path fault current going through the system compared to larger protection solutions.

9.2.3 Application Curves

图 9-2 shows how the device will clamp the overvoltage when a surge is applied to a system with the TVS1801.

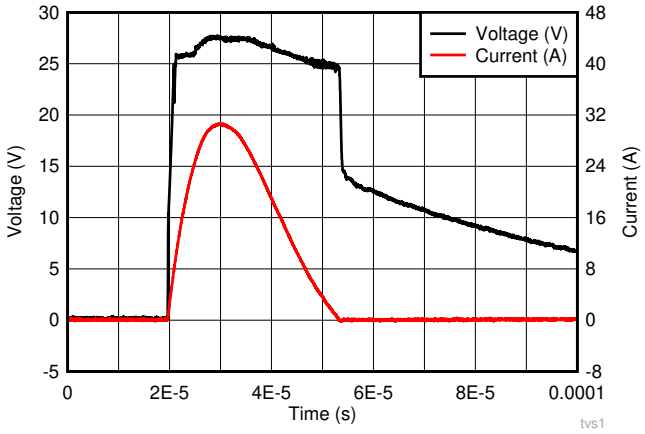


图 9-2. Surge Waveform at 30 A

10 Power Supply Recommendations

The TVS1801 is a clamping device so there is no need to power it. To ensure the device functions properly, do not violate the recommended V_{IN} voltage range (– 18 V to 18 V).

11 Layout

11.1 Layout Guidelines

The optimum placement is close to the connector. EMI during an ESD event can couple from the tested trace to other nearby unprotected traces, which could result in system failures. The PCB designer must minimize the possibility of EMI coupling by keeping all unprotected traces away from protected traces between the TVS and the connector. Route the protected traces straight. Use rounded corners with the largest radii possible to eliminate any sharp corners on the protected traces between the TVS1801 and the connector. Electric fields tend to build up on corners, which could increase EMI coupling.

Ensure that the thermal pad on the layout is floating rather than grounded. Grounding the thermal pad will impede the operating range of the TVS1801, and can cause failures when the applied voltage is negative. A floating thermal pad allows the maximum operating range without sacrificing any transient performance.

11.2 Layout Example

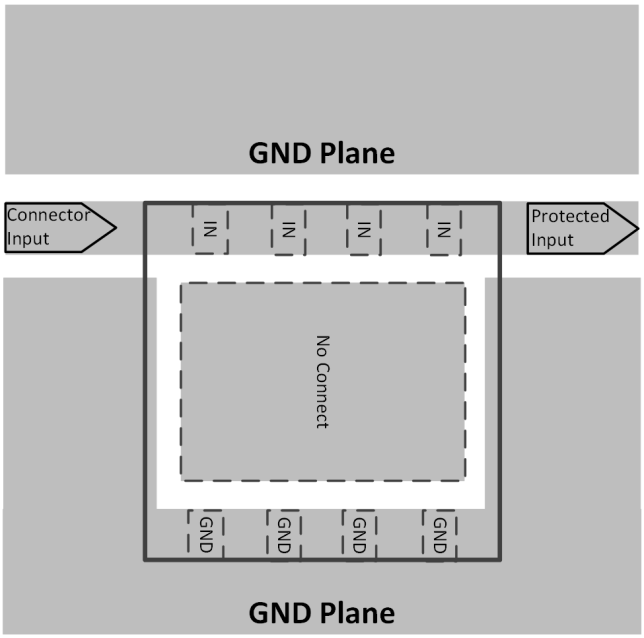


图 11-1. TVS1801 Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documenation

For related documenation, see the following:

- Texas Instruments, *Flat-Clamp Surge Protection Technology for Efficient System Protection* white paper
- Texas Instruments, *TI's IEC 61000-4-x Tests for TI's Protection Devices* application report
- Texas Instruments, *TVS Surge Protection in High-Temperature Environments* application report

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TVS1801DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1PUP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

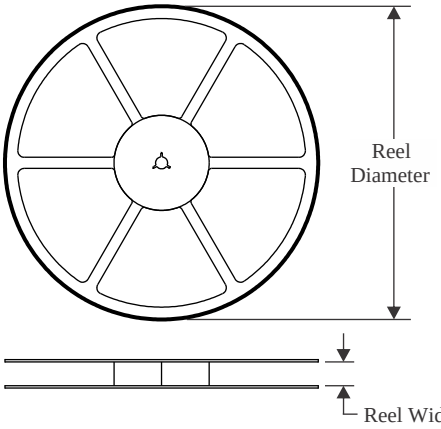
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

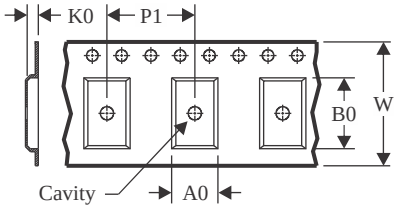
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

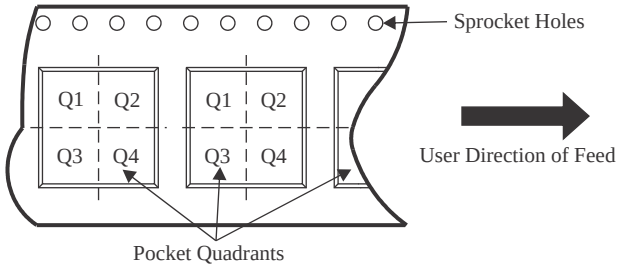


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

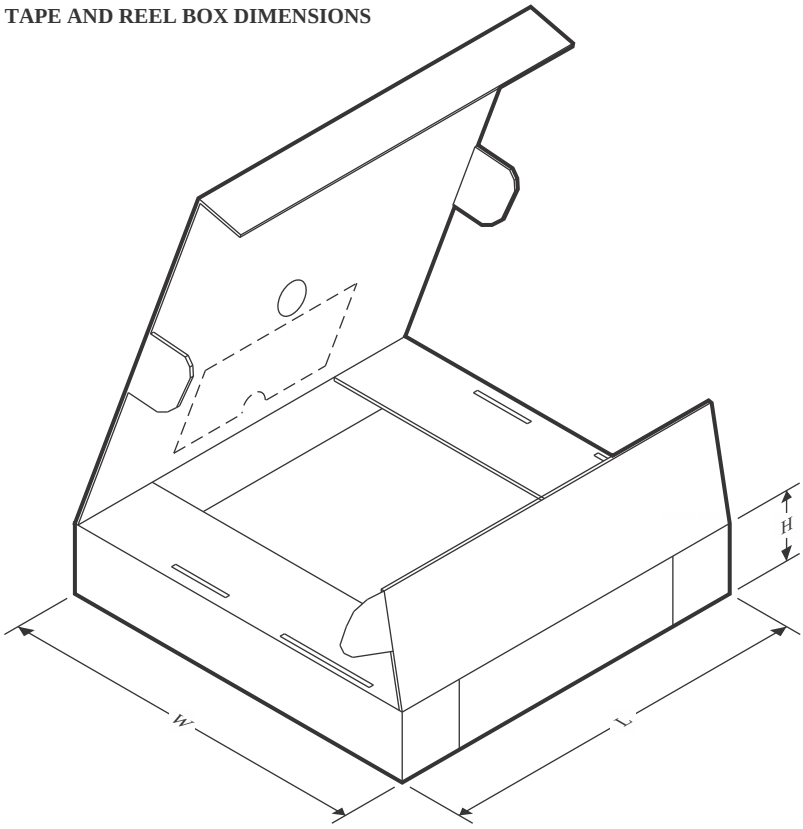
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS1801DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS1801DRBR	SON	DRB	8	3000	338.0	355.0	50.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

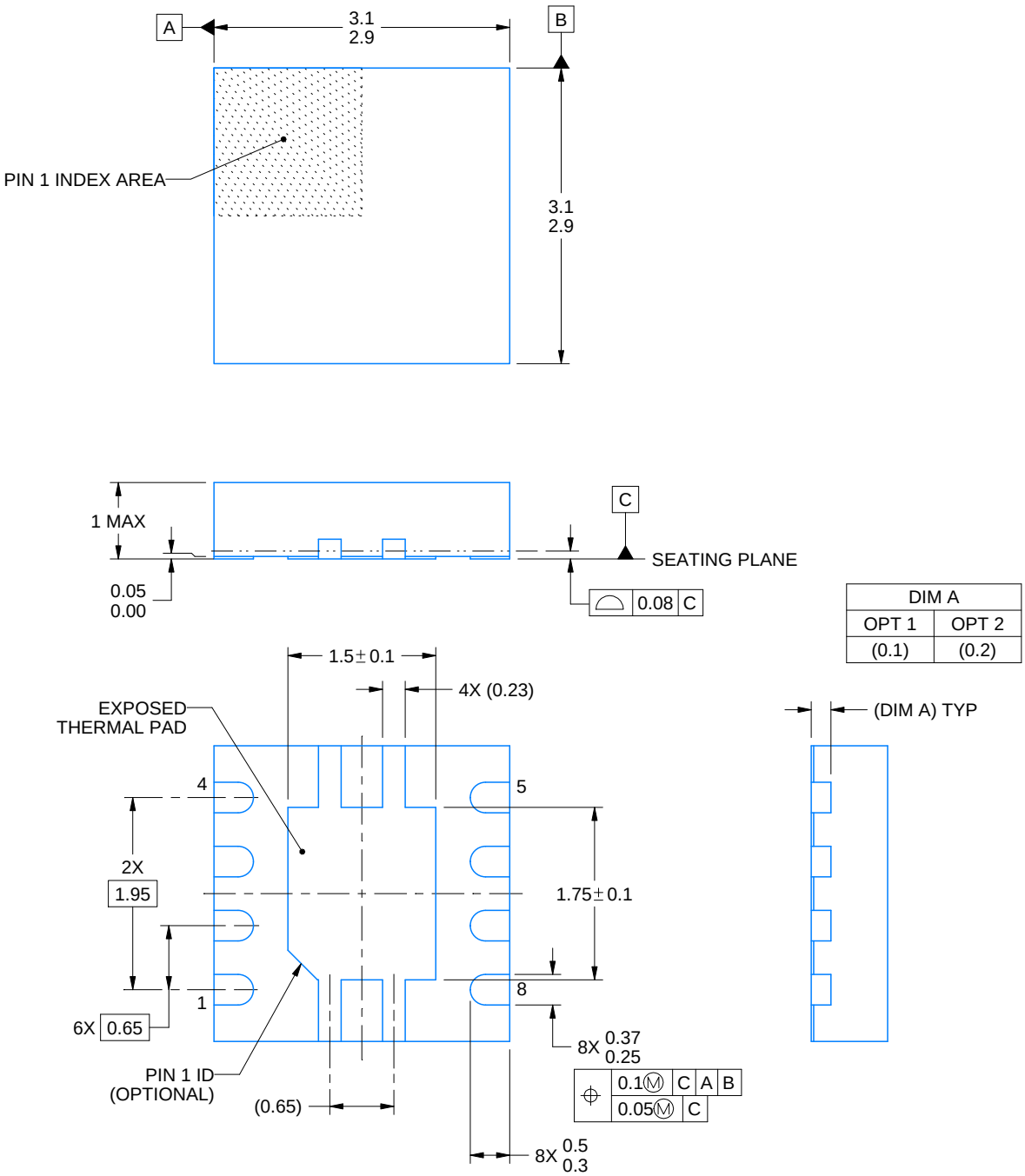
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

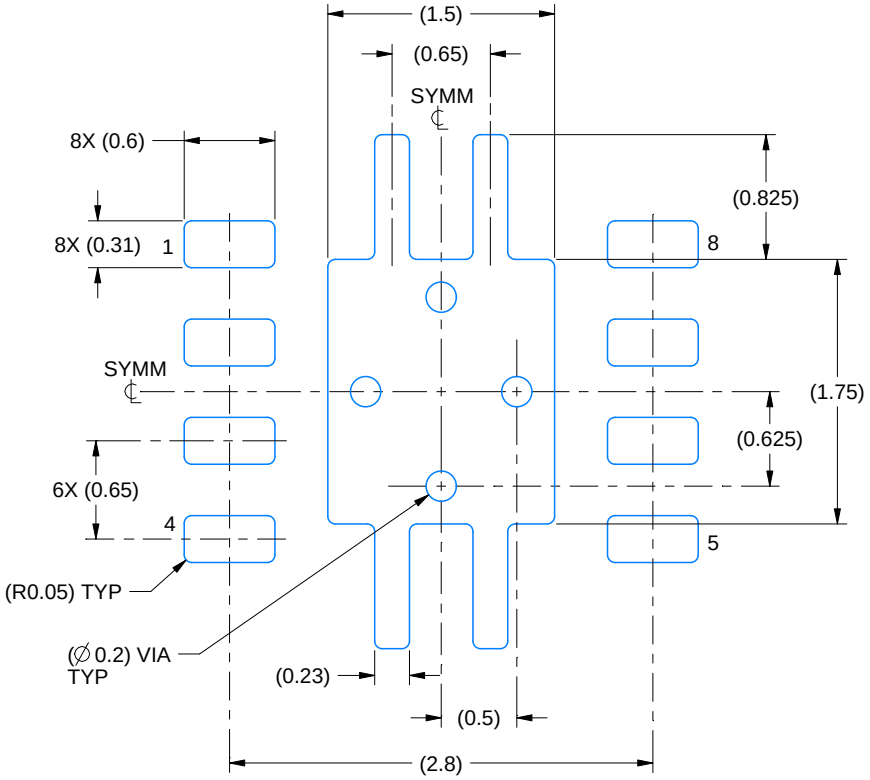
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

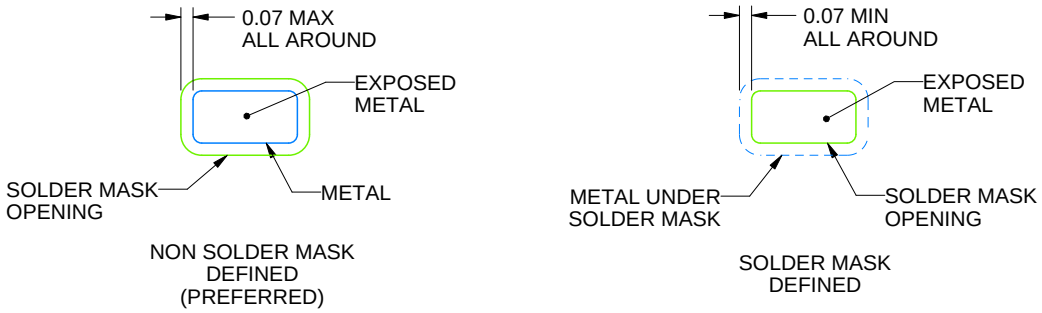
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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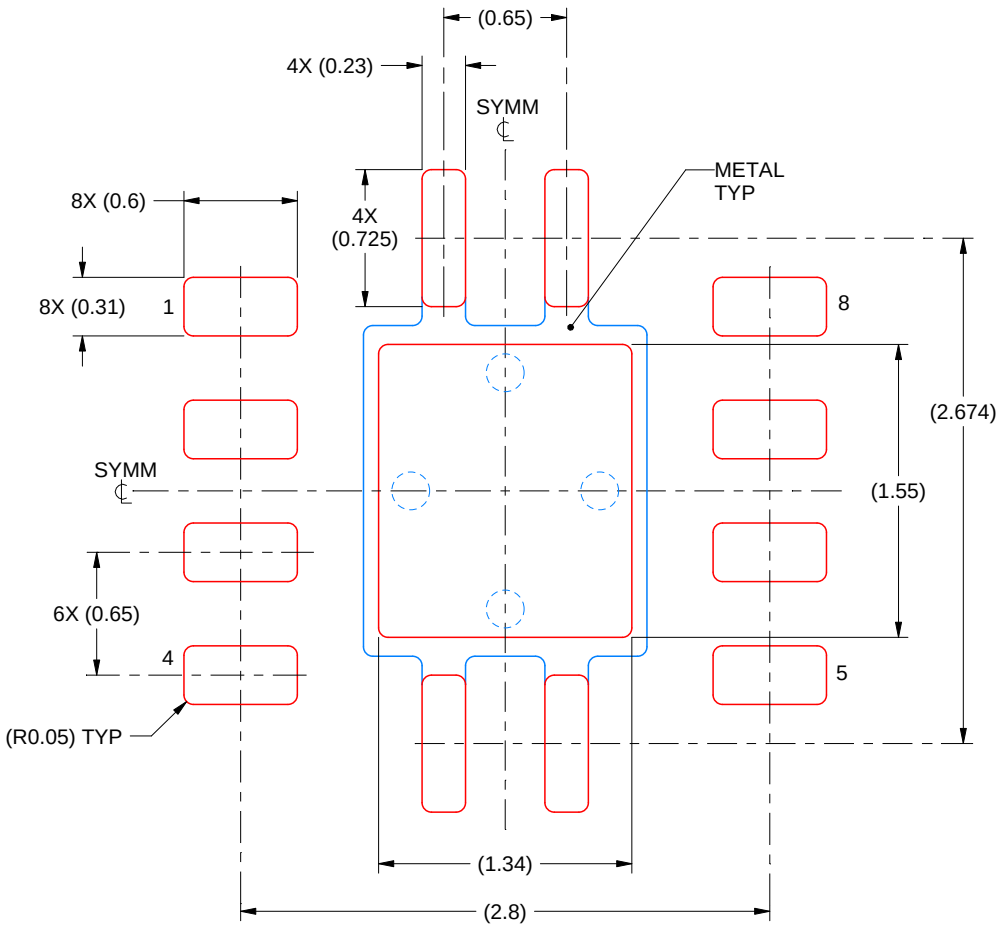
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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