









TSM24B ZHCSTB3A - OCTOBER 2023 - REVISED OCTOBER 2023

TSM24B 采用 SOT-23 封装的单向浪涌保护器件

1 特性

- 强大的浪涌保护:
 - IEC61000-4-5 (8/20µs) : 20A
- 对于持续 8/20µs 的 20 A 浪涌电流,钳位电压低至 33 V (典型值),可保护下游元件
- 单向极性,可优化单端数据线路和电源轨上的钳位
- 工作电压为 24V,用于保护 12V 系统中的信号
- 75nA 低漏电流(最大值)
- 24pF的低 I/O 电容(典型值)
- 集成 IEC 61000-4-2 ESD 保护
 - ±30kV 接触放电
 - ±30kV 气隙放电
- 小型 SOT-23 引线式封装,可更大限度地减小布板 空间并实现自动光学检查 (AOI)

2 应用

- 工业传感器
- 控制器局域网 (CAN)
- PLC I/O 模块
- 24V 电源线或数字输入或输出线
- 电器
- 医疗设备
- 电机驱动器

3 说明

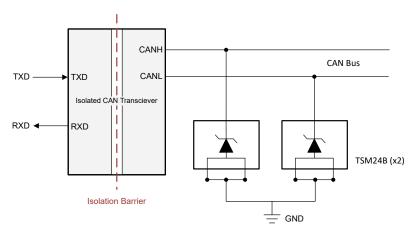
TSM24B 是 TI 浪涌保护器件系列的一款产品。 TSM24B 可将高达 20 A 的 IEC 61000-4-5 故障电流可 靠分流,从而保护系统免受高功率瞬态冲击或雷击。 TSM24B 旨在耗散超过 IEC 61000-4-2 国际标准所规 定最高水平(±30kV 接触放电,±30kV 气隙放电)的 ESD 冲击。TSM24B 在浪涌事件期间进行钳制,确保 系统在 I PP = 20 A 时承受低于 33 V 的电压。

此外, TSM24B 采用小型引线式 SOT-23 (DBZ) 封 装,尺寸大概比业界通用 SMA 封装小 50%。该器件具 有极低的器件泄露,旨在尽可能地降低对受保护线路的 影响。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
TSM24B	DBZ (SOT-23 , 3)	2.92mm × 2.37mm

- 如需了解所有可用封装,请参阅数据表末尾的可订购产品附 (1)
- 封装尺寸(长×宽)为标称值,并包括引脚(如适用)。 (2)



功能方框图



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4 Revision History 注:以前版本的页码可能与当前版本的页码不同

С	hanges from Revision * (October 2023) to Revision A (October 2023)	Page
•	Changed I _{LEAK} typ value from: 50 nA to: 25 nA and max value from: 100 nA to: 75 nA	5
•	Changed V _{BR} min value from: 24.8 V to: 26.5 V	5
•	Changed V _{CLAMP} typ value from: 37 V to: 33 V and deleted the max value	5



5 Pin Configuration and Functions

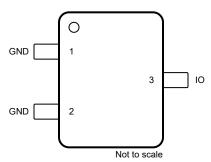


图 5-1. DBZ Package, 3-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION	
NAME	NO.	IIFE\/	DESCRIPTION	
Ю	3	I/O	Surge and ESD protected IO	
GND	1, 2	G	Connect to ground. To achieve the rated performance, connect pin 1 and 2 together on the PCB as close to the device as possible.	

Product Folder Links: TSM24B

(1) I = Input, O = Output, I/O = Input or Output, G = Ground



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	Parameter	MIN	MAX	UNIT
P _{PPM}	IEC 61000-4-5 Surge (t_p = 8/20 μ s) Peak Pulse Power at 25 °C $^{(2)}$		800	W
I _{PPM}	IEC 61000-4-5 Surge (t_p = 8/20 μ s) Peak Pulse Current at 25 °C $^{(2)}$		20	Α
T _A	Operating free-air temperature	-40	125	°C
T _{stg}	Storage temperature	- 65	155	°C

Operation outside the Absolute Maximum Rating may cause permanent device damage. Absolute Maximum Rating do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Condition. If used outside the Recommended Operating Condition but within the Absolute Maximum Rating, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings -JEDEC Specifications

Parameter		Test Conditions	VALUE	UNIT
V	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2500	V
V _(ESD)	Lieutiostatic disorialge	Charged device model (CDM), per JEDEC specification JS-002, all pins ⁽²⁾	±1000	V

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

	Parameter	Test Conditions	VALUE	UNIT
V	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	\/
V _(ESD)	Liectiostatic discharge	IEC 61000-4-2 Air Discharge, all pins	±30000	v

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
V _{IN}	Input voltage	0	24	V
T _A	Operating free-air temperature	-40	125	°C

6.5 Thermal Information

		TSM24B	
	THERMAL METRIC ⁽¹⁾	DBZ (SOT-23)	UNIT
		3 PINS	
R ₀ JA	Junction-to-ambient thermal resistance	220.6	°C/W
R _{θ JC(top)}	Junction-to-case (top) thermal resistance	122.8	°C/W
R ₀ JB	Junction-to-board thermal resistance	54.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.6	°C/W
ΨЈВ	Junction-to-board characterization parameter	53.7	°C/W
R _{θ JC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Product Folder Links: TSM24B English Data Sheet: SLVSHG9

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⁽²⁾ Voltages are with respect to GND unless otherwise noted.

JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

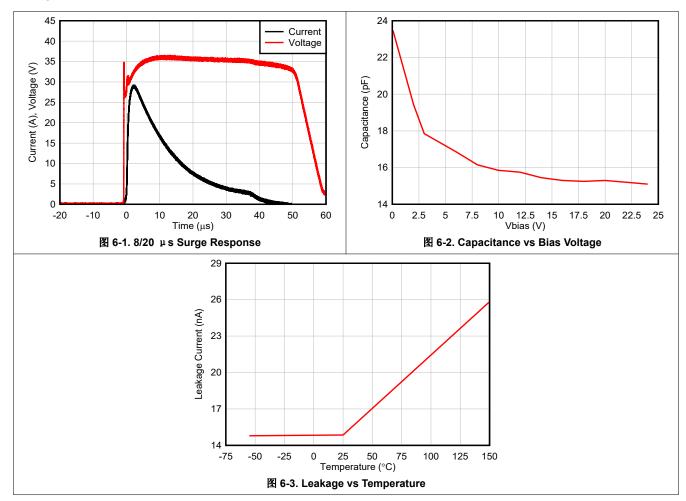
6.6 Electrical Characteristics

At T_A = 25°C unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	I _{IO} < 100 nA			24	V
I _{LEAK}	Leakage current at V _{RWM}	V _{IO} = 24 V, I/O to GND		25	75	nA
V_{BR}	Breakdown voltage, I/O to GND (1)	I _{IO} = 10 mA	26.5			V
V _{FWD}	Forward Voltage, GND to I/O (1)	I _{IO} = 10 mA		0.7		V
V _{CLAMP}	Surge clamping voltage, t _p = 8/20 μs (2)	I _{PP} = 20 A, I/O to GND		33		V
V _{CLAMP}	Surge clamping voltage, t _p = 8/20 μs (2)	I _{PP} = 20 A, GND to I/O		6	8	V
C _{LINE}	Line capacitance, IO to GND	V _{IO} = 0 V, f = 1 MHz		24	37.5	pF

- (1) V_{BR} is defined as the voltage when 10 mA is applied in the positive-going direction.
- (2) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.

6.7 Typical Characteristics



Product Folder Links: TSM24B



7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TSM24B is a diode type TVS that provides a path to ground for dissipating transient voltage spikes (such as ESD or surge) on signal lines and power lines. The device should be connected in parallel to the down stream circuitry it is protecting. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the *ESD Packaging and Layout Guide*.

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, TI's IEC 61000-4-x Testing application note
- · Texas Instruments, ESD Layout Guide user's guide
- Texas Instruments, ESD Protection Diodes EVM user's guide
- · Texas Instruments, Generic ESD Evaluation Module user's guide
- Texas Instruments, Reading and Understanding an ESD Protection Data Sheet user's guide

8.2 接收文档更新通知

要接收文档更新通知,请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册,即可每周接收产品信息更改摘要。有关更改的详细信息,请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E[™] 中文支持论坛是工程师的重要参考资料,可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题,获得所需的快速设计帮助。

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8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序,可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级,大至整个器件故障。精密的集成电路可能更容易受到损坏,这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI术语表本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: TSM24B



www.ti.com 27-Oct-2023

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
							(6)				
TSM24BDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	35H8	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

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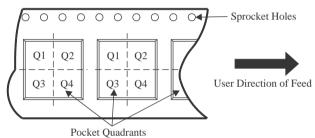
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSM24BDBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

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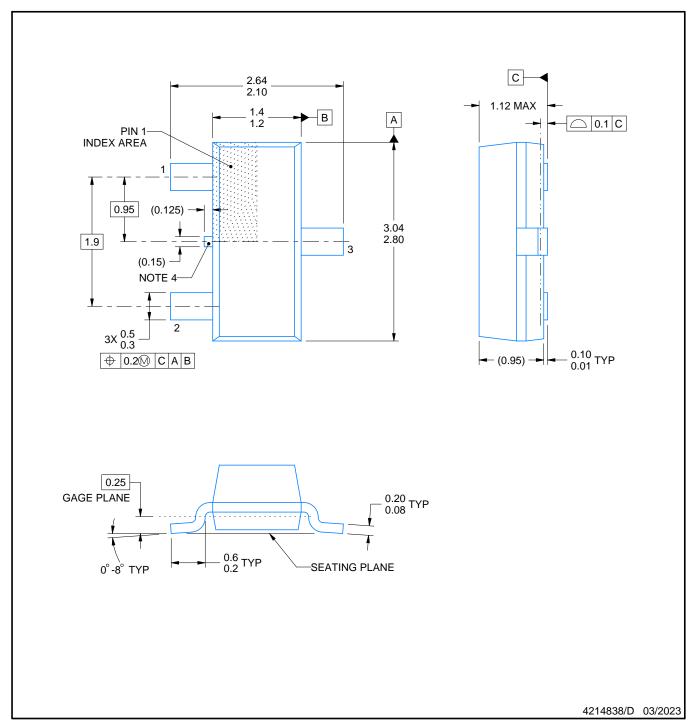


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
TSM24BDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0	



SMALL OUTLINE TRANSISTOR



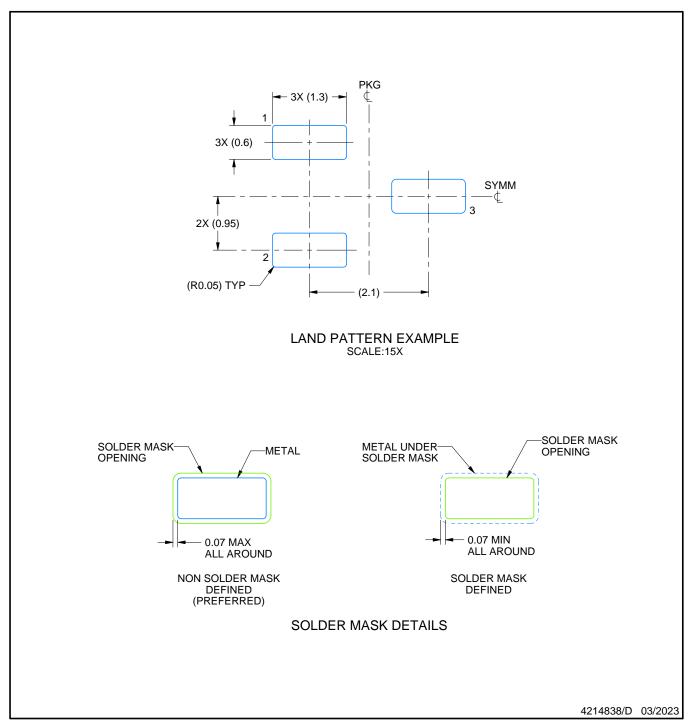
NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 Reference JEDEC registration TO-236, except minimum foot length.

- 4. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR

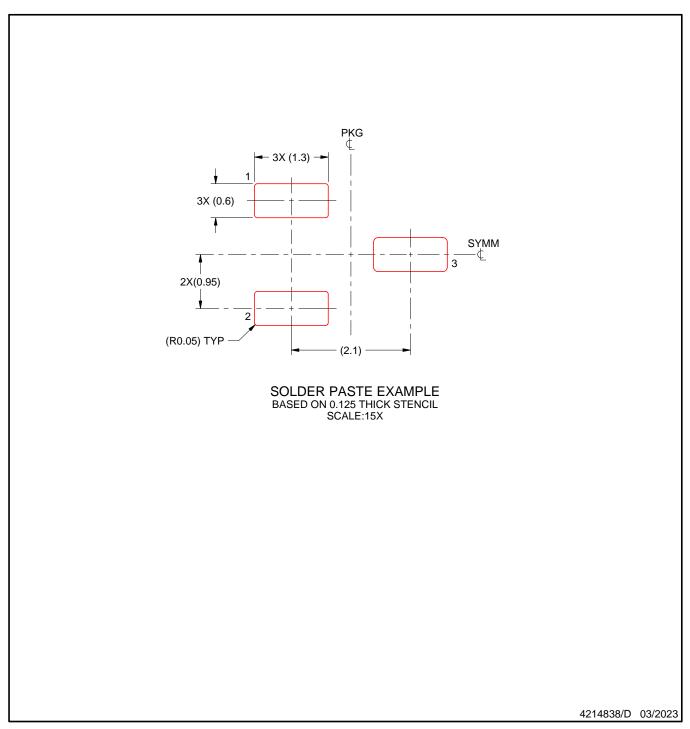


NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.



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