TPS7H3014-SP 耐辐射加固保障、14V、4 通道序列发生器

1 特性

- 辐射性能：
  - 耐辐射加固保障 (RHA) 高达 100krad(Si) 总电离剂量 (TID)
  - 单粒子锁定 (SEL)、单粒子烧毁 (SEB) 和单粒子栅穿 (SEGR) 对于线性能量传递 (LET) 的抗扰度高达 75MeV-cm^2/mg
  - 单粒子功能中断 (SEFI) 和单粒子瞬变 (SET) 对于 LET 的额定值高达 75MeV-cm^2/mg
- 宽电源输入电压范围 (V_{IN})：3V 至 14V
- 使用单个器件对多达 4 个电压轨进行定序和监控
  - 菊花链连接功能支持扩展的通道数
- 单电阻器可编程全局计时器用于：
  - 定序开启和关闭延迟
  - 定序开启到稳压的时间
- 倒序定序关闭
- 高精度阈值电压和迟滞电流
  - 电压、温度和辐射 (TID) 范围内的 V_{TH_SENSEx} 为 599mV ± 1%
  - 电压、温度和辐射 (TID) 范围内的 I_{HYS_SENSEx} 为 24 µA ± 3%
- 具有 1.6V 至 7V 可编程上拉电压的推挽输出
  - 全局 ENx 上拉域 (V_{PULL_UP1})
  - 通用 SEQ_DONE 和 PWRGD 上拉域 (V_{PULL_UP2})
- $\overline{FAULT}$ 开漏输出，用于监控状态机引起的故障
- 支持军用（ –55°C 至 125°C ）温度范围

2 应用

- 卫星电力系统 (EPS)
- 复杂数字处理器的控制序列和监控，例如：适用于航天应用的 FPGA、SoC、AFE 和电源系统

3 说明

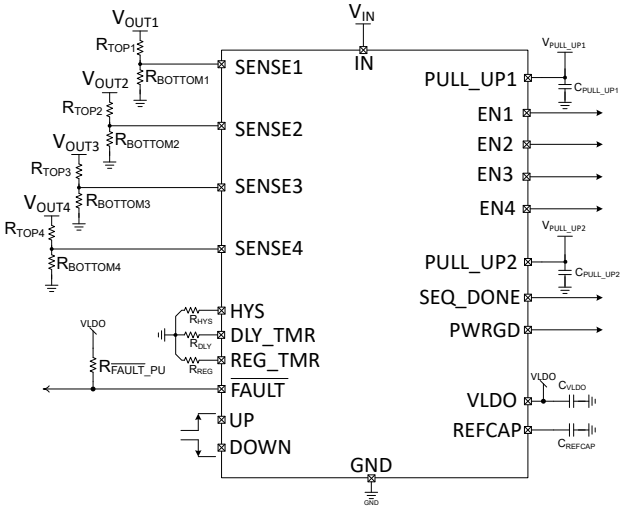
TPS7H3014 是一款集成式 3V 至 14V、四通道耐辐射加固保障电源序列发生器。通过在菊花链配置中连接多个器件可扩展通道数。该器件可为具有高电平有效（“开启”）输入的集成电路 (IC) 提供定序开启和关闭控制信号。此外，还提供了 SEQ_DONE 和 PWRGD 标志，用于监控电源树的序列和电源状态。

精确的 599mV ± 1% 阈值电压和 24 µA ± 3% 迟滞电流提供可编程上升和下降监控电压。上升和下降延迟时间可通过单个电阻进行全局编程。此外，提供的至稳压时间计时器可跟踪 SENSEx 上的上升电压。除了这些特性外，该器件还包含一个故障检测引脚，用于监控内部产生的故障并为电源时序航天应用提供更高的系统级可靠性。QML 型号 5962R23201VXC 提供了标准微电路图 (SMD)。

器件信息

器件型号 (1)	等级 (2)	封装 (3)
5962R23201VXC	QMLV-RHA	22 引脚陶瓷 (CFP) 6.21mm x 7.69mm 质量 = 415.6mg
TPS7H3014HFT/EM	工程样片	

(1) 有关更多信息，请参阅第 5 节中的表格。
(2) 有关器件等级的其他信息，请查看 SLYB235。
(3) 尺寸和质量为标称值。



典型应用

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4 Device Options

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H3014-SP	TID of 100krad(Si) RLAT, DSEE free to 75 MeV-cm^2/mg	QMLV-RHA	22-pin CFP HFT	5962R23201VXC(3)
	None	Engineering model	22-pin CFP HFT	TPS7H3014HFT/EM

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view SLYB235.
(3) Product preview.

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5 Pin Configuration and Functions

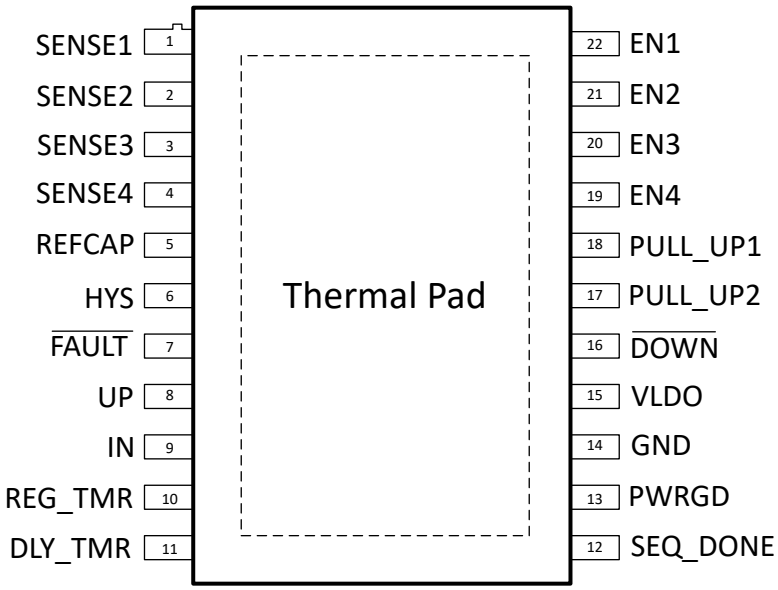

图 5-1. HFT Package, 22-Pin CFP (Top View)

表 5-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
SENSE1	1	I	Non-inverting input of the comparator used to monitor the first rail to be sequenced up/down. To set the V_{ON} and V_{OFF} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE1. A voltage greater than 599mV (typ) on this pin is considered as a regulated voltage rail (V_{ON}). The V_{OFF} is set by the I_{HYS} current and the top resistor from the resistive divider. Refer to Top and Bottom Resistive Divider Design Equations.
SENSE2	2	I	Non-inverting input of the comparator used to monitor the second rail to be sequenced up/down. To set the V_{ON} and V_{OFF} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE2. A voltage greater than 599mV (typ) on this pin is considered as a regulated voltage rail (V_{ON}). The V_{OFF} is set by the I_{HYS} current and the top resistor from the resistive divider. Refer to Top and Bottom Resistive Divider Design Equations.
SENSE3	3	I	Non-inverting input of the comparator used to monitor the third rail to be sequenced up/down. To set the V_{ON} and V_{OFF} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE3. A voltage greater than 599mV (typ) on this pin is considered as a regulated voltage rail (V_{ON}). The V_{OFF} is set by the I_{HYS} current and the top resistor from the resistive divider. Refer to Top and Bottom Resistive Divider Design Equations.
SENSE4	4	I	Non-inverting input of the comparator used to monitor the fourth rail to be sequenced up/down. To set the V_{ON} and V_{OFF} voltages, connect an external resistive divider between the rail to be monitored and GND with the middle point tied to SENSE4. A voltage greater than 599mV (typ) on this pin is considered as a regulated voltage rail (V_{ON}). The V_{OFF} is set by the I_{HYS} current and the top resistor from the resistive divider. Refer to Top and Bottom Resistive Divider Design Equations.
REFCAP	5	O	1.2V internal reference. Requires a 470nF external capacitor to GND. Do not load this pin.
HYS	6	O	Hysteresis. Connect a 50kΩ resistor between this pin and GND, to program the hysteresis current (typically 24 μA) at SENSE1 to SENSE4. Is recommended using a resistor with a 0.1% or better tolerance for hysteresis current accuracy.
$\overline{\text{FAULT}}$	7	O	$\overline{\text{FAULT}}$. Open drain output which is forced low by the state machine to indicate an internally generated fault. Is recommended to pull-up this pin to VLDO with a 10kΩ resistor. However, a different external voltage source can be used as the pull-up as long as it is stable before commanding the sequence up and never drops below 1V during the operation of the device.

表 5-1. Pin Functions（续）

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
UP	8	I	Non-inverting input of a comparator. A rising voltage greater than 599mV (typ) will induce a rising edge and will start a sequence up. This pin can be driven by an external controller, or connected to a main rail trough an external resistive divider with the middle point connected to the UP pin to start the sequence up automatically. This threshold has a fixed hysteresis of 100mV (typ).
IN	9	I	Input supply to the device. Input voltage range is from 3V to 14V. Connect at least a 0.1 µF ceramic capacitor as close as possible to the pin.
REG_TMR	10	I/O	Time to regulation timer. Connect a resistor to GND between 10.5kΩ and 1.18MΩ to set the allowed time for a $SENSE_x$ rail to reach the regulation threshold (V_{ON}). The delay can be adjusted from 0.25ms to 25ms. Leave this pin floating to deactivate this feature.
DLY_TMR	11	I/O	Delay timer. Connect a resistor to GND between 10.5kΩ and 1.18MΩ to set the sequence up and down delay. The delay can be adjusted from 0.25ms to 25ms. Leave this pin floating for no delay.
SEQ_DONE	12	O	Sequence done. Push-pull output with V_{OH} level set by PULL_UP2 input supply voltage. Indicates when the sequence up or down is completed.
PWRGD	13	O	Power Good. Push-pull output with V_{OH} level set by PULL_UP2 input supply voltage. Indicates when all rails (SENSE1 to SENSE4) are in regulation (greater than V_{ONx}).
GND	14	—	Ground.
VLDO	15	O	Output of internal regulator. Requires at least 1 µF external ceramic capacitor to GND. Allowed loading of this regulator are: $\overline{\text{FAULT}}$ pull-up using a 10kΩ resistor or to turn-off unused channels by connecting directly to SENSE2 to SENSE4 as needed.
$\overline{\text{DOWN}}$	16	I	Non-inverting input of a comparator. A falling voltage lower than 498mV (typ) will induce a falling edge and will start a sequence down. This pin can be driven by an external controller, or connected to a main rail through an external resistive divider with the middle point connected to the $\overline{\text{DOWN}}$ pin to start the sequence down automatically. This threshold has a fixed hysteresis of 100mV (typ).
PULL_UP2	17	I	Input supply voltage to program the pull-up voltage for the push-pull output stage on SEQ_DONE and PWRGD. Connect at least a 1 µF ceramic capacitor as close as possible to the pin.
PULL_UP1	18	I	Input supply voltage to program the global pull-up voltage for the push-pull output stages on EN1 to EN4. Connect at least a 1 µF ceramic capacitor as close as possible to the pin.
EN4	19	O	Enable 4. Push pull output with V_{OH} level set by the PULL_UP1 input supply voltage. Connect to the logic enable signal of the device to control and to be monitored by SENSE4.
EN3	20	O	Enable 3. Push pull output with V_{OH} level set by the PULL_UP1 input supply voltage. Connect to the logic enable signal of the device to control and to be monitored by SENSE3.
EN2	21	O	Enable 2. Push pull output with V_{OH} level set by the PULL_UP1 input supply voltage. Connect to the logic enable signal of the device to control and to be monitored by SENSE2.
EN1	22	O	Enable 1. Push pull output with V_{OH} level set by the PULL_UP1 input supply voltage. Connect to the logic enable signal of the device to control and to be monitored by SENSE1.
Thermal pad		—	Internally grounded. It is recommended to connect this metal thermal pad to a large ground plane for effective heat dissipation.
Metal lid	Lid	—	The lid is internally connected to the thermal pad and GND through the seal ring.

(1) I = Input, O = Output, I/O = Input or Output, — = Other

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input voltage	IN	–0.3	16	V
	UP, $\overline{\text{DOWN}}$	–0.3	7.5	
	SENSE1, SENSE2, SENSE3, SENSE4	–0.3	3.6	
	PULL_UP1, PULL_UP2	–0.3	7.5	
	$\overline{\text{FAULT}}$	–0.3	7.5	
	DLY_TMR, REG_TMR	–0.3	3.6	
Output voltage	VLDO	–0.3	3.6	V
	EN1, EN2, EN3, EN4	–0.3	7.5	
	REFCAP	–0.3	2	
	HYS	–0.3	3.6	
	SEQ_DONE, PWRGD	–0.3	7.5	
Output current	EN1, EN2, EN3, EN4	–20	20	mA
	SEQ_DONE, PWRGD	–20	20	
Junction temperature	T_J	–65	150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages values are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range, T_A = – 55°C to 125°C (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
Input voltage	IN	3		14	V
	UP, $\overline{\text{DOWN}}$	0		7	
	SENSE1, SENSE2, SENSE3, SENSE4	0		3.5	
	PULL_UP1, PULL_UP2	1.6		7	
	$\overline{\text{FAULT}}$	0		7	
Output voltage	EN1, EN2, EN3, EN4	0		7	V
	SEQ_DONE, PWRGD	0		7	
Output current	EN1, EN2, EN3, EN4	– 10		10	mA
	SEQ_DONE,PWRGD	– 10		10	
	$\overline{\text{FAULT}}$	– 2			
Junction temperature	T_J	– 55		125	°C
Input voltage slew rate	SR_{IN}	0.001		10	V/µs

(1) All voltages values are with respect to GND.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7H3014-SP HFT (CFP) 22 pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS		SUB-GROUP (3)	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGES AND CURRENTS								
I_{Q_IN}	V_{IN} quiescent current	In Waiting to sequence up and down states with all outputs floating. See State Diagram		1, 2, 3		2.5	4	mA
$UVLO_{RISE}$	V_{IN} rising undervoltage lockout			1, 2, 3	2.72	2.79	2.84	V
$UVLO_{FALL}$	V_{IN} falling udervoltage lockout			1, 2, 3	2.59	2.64	2.69	V
V_{LDO}	Internal linear regulator output voltage	5V ≤ V_{IN} ≤ 14V		1, 2, 3	3.19	3.29	3.38	V
		V_{IN} < 3.24V		1, 2, 3	97%	99%		× V_{IN}
REFCAP	Internal bandgap voltage			1, 2, 3	1.188	1.2	1.212	V
V_{POR_IN}	Power on reset voltage (4)	1.6V ≤ V_{PULL_UPx} ≤ 7V, V_{OL} ≤ 320mV with I_{ENx} = –2mA		1, 2, 3		1.41	2	V
$V_{POR\_PULL\_UPx}$	Power on reset voltage (5)	V_{IN} = 0V, V_{OL} ≤ 320mV with I_{ENx} = –100µA		1, 2, 3		0.89	1.4	V
SENSE1 TO SENSE4, UP AND $\overline{\text{DOWN}}$ COMPARATOR INPUTS								
V_{TH_SENSEx}	Threshold voltage at SENSEx			1, 2, 3	593	599	605	mV
I_{HYS_SENSEx}	SENSEx hysteresis current	V_{SENSEx} = 700mV		1, 2, 3	23.28	24	24.72	µA
I_{LKG_SENSEx}	Input leakage current at SENSEx	V_{SENSEx} = 500mV		1, 2, 3		2	100	nA
V_{TH_UP}	Rising threshold voltage at UP	V_{UP} rising to 1V		1, 2, 3	580	598	615	mV
$V_{TH\_\overline{DOWN}}$	Falling threshold voltage at $\overline{\text{DOWN}}$	$V_{\overline{DOWN}}$ falling from 1V		1, 2, 3	483	498	512	mV
$V_{HYS\_UP\_\overline{DOWN}}$	UP and $\overline{\text{DOWN}}$ hysteresis voltage			1, 2, 3		100		mV
$I_{LKG\_UP\_\overline{DOWN}}$	Input leakage current at UP and $\overline{\text{DOWN}}$	V_{UP} = $V_{\overline{DOWN}}$ = 500mV		1, 2, 3		2	100	nA
V_{TURN_OFF}	Channel 2, 3, 4 turn off voltage			1, 2, 3	87%	89%	91%	× VLDO
EN1 TO EN4, SEQ_DONE AND PWRGD PUSH PULL OUTPUTS								
V_{OL_ENx}	Low-level ENx output voltage	1.6V ≤ V_{PULL_UP1} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			10%	x V_{PULL_UP1}
			I_{LOAD} = –10mA	1, 2, 3			25%	
V_{OH_ENx}	High-level ENx output voltage	1.6V ≤ V_{PULL_UP1} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	90%			
			I_{LOAD} = 10mA	1, 2, 3	70%			
$V_{OL\_SEQ\_DONE}$	Low-level SEQ_DONE output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			10%	x V_{PULL_UP2}
			I_{LOAD} = –10mA	1, 2, 3			25%	
$V_{OH\_SEQ\_DONE}$	High-level SEQ_DONE output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	90%			
			I_{LOAD} = 10mA	1, 2, 3	70%			
V_{OL_PWRGD}	Low-level PWRGD output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = –2mA	1, 2, 3			10%	
			I_{LOAD} = –10mA	1, 2, 3			25%	
V_{OH_PWRGD}	High-level PWRGD output voltage	1.6V ≤ V_{PULL_UP2} ≤ 7V	I_{LOAD} = 2mA	1, 2, 3	90%			
			I_{LOAD} = 10mA	1, 2, 3	70%			

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6.5 Electrical Characteristics（续）

Over 3V ≤ V_{IN} ≤ 14V, R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS		SUB-GROUP (3)	MIN	TYP	MAX	UNIT
$PULL\_UPx_{LKG}$	PULL_UPx leakage current	V_{PULL_UPx} = 7V		1, 2, 3		48	121	µA
SR_{ENx_RISE}	Enable rising output voltage slew rate	10% to 90% of V_{PULL_UP1}, R_{LOAD} = 50kΩ, C_{LOAD} = 100pF	1.6V ≤ V_{PULL_UP1} ≤ 7V	9, 10, 11	17	125		V/µs
$SR_{SEQ\_DONE\_RISE}$	SEQ_DONE rising output voltage slew rate	10% to 90% of V_{PULL_UP2}, R_{LOAD} = 50kΩ, C_{LOAD} = 100pF	1.6V ≤ V_{PULL_UP2} ≤ 7V	9, 10, 11	17	125		
SR_{PWRGD_RISE}	PWRGD rising output voltage slew rate			9, 10, 11	17	125		
SR_{ENx_FALL}	Enable falling output voltage slew rate	90% to 10% of V_{PULL_UP1}, R_{LOAD} = 50kΩ, C_{LOAD} = 100pF	1.6V ≤ V_{PULL_UP1} ≤ 7V	9, 10, 11	44	126		
$SR_{SEQ\_DONE\_FALL}$	SEQ_DONE falling output voltage slew rate		1.6V ≤ V_{PULL_UP2} ≤ 7V	9, 10, 11	44	126		
SR_{PWRGD_FALL}	PWRGD falling output voltage slew rate			9, 10, 11	44	126		
$R_{ENx\_PULL\_UP}$	EN PMOS source output resistance	I_{LOAD} = 2mA	1.6V ≤ V_{PULL_UP1} ≤ 3.3V	1, 2, 3		18	40	Ω
			3.3V ≤ V_{PULL_UP1} ≤ 7V	1, 2, 3		7	20	
$R_{SEQ\_DONE\_PULL\_UP}$	SEQ_DONE PMOS source output resistance	I_{LOAD} = 2mA	1.6V ≤ V_{PULL_UP2} ≤ 3.3V	1, 2, 3		18	40	
			3.3V ≤ V_{PULL_UP2} ≤ 7V	1, 2, 3		7	20	
$R_{PWRGD\_PULL\_UP}$	PWRGD PMOS source output resistance	I_{LOAD} = 2mA	1.6V ≤ V_{PULL_UP2} ≤ 3.3V	1, 2, 3		18	40	
			3.3V ≤ V_{PULL_UP2} ≤ 7V	1, 2, 3		7	20	
$R_{ENx\_PULL\_DOWN}$	EN NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		7	28	
$R_{SEQ\_DONE\_PULL\_DOWN}$	SEQ_DONE NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		7	28	
$R_{PWRGD\_PULL\_DOWN}$	PWRGD NMOS sink output resistance	I_{LOAD} = –2mA, 1.6V ≤ V_{PULL_UP1} ≤ 7V		1, 2, 3		7	28	
$\overline{FAULT}$ OUTPUT								
$R_{\overline{FAULT}\_PULL\_DOWN}$	$\overline{FAULT}$ pull down resistance	$I_{\overline{FAULT}}$ = 100µA		1, 2, 3		131	512	Ω
$I_{LKG\_\overline{FAULT}}$	$\overline{FAULT}$ leakage current	$V_{\overline{FAULT}}$ = 7V		1, 2, 3		23	600	nA
THERMAL PROTECTION								
T_{SD_ENTER}	Thermal shutdown enter temperature					177		℃
T_{SD_EXIT}	Thermal shutdown exit temperature					164		

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6.5 Electrical Characteristics（续）

Over 3V ⩽ V_{IN} ⩽ 14V, R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, over temperature range (T_A= –55°C to 125°C), unless otherwise noted; includes group E radiation testing at T_A = 25°C for QML RHA devices (1) (2)

PARAMETER		TEST CONDITIONS	SUB-GROUP (3)	MIN	TYP	MAX	UNIT
DELAY AND TIME TO REGULATION TIMERS							
t_{DLY_TMR}	Delay time	R_{DLY_TMR} = 10.5kΩ	1, 2, 3	0.205	0.268	0.342	ms
		R_{DLY_TMR} = 619kΩ	1, 2, 3	10.77	12.5	14.14	
		R_{DLY_TMR} = 1.18MΩ	1, 2, 3	20	23.37	27.2	
t_{REG_TMR}	Time to regulation	R_{REG_TMR} = 10.5kΩ	1, 2, 3	0.197	0.264	0.34	
		R_{REG_TMR} = 619kΩ	1, 2, 3	10.8	12.4	14.1	
		R_{REG_TMR} = 1.18MΩ	1, 2, 3	20.3	23.63	27.2	

(1) See the 5962R23201VXC SMD (standard microcircuit drawing) for additional information on the RHA devices.
(2) All voltage values are with respect to GND.
(3) For subgroup definitions, see Quality Conformance Inspection table.
(4) V_{POR_IN} is the minimum V_{IN} voltage for a controlled output state, when 1.6V ⩽ V_{PULL_UPx} ⩽ 7V. Below V_{POR_IN}, the output cannot be determined.
(5) $V_{POR\_PULL\_UPx}$ is the minimum V_{PULL_UPx} voltage for a controlled output state, when V_{IN} ⩽ 3V. Below $V_{POR\_PULL\_UPx}$ the output cannot be determined.

6.6 Timing Requirements

Over 3V ⩽ V_{IN} ⩽ 14V, R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1µF, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, C_{PULL_UP1} = 1µF, C_{PULL_UP2} = 1µF, over temperature range (T_A = –55°C to 125°C) unless otherwise noted; includes group E radiation testing at T_A = 25°C for RHA devices (1)

PARAMETER		TEST CONDITIONS	SUB-GROUP (2)	MIN	TYP	MAX	UNIT
$t_{Start\_up\_delay}$	Start-up delay time (3)	V_{REFCAP} ⩾ 1.1V	1, 2, 3			2.8	ms
t_{pd_ENx}	ENx propagation delay	DLY_TMR = Open, $V_{OVERDRIVE}$ = 10mV, V_{PULL_UPx}=1.6V, from 50% of IN to 50% OUT	1, 2, 3		3.4	6.5	µs
$t_{pd\_SEQ\_DONE}$	SEQ_DONE propagation delay	DLY_TMR = Open, $V_{OVERDRIVE}$ = 10mV	1, 2, 3		3.4	6.5	
t_{pd_PWRGD}	PWRGD propagation delay	DLY_TMR = Open, $V_{OVERDRIVE}$ = 10mV	1, 2, 3		3.4	6.5	
$t_{pd\_SM\_FAULT}$	State machine fault propagation delay	Out of order fault	1, 2, 3		3.4	4.3	
t_{MIN_UP}	V_{UP} rising minimum time for valid UP		4, 5, 6		0.27	0.7	µs
$t_{MIN\_\overline{DOWN}}$	V_{DOWN} rising minimum time for valid DOWN		4, 5, 6		0.42	0.9	
$t_{h\_VTH\_RISE}$	Rising theshold on VSENSEx hold time		4, 5, 6		0.84	1.6	µs
$t_{h\_VTH\_FALL}$	Falling theshold on VSENSEx hold time		4, 5, 6		0.35	1	µs

(1) See the 5962R23201VXC SMD (standard microcircuit drawing) for additional information on the RHA devices (coming later)
(2) For subgroup definitions, see Quality Conformance Inspection table.
(3) During the power-on, V_{IN} must be at or above V_{IN} (MIN) for at least $t_{Start\_up\_delay}$ for all internal references to be within specification.

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6.7 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	– 55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	– 55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	– 55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	– 55

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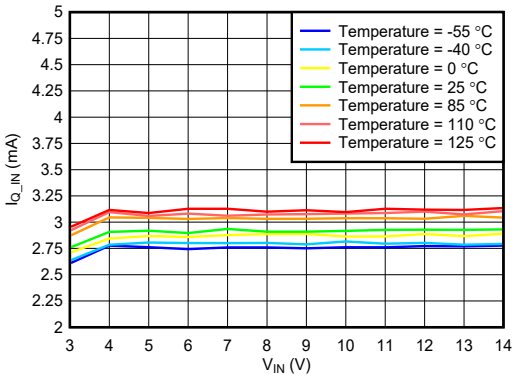
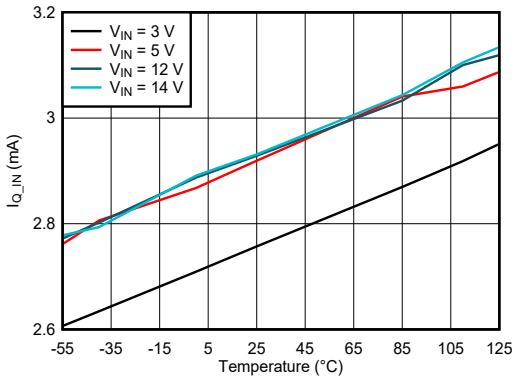
6.8 Typical Characteristics

R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, $V_{\overline{FAULT}}$ = 10kΩ pull-up to VLDO, R_{HYS} = 50kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1 µF, C_{PULL_UP1} = 1 µF, C_{PULL_UP2} = 1 µF, unless otherwise noted.



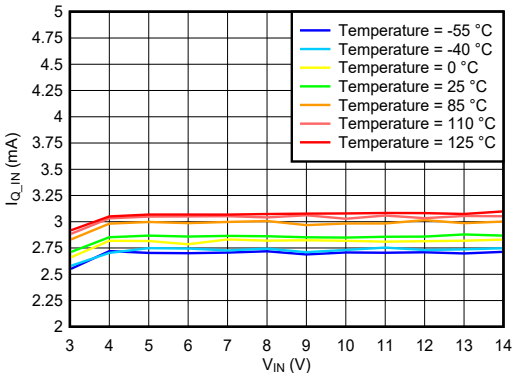
V_{UP} = $V_{\overline{DOWN}}$ = 0V

图 6-1. I_{Q_IN} vs V_{IN} Across Temperature in Waiting to Sequence UP State



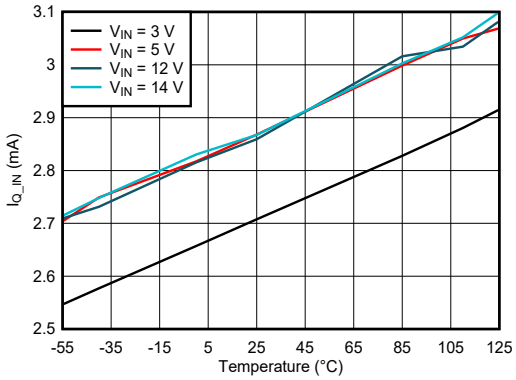
V_{UP} = $V_{\overline{DOWN}}$ = 0V

图 6-2. I_{Q_IN} vs Temperature Across V_{IN} in Waiting to Sequence UP State



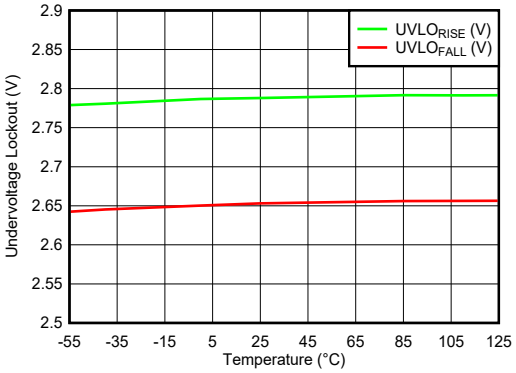
V_{UP} = $V_{\overline{DOWN}}$ = 3.3V

图 6-3. I_{Q_IN} vs V_{IN} Across Temperature in Waiting to Sequence DOWN State



V_{UP} = $V_{\overline{DOWN}}$ = 3.3V

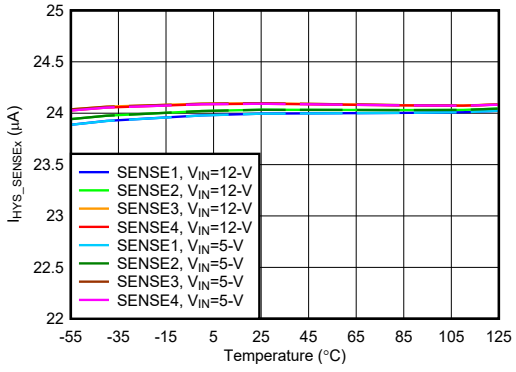
图 6-4. I_{Q_IN} vs Temperature Across V_{IN} in Waiting to Sequence DOWN State



R_{DLY_TMR} = Floating V_{UP} = $V_{\overline{DOWN}}$ = 3.3V

R_{REG_TMR} = 1.18MΩ

图 6-5. Undervoltage Lockout vs Temperature

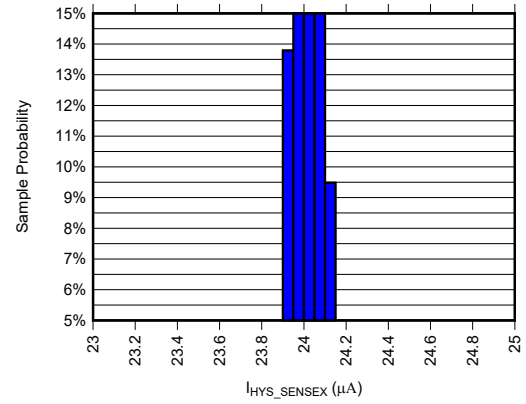


V_{SENSEx} = 700mV R_{REG_TMR} = Floating

图 6-6. I_{HYS_SENSEx} vs Temperature Across V_{IN} and SENSEx Channel

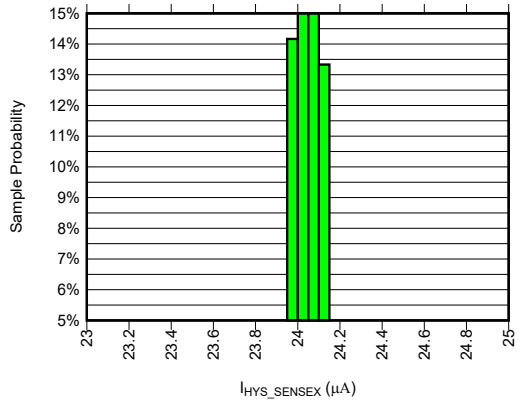
6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, $V_{\overline{FAULT}}$ = 10kΩ pull-up to VLDO, R_{HYS} = 50kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1 µF, C_{PULL_UP1} = 1 µF, C_{PULL_UP2} = 1 µF, unless otherwise noted.



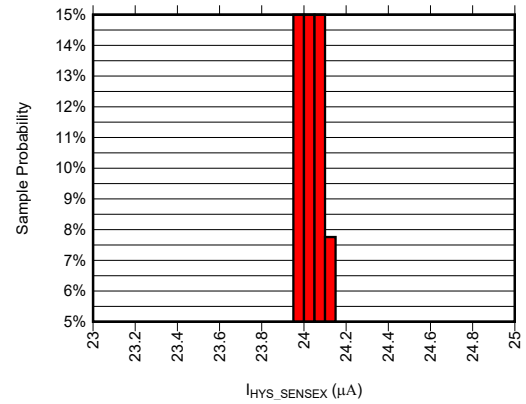
V_{IN} = 3V V_{SENSEx} = 700mV

图 6-7. I_{HYS_SENSEx} Current Distribution at Temperature of – 55°C



V_{IN} = 3V V_{SENSEx} = 700mV

图 6-8. I_{HYS_SENSEx} Current Distribution at Temperature of 25°C



V_{IN} = 3V V_{SENSEx} = 700mV

图 6-9. I_{HYS_SENSEx} Current Distribution at Temperature of 125°C

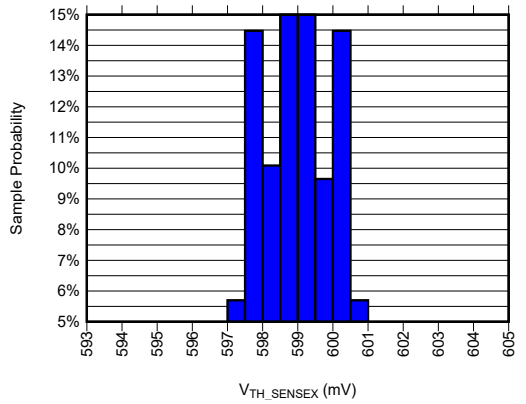


图 6-10. V_{TH_SENSEx} Voltage Distribution at Temperature of – 55°C

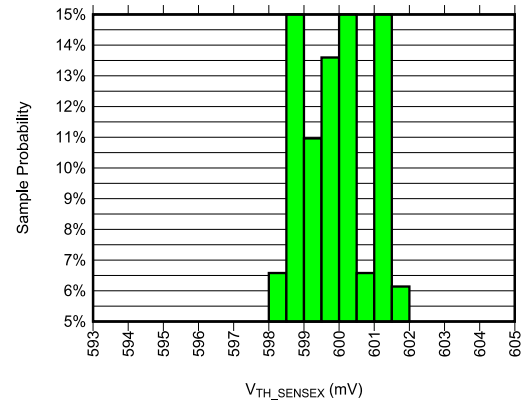


图 6-11. V_{TH_SENSEx} Voltage Distribution at Temperature of +25°C

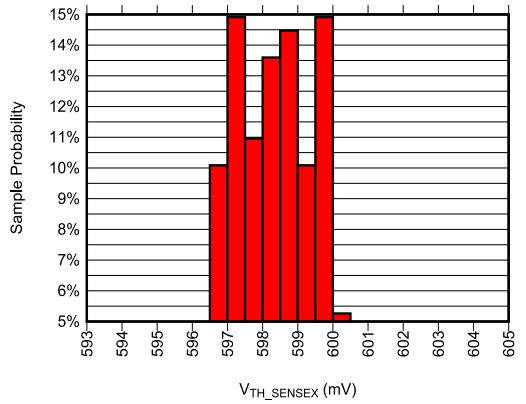


图 6-12. V_{TH_SENSEx} Voltage Distribution at Temperature of 125°C

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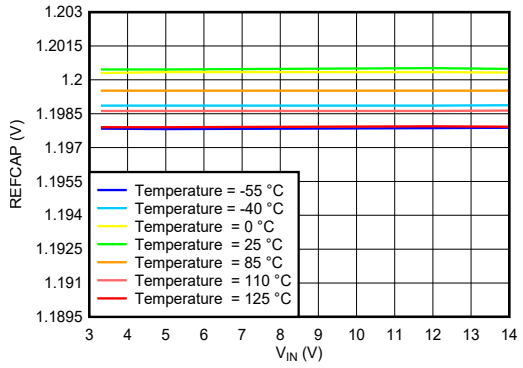
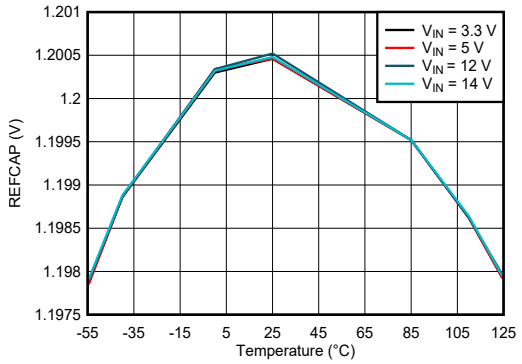
6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, $V_{\overline{FAULT}}$ = 10kΩ pull-up to VLDO, R_{HYS} = 50kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1 µF, C_{PULL_UP1} = 1 µF, C_{PULL_UP2} = 1 µF, unless otherwise noted.



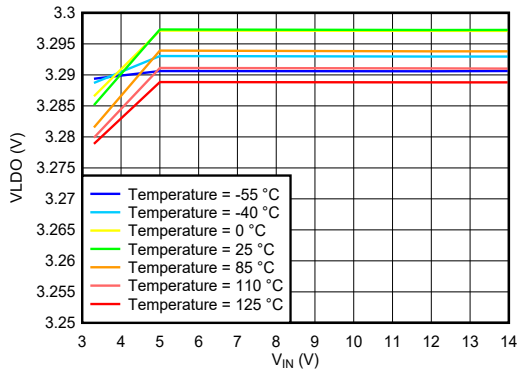
V_{UP} = $V_{\overline{DOWN}}$ = 0V

图 6-13. REFCAP vs V_{IN} Across Temperature



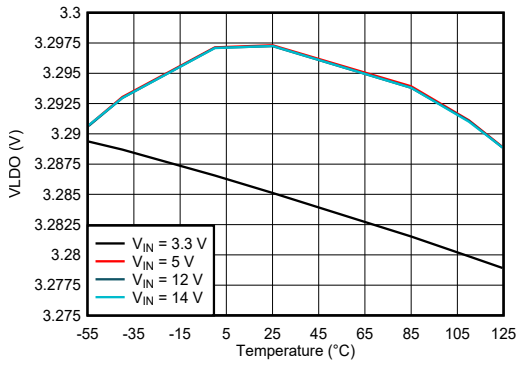
V_{UP} = $V_{\overline{DOWN}}$ = 0V

图 6-14. REFCAP vs Temperature Across V_{IN}



V_{UP} = $V_{\overline{DOWN}}$ = 0V

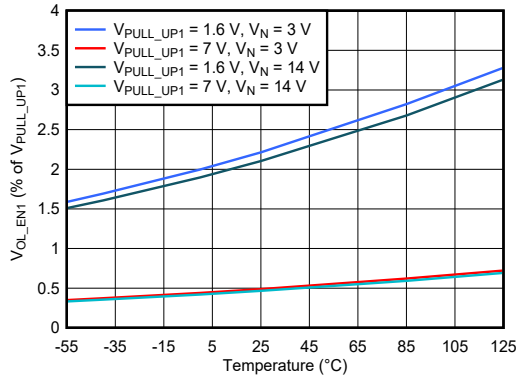
图 6-15. VLDO vs V_{IN} Across Temperature



V_{UP} = $V_{\overline{DOWN}}$ = 0V

R_{REG_TMR} = Floating

图 6-16. VLDO vs Temperature Across V_{IN}

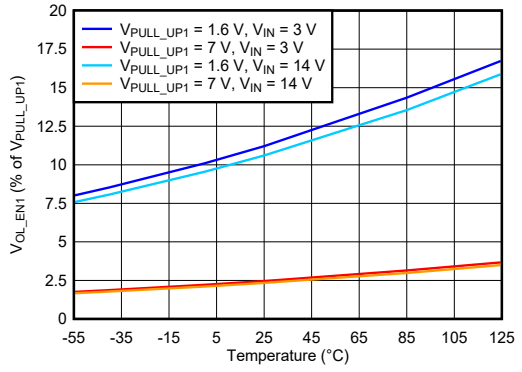


V_{UP} = $V_{\overline{DOWN}}$ = 0V

I_{LOAD} = – 2mA

R_{REG_TMR} = Floating

图 6-17. V_{OL_EN1} vs Temperature Across V_{PULL_UP1} and V_{IN} at I_{LOAD} = – 2mA



V_{UP} = $V_{\overline{DOWN}}$ = 0V

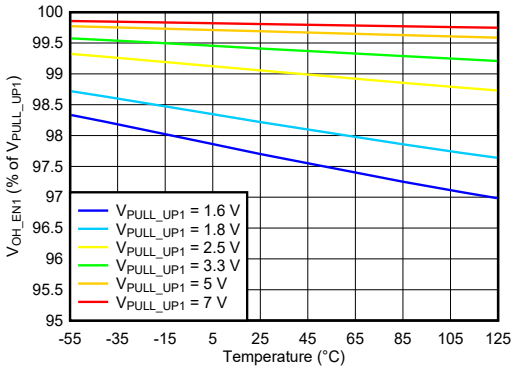
I_{LOAD} = – 10mA

R_{REG_TMR} = Floating

图 6-18. V_{OL_EN1} vs Temperature Across V_{PULL_UP1} and V_{IN} at I_{LOAD} = – 10mA

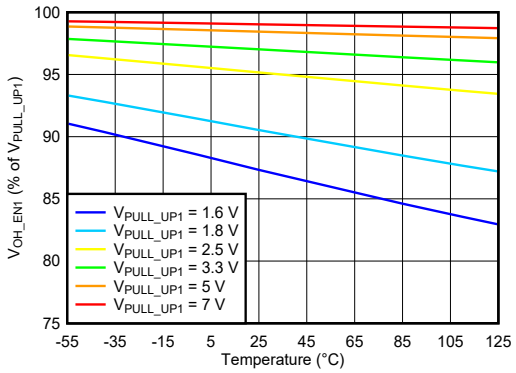
6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, $V_{\overline{FAULT}}$ = 10kΩ pull-up to VLDO, R_{HYS} = 50kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1 µF, C_{PULL_UP1} = 1 µF, C_{PULL_UP2} = 1 µF, unless otherwise noted.



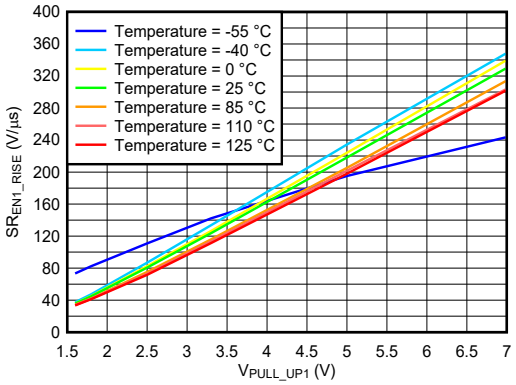
V_{UP} = $V_{\overline{DOWN}}$ = 3.3V
R_{REG_TMR} = Floating
I_{LOAD} = 2mA
V_{IN} = 12V

图 6-19. V_{OH_EN1} vs Temperature Across V_{PULL_UP1} at I_{LOAD} = 2mA



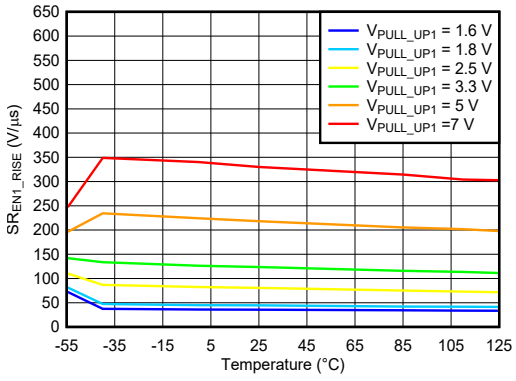
V_{UP} = $V_{\overline{DOWN}}$ = 3.3V
R_{REG_TMR} = Floating
I_{LOAD} = 10mA
V_{IN} = 12V

图 6-20. V_{OH_EN1} vs Temperature Across V_{PULL_UP1} at I_{LOAD} = 10mA



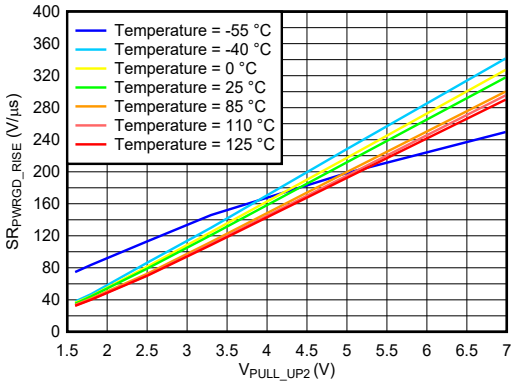
V_{UP} = $V_{\overline{DOWN}}$ = ↑ 3.3V
R_{REG_TMR} = Floating
V_{IN} = 12V

图 6-21. SR_{EN1_RISE} vs V_{PULL_UP1} Across Temperature



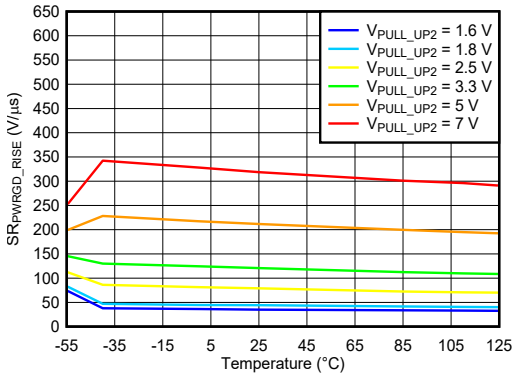
V_{UP} = $V_{\overline{DOWN}}$ = ↑ 3.3V
R_{REG_TMR} = Floating
V_{IN} = 12V

图 6-22. SR_{EN1_RISE} vs Temperature Across V_{PULL_UP1}



V_{UP} = $V_{\overline{DOWN}}$ = ↑ 3.3V
R_{REG_TMR} = Floating
V_{IN} = 12V

图 6-23. SR_{PWRGD_RISE} vs V_{PULL_UP2} Across Temperature



V_{UP} = $V_{\overline{DOWN}}$ = ↑ 3.3V
R_{REG_TMR} = Floating
V_{IN} = 12V

图 6-24. SR_{PWRGD_RISE} vs Temperature Across V_{PULL_UP2}

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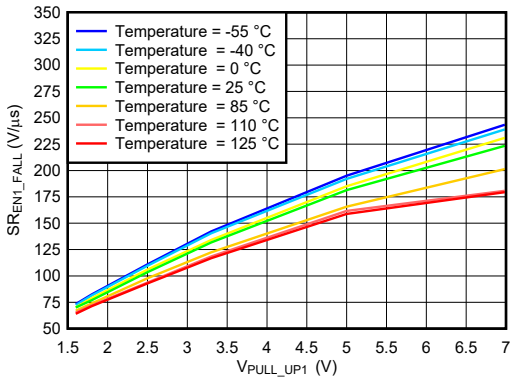
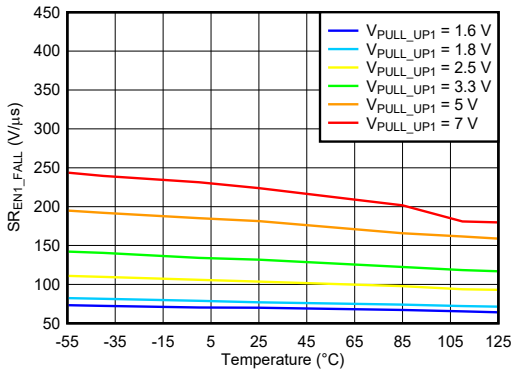
6.8 Typical Characteristics (continued)

R_{DLY_TMR} = 10kΩ, R_{REG_TMR} = 10kΩ, V_{PULL_UP1} = 3.3V, V_{PULL_UP2} = 3.3V, $V_{\overline{FAULT}}$ = 10kΩ pull-up to VLDO, R_{HYS} = 50kΩ, C_{REFCAP} = 470nF, C_{VLDO} = 1 µF, C_{PULL_UP1} = 1 µF, C_{PULL_UP2} = 1 µF, unless otherwise noted.



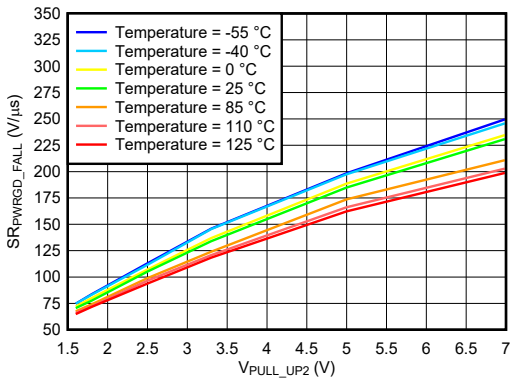
V_{UP} = $V_{\overline{DOWN}}$ = ↓ 0V
V_{IN} = 12V
R_{REG_TMR} = Floating

图 6-25. SR_{EN1_FALL} vs V_{PULL_UP1} Across Temperature



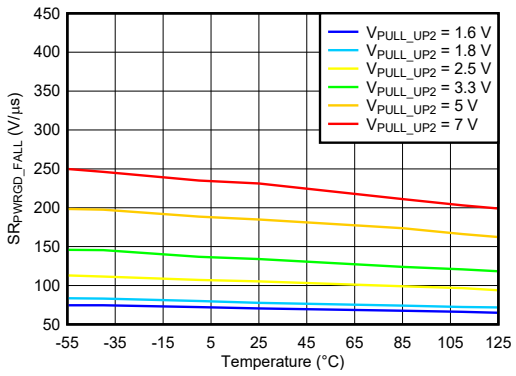
V_{UP} = $V_{\overline{DOWN}}$ = ↓ 0V
V_{IN} = 12V
R_{REG_TMR} = Floating

图 6-26. SR_{EN1_FALL} vs Temperature Across V_{PULL_UP1}



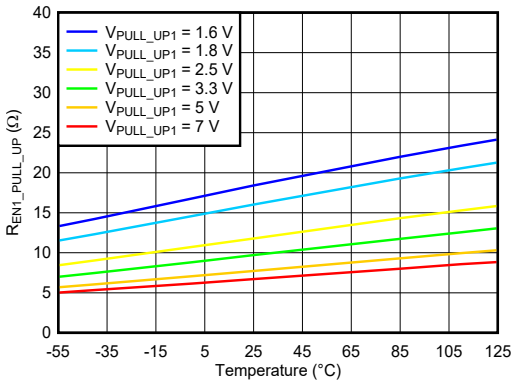
V_{UP} = $V_{\overline{DOWN}}$ = ↓ 0V
V_{IN} = 12V
R_{REG_TMR} = Floating

图 6-27. SR_{PWRGD_FALL} vs V_{PULL_UP2} Across Temperature



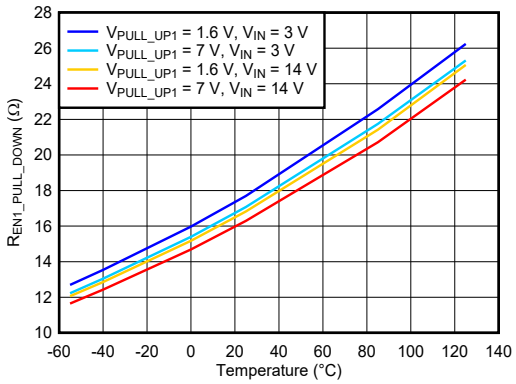
V_{UP} = $V_{\overline{DOWN}}$ = ↓ 0V
V_{IN} = 12V
R_{REG_TMR} = Floating

图 6-28. SR_{PWRGD_FALL} vs Temperature Across V_{PULL_UP2}



V_{UP} = $V_{\overline{DOWN}}$ = 3.3V
V_{IN} = 12V
R_{REG_TMR} = Floating
I_{LOAD} = 2mA

图 6-29. $R_{EN1\_PULL\_UP}$ vs Temperature Across V_{PULL_UP1}



V_{UP} = $V_{\overline{DOWN}}$ = 0V
V_{IN} = 12V
R_{REG_TMR} = Floating
I_{LOAD} = – 2mA

图 6-30. $R_{EN1\_PULL\_DOWN}$ vs Temperature Across V_{PULL_UP1}

7 Detailed Description

7.1 Overview

The TPS7H3014 is a four-Channel, 3V to 14V, sequencer and supervisor for space applications. The device is intended to drive devices with enable high logic inputs. The channel count can be incremented as needed for the application by connecting multiple ICs. in a daisy-chain configuration. Each output incorporates a push-pull architecture. The logic high of these outputs are externally provided by the user by supplying a voltage to the PULL-UPx inputs. All ENx push-pull outputs are tied to the PULL_UP1 domain while SEQ_DONE and PWRGD are tied to the PULL_UP2 domain.

The SENSEx inputs are connected to the non-inverting input (undervoltage) of a comparator which is used to determine the on (in regulation) and off (not in regulation) voltage level of the monitored power supply (V_{OUTx}). Each of these inputs feature a threshold level of 599mV (typ) with an accuracy of ±1% across: voltage, temperature, and radiation (TID). The hysteresis voltage threshold level can be adjusted by the user and determined by the R_{TOPx} resistance and the hysteresis current (I_{HYS}). The I_{HYS} becomes active once the rising voltage at SENSEx exceeds the threshold (599mV typ), indicating the monitored voltage rail is in regulation. I_{HYS} is 24 μA with an accuracy of ±3% across: voltage, temperature, and radiation (TID).

The device incorporates two timers:

1. **DLY_TMR**: Set the rising and falling ENx delay. Once the $SENSE_{x-1}$ is above the on voltage during a sequence up, the EN_x will be asserted high once the delay set by the user using the DLY_TMR input is expired. The same is true during sequence down, this means that once $SENSE_x$ is below the off voltage the EN_{x-1} will be asserted low once the timer is expired. This timer can be set from 0.25ms to 25ms, by using a 10.5kΩ to a 1.18MΩ, respectively.
2. **REG_TMR**: Set the allowed time that a sensed voltage rail has to be above the on threshold (in regulation). Once the EN_x is asserted high, the $SENSE_x$ has up to the time set by the user, using REG_TMR, to be above 599mV (typ). Otherwise a reverse sequence down from EN_{x-1} is started.

Separate UP and $\overline{\text{DOWN}}$ pins are provided by the device in order to enable daisy-chain configurations. The UP pin has a threshold (V_{TH_UP}) of 599mV (typ), while the $\overline{\text{DOWN}}$ pin has an threshold ($V_{TH\_\overline{DOWN}}$) of 498mV. A fixed hysteresis of 100mV is incorporated in both input comparators for noise stability. These pins are edge sensitive, a rising edge in UP starts the sequence up, while a falling edge in $\overline{\text{DOWN}}$ will start the sequence down.

When using a single device and driven externally, both pins (UP and DOWN) are typically tied together. Since UP and $\overline{\text{DOWN}}$ inputs have an accurate threshold, they can be used to initiate the sequence up and down by accurately sensing another rail (using a resistive divider), or they can be externally driven by a controller. Once UP is driven above V_{TH_UP}, the device will start a sequence up by asserting EN1 high after the programmed delay time (DLY_TMR), at which point the SENSE1 will start rising up. If SENSE1 crosses the on voltage before the REG_TMR is expired, then EN2 will be asserted high after the programmed delay. This process continues until the SEQ_DONE and PWRGD are asserted high indicating a complete sequence up and system power good, respectively.

Once the $\overline{\text{DOWN}}$ pin is driven below $V_{TH\_\overline{DOWN}}$, the device will start a sequence down by forcing EN4 low after the programmed delay. At this point, the SENSE4 voltage will start falling until is lower than the set off voltage. Once this happens, EN3 will be asserted low after the programmed delay. This will continue until EN1 is forced low. As the discharge time of the sequenced devices is unknown, the REG_TMR is not active during power down.

During sequence up, SEQ_DONE and PWRGD are asserted high after the last used channel crosses the on voltage threshold and the programmed DLY_TMR is expired (assuming it is active). During sequence down, SEQ_DONE is forced low once V_{OUT1} is below the off voltage and the DLY_TMR is expired. However PWRGD is forced low immediately after the commanded sequence down.

The TPS7H3014 also incorporates a comprehensive FAULT management system described in the State Machine section.

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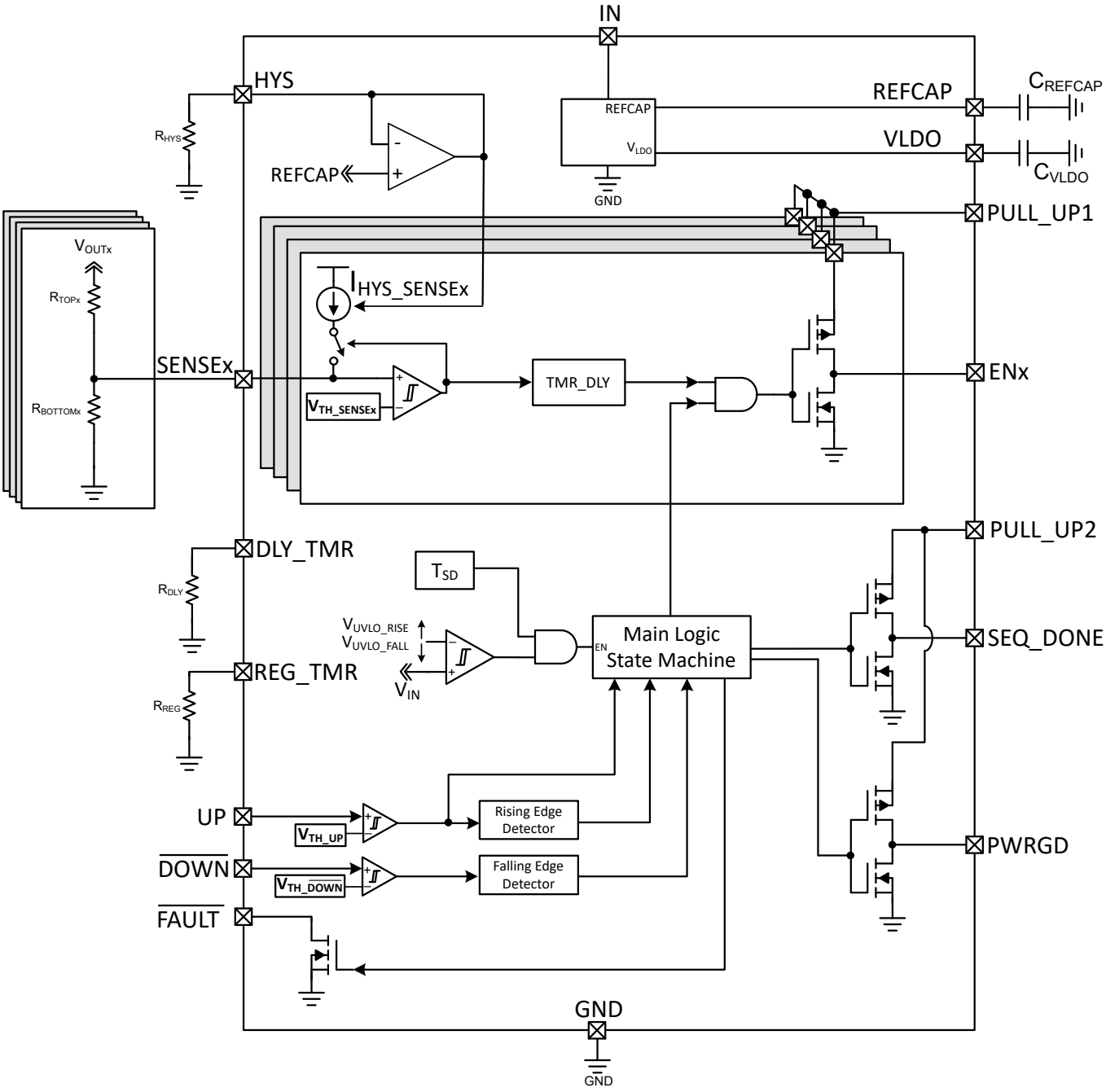
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage (IN), VLDO and REFCAP

During steady state operation, the input voltage of the TPS7H3014 must be between 3V and 14V. A minimum bypass capacitance of at least 0.1 μF is needed between V_{IN} and GND. The input bypass capacitors should be placed as close to the sequencer IC as possible. Is recommended that V_{IN} slew rate is controlled between 10V/μs to 1mV/μs for proper IC operation.

The voltage applied at V_{IN} serves as the input for the internal regulator that generates the VLDO voltage, typically 3.29V. At input voltages less the 3.29V (typ), the VLDO voltage will follow the voltage at V_{IN}. Recommended capacitance for VLDO is 1 μF. Unused SENSE2 to SENSE4 can be tied to VLDO to by-pass the channel delay during sequence up and down. It is recommended to pull-up the $\overline{FAULT}$ pin to VLDO via a 10kΩ resistor, but otherwise it is recommended not to externally load this pin due to limited output current capability. During power up, the user should wait at least the 2.8ms ($t_{Start\_up\_delay}$) after V_{IN} > $UVLO_{RISE}$ before attempting to start a sequence up, this is due to internal time constants in the device.

Each device generates an internal 1.2V bandgap reference that is utilized throughout the various internal control logic blocks. This is the voltage present on the REFCAP pin during steady state operation. This voltage is divided down to produce the reference for the comparator inputs $SENSE_x$ (599mV typ), UP (598mV typ) and $\overline{DOWN}$ (498mV typ). The V_{TH_SENSEx} reference is measured at the EN_x outputs to account for offsets in the error amplifier and maintains regulation within ±1% across: voltage, temperature, and radiation TID (up to 100krad in Silicon). This tight reference tolerance allows the user to monitor voltage rails with high accuracy. A 470nF capacitor to GND is required at the REFCAP pin for proper electrical operation as well as to ensure robust SET performance of the device.

7.3.1.1 Undervoltage Lockout (V_{POR_IN} < V_{IN} < UVLO)

When the voltage on V_{IN} is less than the UVLO (2.79V typ) voltage, but greater than the power-on reset voltage (V_{POR_IN}, 1.41V typ), the output pins (ENx, SEQ_DONE and PWRGD) will be in a logic low state, regardless of the voltage at the inputs of the device, named as:

- $SENSE_x$
- UP
- $\overline{DOWN}$

7.3.1.2 Power-On Reset (V_{IN} < V_{POR_IN})

When the voltage on V_{IN} is lower than the power on reset voltage (V_{POR_IN}), the output signal is undefined and is not to be relied upon for proper device function.

图 7-1 shows the ENx outputs relationship to a rising input voltage (V_{IN}). As can be observed, the ENx are undefined when V_{IN} is lower than V_{POR_IN} (typically 1.41V). During this time the outputs can be any value from 0V to V_{IN}. In this case, the input voltages to all undervoltage (UV) input comparators (SENSEx) are below the V_{TH_SENSEx} (599mV). For this reason (in conjunction with waiting for a rising edge on UP), the ENx, SEQ_DONE and PWRGD stays low after V_{IN} rises above $UVLO_{RISE}$ (typically 2.79V).

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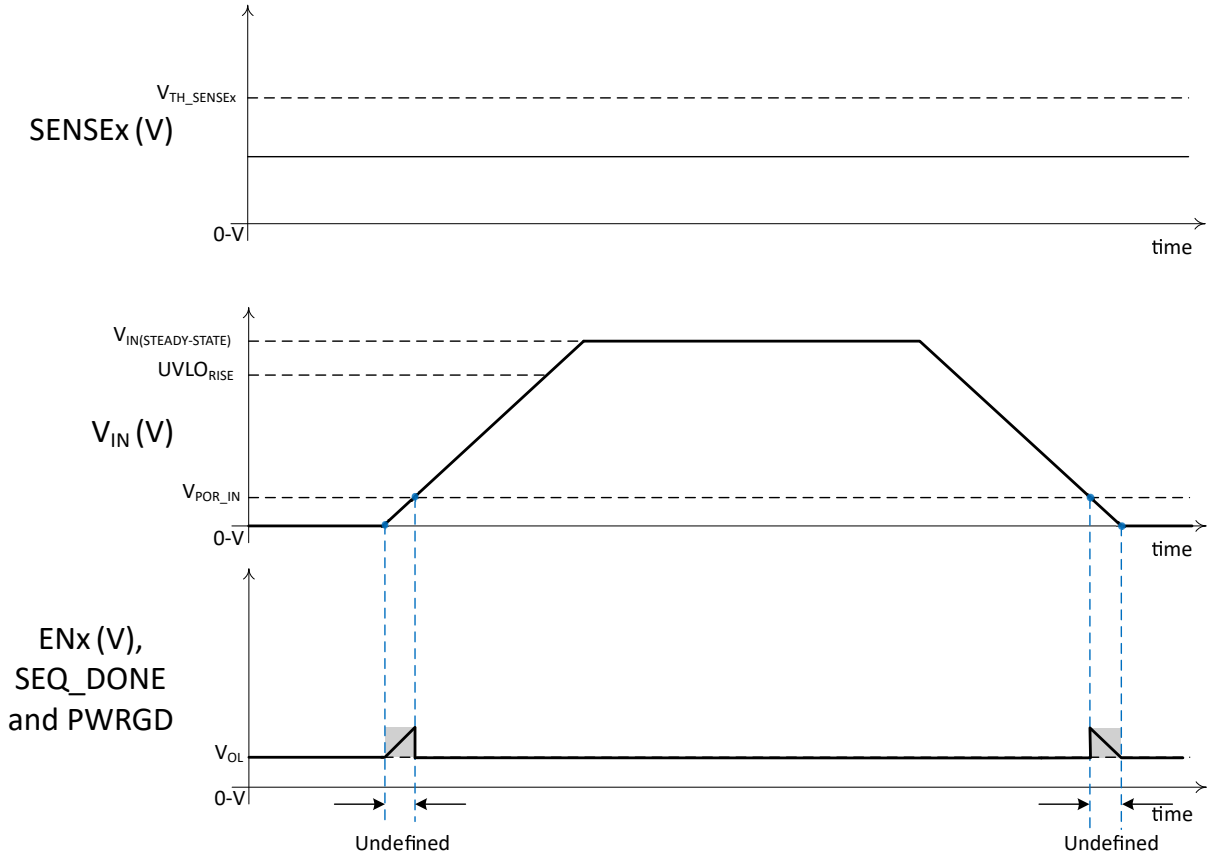

图 7-1. Outputs in a Valid Low State After V_{IN} > V_{IN-MIN}

A. This figures assumes:

1. A valid external pull-up voltage is connected to the PULL_UPx inputs (1.6V ⩽ V_{PULL_UPx} ⩽ 7V).
2. $V_{IN(STEADY-SATE)}$ is a valid V_{IN} voltage between 3V to 14V.
3. $V_{\overline{FAULT}}$ pull up to VLDO.
4. Device is in the: Waiting to Sequence UP State (Refer to State Machine for more details).
5. V_{OL} represents: V_{OL_ENx}, $V_{OL\_SEQ\_DONE}$, and V_{OL_PWRGD}, or the low logic output voltage for all outputs.

7.3.2 SENSEx Inputs

7.3.2.1 V_{TH_SENSEX} and V_{ONx}

The TPS7H3014 sequencer integrates four under-voltage (UV) comparators, with an accurate (±1%) threshold voltage (V_{TH_SENSEx}) of 599mV nominal. V_{TH_SENSEx} is measured at the ENx outputs to account for comparator offsets in the threshold. Maximum flexibility is provided as external resistive dividers can be adjusted to sense any voltage rail (V_{OUTx}). 图 7-2 shows a conceptual diagram of the comparators connected to the SENSEx inputs. As can be observed, the sensed voltage rail (V_{OUTx}) is attenuated (using an external resistive divider, R_{TOPx} and $R_{BOTTOMx}$) and compared against the V_{TH_SENSEx} voltage. Is recommended to maintain the steady-state SENSEx voltage below 1.6V, in order to maintain the threshold (V_{TH_SENSEx}) accuracy.

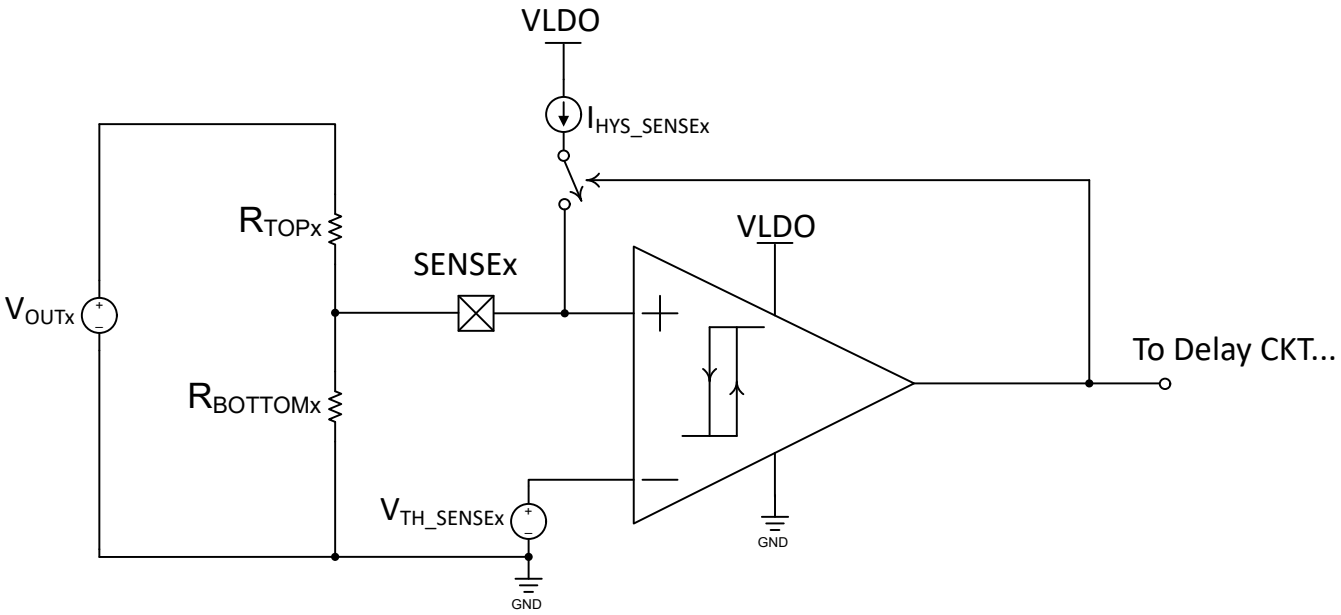

图 7-2. SENSEx Comparators Inputs

When the voltage at the monitored rail (V_{OUTx}) is rising, the hysteresis current (I_{HYS}) is not connected to SENSEx input. At this time the SENSEx (attenuated V_{OUTx}) voltage is compared against the SENSEx threshold (V_{TH_SENSEx}). When $V_{SENSEx} > V_{TH\_SENSEx}$ the voltage is considered within regulation limits. We can calculate the on (within regulation) voltage by doing a simple voltage divider as:

$$V_{ONx\_NOMINAL}\ (V) = \left(1 + \frac{R_{TOPx}}{R_{BOTTOMx}}\right) \times V_{TH\_SENSEx} \quad (1)$$

Where:

- V_{TH_SENSEx} is the nominal sense threshold voltage of 599mV.

As with any system, there is some variation (or errors) of the design variables, in this case the top and bottom resistors and the SENSEx threshold voltage. Using the derivative method to calculate the total error (and assuming these variables are uncorrelated) with both resistors having the same tolerance value, the V_{ONx} error can be calculated as:

$$V_{ONx\_ERROR}\ (V) = \pm\sqrt{\frac{V_{TH\_SENSEx}^2 \times \left[\left(2 \times R_{TOL}^2 \times R_{TOPx}^2\right) + \left(V_{TH\_SENSEx\_ACC}^2 \times \left(R_{TOPx} + R_{BOTTOMx}\right)^2\right)\right]}{R_{BOTTOMx}^2}} \quad (2)$$

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Where:

- R_{TOL} is the resistors tolerance (same for top and bottom resistors) as numeric value. For example, for 0.1% tolerance resistors, we use 0.001.
- $V_{TH\_SENSEx\_ACC}$ is the SENSEx threshold accuracy as numeric value (in this case 0.01).
- R_{TOPx} and $R_{BOTTOMx}$ are in Ohms (Ω).
- V_{TH_SENSEx} is 0.599 Volts.

Using 方程式 1 and 方程式 2 we can calculate the on voltage range as:

$$V_{ONx} = V_{ONx\_NOMINAL} \pm V_{ONx\_ERROR} \quad (3)$$

备注

Remember V_{TH_SENSEx} is the reference voltage when accounting for the comparator offsets $V_{TH\_SENSEx} = V_{REF} + V_{OFFSETx}$.

As this device is intended for sequencing of multirail systems, the ENx to SENSEx order is defined in ascending channel number (EN1 to EN4) for sequence up, and descending (EN4 to EN1) for sequence down. When a channel of the sequencer is not needed (unused) the channel can be connected to VLDO to skip the channel during sequence up/down. Is recommended to connect all disabled channels to VLDO, but an external voltage greater than 91% of VLDO (max) will disabled the channel (the voltage at SENSEx cannot exceed 3.5V). Only channels 2 through 4 can be disabled. It is recommended to disabled channels starting from high (channel #4) to low (channel #2). The channels are disabled starting from the lowest channel count and higher. This means that if channel #2 is disabled, by definition channels #3 and #4 will also be disabled.

备注

The channels to be disabled must be valid at power up and not be dynamically changed during the sequence up and down.

Any voltage at SENSE 2 to SENSE4 > V_{TURN_OFF} [91% of VLDO(max)] will disable (or turn-off) the channel. This will disable the delay (set by TMR_DLY) for those channels during sequence up and down.

Although it is not required, in noisy applications it is good analog design practice to place a small bypass capacitor at the SENSEx inputs in order to reduce sensitivity to transient voltages on the monitored signal.

7.3.2.2 I_{HYS_SENSEx} and V_{OFFx}

The TPS7H3014 has a built-in hysteresis current of 24 μA with an accuracy of ±3% (with R_{HYS} = 50kΩ). The hysteresis current is equivalent to REFCAP/R_{HYS}. A tolerance of 0.1% for the R_{HYS} is recommended as it ultimately affects the hysteresis current accuracy. This current is mirrored internally across all SENSEx inputs. This hysteresis current becomes active when the SENSEx voltage is greater than the threshold voltage (599mV ±1%), same as V_{OUTx} > V_{ONx} (Refer to 方程式 3 and 图 7-2). This current (I_{HYS}) multiplied by the R_{TOPx} resistance induces a voltage (V_{HYSx}) that is added to the SENSEx node, effectively boosting (incrementing) the node voltage. During sequence down, or an undervoltage event when the V_{OUTx} is decrementing, it will need to drop below the V_{OFF} voltage in order to be considered as an out of regulation (or fault). The hysteresis voltage is defined as:

$$V_{HYSx\_NOMINAL}\ (V) = I_{HYS\_SENSEx} \times R_{TOPx} \quad (4)$$

Where:

- I_{HYS_SENSEx} = 24 × 10^{-6} Amps (or 24 μA)
- R_{TOPx} units are in Ohms (Ω)

The "off" voltage (or out of regulation) voltage can be calculated as:

$$V_{OFFx\_NOMINAL}\ (V) = V_{ONx\_NOMINAL} - V_{HYSx\_NOMINAL} \quad (5)$$

Using 方程式 1 and 方程式 5

$$V_{OFFx\_NOMINAL}\left(V\right) = \left[\left(1 + \frac{R_{TOPx}}{R_{BOTTOMx}}\right) \times V_{TH\_SENSEx}\right] - \left(I_{HYS\_SENSEx} \times R_{TOPx}\right) \quad (6)$$

Where:

- V_{TH_SENSEx} is the nominal sense threshold voltage of 0.599V
- I_{HYS_SENSEx} = 24 × 10^{-6} Amps (or 24 µ A)
- R_{TOPx} and $R_{BOTTOMx}$ units are in Ohms (Ω)

The V_{OFF} error (using the derivative method and assuming all variables are uncorrelated) can be calculated as:

$$V_{OFFx\_ERROR}\left(V\right) = \pm\sqrt{\frac{A + B + C + D}{R_{BOTTOMx}^{2}}} \quad (7)$$

Where the equation terms are:

$$A = I_{HYS\_SENSEx}^{2} \times I_{HYS\_SENSEx\_ACC}^{2} \times R_{TOPx}^{2} \times R_{BOTTOMx}^{2} \quad (8)$$

$$B = R_{TOL}^{2} \times R_{TOPx}^{2} \times V_{TH\_SENSEx}^{2} \quad (9)$$

$$C = R_{TOL}^{2} \times R_{TOPx}^{2} \times \left[\left(I_{HYS\_SENSEx} \times R_{BOTTOMx}\right) - V_{TH\_SENSEx}\right]^{2} \quad (10)$$

$$D = V_{TH\_SENSEx}^{2} \times V_{TH\_SENSEx\_ACC}^{2} \times \left(R_{TOPx} + R_{BOTTOMx}\right)^{2} \quad (11)$$

Where:

- R_{TOL} is the resistors tolerance (same for top and bottom resistors) as numeric value. For example, for 0.1% tolerance resistors, we use 0.001.
- $V_{TH\_SENSEx\_ACC}$ is the SENSEx threshold accuracy as numeric value (in this case 0.01).
- $I_{HYS\_SENSEx\_ACC}$ is the hysteresis current accuracy as numeric value (in this case 0.03)
- V_{TH_SENSEx} is the nominal sense threshold voltage of 0.599V
- I_{HYS_SENSEx} = 24 × 10^{-6} Amps (or 24 µ A)
- R_{TOPx} and $R_{BOTTOMx}$ units are in Ohms (Ω)

$$V_{OFFx} = V_{OFFx\_NOMINAL} \pm V_{OFFx\_ERROR} \quad (12)$$

Using 方程式 6 and 方程式 7 we can calculate the off voltage range as:

图 7-3, shows a conceptual diagram of the rising and falling voltage, it also shows the errors on this voltage due to V_{TH} accuracy, I_{HYS} accuracy, and the resistive divider tolerances. At the system level, these errors have to be taken into account for a robust design.

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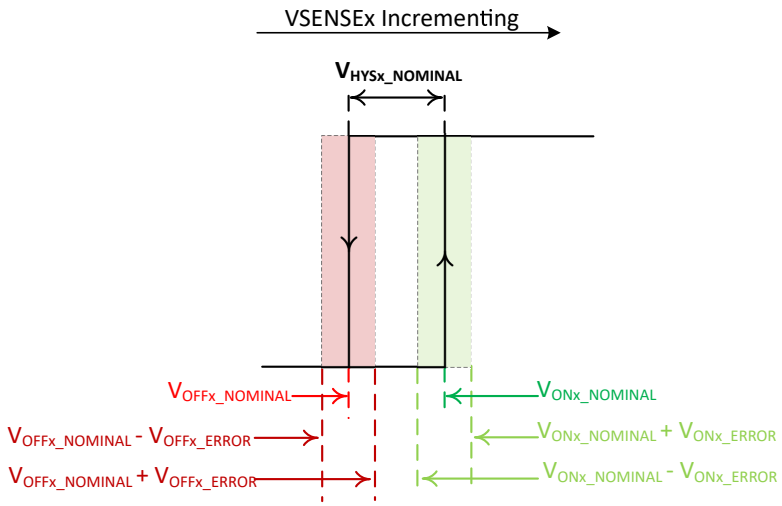

图 7-3. Rising and Falling Thresholds Voltages for the SENSE$_x$ Comparators

7.3.2.3 Top and Bottom Resistive Divider Design Equations

At the system level the designer knows (or selects) the V_{ONx} and V_{OFFx} levels. Usually these voltages are selected as percentages of the nominal rail voltage (V_{OUTx}) being monitored. Knowing this information, we can calculate the resistive divider components values (R_{TOPx} and $R_{BOTTOMx}$) for the desired target levels. Using 方程式 4 and 方程式 5 we can calculate the top resistor as:

$$R_{TOPx} = \frac{V_{ONx} - V_{OFFx}}{I_{HYS\_SENSEx}} \quad (13)$$

From 方程式 1 we can calculate the bottom resistor as:

$$R_{BOTTOMx} = \frac{R_{TOPx} \times V_{TH\_SENSEx}}{V_{ONx} - V_{TH\_SENSEx}} \quad (14)$$

It's important to notice that the larger the separation between V_{ONx} and V_{OFFx} (referred as V_{HYSx}), the bigger the error in the off voltage. 图 7-4 shows a plot of the error in the V_{OFFx} for different hysteresis voltages (V_{HYSx} = V_{ONx} – V_{OFFx}). The plot is created for three different V_{ON} voltages (or percentages of the nominal output voltage: 90, 95, and 97%) and two different output voltages (0.8V and 28V). As can be observed, the output voltage has very little impact on the off voltage error (differences cannot be appreciated on the plot). The error (in percent) can go from approximately 1% (at V_{HYS} = 3%) to around 2.6% (at V_{HYS} = 80%).

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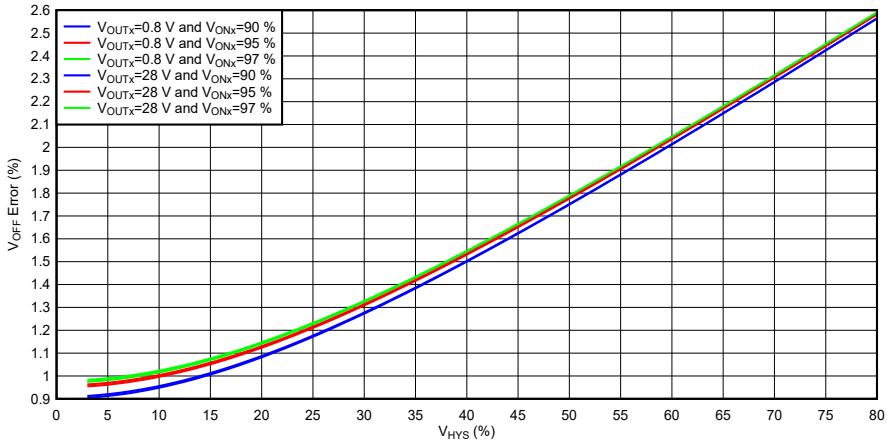

图 7-4. V_{OFFx} Error vs V_{HYS}

A. This plot does not includes the error on the V_{OFFx} due to the difference between the calculated top and bottom resistors using 方程式 13 and 方程式 14 and the actual resistance values that a designer can procure.
B. The resistor tolerance used for the calculation is 0.1%, V_{TH_SENSEx} accuracy is 1%, and the I_{HYS_SENSEx} accuracy is 3%.
C. In this plot the V_{HYS} (%) represents the separation as percentages of the nominal output voltage (V_{OUTx}).
D. In this plot, the V_{OFF} error in % is normalized with respect to the full-scale voltage (or V_{OUTx}).

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7.3.3 Output Stages (ENx,SEQ_DONE,PWRGD,PULL_UP1 and PULL_UP2)

The output stage's (EN1 to EN4), SEQ_DONE and PWRGD are of push-pull, active high type. The pull-up voltage for the push-pull outputs is externally provided by the user. PULL_UP1 (input) is the pull-up voltage domain for all ENx outputs (EN1 to EN4), while PULL_UP2 (input) is the pull-up voltage domain for the SEQ_DONE and PWRGD outputs.

备注

There are no sequencing requirements for IN, PULL_UP1, and PULL_UP2, however, both must be biased before commanding a sequence up and down.

备注

TI recommends to decouple PULL_UPx inputs with a 1 µF ceramic capacitor as close to the pins as possible. This is to ensure clean voltages signals at the outputs (ENx, PWRGD, and SEQ_DONE).

Each output stage consists of a PMOS/NMOS (CMOS) pair. Each leg has an output resistance of typically 7 Ω for V_{PULL_UPx} > 3.3V. PULL_UP1 and PULL_UP2, have a voltage range of 1.6V to 7V, and can be independently biased or tied to the same voltage rail, however both most be biased. The output resistance of the PMOS leg has a PULL_UPx voltage dependency. The lower the PULL_UPx voltage, the higher the PMOS resistance.

When V_{IN} < V_{POR_IN} and V_{PULL_UPx} > $V_{POR\_PULL\_UPx}$ (1.4V maximum) the output will be in a known pull-down state. At this condition the outputs have reduced sinking capabilities with V_{OL} ≤ 320mV when the device is sinking 100 µA of current into the outputs:

- ENx
- PWRGD
- SEQ_DONE

Once the input voltage range is withing the recommended input voltage range of 3V to 14 V, the output will have the full strength capabilities of ±10mA, per output.

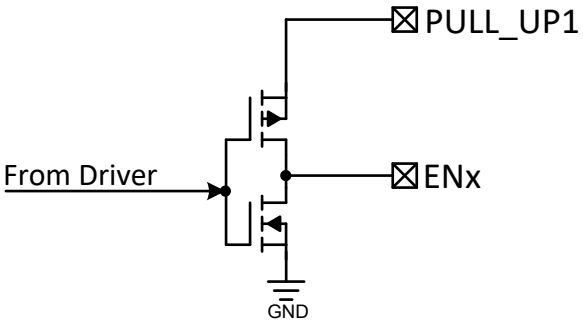

图 7-5. ENx Push-Pull Output Stages

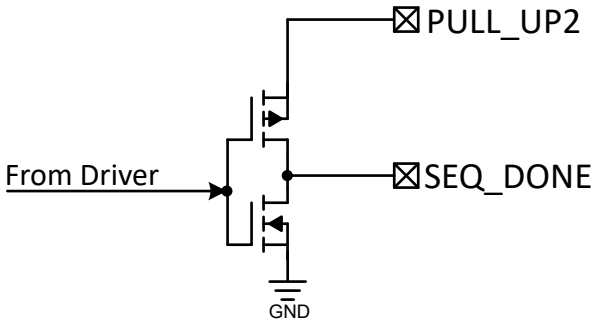

图 7-6. SEQ_DONE Push-Pull Output Stage

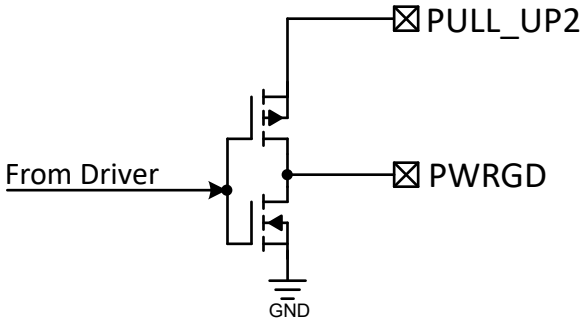

图 7-7. PWRGD Push-Pull Output Stage

7.3.4 User-Programmable TIMERS

The TPS7H3014 has two global (or common to all SENSEx channels) adjustable timers:

- DLY_TMR
- REG_TMR

Both timers are programmed via a single resistor from the DLY_TMR and REG_TMR pin to GND. The resistors are used to program the internal oscillator frequency of the timers. Leaving the DLY_TMR or the REG_TMR pin floating will disable the timer, respectively. The range for both timers is 250 µs to 25ms.

备注

Timers conditions must be valid at power up and must not be dynamically changed.

图 7-8 shows a sequence up and down assuming no faults and UP/DOWN pins tied together. The DLY_TMR is shown in orange and the REG_TMR time is shown with arrows (starting from ENx going high).

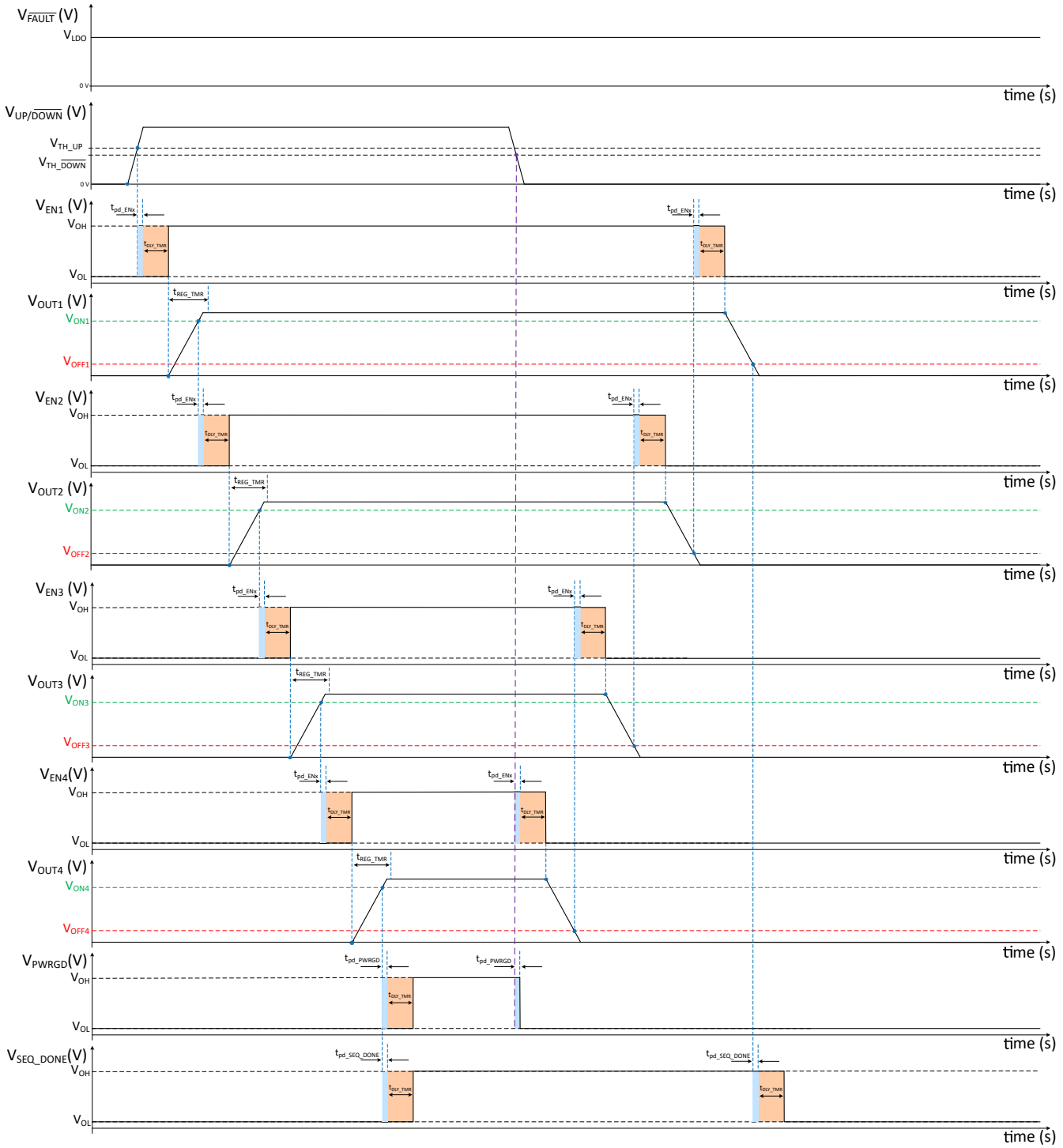

图 7-8. Sequence UP and DOWN

A. It's important to notice the t_{pd_ENx}, t_{pd_PWRGD}, and $t_{pD\_SEQ\_DONE}$ in blue. This is a propagation delay in the outputs (ENx,PWRGD and SEQ_DONE). If no DLY_TMR (floating) is used, the output signals will change to the valid state after this delay. When using the DLY_TMR, then this time has to be added to the programmed timer time.

B. The REG_TMR is only valid during sequence up.

7.3.4.1 DLY_TMR

The TPS7H3014 includes an adjustable time delay. A single resistor connected between the DLY_TMR pin and GND will program the delay. Possible resistor (R_{DLY}) values are between 10.5kΩ and 1.18MΩ for a 268μs to 23.63ms delay, respectively. During sequence up, this delay holds the EN_{x+1}, SEQ_DONE, and PWRGD low after the monitored voltage crosses the "on" voltage ($V_{OUTx} > V_{ONx}$) for the user programmed time. During sequence down, the EN_{x-1} and SEQ_DONE are held high for the programmed delay time after the monitored voltage crosses the "off" voltage ($V_{OUTx} < V_{OFFx}$).

备注

During sequence down, PWRGD goes low immediately after the $V_{\overline{DOWN}} < V_{TH\_\overline{DOWN}}$.

If no delay is preferred for the system, the pin (DLY_TMR) can be left floating. When no delay is preferred, an inherent propagation delay of 6.5μs (max) will be observed during sequence up, between V_{OUTx} crossing the V_{ONx} and EN_{x+1} going high. The propagation delay is also observed during sequence down when V_{OUTx} cross the V_{OFFx} and the EN_{x-1} is forced low. SEQ_DONE and PWRGD also have this propagation delay during $V_{OUT4} > V_{ON4}$ during sequence up. During sequence down, SEQ_DONE will go low after the propagation delay when $V_{OUT1} < V_{OFF1}$ and PWRGD will go low after the propagation delay when the sequence down is commanded. 图 7-8 shows the propagation delay in blue (t_{pd_ENx}, $t_{pd\_SEQ\_DONE}$, t_{pd_PWRGD}) and the programmed delay (t_{DLY_TMR}) in orange. The DLY_TMR resistor can be selected using 方程式 15. 图 7-9 shows the linear trend between the DLY_TMR resistor and the delay time.

$$R_{DLY\_TMR}(k\Omega) = \left[50.61 \times t_{DLY\_TMR}(ms)\right] - 6.422 \quad (15)$$

表 7-1 shows nominal resistors value for different delay times.

表 7-1. Typical DLY_TMR Resistors

Delay (ms)	R_{DLY_TMR} (kΩ)
0.268	10.5
12.5	619
23.37	1180

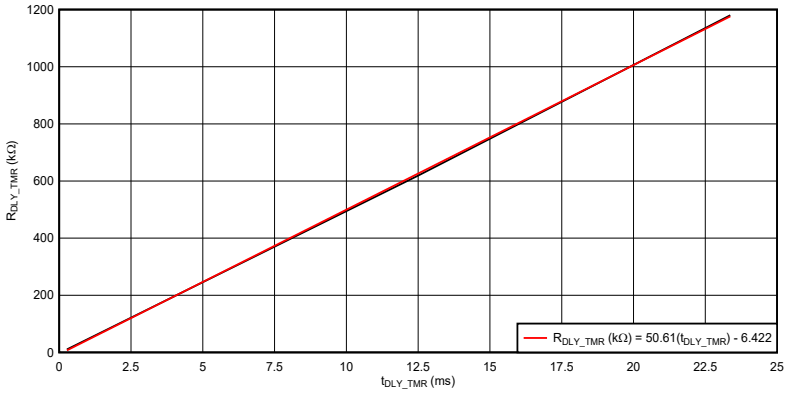

图 7-9. R_{DLY_TMR} vs t_{DLY_TMR} Across Full Oscillator Range

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7.3.4.2 REG_TMR

The REG_TMR (for regulation timer) is an adjustable time monitor that monitors the time it takes to V_{OUTx} > V_{ONx}. The user can program the REG_TMR using a single resistor between REG_TMR and GND. The range of the resistor (R_{REG}) is between 10.5kΩ to 1.18MΩ, for a 264 µs to 23.63ms, respectively. If the user does not want the REG_TMR to be active, the pin can be left floating. In this case, V_{OUTx} has infinite time to cross the V_{ONx} voltage. The REG_TMR is only active during the sequence up.

备注

If the REG_TMR is left floating and the V_{ONx} voltage is never crossed, the state machine will stay waiting indefinitely.

If active, the REG_TMR will monitor the time a V_{OUTx} takes to cross the V_{ONx} voltage once the ENx signal is forced high. In the case the REG_TMR is expired and V_{OUTx} has not crossed the V_{ONx} voltage, a reverse sequence down from the previously sequenced rail will be started as described in the State Machine section. 图 7-8 shows the REG_TMR active during sequence up, from the time ENx is forced high (V_{OUTx} starts rising). In this case, V_{OUTx} always crosses V_{ON} before the timer is expired. The REG_TMR resistor can be selected using 方程式 16. 图 7-10 shows the linear trend between the REG_TMR resistor and the regulation time allowed for the rail to be in regulation (V_{OUTx} > V_{ONx}).

$$R_{DLY\_TMR}(k\Omega) = \left[50.05 \times t_{DLY\_TMR}\,(ms)\right] - 2.369 \quad (16)$$

表 7-2 shows typical resistor values for different allowed regulation times.

表 7-2. Typical REG_TMR Resistors

Allowed Regulation Time (ms)	R_{REG_TMR} (kΩ)
0.264	10.5
12.4	619
23.63	1180

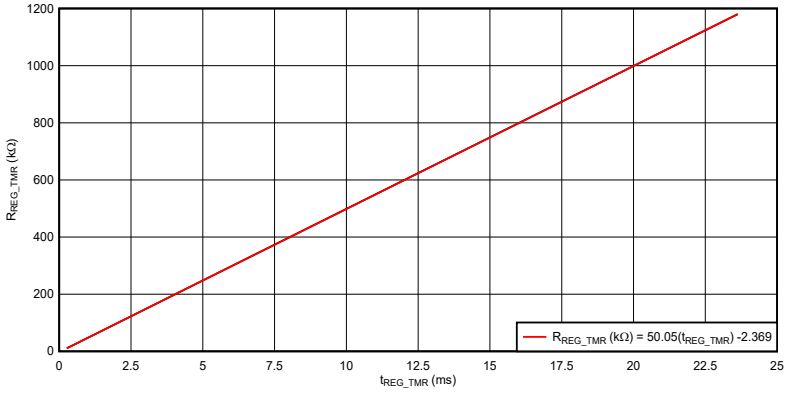

图 7-10. R_{REG_TMR} vs t_{REG_TMR} Across Full Oscillator Range

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7.3.5 UP and $\overline{\text{DOWN}}$

The UP and $\overline{\text{DOWN}}$ pins are the inputs that initiate a sequence up or down. Both pins incorporate an accurate comparator with a threshold voltage of V_{TH_UP} = 599mV (for UP) and $V_{TH\_\overline{DOWN}}$ = 498mV (for $\overline{\text{DOWN}}$) with an accuracy of ±3% for both inputs.

A fixed hysteresis of 100mV is incorporated in both comparators for noise stability. The edges on these pins are used to initiate the command as:

- Rising edge on UP starts a sequence up.
- Falling edge on $\overline{\text{DOWN}}$ starts a sequence down.

The UP voltage is also used in the state machine as a latch method to prevent oscillations during a FAULT. In order to move away from the Fault state, the UP voltage has to be logic low. As UP is a comparator with 100mV of hysteresis, depending on whether the V_{UP} have been previously above the V_{TH_UP}, the logic low level is:

- $V_{TH\_UP} \leqslant$ 599mV (typ) if UP has not previously been above V_{TH_UP}.
- V_{UP_TH} (typically 600mV) – 100mV $\leqslant$ 500mV (typ) if UP has previously crossed V_{UP_TH}.

These inputs can be driven externally by a house-keeping controller or via a resistive divider connected to a voltage source.

As these inputs are edge sensitive, is important to have a stable input voltage ($UVLO_{RISE}$ < V_{IN} < 14V) for at least 2.8ms ($t_{Start\_up\_delay}$) before sending the sequence up command. This is due to internal time constants in the device. During sequence down, it's important to maintain a stable input voltage until the SEQ_DONE flag is set low to allow all rails to be properly sequenced down.

As both the UP and $\overline{\text{DOWN}}$ pins have accurate undervoltage comparators, the user can program the voltage at which the system will automatically start the sequence up and down when monitoring a main power rail (V_{MAIN}) via a resistive divider. However, in this case it is important to make sure the rising and falling edge are sent when V_{IN} is stable, as mentioned before. A capacitor can be added from UP to GND to delay the signal when the slew rate at V_{MAIN} is fast.

Usually the designer knows the voltages at which it's desired to start the sequence up (referred to as V_{UP_IDEAL}) and down (referred to as $V_{\overline{DOWN}\_IDEAL}$). With that information we can calculate the resistive divider values using 方程式 17 and 方程式 18. Usually the top resistor is fixed to a 10kΩ value.

$$R_{BOTTOM\_UP} = R_{TOP\_UP} \times \frac{V_{TH\_UP}}{V_{UP\_IDEAL} - V_{TH\_UP}} \tag{17}$$

$$R_{BOTTOM\_\overline{DOWN}} = R_{TOP\_\overline{DOWN}} \times \frac{V_{TH\_\overline{DOWN}}}{V_{\overline{DOWN}\_IDEAL} - V_{TH\_\overline{DOWN}}} \tag{18}$$

where:

- V_{TH_UP}= 598mV (typical)
- $V_{TH\_\overline{DOWN}}$= 498mV (typical)

Once the designer knows the actual (real) resistive divider values, 方程式 19 and 方程式 20 can be used to calculate the sequence up and down nominal voltages as:

$$V_{UP\_NOMINAL}\ (V) = \left(1 + \frac{R_{TOP\_UP}}{R_{BOTTOM\_UP}}\right) \times V_{TH\_UP} \tag{19}$$

$$V_{\overline{DOWN}\_NOMINAL}\ (V) = \left(1 + \frac{R_{TOP\_\overline{DOWN}}}{R_{BOTTOM\_\overline{DOWN}}}\right) \times V_{TH\_\overline{DOWN}} \tag{20}$$

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If desired, to select the capacitance (C_{DELAY}) for the UP pin we can use 方程式 21.

$$C_{DELAY}\left(F\right) > \frac{t_{DELAY}(s)}{R_{TH}\left(\Omega\right) \times \ln\left(-\frac{V_{TH}(V)}{V(t) - V_{TH}(V)}\right)} \quad (21)$$

where:

- t_{DELAY} (s) is the desired delay time in seconds (at least 2.8ms after V_{IN} > $UVLO_{RISE}$).
- R_{TH} is the Thévenin equivalent resistance. In this case the parallel between R_{TOP} and R_{BOTTOM} in ohms.
  - $$R_{TH}\left(\Omega\right) = \frac{R_{TOP}\left(\Omega\right) \times R_{BOTTOM}(\Omega)}{R_{TOP}\left(\Omega\right) + R_{BOTTOM}(\Omega)} \quad (22)$$
- V_{TH} is the Thévenin equivalent voltage. In this case the voltage at V_{UP} during steady state operation in volts.
  - $$V_{TH}\left(V\right) = \left(\frac{R_{BOTTOM}(\Omega)}{R_{TOP}\left(\Omega\right) + R_{BOTTOM}(\Omega)}\right) \times V_{MAIN}\left(V\right) \quad (23)$$
- V(t) is the voltage at UP (V_{UP}) which will start the sequence up. In this case 598mV ±3%, in volts.

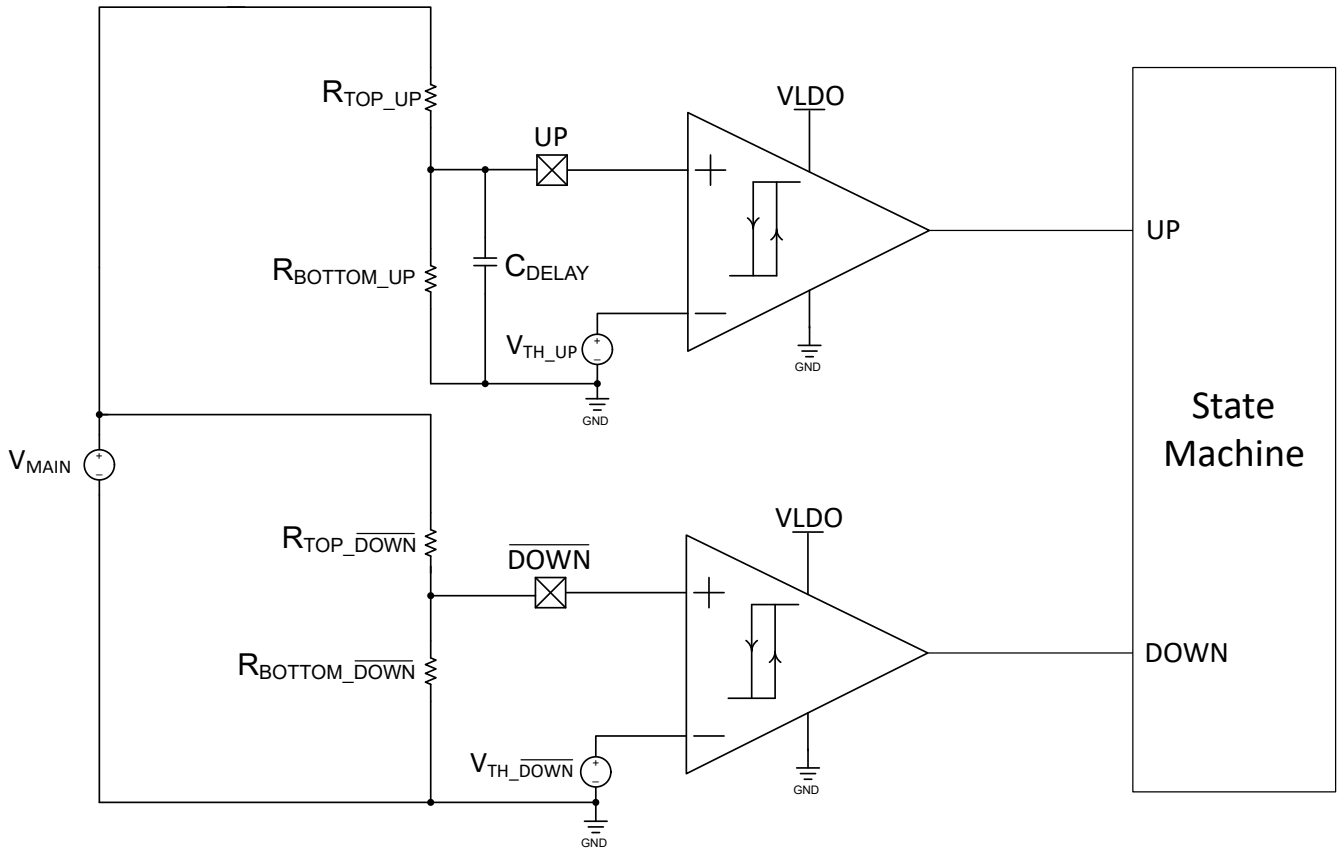

图 7-11. Monitor a Main Rail to Automatically Start the Sequence UP and $\overline{DOWN}$

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7.3.6 FAULT

The $\overline{\text{FAULT}}$ pin is an open-drain output that the user can use to monitor if an internal fault has been induced by the state machine. Is recommended to pull this pin to the VLDO output via a 10kΩ resistor. Another voltage source can be used if needed, but is important that this voltage is stable and greater than 1V at all times. The maximum voltage at this pin is 7V. For proper operation this voltage must be stable before attempting a sequence up/down and must never go below 1V during the device operation. The open-drain FET is forced low when the internal state machine of the sequencer detects a fault as described in State Machine .

7.3.7 State Machine

The TPS7H3014 incorporates a comprehensive state machine engine. Three possible outcomes are possible depending on the detected inputs states.

1. A reverse sequence down from previously deemed-good (forced high) ENx signals, is started if:
   - V_{OUTx} fails to reach the V_{ONx} voltage during sequence up within the time establish by the REG_TMR, when ENx is high.
   - Any V_{OUTx} crosses the V_{OFFx} after previously crossing the V_{ONx} and the V_{OUTx+1} has not yet crossed the V_{ONx+1}.
   - The users command a sequence down in the middle of a sequence up.
2. All outputs (ENx, SEQ_DONE and PWRGD) are forced low if an out-of-order is detected, this means:
   - A previously deemed-good rail V_{OUTx} drops below V_{OFFx} when at least the V_{OUTx+1} is already in regulation (deemed-good).
   - Any $V_{OUTx} > V_{ONx}$ when EN_X is not high. **Valid only during sequence up**.

   备注

   It is typical in sequencers to set V_{ONx} as some percentage of the nominal voltage to be monitored (E.g. $V_{ONx} = 0.8 \times V_{OUTx}$). There is a period of time during sequence down at which the $V_{OUTx} \geqslant V_{ONx}$. As the discharge rate of the rail (V_{OUTx}) is unknown to the TPS7H3014, this feature is only valid during sequence up.
3. A sequence up from previously forced low ENx signals, after the DLY_TMR is expired is started if:
   - The users command a sequence up in the middle of a sequence down.

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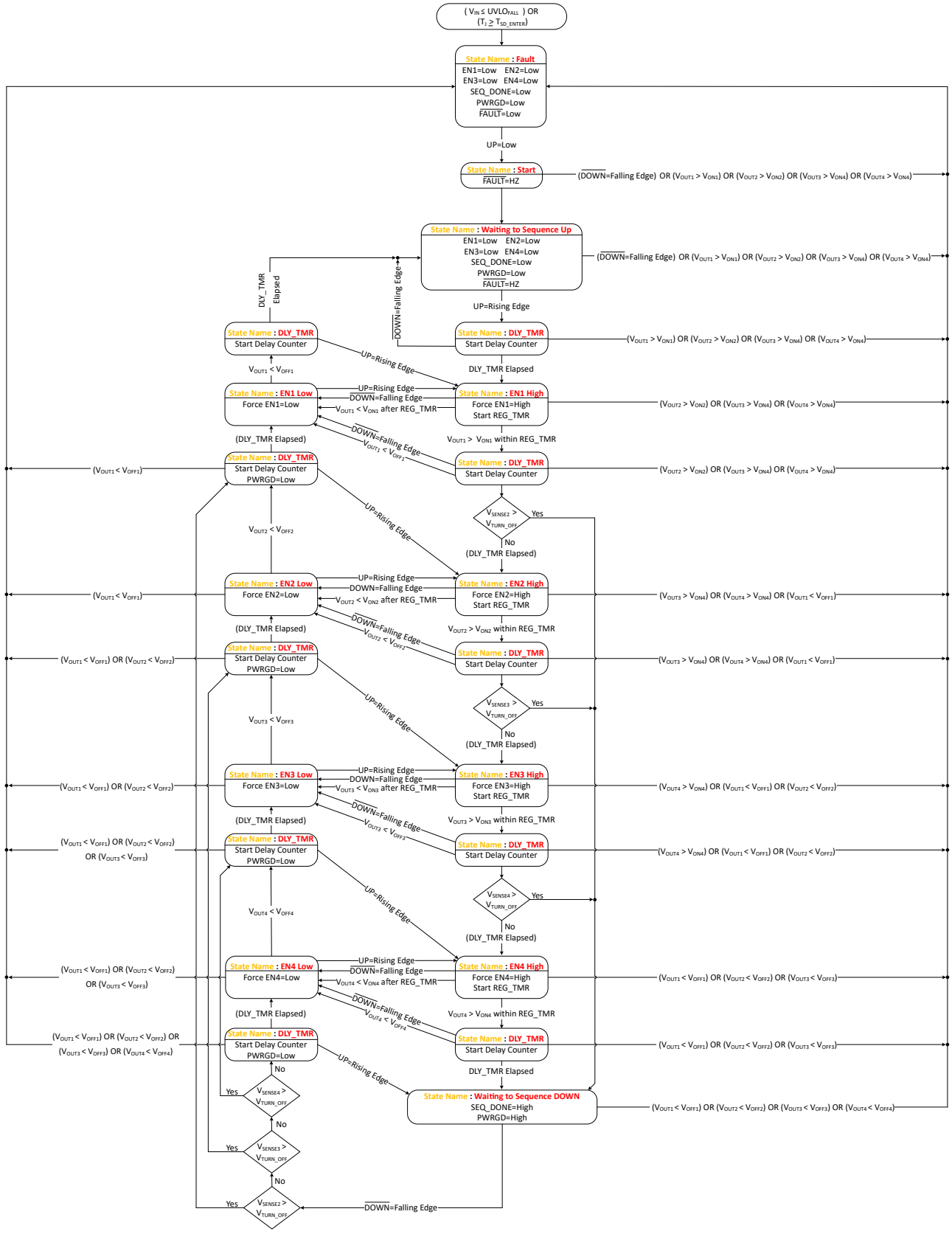

图 7-12. TPS7H3014 State Machine Diagram

7.4 Daisy Chain

The TPS7H3014 incorporates four input channels to sequence/monitor up to four voltage rails. However, in the case where more than four channels are needed in the application, multiple devices can be daisy chained as needed. The daisy chain configuration is shown in 图 7-13. In this case, only two devices are shown, however multiple IC can be configured as needed by the application.

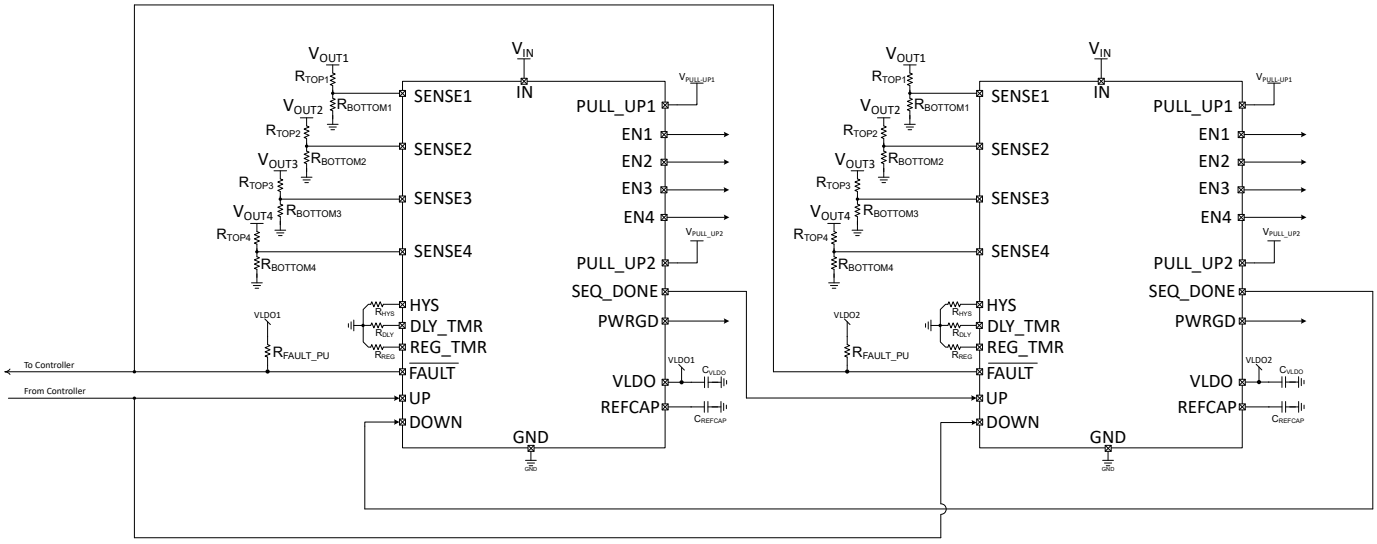

图 7-13. Daisy Chain Configuration

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8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS7H3014 is a radiation hardened 4-channel sequencer. It can be used to sequence FPGAs, ASICs, AFEs, and various power systems

8.2 Typical Application

8.2.1 Self Contained – Sequence UP and DOWN

In many modern systems (or sub-systems), multiple voltage rails are often needed (we refer to this as the power tree). Often these power trees have a specified sequencing up order and reverse sequence down needed to guarantee reliable system operation. Is not uncommon for these systems to also have timing specifications which cannot be infringed for correct operation. In this example, four voltage rails are sequenced and monitored via the ENx outputs and SENSEx inputs, respectively. Detailed design procedure and component selection is provided below. The design is summarized in 图 8-1.

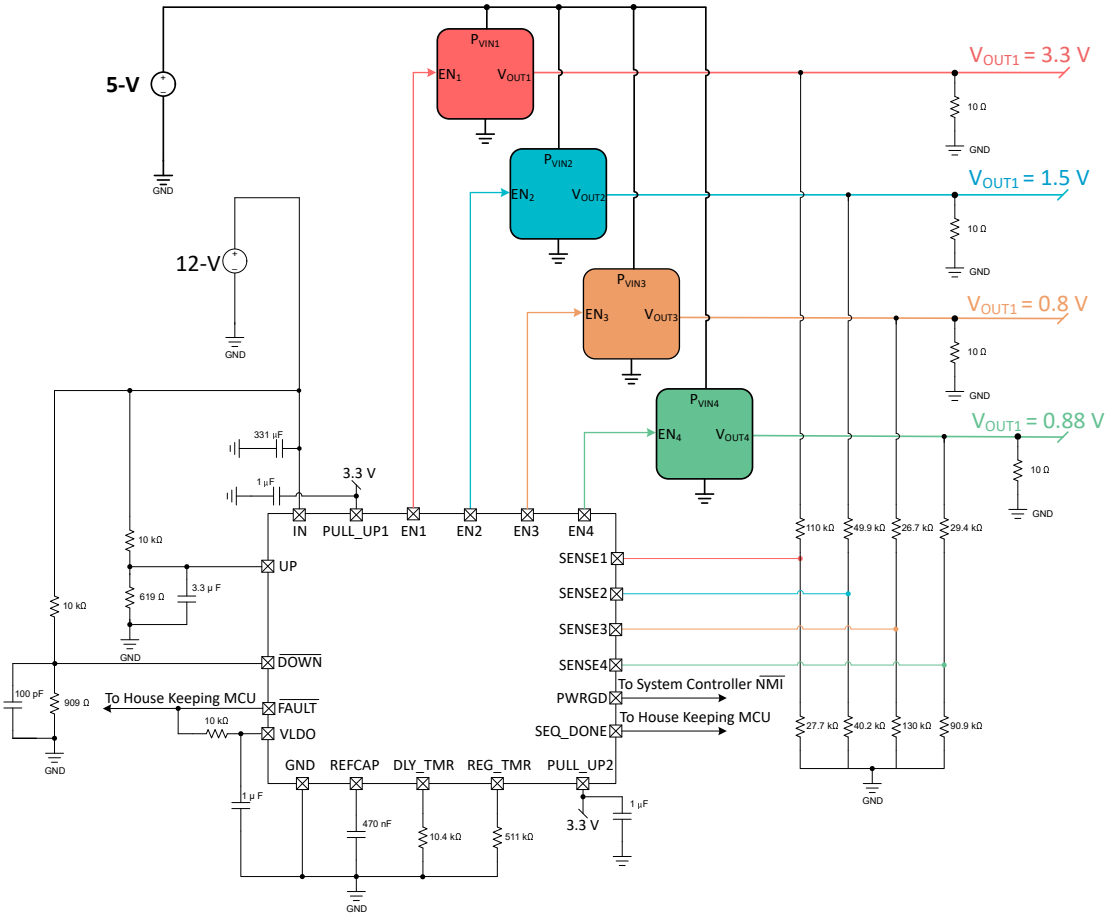

图 8-1. Self Contained Sequence UP/DOWN Design for a Four Voltage Rail Power Tree

8.2.1.1 Design Requirements

This design requires voltage sequencing of four voltage rails. The nominal TPS7H3014 input voltage is 12V and the sequencer is set to start the sequence up and down automatically when the voltage reaches the desired target voltage levels. All the voltage regulators are powered by a nominal 5V voltage rail. The system housekeeping microcontroller can monitor a fault via the voltage at the $\overline{\text{FAULT}}$ pin, which is pulled-up to VLDO. The PWRGD is the flag to be connected to the non-maskable interrupt of the system if it exists, or monitored by the MCU to know the status of the power tree. The SEQ_DONE can also be monitored to know if the sequence up/down are completed. All design conditions are defined in 表 8-1.

表 8-1. Design Conditions

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
System nominal voltage	Monitor the 12V input voltage and start the sequence up when the voltage is greater than 10.7V (88%) for at least 3.7ms. When the voltage decrements below 6V (or 50%) a sequence down is started.	The TPS7H3014 can monitor a voltage and start a sequence up and down automatically via a resistive divider. The internal reference in UP and $\overline{\text{DOWN}}$ have an accuracy of 3%. For minimal error, it is recommended to use 0.1% tolerance resistors.
V_{OUT1}	3.3V nominal with: V_{ON} = 90% and V_{OFF} = 10%	V_{ON} = 2.978V ±29.97mV V_{OFF} = 0.338V ±84.61mV Using 0.1% tolerance resistors
V_{OUT2}	0.8V nominal with: V_{ON} = 90% and V_{OFF} = 10%	V_{ON} = 0.722V ±7.22 mV V_{OFF} = 0.081V ±20.54mV Using 0.1% tolerance resistors
V_{OUT3}	1.5V nominal with: V_{ON} = 90% and V_{OFF} = 10%	V_{ON} = 1.343V ±13.47mV V_{OFF} = 0.145V ±38.35mV Using 0.1% tolerance resistors
V_{OUT4}	0.88V nominal with: V_{ON} = 90% and V_{OFF} = 10%	V_{ON} = 0.793V ±7.93mV V_{OFF} = 0.087V ±22.6mV Using 0.1% tolerance resistors
ENx delay during sequence up and down	Delay of 0.268ms nominal	R_{DLY_TMR} = 10.4kΩ
Allowed time for a rail to reach the V_{ONx}	Allow 10.3ms (nominal) for the rail to reach the V_{ONx}	R_{REG_TMR} = 511kΩ

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Input Power Supplies and Decoupling Capacitors

The TPS7H3014 has three input power supplies:

1. IN, the input supply to provide power to the TPS7H3014 IC. It is recommended to decouple this power supply with at least 1 µF as close to the pin as possible. In this application, V_{IN} = 12V.
2. PULL_UP1, which is the input supply to program the output voltage high (V_{OH}) of all the enable outputs (ENx). These outputs are connected to the regulator enable inputs to control the sequence up and down. It is recommended to decouple this power supply with at least 1 µF as close to the pin as possible. In this application, the V_{PULL_UP1} = 3.3V. This is a typical voltage used in electronic systems and satisfies the logic inputs of most regulators in the market.
3. PULL_UP2, which is the input supply to program the output voltage high (V_{OH}) of PWRGD and SEQ_DONE outputs. These outputs are typically connected to the system controller (typically an FPGA or ASIC) and/or to the house-keeping controller. In daisy chain configurations, SEQ_DONE is connected to UP of subsequent TPS7H3014 I.C. as shown in 图 7-13. It is recommended to decouple this power supply with at least 1 µF as close to the pin as possible. In this application, the V_{PULL_UP1} = 3.3V. This is a typical voltage of controller I/Os.

The TPS7H3014 also has two regulated voltage outputs that need to be decoupled for good electrical and radiation performance. These are:

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1. REFCAP, the 1.2V reference, used internally in the device to generate all ratiometric voltage reference such as:
   - V_{TH_SENSEx}
   - I_{HYS_SENSEx}
   - V_{TH_UP}
   - $V_{TH\_\overline{DOWN}}$

   Decouple this reference with a 470nF ceramic capacitor as close to the pin as possible. Do not load this pin externally.
2. VLDO, this is the output of the internal regulator used to provide power to the internal circuits on the TPS7H3014. Is recommended to decouple this regulator with at least 1 µF as close to the pin as possible. The valid loading of this regulator is:
   - To turn-off channels 2 – 4 as needed.
   - To pull-up the $\overline{FAULT}$ open-drain output.

8.2.1.2.2 UP and $\overline{DOWN}$ Thresholds

In this application the UP and $\overline{DOWN}$ pins are used to monitored the input voltage supply of 12V. A sequence up is started when the rail voltage is greater than 10.7 (typ) and down when the voltage is lower than 6V (typ). As the TPS7H3014 has an internal time constant ($t_{Start\_up\_delay}$) of 2.8ms (max), a delay capacitor of 3.3 µF is added to UP pin. This capacitor is added to introduce a delay in the UP pin when V_{IN} is rising. This capacitor adds a second condition to start the sequence up, if $V_{IN} \geqslant$ 10.7V (typ) for at least 2.8ms then the sequence up is commanded.

Fixing the upper resistor for the resistive divider in UP and $\overline{DOWN}$, we can calculate the bottom resistor per our design requirements. The upper resistor is fixed to 10kΩ for both cases. Using the equations in 方程式 17 and 方程式 18, the bottom resistors for up and down are calculated as:

$$R_{BOTTOM\_UP} = 10\ k\Omega \times \frac{0.598\ V}{10.7\ V - 0.589\ V} \cong 594\ \Omega \quad (24)$$

$$R_{BOTTOM\_\overline{DOWN}} = 10\ k\Omega \times \frac{0.498\ V}{6\ V - 0.498\ V} \cong 905\ \Omega \quad (25)$$

Now that the reference resistors are calculated, we can select the actual (or real) resistors. In this case 0.1% tolerance resistors are used to select the closest value as:

- R_{BOTTOM_UP} = 619Ω
- $R_{BOTTOM\_\overline{DOWN}}$ = 909Ω

With the actual resistor values, we can back-calculate the nominal voltage to start the sequence up and down using 方程式 19 and 方程式 20 as:

$$V_{UP\_NOMINAL}(V) = \left(1 + \frac{10\ k\Omega}{619\ \Omega}\right) \times 12\ V \cong 10.66\ V \quad (26)$$

$$V_{\overline{DOWN}\_NOMINAL}(V) = \left(1 + \frac{10\ k\Omega}{909\ \Omega}\right) \times 12\ V \cong 5.97\ V \quad (27)$$

The delay capacitor is calculated using 方程式 21, 方程式 22, and 方程式 23 as:

$$R_{TH}(\Omega) = \frac{10\ k\Omega \times 619\ \Omega}{10\ k\Omega + 619\ \Omega} = 582.9\ \Omega \quad (28)$$

$$V_{TH}(\Omega) = \left(\frac{619\ \Omega}{10\ k\Omega + 619\ \Omega}\right) \times 12\ V = 0.7\ V \quad (29)$$

$$C_{DELAY}(F) \geq \frac{0.0028\ s}{582.9\ \Omega \times \ln\left(-\frac{0.7\ V}{0.598\ V - 0.7\ V}\right)} = 2.49\ \mu F \quad (30)$$

The delay capacitor is selected as 3.3 µ F.

8.2.1.2.3 SENSEx Thresholds

The SENSEx inputs are used to monitor the voltage rails to be sequenced up and down. For this design the output voltages to be sequenced and monitored are:

1. V_{OUT1} = 3.3V
2. V_{OUT2} = 0.8V
3. V_{OUT3} = 1.5V
4. V_{OUT4} = 0.88V

The V_{ON} and V_{OFF} are selected to be 90% and 10% of the nominal voltage rail, for all the rails. Using 方程式 13 and 方程式 14 we can calculate the top and bottom reference resistors and select the closest resistor values using 0.1% resistor values. 表 8-2 shows the reference (or calculated) top and bottom resistors. 表 8-3 shows the selected resistors for the application.

表 8-2. SENSEx Reference Nominal Resistors

Channel #	V_{ON} (V)	V_{OFF} (V)	R_{TOP} (kΩ)(1)	R_{BOTTOM} (kΩ)(1)
1	2.970	0.330	110.0	27.8
2	1.350	0.150	50.0	39.9
3	0.720	0.080	26.7	132.0
4	0.792	0.088	29.3	91.0

(1) Values are rounded to one decimal place.

An example of how the top and bottom resistors for channel 1 (or SENSE1) were calculated are shown below:

$$\frac{2.970\ \text{V} - 0.330\ \text{V}}{24\ \mu\text{A}} = 110\ \text{k}\Omega \tag{31}$$

$$\frac{110\ \text{k}\Omega \times 0.599\ \text{V}}{2.970\ \text{V} - 0.599\ \text{V}} = 39.88\ \text{k}\Omega \tag{32}$$

表 8-3. SENSEx Selected Resistors Using 0.1 % Tolerance Resistors

Channel #	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)
1	110	27.7
2	49.9	40.2
3	26.7	130
4	29.4	90.9

Now that the actual resistors are known, we can calculate the actual on and off nominal voltages and the error voltages by using 方程式 1, 方程式 2, 方程式 3, 方程式 6, 方程式 7, and 方程式 12. Using the errors, we can calculate the upper and lower voltages and normalize the values with respect to the nominal output voltage.

表 8-4. V_{ON} Nominal Values With Statistics in Volts and Percentage

Channel #	$V_{ON\_NOMINAL}$ (V)(1)	$V_{ON\_NOMINAL}$ (%)(1) (4)	V_{ON_ERROR} (mV)(1)	V_{ON_LSL} (V)(1) (2)	V_{ON_LSL} (%)(1) (2) (4)	V_{ON_USL} (V)(1) (3)	V_{ON_USL} (%)(1) (3) (4)
1	2.978	90.232	29.966	2.948	89.325	3.008	91.141
2	1.343	89.502	13.466	1.329	88.605	1.356	90.400
3	0.722	90.253	7.222	0.715	89.350	0.729	91.156
4	0.793	90.084	7.932	0.785	89.182	0.801	90.985

(1) Values are rounded to three decimal places.
(2) LSL stands for lower specification limit or the min.
(3) USL stands for upper specification limit or the max.
(4) Values are normalized to the nominal output voltage for that rail.

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表 8-5. V_{OFF} Nominal Values with Statistics in Volts and Percentage

Channel #	$V_{OFF\_NOMINAL}$ (V)(1)	$V_{OFF\_NOMINAL}$ (%)(1) (4)	V_{OFF_ERROR} (mV)(1)	V_{OFF_LSL} (V)(1) (2)	V_{OFF_LSL} (%)(1) (2) (4)	V_{OFF_USL} (V)(1) (3)	V_{OFF_USL} (%)(1) (3) (4)
1	0.338	10.233	84.613	0.253	7.669	0.422	12.797
2	0.145	9.662	38.354	0.107	7.105	0.183	12.219
3	0.081	10.153	20.535	0.061	7.586	0.102	12.720
4	0.087	9.902	22.604	0.065	7.333	0.110	12.470

(1) Values are rounded to three decimal places.
(2) LSL stands for lower specification limit.
(3) USL stands for upper specification limit.
(4) Values are normalized to the nominal output voltage for that rail.

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8.2.1.3 Application Curves

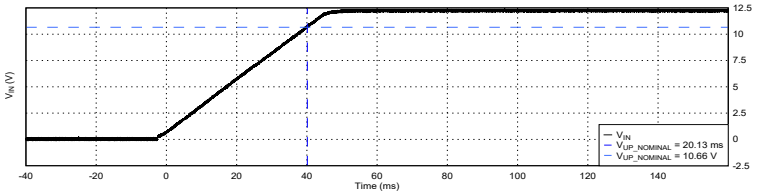


图 8-2. V_{IN} vs Time During Sequence UP

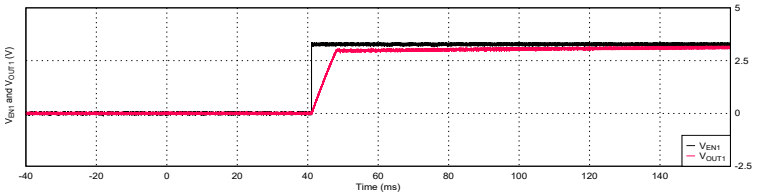


图 8-3. EN1 and V_{OUT1} vs Time During Sequence UP

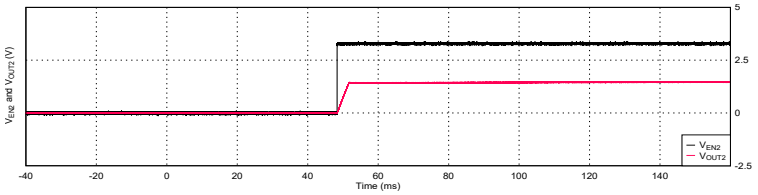


图 8-4. EN2 and V_{OUT2} vs Time During Sequence UP

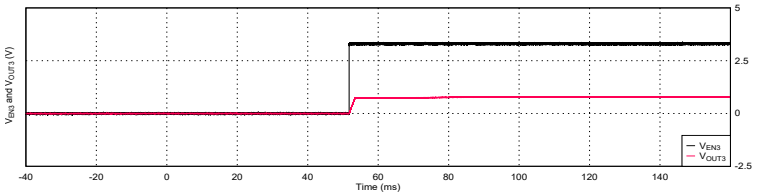


图 8-5. EN3 and V_{OUT3} vs Time During Sequence UP

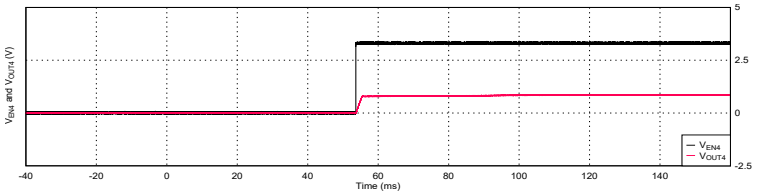


图 8-6. EN4 and V_{OUT4} vs Time During Sequence UP

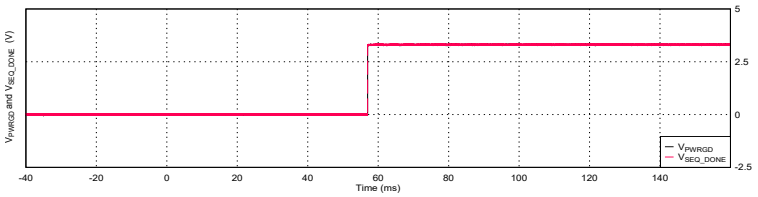


图 8-7. PWRGD and SEQ_DONE vs Time During Sequence UP

ADVANCE INFORMATION

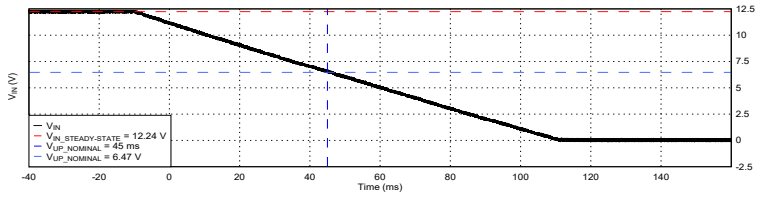


图 8-8. V_{IN} vs Time During Sequence DOWN

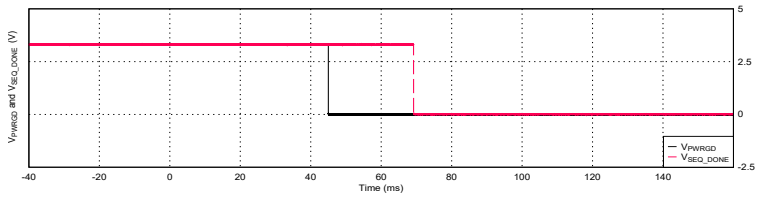


图 8-9. PWRGD and SEQ_DONE vs Time During Sequence DOWN

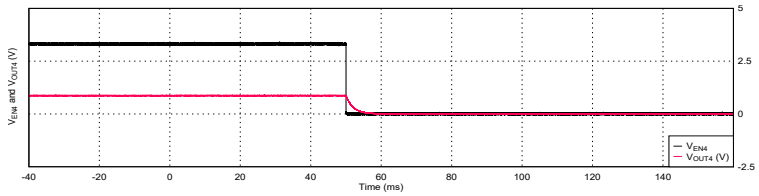


图 8-10. EN4 and V_{OUT4} vs Time During Sequence DOWN

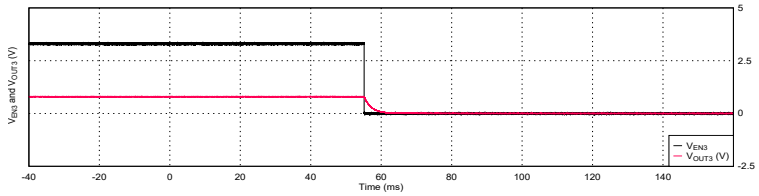


图 8-11. EN3 and V_{OUT3} vs Time During Sequence DOWN

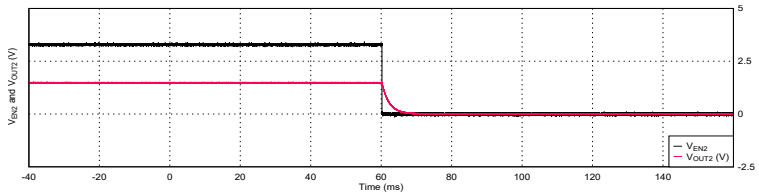


图 8-12. EN2 and V_{OUT2} vs Time During Sequence DOWN

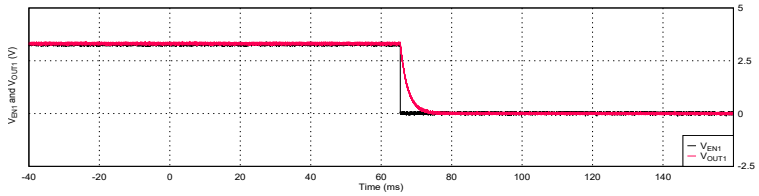


图 8-13. EN1 and V_{OUT1} vs Time During Sequence DOWN

ADVANCE INFORMATION

8.3 Power Supply Recommendations

The TPS7H3014 is designed to operate from an input supply (V_{IN}) with a voltage range between 3V to 14V. It is recommended to add at least one 1 µF ceramic capacitor from V_{IN} to GND as close to the pin as possible.

The PULL_UP1 and PULL_UP2 are also considered power inputs in this case for the push-pull outputs. The voltage range on these inputs are 1.6V to 7V. For these inputs, it is also recommend to add at least one 1 µF ceramic capacitor from PULL_UP1 to GND and from PULL_UP2 to GND. This capacitor must be placed as close to the pins as possible.

8.4 Layout

8.4.1 Layout Guidelines

- Make sure that the connection to the V_{IN} pin is low impedance. Place a greater than 1µF ceramic capacitor as near as possible to the V_{IN} pin.
- Make sure that the connection to the V_{PULL_UP1} and V_{PULL_UP2} pins are low impedance. Place a greater than 1µF ceramic capacitor as near as possible to the pins.
- If needed, place a small capacitor between the SENSEx pins and GND to reduce the sensitivity to transient voltages on the monitored signal.

8.4.2 Layout Example

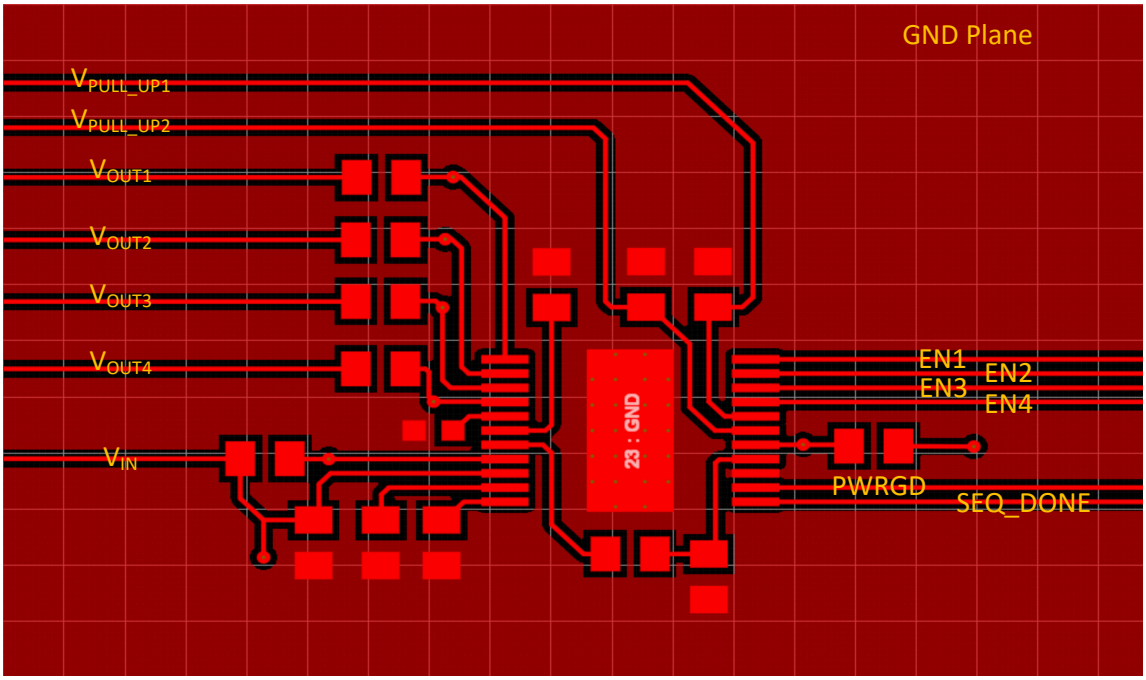


图 8-14. Printed Circuit Board Layout Example: Top Layer

ADVANCE INFORMATION

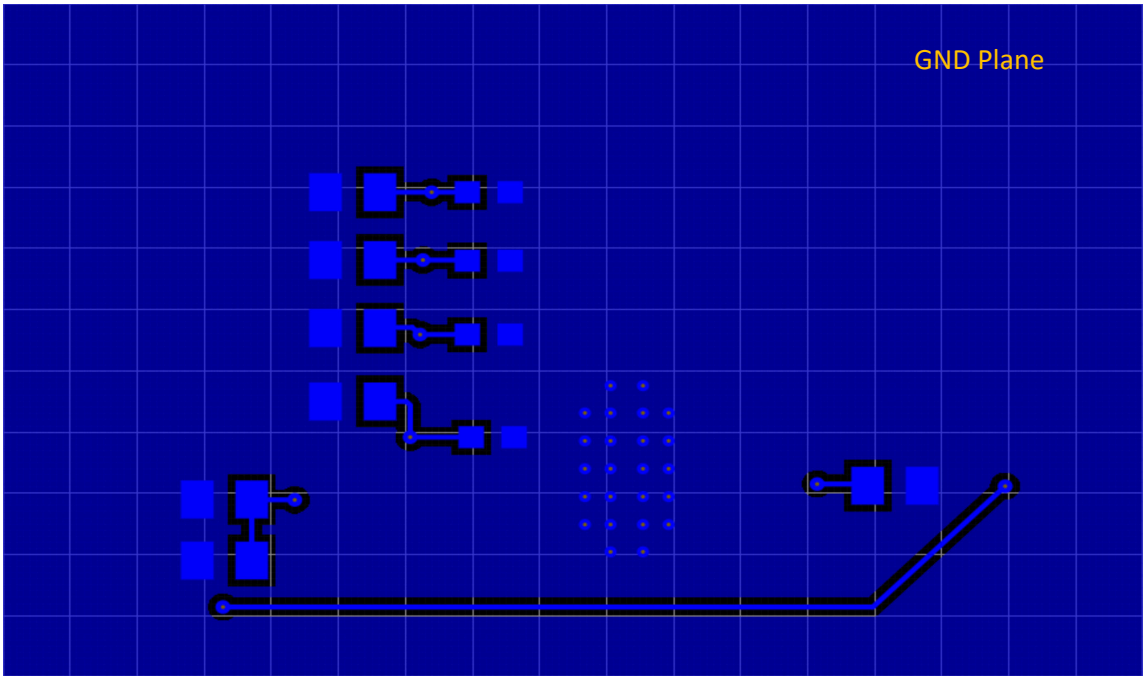


图 8-15. Printed Circuit Board Layout Example: Bottom Layer

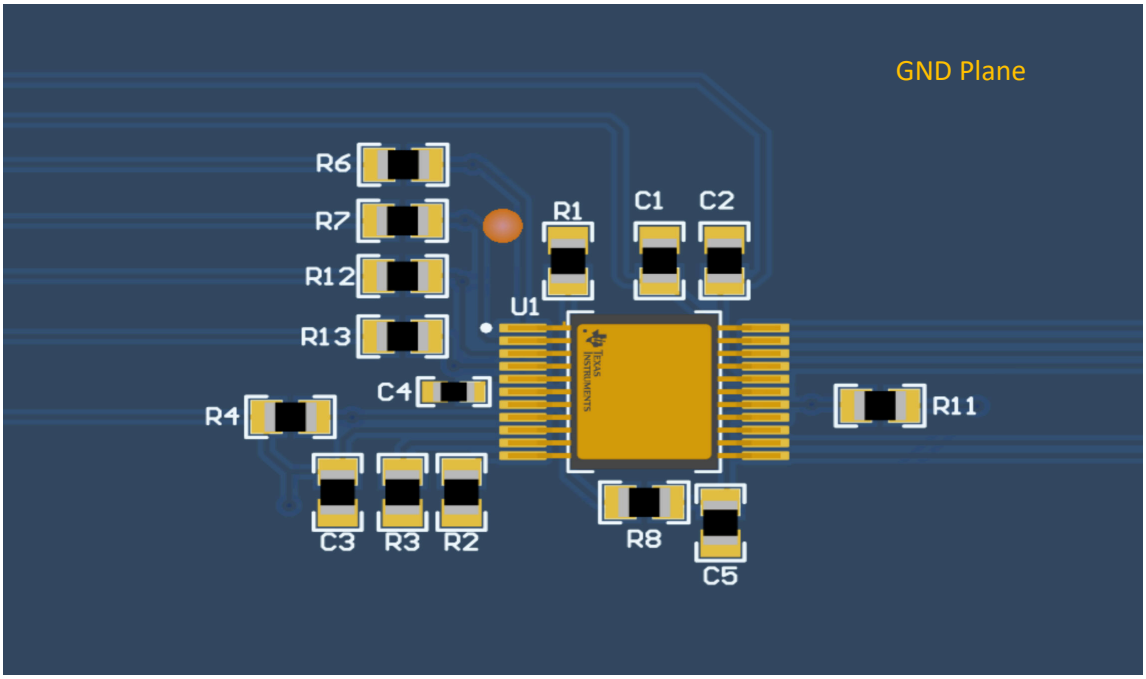


图 8-16. Printed Circuit Board Layout Example: Top Layer 3D View

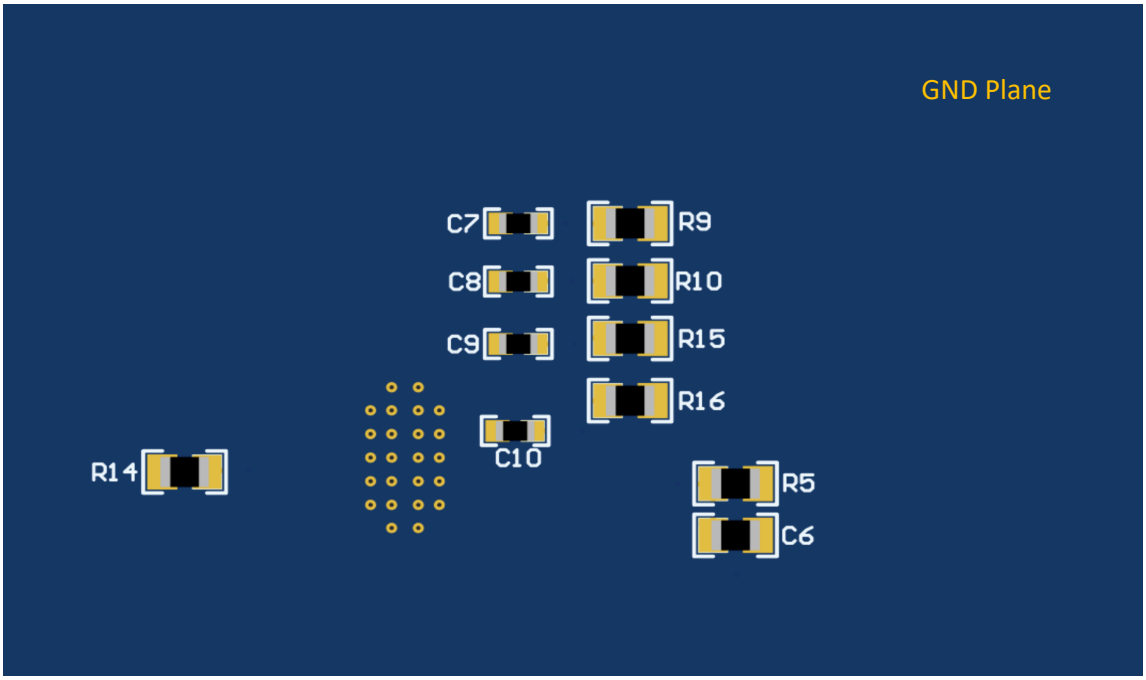


图 8-17. Printed Circuit Board Layout Example: Bottom Layer 3D View

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

The following related documents are available for download at www.ti.com:

- *TPS7H3014EVM-CVAL EVM User Guide*, SLVUCT9

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

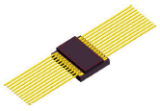
注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
January 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

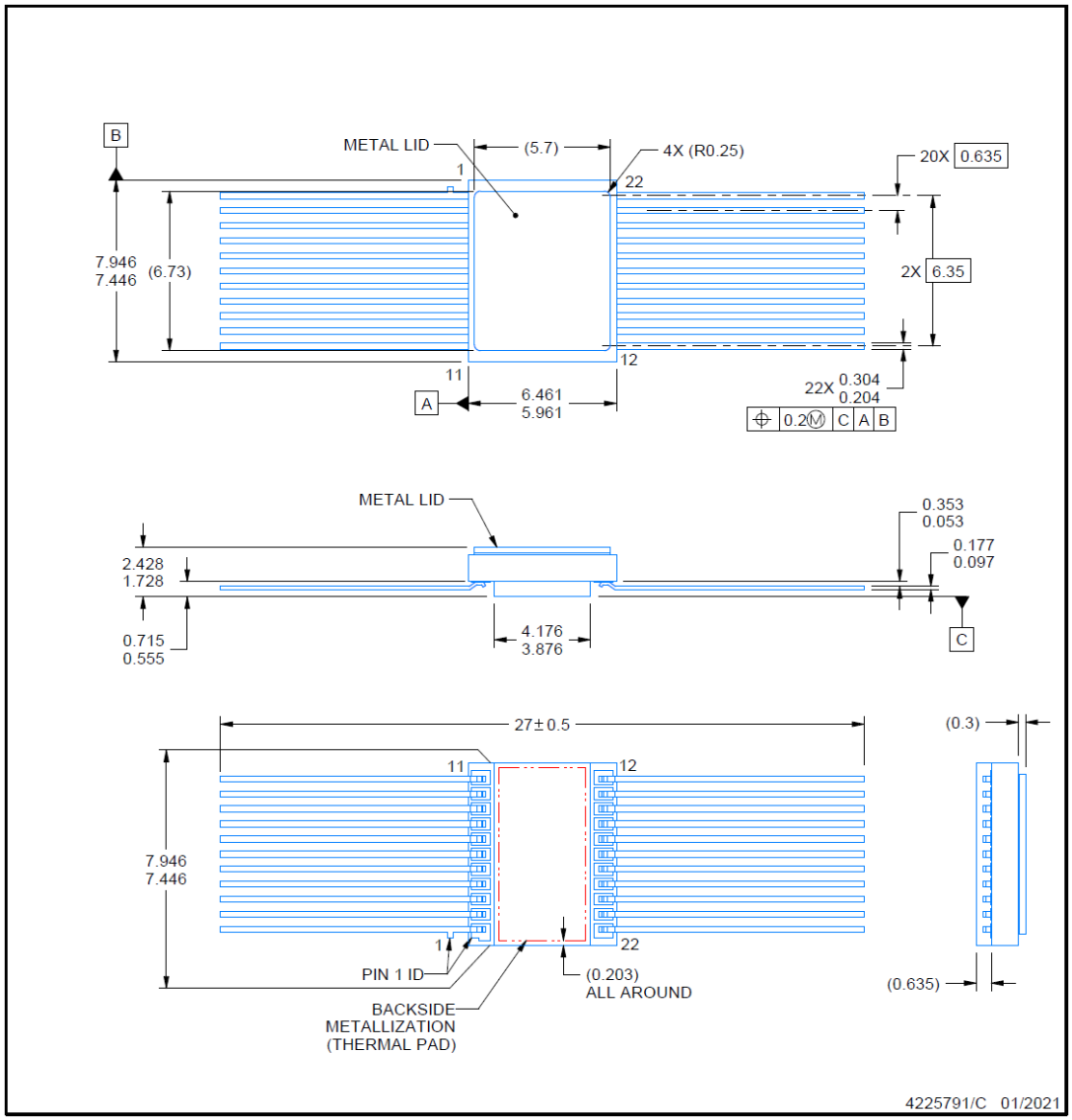


PACKAGE OUTLINE

HFT0022A

CFP - 2.428mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metalization

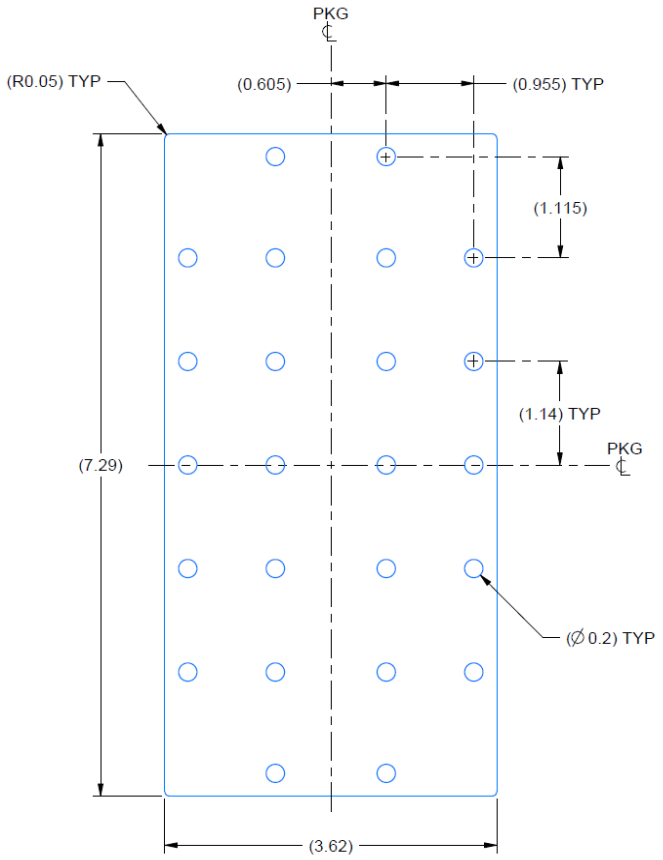
TEXAS INSTRUMENTS
www.ti.com

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

HFT0022A — **CFP - 2.428mm max height**

CERAMIC FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

4225791/C 01/2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7H3014HFT/EM	ACTIVE	CFP	HFT	22	1	TBD	Call TI	Call TI	25 to 25		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

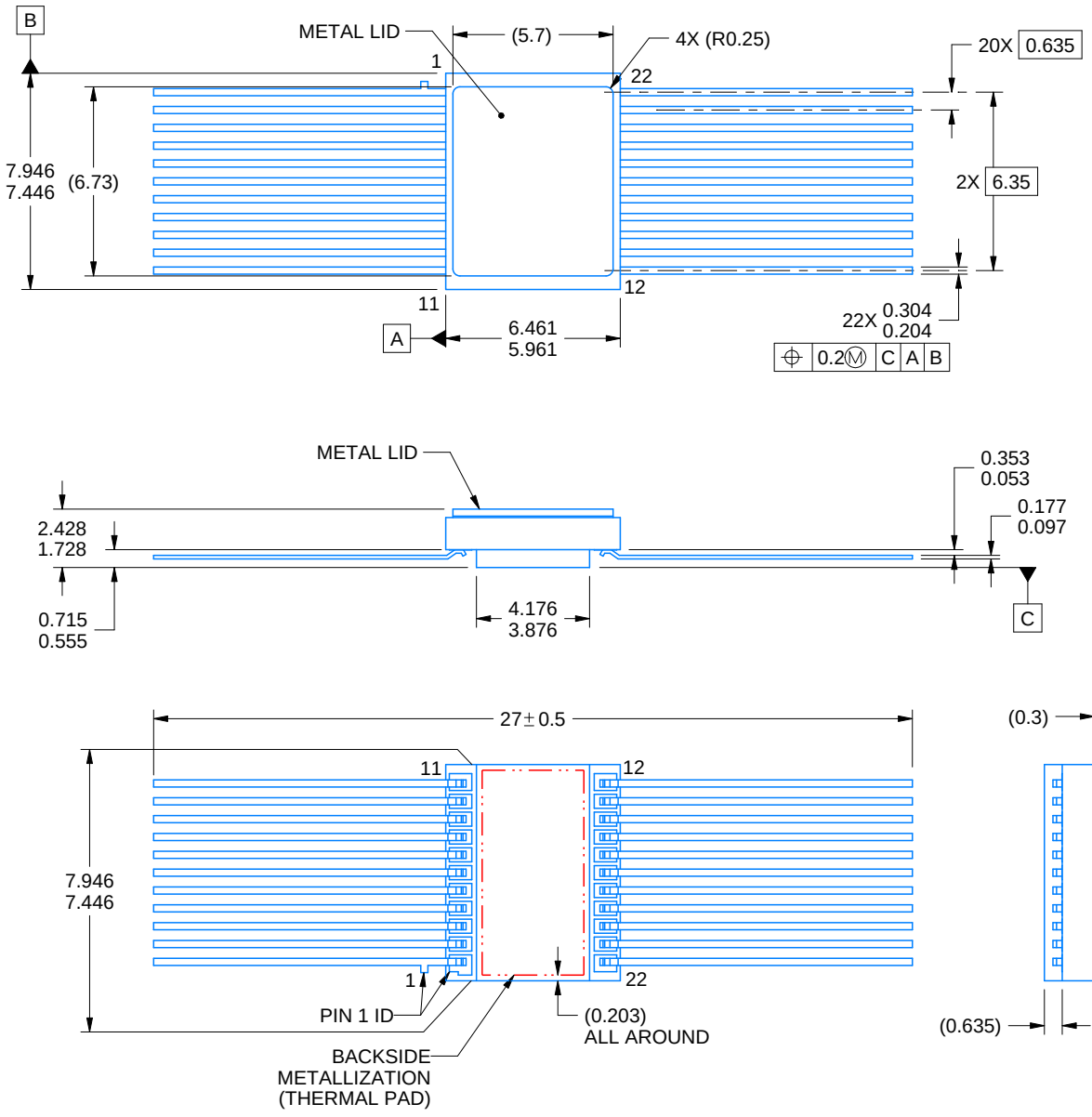
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

HFT0022A

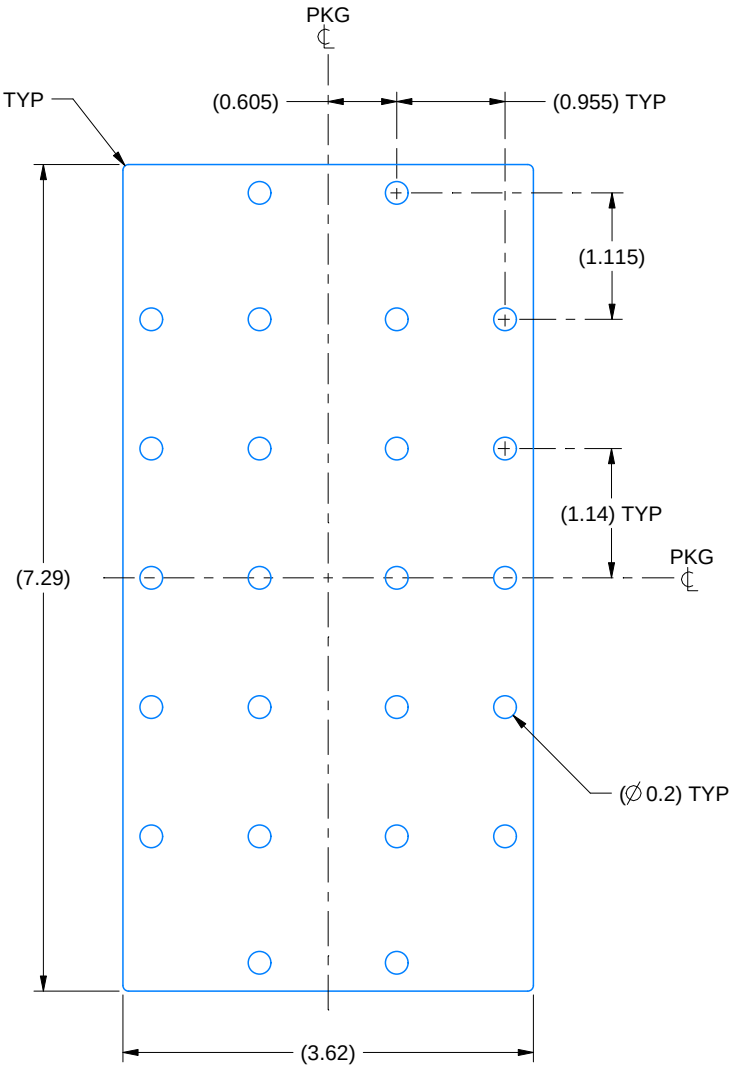
CFP - 2.428mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metalization



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

4225791/C 01/2021

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2186323	03/13/2020	R. RAZAK / ANIS FAUZI
B	ADD LAND PATTERN VIEW / SHEET	2190485	10/22/2020	R. RAZAK / ANIS FAUZI
C	UPDATE TOTAL LEAD LENGTH TO 27± 0.5	2192775	01/28/2021	R. RAZAK / ANIS FAUZI

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