TPS7B4253-Q1 具有 4mV 跟踪容差的 300mA 40V 低压降电压跟踪 LDO

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 3A
  - 器件组件充电模式 (CDM) ESD 分类等级 C6
- –40V 至 45V 宽输入电压范围（最大值）
- 可调节输出电压范围：
  - 1.5V 至 40V (HTSSOP)
  - 2V 至 40 V (SO PowerPAD™)
- 300mA 输出电流能力
- ±4mV 超低输出跟踪容差
- 320mV 低压降 (I_{OUT} = 200mA 时)
- 分别用于使能和跟踪输入的单独引脚（仅限 HTSSOP）
- 低静态电流 (I_Q)：
  - < 4µA（EN = 低电平时）
  - 轻负载时典型值为 60µA
- 超宽等效串联电阻 (ESR) 范围。
  - 与 10µF 至 500µF 范围内的陶瓷输出电容（ESR 为 1mΩ 至 20Ω）搭配使用时可保持稳定
- 反极性保护
- 限流和热关断保护
- 对接地和电源的输出短路保护
- 输出引脚感性钳位
- 提供以下封装：
  - 8 引脚小外形尺寸 (SO) PowerPAD 封装
  - 20 引脚散热薄型小外形尺寸 (HTSSOP) 封装

2 应用

- 非板载传感器电源
- 高精度电压跟踪
- 非板载负载的电源开关

3 说明

对于汽车非板载传感器和小电流非板载模块，电源通过一条长电缆连接主板。 在这类情况下，电源器件需要为非板载负载提供保护，防止板载组件在接地短路或者电缆破损造成的电池短路期间受损。 非板载传感器需要与板载组件采用相同的电源，以确保数据采集的高精度。

TPS7B4253-Q1 器件设计用于具有 45V 负载突降问题的汽车类应用。 该器件可用作一个跟踪低压降 (LDO) 稳压器或者电压跟踪器，通过板载主电源为非板载传感器构建一个封闭电源环路。 该器件的输出由 ADJ 引脚的基准电压精准调节。

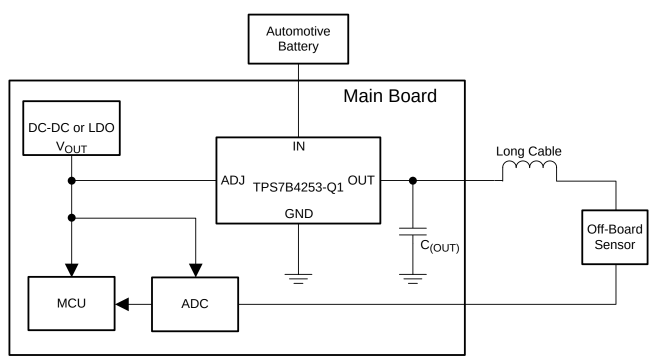
为了给非板载模块提供精确的电源，该器件的 ADJ 与 FB 引脚间在运行温度范围内具有 4mV 超低跟踪容差。 PMOS 背靠背拓扑消除了反极性条件下对外部二极管的需求。 TPS7B4253-Q1 器件还包括热关断、感性钳位、过载和电池短路保护，防止板载组件在极限条件下受损。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TPS7B4253-Q1	SO PowerPAD (8)	4.89mm × 3.90mm
	HTSSOP (20)	6.50mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



目录

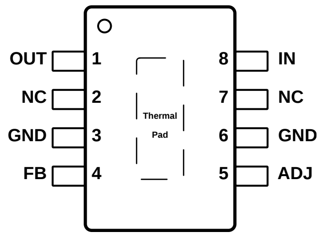
4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2015) to Revision A	Page
• 已更改 器件状态，*从产品预览更改为量产数据*	1

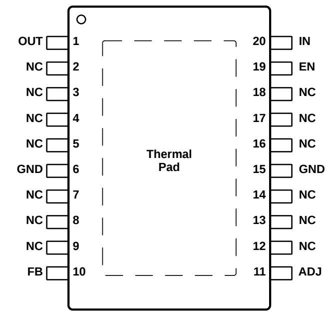
5 Pin Configuration and Functions

DDA Package
8-Pin SO PowerPAD
Top View



NC — No internal connection

PWP Package
20-Pin HTSSOP With Exposed Thermal Pad
Top View



NC — No internal connection

Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	SO PowerPAD	HTSSOP		
ADJ	5	11	I	Connect the reference to this pin. A low signal disables the device and a high signal enables the device. The reference voltage can be connected directly or by a voltage divider for lower output voltages. To compensate for line influences, connect a capacitor close to the device pins.
EN	—	19	I	This pin is the enable pin. The device goes to the STANDBY state when the enable pin goes lower than the threshold value.
FB	4	10	I	This pin is the feedback pin which can connect to the external resistor divider to select the output voltage.
GND	3	6	G	Ground reference
	6	15		
IN	8	20	I	This pin is the device supply. To compensate for line influences, connect a capacitor close to the device pins.
NC	2	2	NC	Not connected
		3		
		4		
		5		
		7		
		8		
		9		
	7	12		
		13		
		14		
		16		
		17		
		18		
OUT	1	1	O	Block to GND with a capacitor close to the device pins with respect to the capacitance and ESR requirements listed in the *Output Capacitor* section.
Exposed thermal pad			—	Connect the thermal pad to the GND pin or leave it floating.

(1) I = input, O = output, G = ground, NC = no connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Unregulated input voltage	IN(2)(3)	–40	45	V
Enable input voltage	Enable input voltage(2)(3)	–40	45	V
Regulated output voltage	Regulated output voltage(2)(4)	–1	45	V
Voltage difference between the input and output	IN – OUT	–40	45	V
Reference voltage	ADJ(2)(3)	–0.3	45	V
Feedback input voltage for the tracker	FB(2)(3)	–1	45	V
Reference voltage minus the input voltage	ADJ – IN(5)		18	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND pin.
(3) Absolute maximum voltage.
(4) An internal diode is connected between the OUT and GND pins with 600-mA DC current capability for inductive clamp protection.
(5) The ADJ voltage cannot be 18 V higher than the IN voltage, otherwise the device can be damaged.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	NC pins	±2000	kV
			All pins except for NC pins	±4000	kV
		Charged device model (CDM), per AEC Q100-011		±1000	kV

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage(2)	4	40	V
V_{EN}	Enable input voltage	0	40	V
V_{ADJ}	Adjust and enable input voltage	1.5	18	V
V_{FB}	Feedback input voltage for the tracker	1.5	18	V
V_{OUT}	Output voltage	1.5	40	V
$C_{(OUT)}$	Output capacitor requirements(3)	10	500	µF
	Output ESR requirements(4)	0.001	20	Ω
T_J	Operating junction temperature range	–40	150	°C

(1) Within the functional range the device operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related *Electrical Characteristics* table.
(2) $V_{IN} > V_{ADJ} + V_{(DROPOUT)}$
(3) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%, when a resistor divider is connected between the OUT and FB pins (the output voltage is higher than reference voltage), a 47-nF feedforward capacitor is required to be connected between the OUT and FB pins for loop stability, and the ESR range of the output capacitor is required to be from 0.001 to 10 Ω.
(4) Relevant ESR value at f = 10 kHz

6.4 Thermal Information

THERMAL METRIC[1]		TPS7B4253-Q1		UNIT
		DDA (SO PowerPAD)	PWP (HTSSOP)	
		8 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.4	45.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.1	29.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.0	24.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.9	24.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.4	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 13.5 V, V_{ADJ} ≥ 1.5 V for HTSSOP, V_{ADJ} ≥ 2 V for SO PowerPAD, V_{EN} ≥ 2 V, T_J = –40ºC to 150ºC unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(UVLO)}$	IN undervoltage detection	V_{IN} rising			3.65	V
		V_{IN} falling			2.8	V
ΔVO	Output voltage tracking accuracy[1]	I_{OUT} = 100 µA to 300 mA, V_{IN} = 4 to 40 V V_{ADJ} < V_{IN} – 1 V 1.5 V < V_{ADJ} < 18 V for HTSSOP 2 V < V_{ADJ} < 18 V for SO PowerPAD	–4		4	mV
$\Delta V_{O(\Delta IO)}$	Load regulation steady-state	I_{OUT} = 0.1 to 300 mA, V_{ADJ}= 5 V			4	mV
$\Delta V_{O(\Delta VI)}$	Line regulation steady-state	I_{OUT}= 10 mA, V_{IN} = 6 to 40 V, V_{ADJ} = 5 V			4	mV
PSRR	Power supply ripple rejection	f_{rip} = 100 Hz, V_{rip} = 0.5 V_{PP}, $C_{(OUT)}$ = 10 µF, I_{OUT} = 100 mA		70		dB
$V_{(DROPOUT)}$	Dropout voltage ($V_{(DROPOUT)}$ = V_{IN} – V_{OUT})	I_{OUT} = 200 mA, V_{IN} = V_{ADJ} ≥ 4 V[2]		320	520	mV
$I_{O(lim)}$	Output current limitation	V_{ADJ} = 5 V, OUT short to GND	301	450	520	mA
$I_{R(IN)}$	Reverse current at IN	V_{IN} = 0 V, V_{OUT} = 40 V, V_{ADJ} = 5 V	–2		0	µA
$I_{R(–IN)}$	Reverse current at negative IN	V_{IN} = –40 V, V_{OUT} = 0 V, V_{ADJ} = 5 V	–10		0	µA
T_{SD}	Thermal shutdown temperature	T_J increases because of power dissipation generated by the IC		175		°C
T_{SD_hys}	Thermal shutdown hysteresis			15		°C
I_Q	Current consumption	4 V ≤ V_{IN} ≤ 40 V, V_{ADJ} = 0 V; V_{EN} = 0 V		2	4	µA
		4 V ≤ V_{IN} ≤ 40 V, V_{EN} ≥ 2 V, V_{ADJ} < 0.8 V		7	18	
		4 V ≤ V_{IN} ≤ 40 V, I_{OUT} < 100 µA, V_{ADJ} = 5 V		60	100	
		4 V ≤ V_{IN} ≤ 40 V, I_{OUT} < 300 mA, V_{ADJ} = 5V		350	400	
$I_{Q(DROPOUT)}$	Current consumption in dropout region	V_{IN} = V_{ADJ} = 5 V, I_{OUT} = 100 µA		70	140	µA
$I_{I(ADJ)}$	Adjust input current	HTSSOP package, V_{ADJ} = V_{FB} = 5 V			0.5	µA
		SO PowerPAD package, V_{ADJ} = V_{FB} = 5 V			5.5	
$V_{(ADJ\_LOW)}$	Adjust low signal valid	V_{OUT} = 0 V	0		0.8	V
$V_{(ADJ\_HIGH)}$	Adjust high signal valid	|V_{OUT} – V_{ADJ}| < 5 mV	1.5		18	V
$V_{(EN\_LOW)}$	Enable low signal valid	V_{OUT} = 0 V	0		0.7	V
$V_{(EN\_HIGH)}$	Enable high Signal Valid	OUT settled	2		40	V
I_{EN}	Enable pulldown current	2V < V_{EN} < 40 V			5	µA
I_{FB}	FB bias current	V_{ADJ} = V_{FB} = 5 V			0.5	µA

(1) The tracking accuracy is specified when the FB pin is directly connected to the OUT pin which means V_{ADJ} = V_{OUT}, external resistor divider variance is not included.
(2) Measured when the output voltage, V_{OUT} has dropped 10 mV from the nominal value.

6.6 Typical Characteristics

V_{IN} = 14 V, V_{ADJ} = 5 V, V_{FB} = V_{OUT}, unless otherwise specified

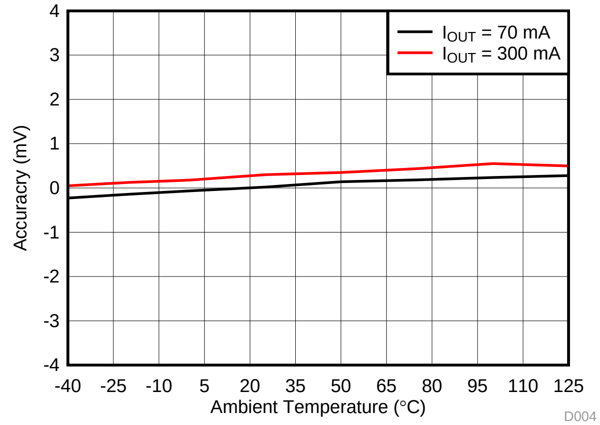


图 1. Tracking Accuracy vs Ambient Temperature

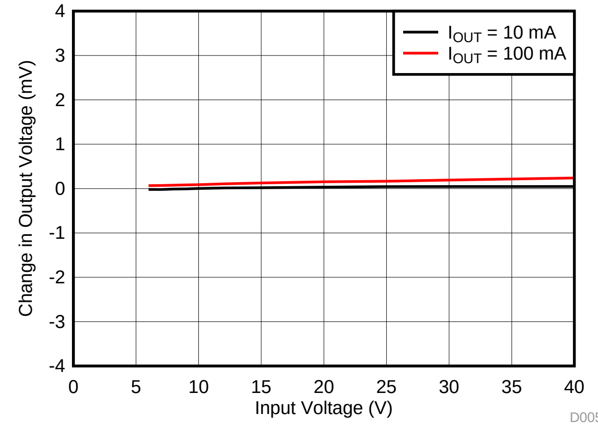


图 2. Line Regulation

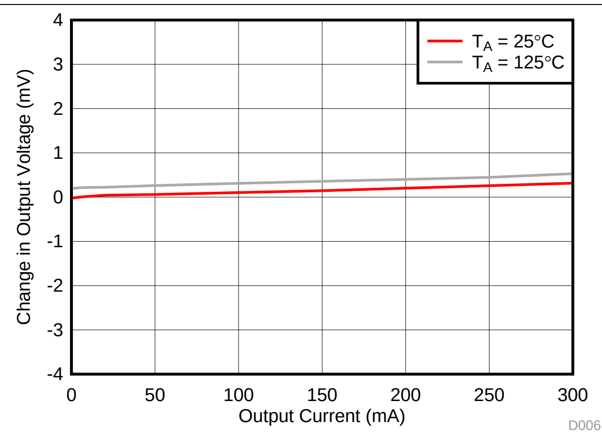
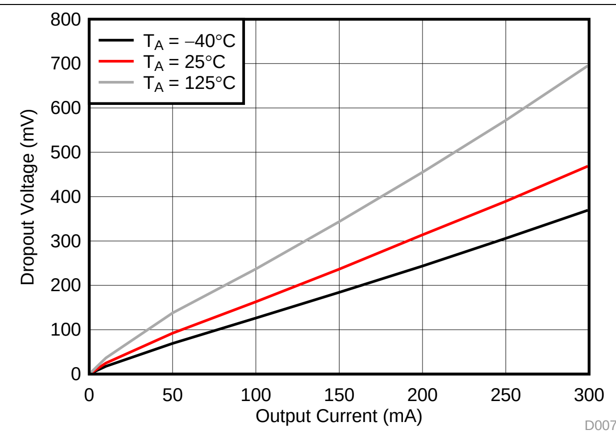
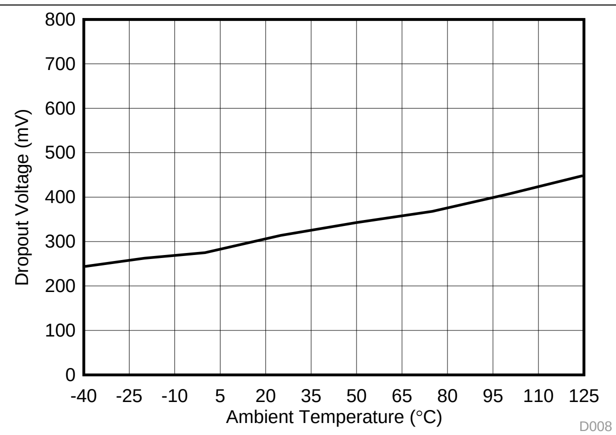


图 3. Load Regulation



V_{IN} = V_{ADJ} = 4 V

图 4. Dropout Voltage vs Output Current



V_{IN} = V_{ADJ} = 4 V I_{OUT} = 200 mA

图 5. Dropout Voltage vs Ambient Temperature

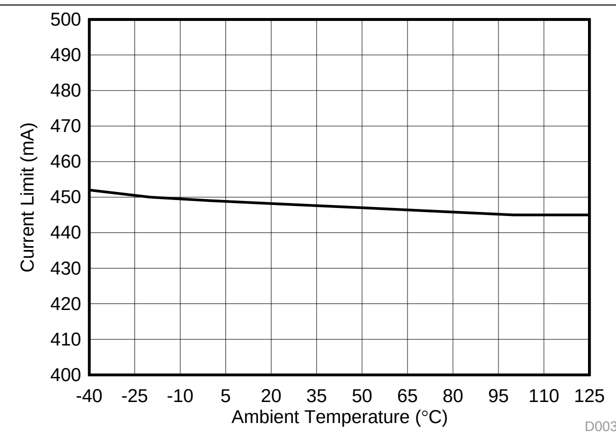


图 6. Current Limit ($I_{O(lim)}$) vs Ambient Temperature

Typical Characteristics (接下页)

V_{IN} = 14 V, V_{ADJ} = 5 V, V_{FB} = V_{OUT}, unless otherwise specified

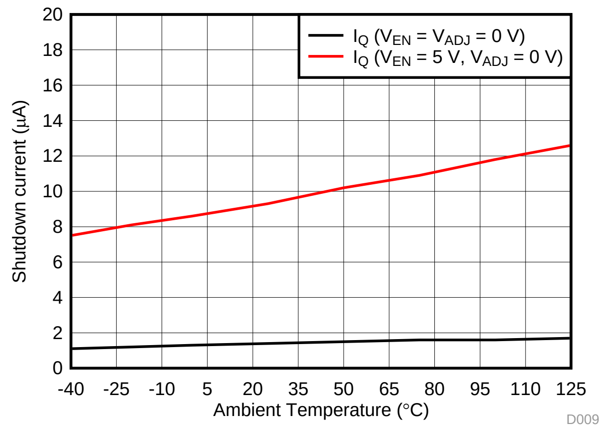


图 7. Shutdown Current vs Ambient Temperature

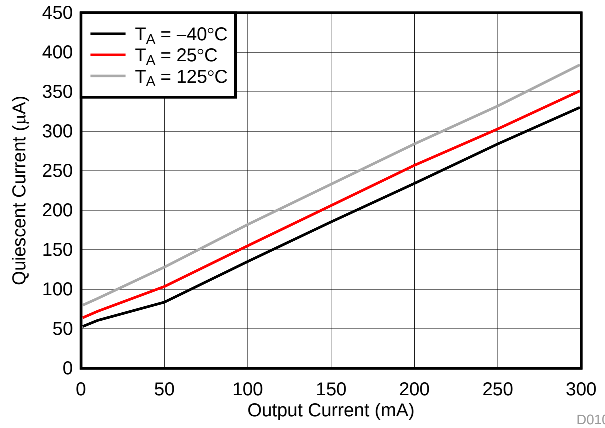


图 8. Quiescent Current vs Output Current

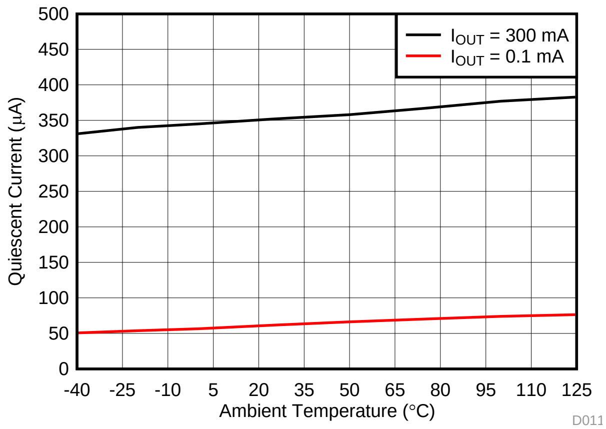
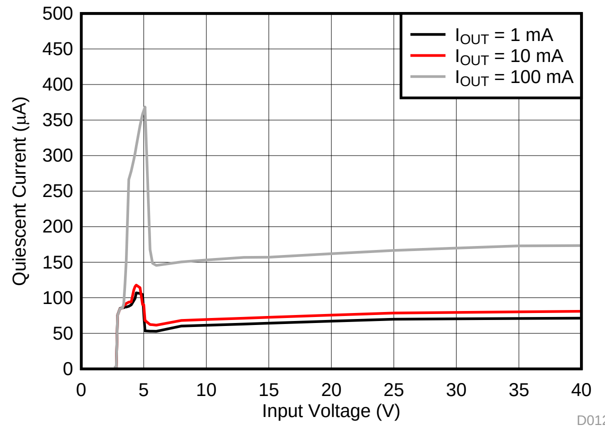
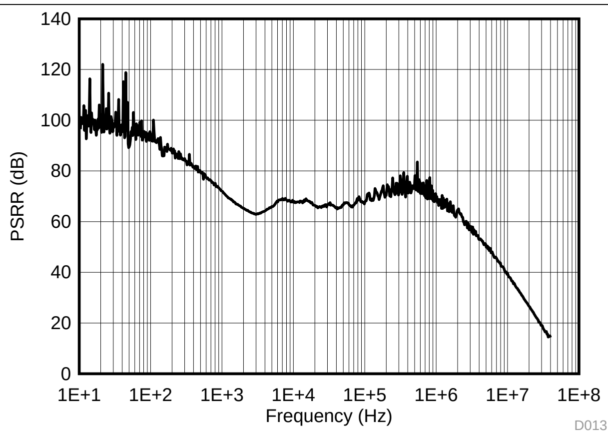


图 9. Quiescent Current vs Ambient Temperature



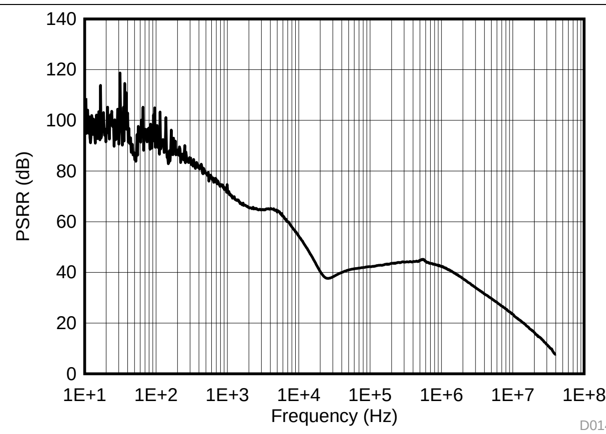
V_{ADJ} = V_{EN} = 5 V

图 10. Quiescent Current vs Input Voltage



$C_{(OUT)}$ = 10 µF I_{OUT} = 1 mA T_A = 25°C

图 11. PSRR

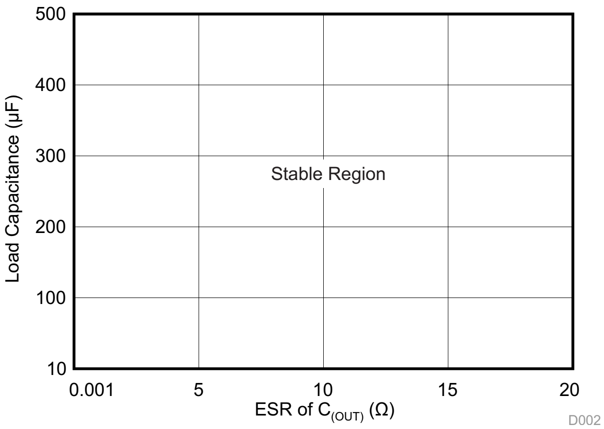


$C_{(OUT)}$ = 10 µF I_{OUT} = 100 mA T_A = 25°C

图 12. PSRR

Typical Characteristics (接下页)

V_{IN} = 14 V, V_{ADJ} = 5 V, V_{FB} = V_{OUT}, unless otherwise specified



V_{FB} = V_{OUT}

图 13. ESR Stability vs Load Capacitance

V_{FB} < V_{OUT}

图 14. ESR Stability vs Load Capacitance

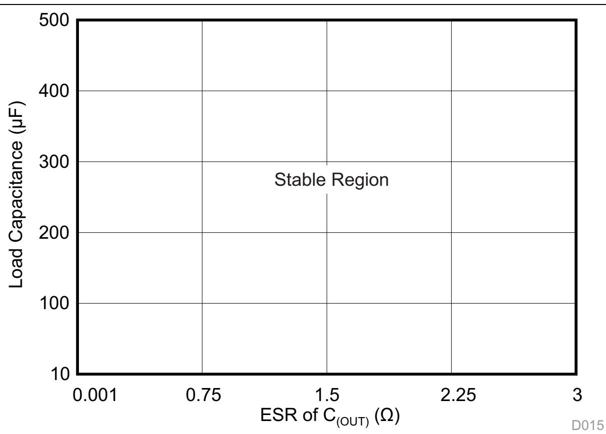
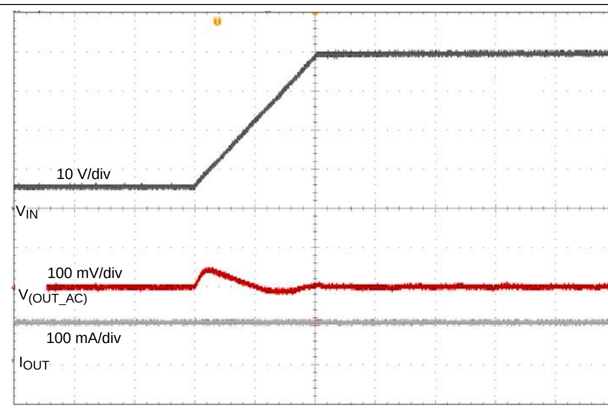
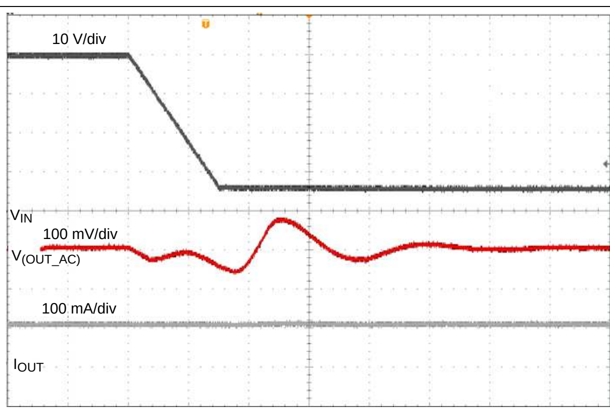


图 15. ESR Stability vs Load Capacitance (Multiple Output Capacitors)



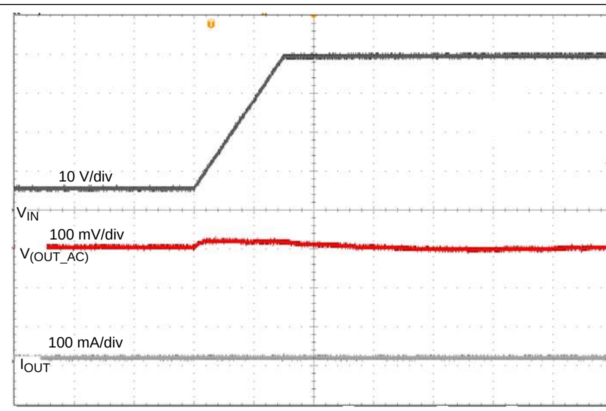
V_{IN} = 6 to 40 V V_{ADJ} = 5 V $C_{(OUT)}$ = 10 µF
I_{OUT} = 100 mA, 20 µs/div

图 16. 6- to 40-V Line Transient



V_{IN} = 40 to 6 V V_{ADJ} = 5 V $C_{(OUT)}$ = 10 µF
I_{OUT} = 100 mA, 20 µs/div

图 17. 40- to 6-V Line Transient

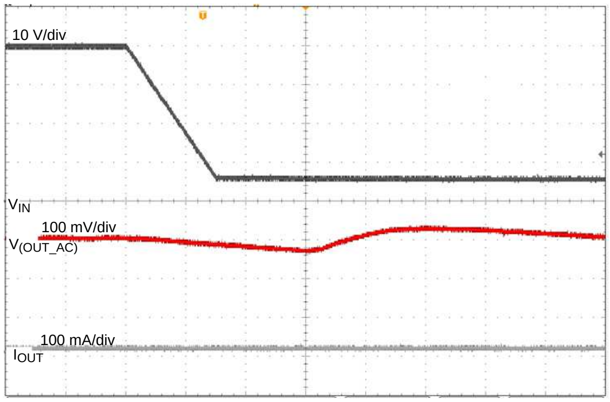


V_{IN} = 6 to 40 V V_{ADJ} = 5 V $C_{(OUT)}$ = 10 µF
I_{OUT} = 10 mA, 20 µs/div

图 18. 6- to 40-V Line Transient

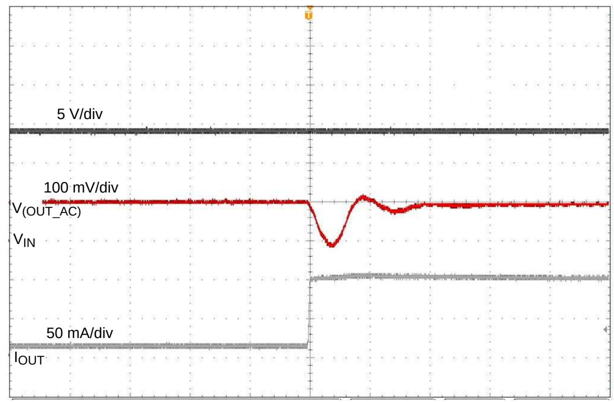
Typical Characteristics (接下页)

V_{IN} = 14 V, V_{ADJ} = 5 V, V_{FB} = V_{OUT}, unless otherwise specified



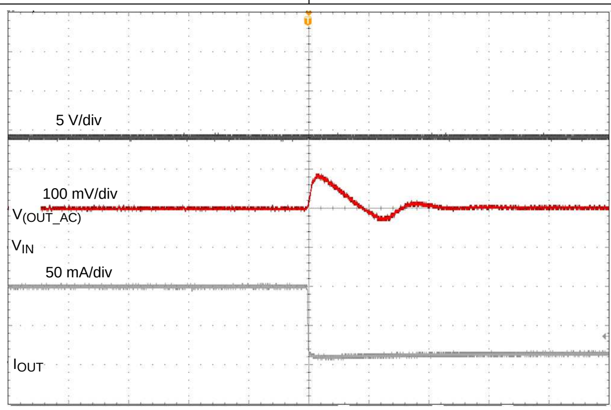
V_{IN} = 40 to 6 V V_{ADJ} = 5 V $C_{(OUT)}$ = 10 µF
I_{OUT} = 10 mA, 20 µs/div

图 19. 40- to 6-V Line Transient



V_{IN} = 14 V V_{ADJ} = 5 V $C_{(OUT)}$ = 10 µF
I_{OUT} = 10 to 100 mA, 40 µs/div

图 20. 10- to 100-mA Load Transient



V_{IN} = 14 V V_{ADJ} = 5 V $C_{(OUT)}$ = 10 µF
I_{OUT} = 100 to 10 mA, 40 µs/div

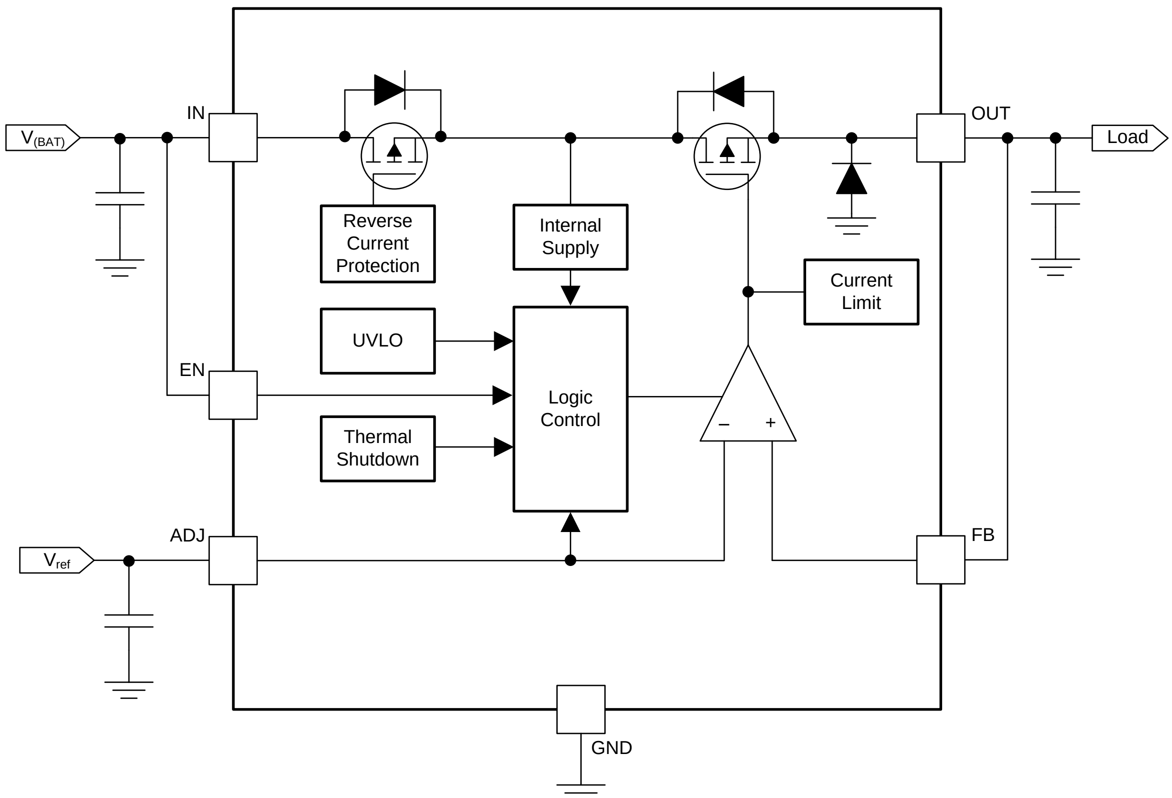
图 21. 100- to 10-mA Load Transient

7 Detailed Description

7.1 Overview

The TPS7B4253-Q1 device is a monolithic integrated low-dropout voltage tracker with an ultralow tracking tolerance. Key protection circuits are integrated in the device, including output current limitation, reverse polarity protection, inductive load clamp, output short-to-battery protection, and thermal shutdown in case of an overtemperature event.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Short Circuit and Overcurrent Protection

The TPS7B4253-Q1 device features integrated fault protection which makes the device ideal for automotive applications. To keep the device in a safe area of operation during certain fault conditions, internal current-limit protection is used to limit the maximum output current. This protection protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, the current through the pass element is limited to $I_{O(lim)}$ to protect the device from excessive power dissipation.

7.3.2 Integrated Inductive Clamp Protection

During output turnoff, the cable inductance continues to source the current from the output of the device. The device integrates an inductive clamp at the OUT pin to help to dissipate the inductive energy stored in the cable. An internal diode is connected between the OUT and GND pins with a DC-current capability of 600 mA for inductive clamp protection.

Feature Description (接下页)

7.3.3 OUT Short to Battery and Reverse Polarity Protection

The TPS7B4253-Q1 device can withstand a short to battery when the output is shorted to the battery, as shown in 图 22. Therefore, no damage to the device occurs.

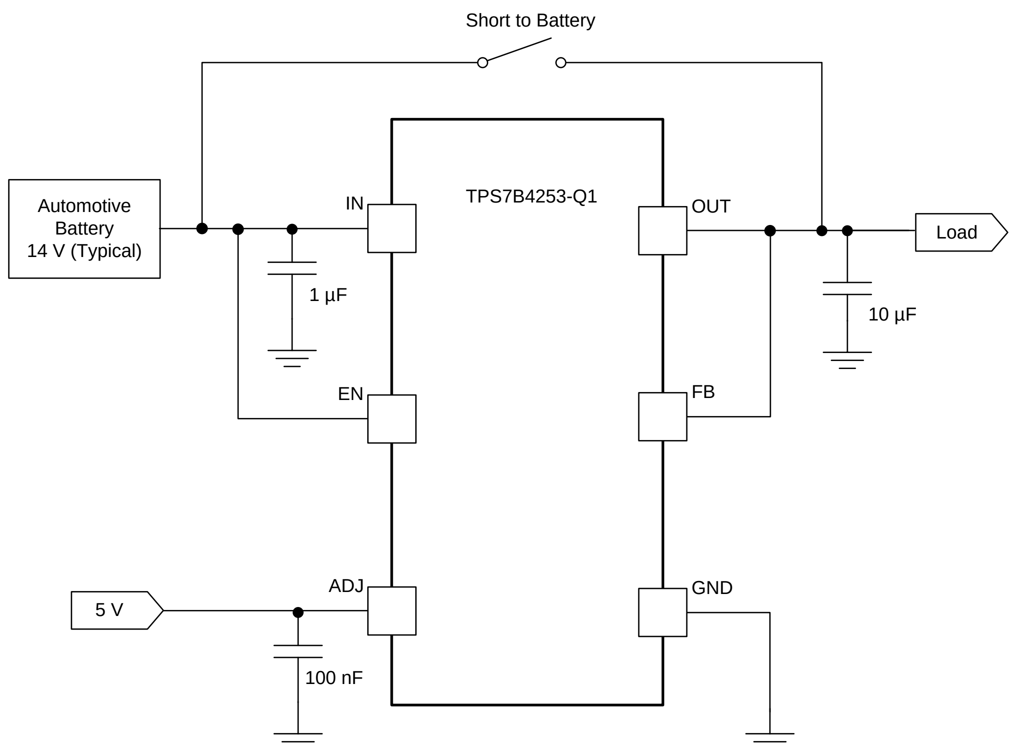


图 22. OUT Short to Battery, $V_{IN} = V_{(BAT)}$

A short to the battery can also occur when the device is powered by an isolated supply at lower voltage, as shown in 图 23. In this case, the TPS7B4253-Q1 supply-input voltage is set to 7 V when a short to battery (14 V typical) occurs on the OUT pin which operates at 5 V. The internal back-to-back PMOS remains on for 1 ms during which the input voltage of the TPS7B4253-Q1 device charges up to the battery voltage. A diode connected between the output of the DC-DC converter and the input of the TPS7B4253-Q1 device is required in case the other loads connected behind the DC-DC converter cannot withstand the voltage of an automotive battery. To achieve a lower dropout voltage, TI recommends using a Schottky diode. This diode can be eliminated if the output of the DC-DC converter and the loads connect behind it withstand automotive battery voltage.

The internal back-to-back PMOS is switched to OFF when reverse polarity or short to battery occur for 1 ms. After that, the reverse current flows out through the IN pin with less than 10 µA. In the meanwhile, a special ESD structure implemented at the input ensures the device can withstand –40 V.

Feature Description (接下页)

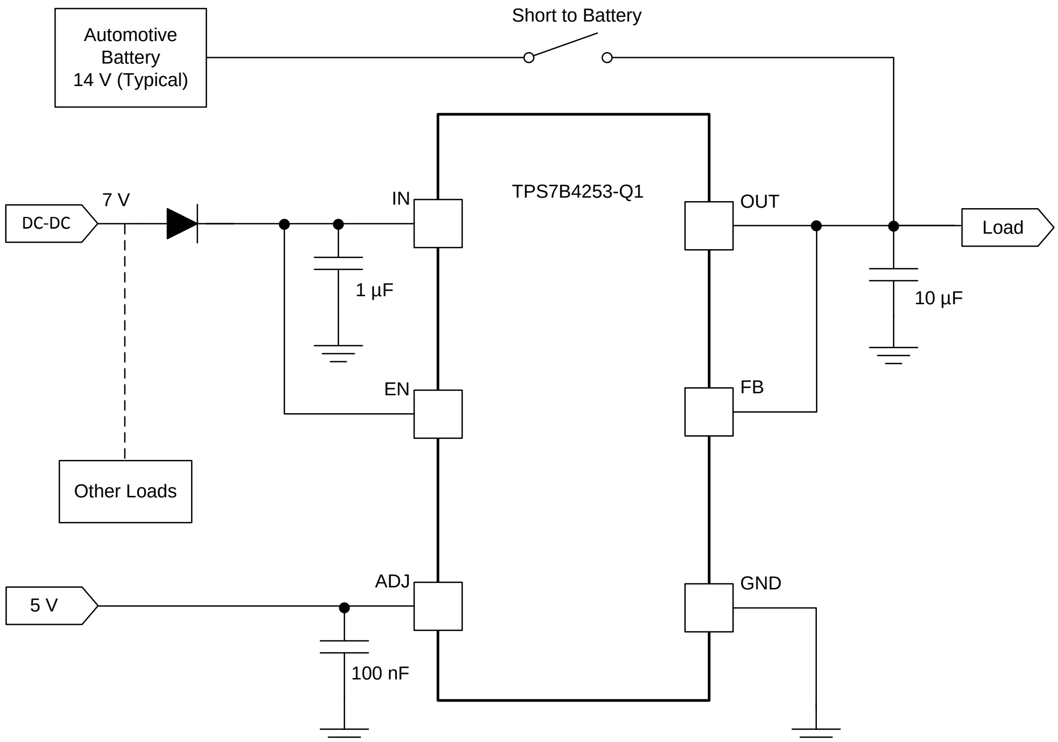


图 23. OUT Short to Battery, $V_{IN} < V_{(BAT)}$

In most cases, the output of the TPS7B4253-Q1 device is shorted to the battery through an automotive cable. The parasitic inductance on the cable results in LC oscillation at the output of the TPS7B4253-Q1 device when the short to battery occurs. Ideally, the peak voltage at the output of the TPS7B4253-Q1 device should be lower than the absolute-maximum voltage rating (45 V) during LC oscillation.

7.3.4 Undervoltage Shutdown

The device has an internally fixed undervoltage-shutdown threshold. Undervoltage shutdown activates when the input voltage on IN drops below UVLO. This activation ensures the regulator is not latched into an unknown state during a low input-supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down and then powers up with a standard power-up sequence when the input voltage is above the required levels.

7.3.5 Thermal Protection

The device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. During continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature decreases to 15°C (typical) lower than the TSD trip point, the output turns on.

注

The purpose of the design of the internal protection circuitry of the TPS7B4253-Q1 device is to protect against overload conditions and is not intended as a replacement for proper heat-sinking. Continuously running the device into thermal shutdown degrades device reliability.

Feature Description (接下页)

7.3.6 Regulated Output (OUT)

The OUT pin is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has an incorporated soft-start feature to control the initial current through the pass element.

7.3.7 Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input on the EN pin acitvates the device and turns on the regulator. The device consumes a maximum of shutdown current 4 µA when the EN pin is low. The EN pin has a maximum internal pulldown of 5 µA.

7.3.8 Adjustable Output Voltage (FB and ADJ)

7.3.8.1 OUT Voltage Equal to the Reference Voltage

With the reference voltage applied directly at the ADJ pin and the FB pin connected to the OUT pin, the voltage at the OUT pin equals to the reference voltage at the ADJ pin, as shown in 图 24.

$$V_{OUT} = V_{ADJ} \tag{1}$$

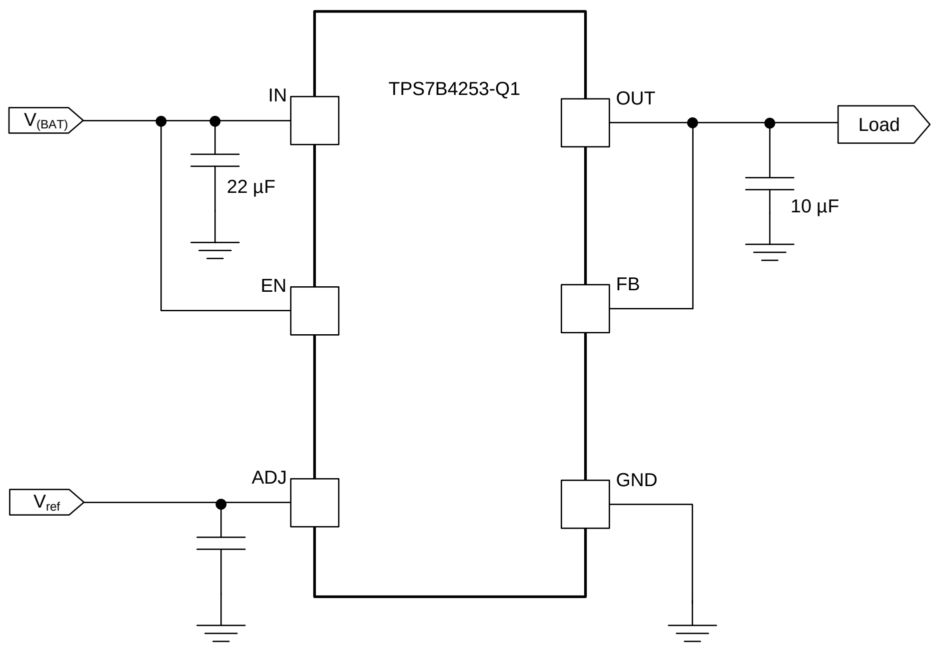


图 24. OUT Voltage Equal to the Reference Voltage

7.3.8.2 OUT Voltage Higher Than Reference Voltage

By using an external resistor divider connected between the OUT and FB pins, an output voltage higher than reference voltage can be generated as shown in 图 25. Use 公式 2 to calculate the value of the output voltage. The recommended range for R1 and R2 is from 10 kΩ to 100 kΩ.

$$V_{OUT} = \frac{V_{ADJ} \times (R1 + R2)}{R2} \tag{2}$$

Feature Description (接下页)

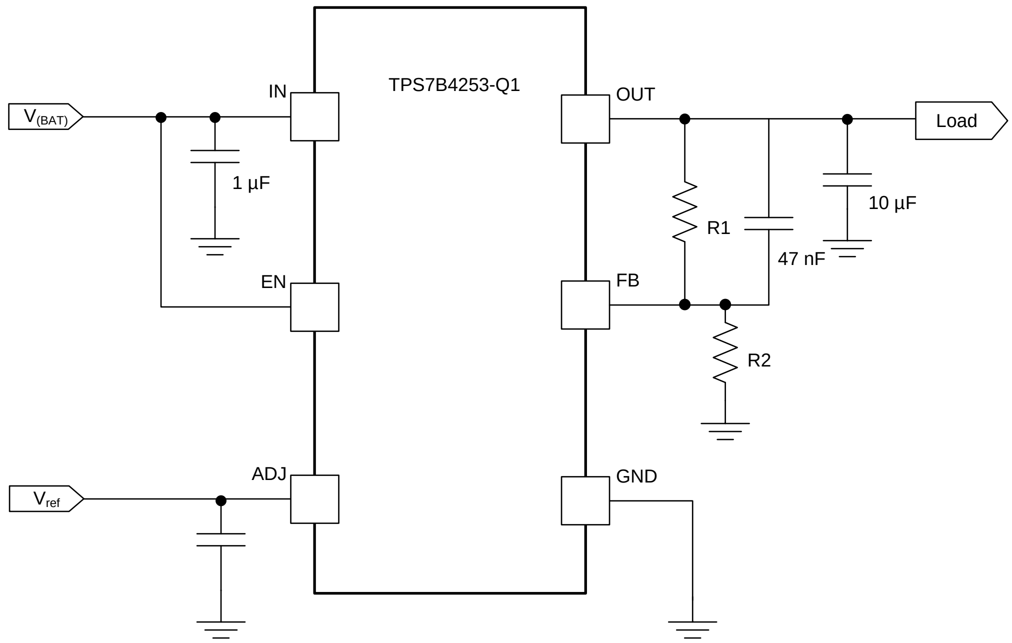


图 25. OUT Voltage Higher Than the Reference Voltage

7.3.8.3 Output Voltage Lower Than Reference Voltage

By using an external resistor divider connected at the ADJ pin, an output voltage lower than reference voltage can be generated as shown in 图 26. Use 公式 3 to calculate the output voltage. The recommended value for both R1 and R2 is less than 100 kΩ.

$$V_{OUT} = \frac{V_{ref} \times R2}{R1 + R2} \quad (3)$$

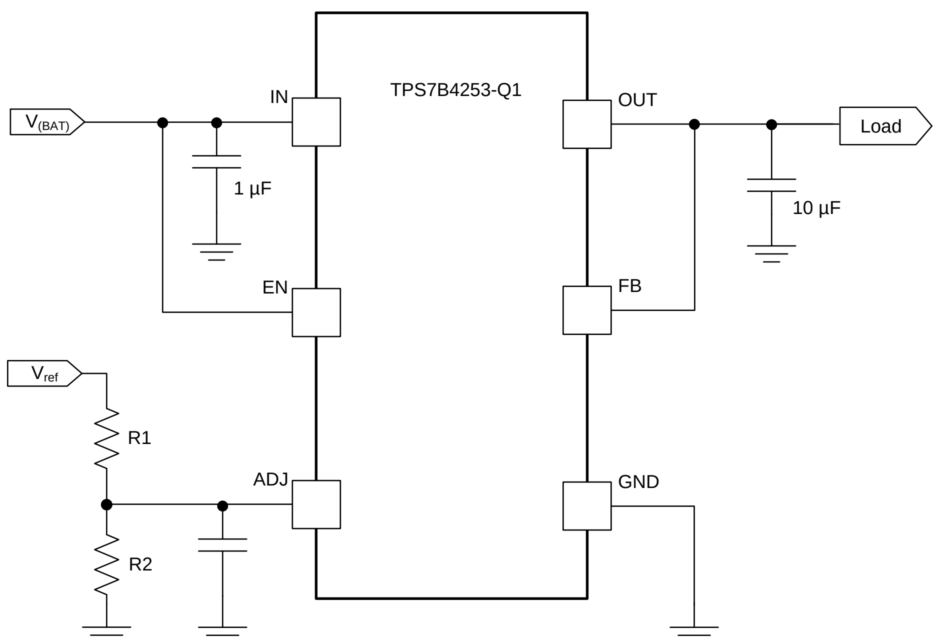


图 26. OUT Voltage Lower Than the Reference Voltage

7.4 Device Functional Modes

7.4.1 Operation With V_{IN} < 4 V

The maximum UVLO voltage is 3.65 V, and the device generally operates at an input voltage above 4 V. The device can also operate at a lower input voltage; no minimum UVLO voltage is specified. At an input voltage below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With EN Control

The enable rising edge threshold is 2 V (maximum). With the EN pin held above that voltage and the input voltage above 4 V, the device becomes active. The falling edge of the EN pin is 0.7 V (minimum). Holding the EN pin below that voltage disables the device, thus reducing the quiescent current of the device.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B4253-Q1 device is a 300-mA low-dropout tracking regulator with ultralow tracking tolerance. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Application

8.2.1 Application With Output Voltage Equal to the Reference Voltage

图 27 shows the typical application circuit for the TPS7B4253-Q1 device. Different values of external components can be used depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

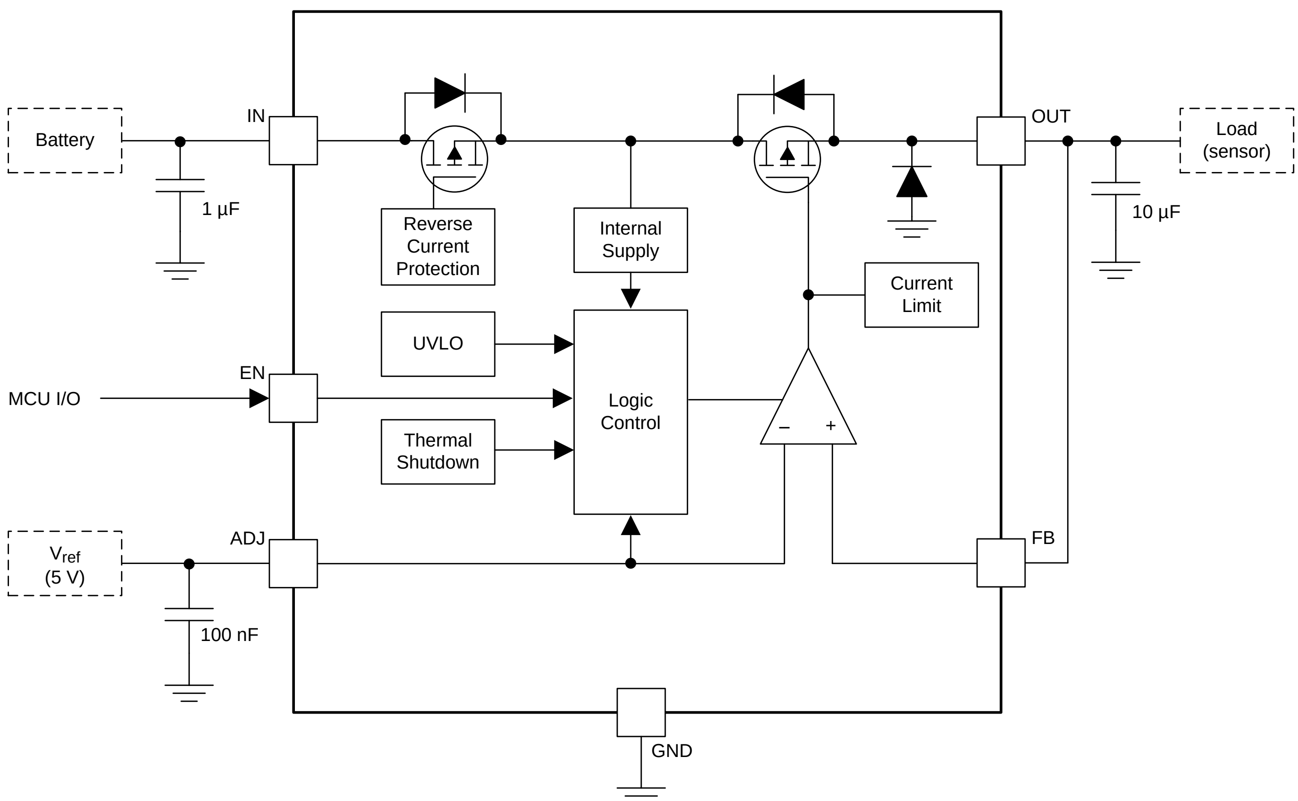


图 27. Output Voltage Equals the Reference Voltage

Typical Application（接下页）

8.2.1.1 Design Requirements

For this design example, use the parameters listed in 表 1 as the design parameters.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	4 to 40 V
Output voltage	1.5 to 40 V
Enable voltage	2 to 40 V
ADJ voltage	1.5 to 18 V
Output capacitor	10 to 500 µF
Output capacitor ESR range	0.001 to 20 Ω

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Reference voltage
- Output current
- Current limit

8.2.1.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 2.2 µF. The voltage rating must be greater than the maximum input voltage.

8.2.1.2.2 Output Capacitor

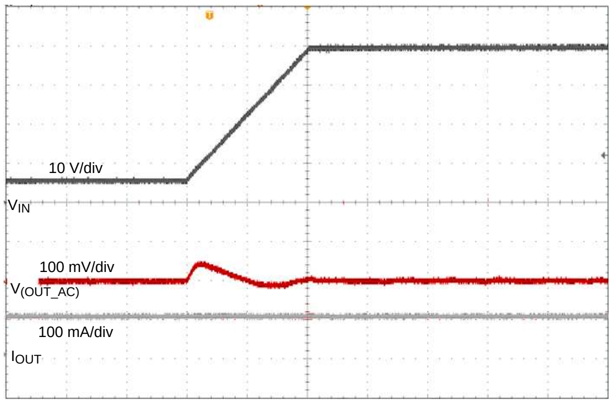
To ensure the stability of the TPS7B4253-Q1 device, the device requires an output capacitor with a value in the range from 10 µF to 500 µF and with an ESR range from 0.001 Ω to 20 Ω when the FB pin is directly connected to the OUT pin. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

To achieve an output voltage higher than the reference voltage, a resistor divider is connected between the OUT pin and the FB pin. In this case, a 47-nF feed forward capacitor must be connected between the OUT and FB pins for loop stability. The ESR of the output capacitor must be from 0.001 Ω to 10 Ω.

When multiple capacitors (two or more) are connected in parallel at the OUT pin, the ESR range of each output capacitor must be from 0.001 Ω to 3 Ω for loop stability.

In case the FB pin is shorted to ground, the TPS7B4253-Q1 device functions as a power switch with no need for the output capacitor.

8.2.1.3 Application Curves



V_{IN} = 6 to 40 V V_{ADJ} = 5 V $C_{(OUT)}$ = 10 µF

I_{OUT} = 100 mA, 20 µs/div

图 28. 6- to 40-V Line Transient

8.2.2 High-Side Switch Configuration

As shown in 图 29, by connecting the FB pin to the GND pin, the TPS7B4253-Q1 device can be used as a high-side switch with current-limit, thermal shutdown, output short-to-battery, and reverse polarity protection. The switching on and off of the device is then controlled through the EN and ADJ pins.

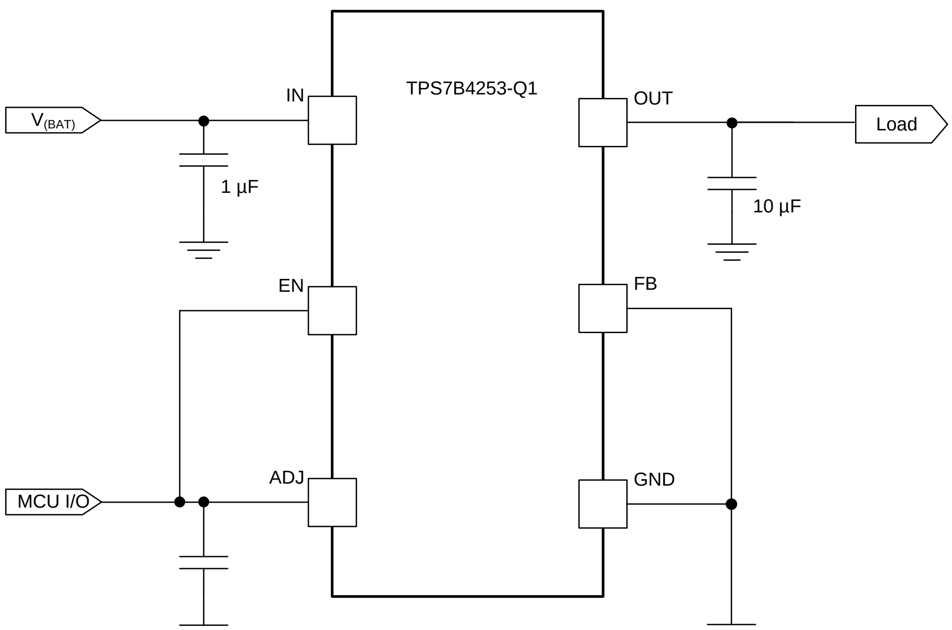


图 29. High-Side Switch Application

8.2.3 High Accuracy LDO

With an accurate voltage rail, the TPS7B4253-Q1 device can be used as an LDO with ultrahigh-accuracy output voltage by configuring the device as shown in 图 30.

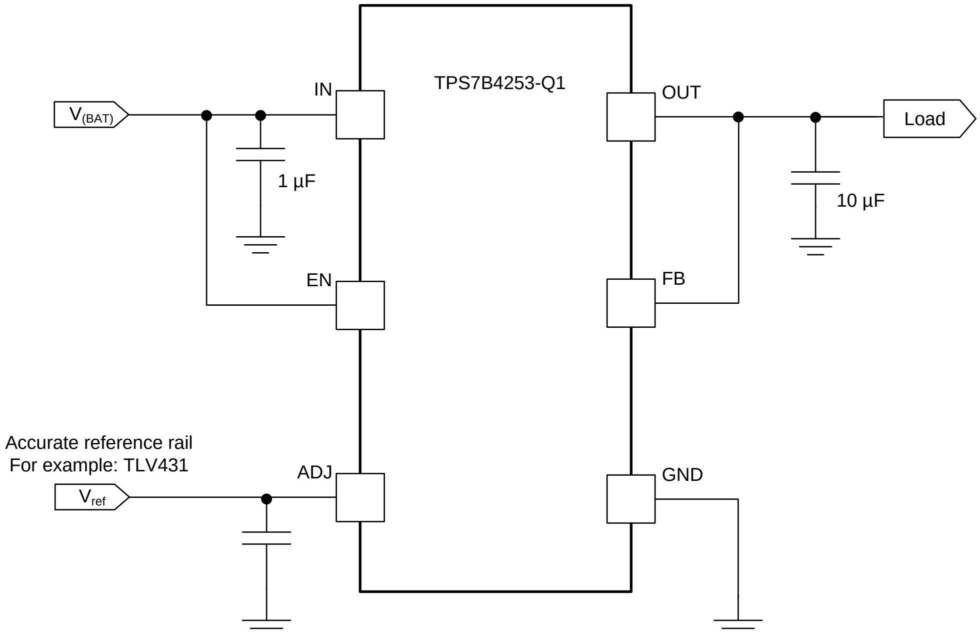


图 30. High-Accuracy LDO Application

For example, assume the reference voltage is a 5-V rail with 0.5% accuracy. Because the tracking accuracy between the ADJ and OUT pins is specified below 4 mV across temperature, the output accuracy of the TPS7B4253-Q1 device can be calculated with 公式 4.

$$\text{Accuracy of } V_{OUT} = \frac{V_{ADJ} \times 0.5\% + 4\text{ mV}}{V_{ADJ}} \times 100\% = \frac{5 \times 0.5\% + 0.004}{5} \times 100\% = 0.58\% \quad (4)$$

9 Power Supply Recommendations

The device is designed to operate with an input voltage supply from 4 V to 40 V. This input supply must be well regulated. If the input supply is more than a few inches away from the TPS7B4253-Q1 device, TI recommends adding an electrolytic capacitor with a value of 2.2 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For the layout of the TPS7B4253-Q1 device, place the input and output capacitors close to the devices as shown in the *Functional Block Diagram*. To enhance the thermal performance, TI recommends surrounding the device with some vias.

Minimize equivalent series inductance (ESL) and ESR to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces for the path between the output capacitor and the OUT pins because vias can negatively impact system performance and even cause instability.

If possible, and to ensure the maximum performance specified in this data sheet, use the same layout pattern used for the TPS7B4253-Q1 evaluation board, TPS7B4253EVM, which is available at www.ti.com/tool/TPS7B4253EVM.

10.2 Layout Example

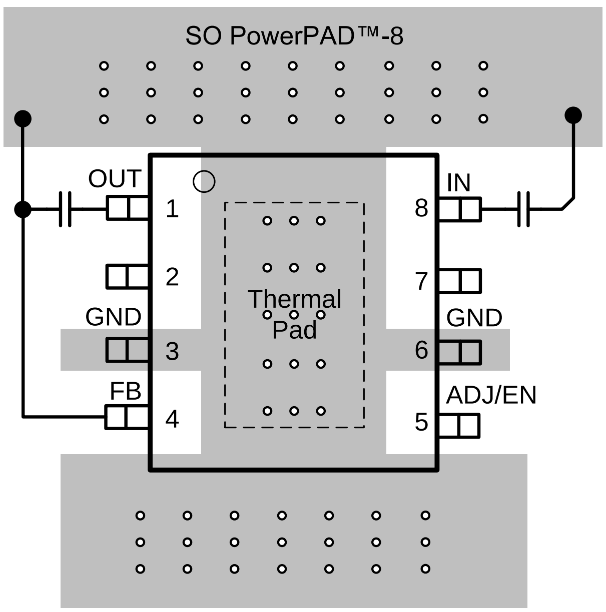


图 31. SO PowerPAD Package TPS7B4253-Q1 Layout Example

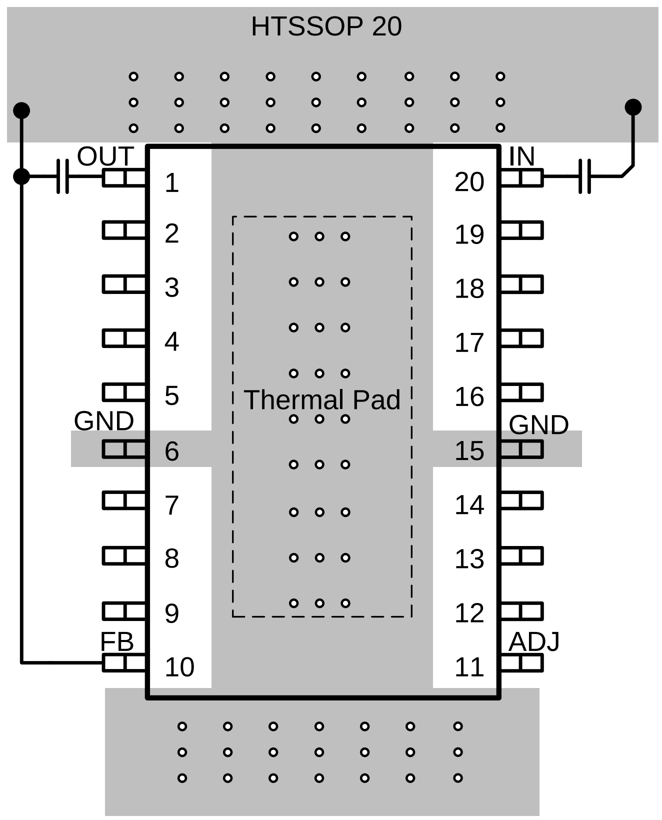


图 32. HTSSOP Package TPS7B4253-Q1 Layout Example

10.3 Power Dissipation and Thermal Considerations

Use 公式 5 to calculate the device power dissipation.

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I$$

where

- P_D = continuous power dissipation
- I_O = output current
- V_I = input voltage
- V_O = output voltage
- I_Q = quiescent current (5)

As $I_Q \ll I_O$, the term $I_Q \times V_I$ in 公式 5 can be ignored.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) with 公式 6.

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where

- θ_{JA} = junction-to-junction-ambient air thermal impedance (6)

A rise in junction temperature because of power dissipation can be calculated with 公式 7.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D) \quad (7)$$

For a given maximum junction temperature ($T_J$max), the maximum ambient air temperature ($T_A$max) at which the device can operate can be calculated with 公式 8.

$$T_A \max = T_J \max - (\theta_{JA} \times P_D) \quad (8)$$

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

如需 TPS7B4253 PSpice 瞬态模型，请访问 www.ti.com.cn/product/cn/TPS7B4253-Q1/toolssoftware。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

《*TPS7B4253-Q1 评估模块*》，SLVUAE3

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B4253QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	4253	Samples
TPS7B4253QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B4253Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

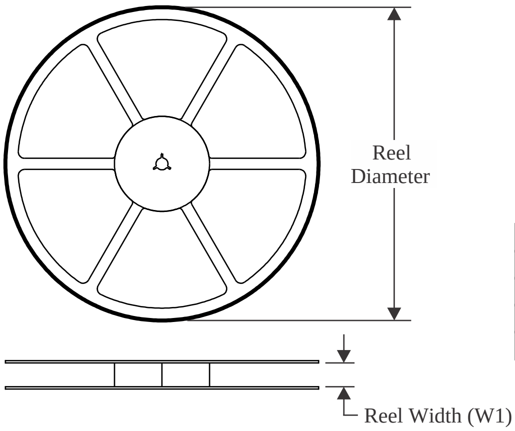
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

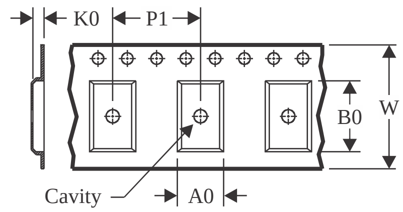
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

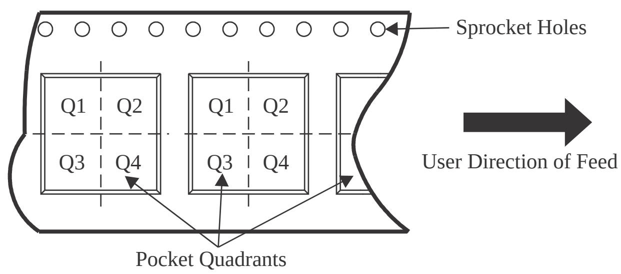


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

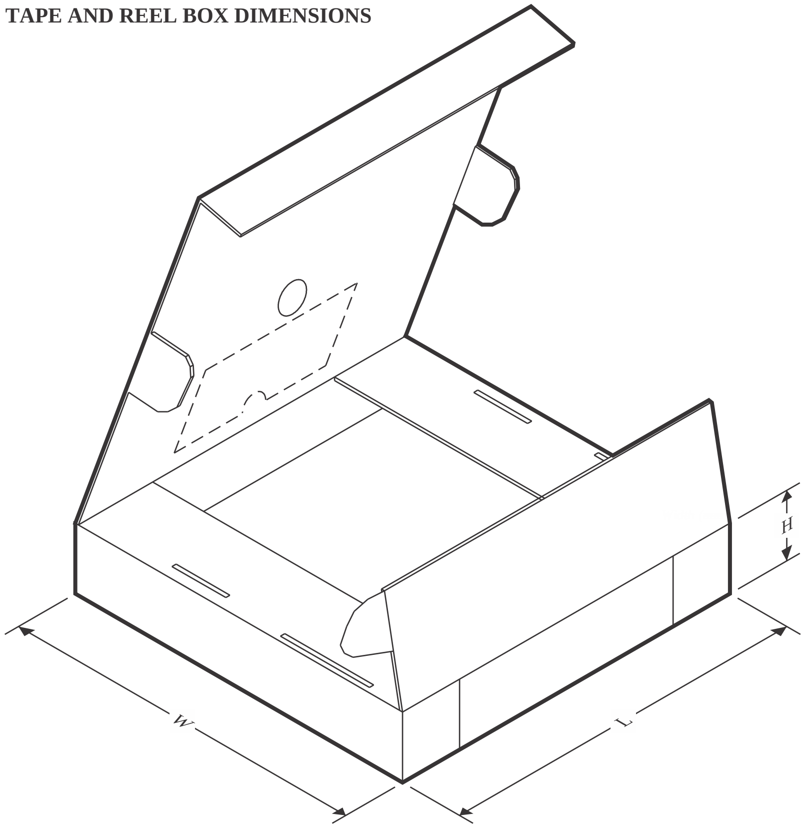
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B4253QDDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS7B4253QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

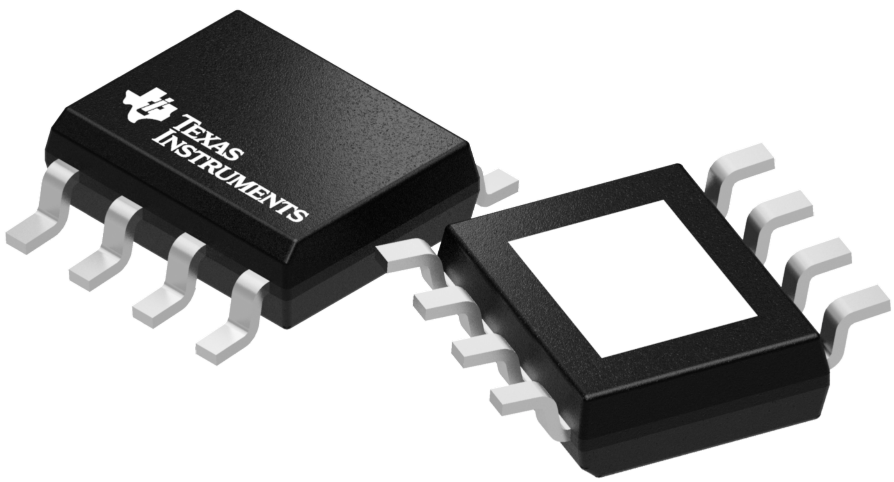


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B4253QDDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS7B4253QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

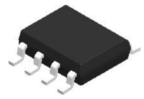
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

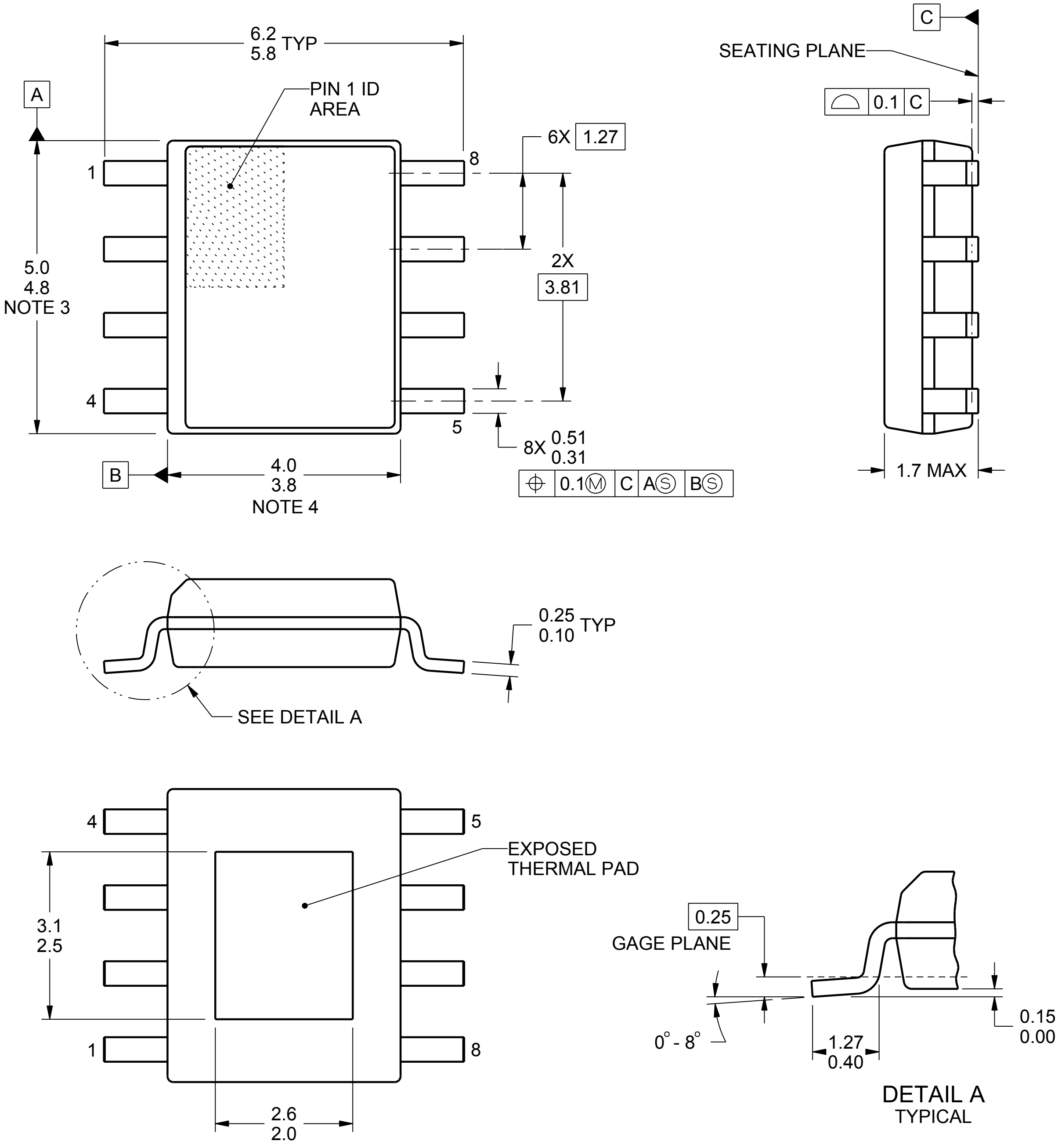
PACKAGE OUTLINE



DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE

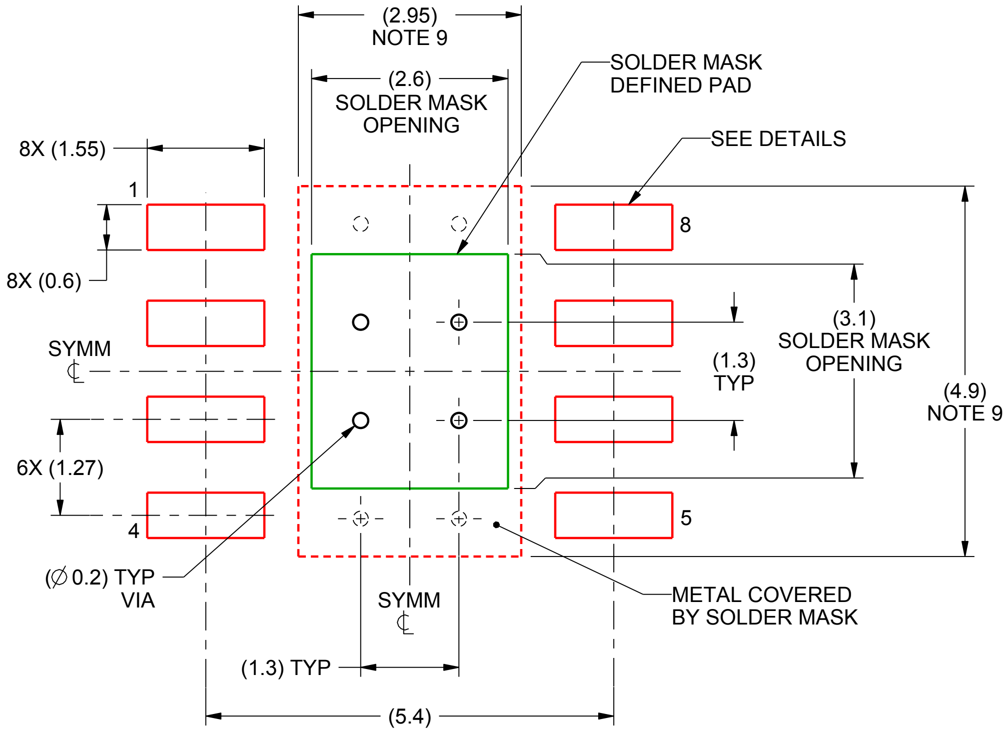


4221637/B 03/2016

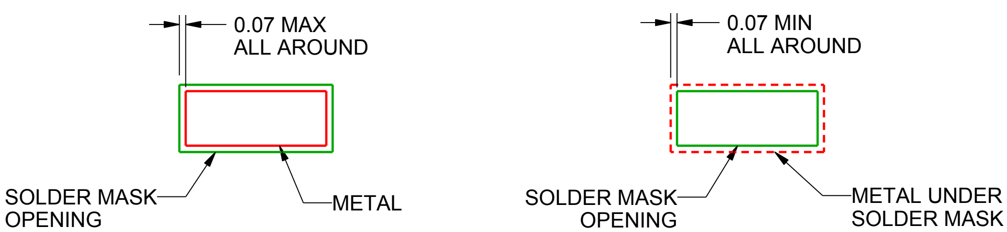
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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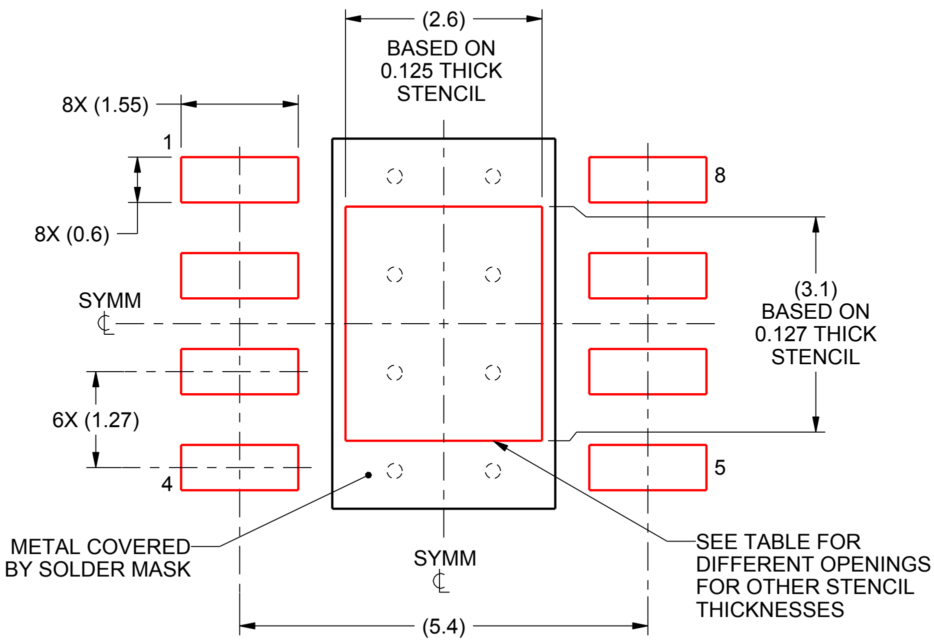
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

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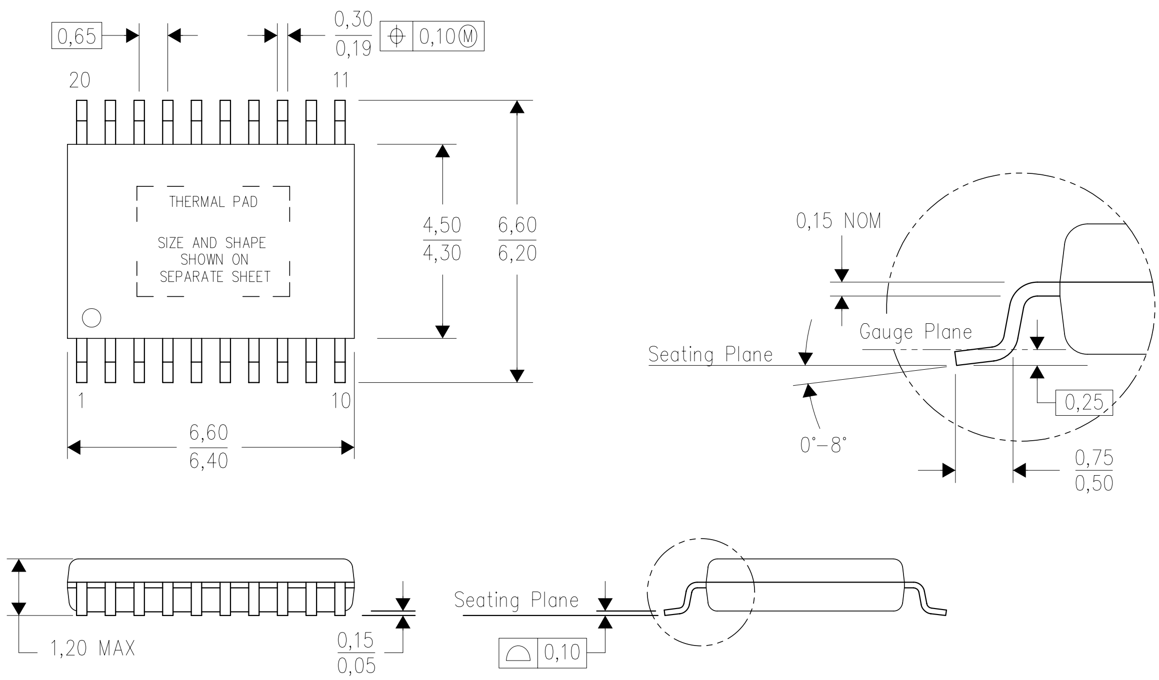
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO-153

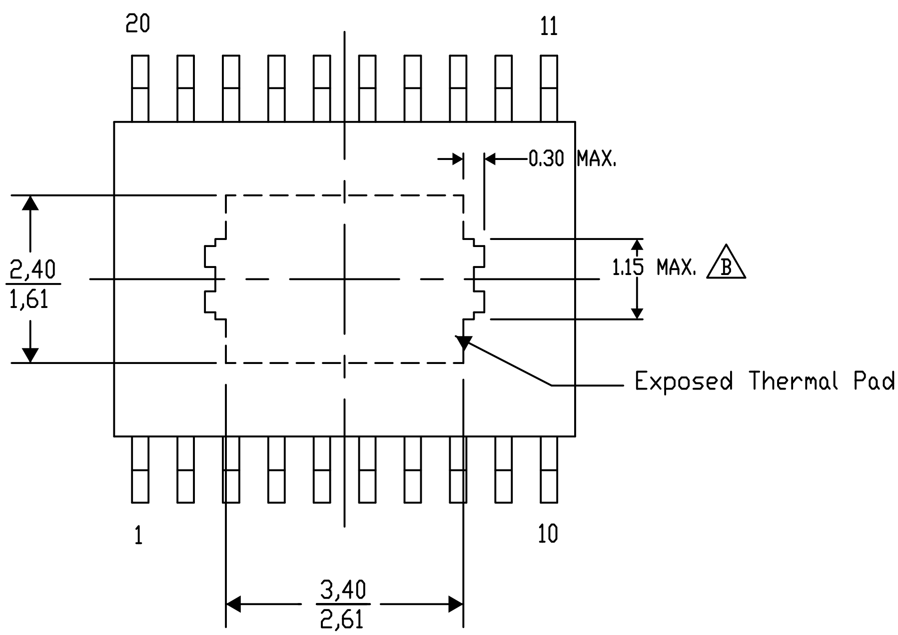
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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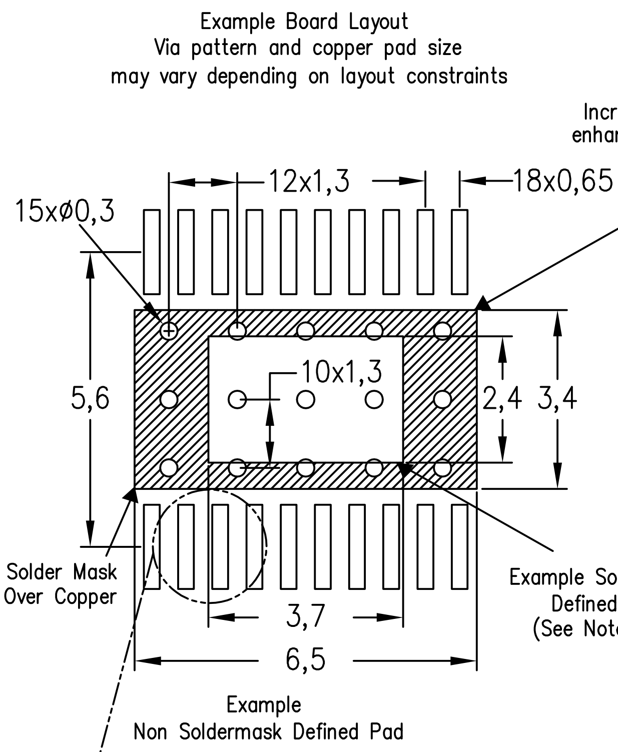
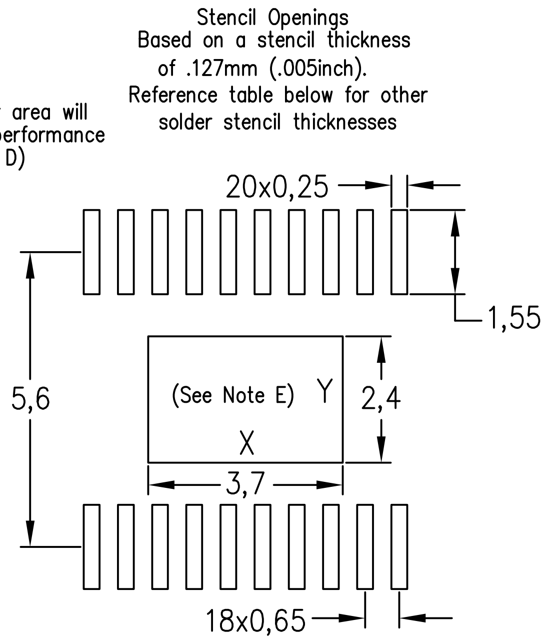
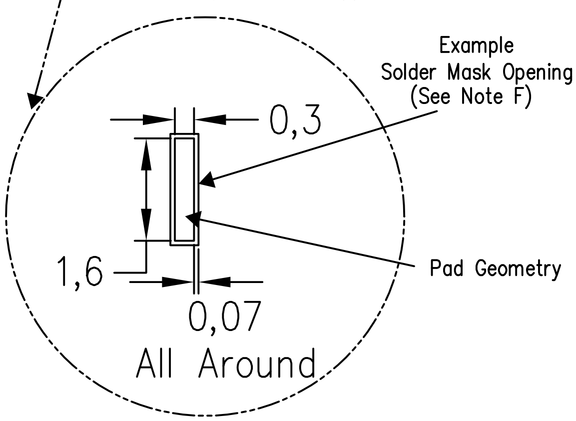
PWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE







Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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