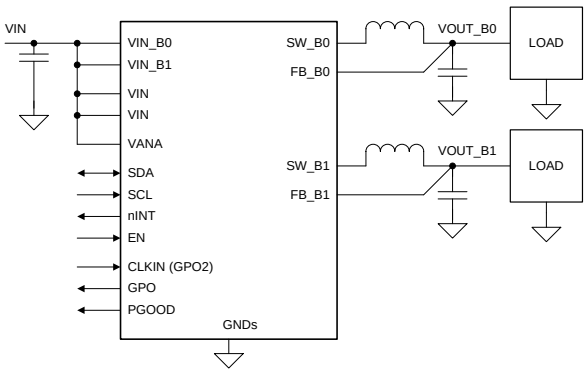
TPS65653-Q1 双路 3A 降压转换器

1 特性

- 下列性能符合 AEC-Q100 标准：
  - 器件温度 1 级：-40°C 至 +125°C 的环境工作温度范围
- 输入电压：2.8V 至 5.5V
- 两个高效降压直流/直流转换器：
  - 输出电压：1V 至 3.36V
  - 最大输出电流为每相 3A
  - 可编程输出电压压摆率范围：0.5mV/µs 至 10mV/µs
  - 4MHz 开关频率
  - 用于降低 EMI 的扩频模式和相位交错
- 可配置通用输出信号（GPO、GPO2）
- I^2C 兼容接口，支持标准 (100kHz)、快速 (400kHz)、快速+ (1MHz) 和高速 (3.4MHz) 模式
- 具有可编程屏蔽的中断功能
- 可编程电源正常信号 (PGOOD)
- 外部时钟输入以同步开关
- 输出短路和过载保护
- 过热警告和保护
- 过压保护 (OVP) 和欠压锁定 (UVLO)
- 具有可湿性侧面的 28 引脚、5mm × 5mm VQFN 封装

简化原理图



2 应用

- 雷达系统 ECU
- 汽车音响主机和仪表组
- 汽车摄像头模块
- 环视系统 ECU
- 汽车显示屏

3 说明

TPS65653-Q1 设计用于为雷达等噪声敏感型 应用提供严格的电源规范。该器件包含两个降压直流/直流转换器以及通用数字输出信号。该器件由 I^2C 兼容串行接口和使能信号进行控制。

自动 PWM/PFM（AUTO 模式）操作可在较宽输出电流范围内最大限度地提高效率。TPS65653-Q1 支持远程电压检测，可补偿稳压器输出与负载点 (POL) 之间的 IR 压降，从而提高输出电压的精度。此外，可以强制开关时钟进入 PWM 模式以及将其与外部时钟同步，从而最大限度地降低干扰。

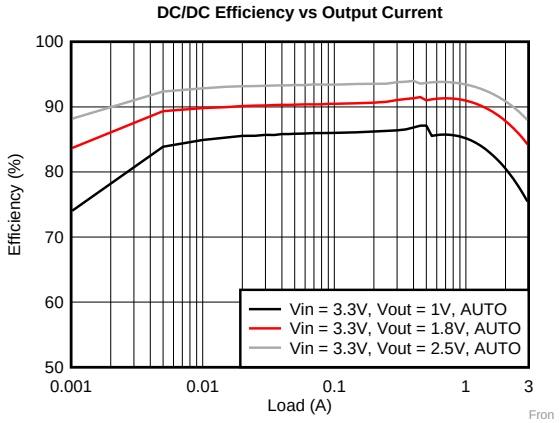
TPS65653-Q1 器件支持可编程启动和关断延迟与排序（包括与使能信号同步的 GPO 信号）。在启动和电压变化期间，器件会对输出转换率进行控制，从而最大限度地减小输出电压过冲和浪涌电流。

器件信息

器件型号	封装	封装尺寸（标称值）
TPS65653-Q1	VQFN (28)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

直流/直流效率与输出电流



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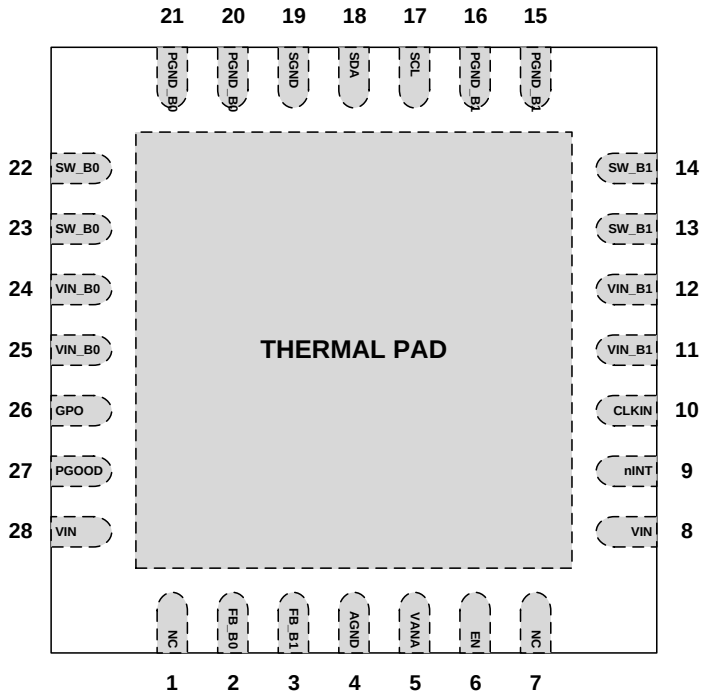
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 3 月	*	初始发行版

5 Pin Configuration and Functions

RHD Package
28-Pin VQFN With Thermal Pad
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NUMBER	NAME		
1	NC	O	Unused. Leave this pin floating.
2	FB_B0	A	Output voltage feedback (positive) for Buck 0
3	FB_B1	A	Output voltage feedback (positive) for Buck 1
4	AGND	G	Ground
5	VANA	P/I	Supply voltage for analog and digital blocks. Must be connected to same node with VIN_Bx.
6	EN	D/I	Programmable enable signal for regulators and GPOs. If the pin is not used, leave the pin floating.
7	NC	O	Unused. Leave this pin floating.
8	VIN	I	Unused. Connect this pin to VANA.
9	nINT	D/O	Open-drain interrupt output. Active LOW. If the pin is not used, connect the pin to ground.
10	CLKIN	D/I/O	External clock input. Alternative function is general-purpose digital output (GPO2). If the pin is not used, leave the pin floating.
11, 12	VIN_B1	P/I	Input for Buck 1. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
13, 14	SW_B1	P/O	Buck 1 switch node. If the Buck 1 is not used, leave the pin floating.
15, 16	PGND_B1	P/G	Power ground for Buck 1
17	SCL	D/I	Serial interface clock input for I^2C access. Connect a pullup resistor. If the I^2C interface is not used, connect the pin to Ground.
18	SDA	D/I/O	Serial interface data input and output for I^2C access. Connect a pullup resistor. If the I^2C interface is not used, connect the pin to Ground.
19	SGND	G	Ground

(1) A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NUMBER	NAME		
20, 21	PGND_B0	P/G	Power ground for Buck 0
22, 23	SW_B0	P/O	Buck 0 switch node. If the Buck 0 is not used, leave the pin floating.
24, 25	VIN_B0	P/I	Input for Buck 0. The separate power pins VIN_Bx are not connected together internally - VIN_Bx pins must be connected together in the application and be locally bypassed.
26	GPO	D/O	General-purpose digital output. If the pin is not used, leave the pin floating.
27	PGOOD	D/O	Power-good indication signal. If the pin is not used, leave the pin floating.
28	VIN	I	Unused. Connect this pin to VANA.
Thermal Pad	—	—	Connect to PCB ground plane using multiple vias for good thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
VIN, VIN_Bx, VANA	Voltage on power connections (must use the same input supply)	–0.3	6	V
SW_Bx	Voltage on buck switch nodes	–0.3	(VIN_Bx + 0.3 V) with 6-V maximum	V
FB_Bx	Voltage on buck voltage sense nodes	–0.3	(VANA + 0.3 V) with 6-V maximum	V
SDA, SCL, nINT, EN	Voltage on logic pins (input or output pins)	–0.3	(VANA + 0.3 V) with 6-V maximum	V
PGOOD, GPO, CLKIN (GPO2)	Voltage on logic pins (input or output pins)	–0.3	(VANA + 0.3 V) with 6-V maximum	V
T_{J-MAX}	Junction temperature	−40	150	°C
T_{stg}	Storage temperature	–65	150	
Maximum lead temperature (soldering, 10 seconds)			260	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 7, 8, 14, 15, 21, 22, 28)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
INPUT VOLTAGE				
VIN, VIN_Bx, VANA	Voltage on power connections (must use the same input supply)	2.8	5.5	V
EN, nINT	Voltage on logic pins (input or output pins)	0	5.5	V
CLKIN	Voltage on logic pins (input pin)	0	VANA	V
PGOOD, GPO, GPO2	Voltage on logic pins (output pins)	0	VANA	V
SCL, SDA	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), Fast+ (1 MHz), and High-Speed (3.4 MHz) Modes	0	1.95	V
	Voltage on I2C interface, Standard (100 kHz), Fast (400 kHz), and Fast+ (1 MHz) Modes	0	VANA with 3.6-V maximum	V
TEMPERATURE				
T_J	Junction temperature	−40	140	°C
T_A	Ambient temperature	−40	125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		TPS65653-Q1 RHD (VQFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.7	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	26.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.8	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

Limits apply over the junction temperature range –40°C ≤ T_J ≤ +140°C, specified V_{VANA}, V_{VIN_Bx},V_{VOUT_Bx}, and I_{OUT} range, unless otherwise noted. Typical values are at T_J = 25°C, V_{VANA} = V_{VIN_Bx} = 3.7 V, and V_{OUT} = 1 V, unless otherwise noted.(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL COMPONENTS						
C_{IN_VANA}	Input filtering capacitance for VANA	Effective capacitance, connected from VANA to AGND		100		nF
C_{IN_BUCK}	Input filtering capacitance for buck regulators	Effective capacitance, connected from VIN_Bx to PGND_Bx	1.9	10		µF
C_{OUT_BUCK}	Output filtering capacitance for buck regulators, local	Effective capacitance	10	22		µF
C_{POL_BUCK}	Point-of-load (POL) capacitance for buck regulators	POL capacitance		22		µF
$C_{OUT-TOTAL\_BUCK}$	Buck output capacitance, total (local and POL)	Total output capacitance, VIN_Bx ≤ 4 V and Slew rate ≤ 3.8 mV/µs			150	µF
		Total output capacitance, VIN_Bx > 4 V			100	µF
		Total output capacitance, Slew rate > 3.8 mV/µs			100	µF
ESR_C	Input and output capacitor ESR	[1-10] MHz		2	10	mΩ
L	Inductor	Inductance of the inductor		0.47		µH
			–30%		30%	
DCR_L	Inductor DCR			25		mΩ
BUCK REGULATORS						
$V_{(VIN\_Bx)}$, $V_{(VANA)}$	Input voltage range	VIN_Bx and VANA pins must be connected to the same supply line	2.8	3.3	5.5	V
V_{OUT_Bx}	Output voltage	Programmable voltage range	1	1	3.36	V
		Step size, 1 V ≤ V_{OUT} < 1.4 V		5		mV
		Step size, 1.4 V ≤ V_{OUT} ≤ 3.36 V		20		
I_{OUT_Bx}	Output current	Output current			3(3)	A
	Input and Output voltage difference	Minimum voltage between $V_{(VIN\_Bx)}$ and V_{OUT} to fulfill the electrical characteristics	0.8			V

(1) All voltage values are with respect to network ground.
(2) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers are not verified, but do represent the most likely norm.
(3) The maximum output current can be limited by the forward current limit $I_{LIM\ FWD}$. The power dissipation inside the die increases the junction temperature and limits the maximum current depending of the length of the current pulse, efficiency, board and ambient temperature.

Electrical Characteristics (continued)

Limits apply over the junction temperature range –40°C ≤ T_J ≤ +140°C, specified V_{VANA}, V_{VIN_Bx},V_{VOUT_Bx}, and I_{OUT} range, unless otherwise noted. Typical values are at T_J = 25°C, V_{VANA} = V_{VIN_Bx} = 3.7 V, and V_{OUT} = 1 V, unless otherwise noted.(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT\_Bx\_DC}$	DC output voltage accuracy, includes voltage reference, DC load and line regulations, process and temperature	Force PWM mode	–2%		2%	
		PFM mode. Average output voltage level is increased by max. 20 mV	–2%		2% + 20 mV	
	Ripple voltage	PWM mode, L = 0.47 µH, I_{OUT} = 500 mA, COUT = 22uF + 22uF (GCM31CR71A226KE02)		4		mV_{p-p}
		PFM mode, L = 0.47 µH, I_{OUT} = 10 mA, COUT = 22uF + 22uF (GCM31CR71A226KE02)		25		
DC_{LNR}	DC line regulation	I_{OUT} = 1 A		±0.05		%/V
DC_{LDR}	DC load regulation in PWM mode	V_{OUT_Bx} = 1 V, I_{OUT} from 0 to $I_{OUT(max)}$		0.3%		
T_{LDSR}	Transient load step response	I_{OUT} = 0 A to 3 A, T_R = T_F = 1 µs, PWM mode, V_{VIN_Bx} = 3.3 V, V_{OUT_Bx} = 1 V, C_{OUT} = 44 µF, L = 0.47 µH, f_{SW} = 4 MHz		±60		mV
T_{LNSR}	Transient line response	$V_{(VIN\_Bx)}$ stepping 3 V ↔ 3.5 V, T_R = T_F = 10 µs, I_{OUT} = $I_{OUT(max)}$		±10		mV
$I_{LIM\ FWD}$	Forward current limit per phase (peak for every switching cycle)	Programmable range	1.5		4	A
		Step size		0.5		
		Accuracy, $V_{(VIN\_Bx)}$ ≥ 3 V, I_{LIM} = 4 A	–5%	7.5%	20%	
		Accuracy, 2.8 V ≤ $V_{(VIN\_Bx)}$ < 3 V, I_{LIM} = 4 A	–20%	7.5%	20%	
$I_{LIM\ NEG}$	Negative current limit		1.6	2.0	3.0	A
$R_{DS(ON)\ HS\ FET}$	On-resistance, high-side FET	Between VIN_Bx and SW_Bx pins (I = 1 A)		50	110	mΩ
$R_{DS(ON)\ LS\ FET}$	On-resistance, low-side FET	Between SW_Bx and PGND_Bx pins (I = 1 A)		45	90	mΩ
f_{SW}	Switching frequency	PWM mode	3.6	4	4.4	MHz
	Start-up time (soft start)	From ENx to V_{OUT_Bx} = 0.35 V (slew-rate control begins)		120		µs
	Output voltage slew-rate(4)	SLEW_RATEx[2:0] = 010	–15%	10	15%	mV/µs
		SLEW_RATEx[2:0] = 011		7.5		
		SLEW_RATEx[2:0] = 100		3.8		
		SLEW_RATEx[2:0] = 101		1.9		
		SLEW_RATEx[2:0] = 110		0.94		
		SLEW_RATEx[2:0] = 111		0.47		
$I_{PFM-PWM}$	PFM-to-PWM - current threshold(5)			550		mA
$I_{PWM-PFM}$	PWM-to-PFM - current threshold(5)			290		mA
R_{DIS_Bx}	Output pulldown resistance	Regulator disabled	150	250	350	Ω

(4) The slew-rate can be limited by the current limit (forward or negative current limit), output capacitance and load current.
(5) The final PFM-to-PWM and PWM-to-PFM switchover current varies slightly and is dependent on the output voltage, input voltage and the inductor current level.

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Electrical Characteristics (continued)

Limits apply over the junction temperature range –40°C ≤ T_J ≤ +140°C, specified V_{VANA}, V_{VIN_Bx},V_{VOUT_Bx}, and I_{OUT} range, unless otherwise noted. Typical values are at T_J = 25°C, V_{VANA} = V_{VIN_Bx} = 3.7 V, and V_{OUT} = 1 V, unless otherwise noted.(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		$V_{(VIN\_Bx)}$ and $V_{(VANA)}$ fixed 3.7 V				
	Output voltage monitoring for PGOOD pin and for power-good Interrupt	Overvoltage threshold (compared to DC output voltage level, $V_{VOUT\_Bx\_DC}$)	39	50	64	mV
		Undervoltage threshold (compared to DC output voltage level, $V_{VOUT\_Bx\_DC}$)	–53	–40	–29	
		Deglitch time during operation and after voltage change	4		15	µs
	Gating time for PGOOD signal after regulator enable or voltage change	PGOOD_MODE = 0		800		µs
EXTERNAL CLOCK AND PLL						
f_{EXT_CLK}	External input clock(6)	Nominal frequency	1		24	MHz
		Nominal frequency step size		1		
		Required accuracy from nominal frequency	–10%		10%	
	External clock detection	Delay for missing clock detection			1.8	µs
		Delay and debounce for clock detection			20	
	Clock change delay (internal to external)	Delay from valid clock detection to use of external clock		600		µs
	PLL output clock jitter	Cycle to cycle		300		ps, p-p
PROTECTION FUNCTIONS						
	Thermal warning(7)	Temperature rising, TDIE_WARN_LEVEL = 0	115	125	135	°C
		Temperature rising, TDIE_WARN_LEVEL = 1	127	137	147	
		Hysteresis		20		
	Thermal shutdown(7)	Temperature rising	140	150	160	°C
		Hysteresis		20		
$VANA_{OVP}$	VANA overvoltage	Voltage rising	5.6	5.8	6.1	V
		Voltage falling	5.45	5.73	5.96	
		Hysteresis	40			mV
$VANA_{UVLO}$	VANA undervoltage lockout	Voltage rising	2.51	2.63	2.75	V
		Voltage falling	2.5	2.6	2.7	
	Buck short-circuit detection	Threshold	280	360	440	mV
LOAD CURRENT MEASUREMENT FOR BUCK REGULATORS						
	Current measurement range	Maximum code			10.22	A
	Resolution	LSB		20		mA
	Measurement accuracy	I_{OUT} > 1 A		<10%		
	Measurement time	PFM mode (automatically changing to PWM mode for the measurement)		45		µs
		PWM mode		4		
CURRENT CONSUMPTION						
	Standby current consumption, regulators disabled			9		µA

(6) The external clock frequency must be selected so that buck switching frequency is above 1.7 MHz.
(7) For a given device thermal warning will always happen at a lower temperature than thermal shutdown.

Electrical Characteristics (continued)

Limits apply over the junction temperature range –40°C ≤ T_J ≤ +140°C, specified V_{VANA}, V_{VIN_Bx},V_{VOUT_Bx}, and I_{OUT} range, unless otherwise noted. Typical values are at T_J = 25°C, V_{VANA} = V_{VIN_Bx} = 3.7 V, and V_{OUT} = 1 V, unless otherwise noted.(1)(2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Active current consumption, one buck regulator enabled in auto mode, internal RC oscillator, PGOOD monitoring enabled	I_{OUT_Bx} = 0 mA, not switching		58		µA
	Active current consumption, two buck regulators enabled in auto mode, internal RC oscillator, PGOOD monitoring enabled	I_{OUT_Bx} = 0 mA, not switching		100		µA
	Active current consumption during PWM operation, one buck regulator enabled	I_{OUT_Bx} = 0 mA		15		mA
	Active current consumption during PWM operation, two buck regulators enabled	I_{OUT_Bx} = 0 mA		30		mA
	PLL and clock detector current consumption	f_{EXT_CLK} = 1 MHz, Additional current consumption when enabled		2		mA
DIGITAL INPUT SIGNALS EN, SCL, SDA, CLKIN						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.2			
V_{HYS}	Hysteresis of Schmitt Trigger inputs		10	80	200	mV
	EN/CLKIN pulldown resistance	EN_PD/CLKIN_PD = 1		500		kΩ
DIGITAL OUTPUT SIGNALS nINT, SDA						
V_{OL}	Output low level	nINT: I_{SOURCE} = 2 mA			0.4	V
		SDA: I_{SOURCE} = 20 mA			0.4	V
R_P	External pullup resistor for nINT	To VIO Supply		10		kΩ
DIGITAL OUTPUT SIGNALS PGOOD, GPO, GPO2						
V_{OL}	Output low level	I_{SOURCE} = 2 mA			0.4	V
V_{OH}	Output high level, configured to push-pull	I_{SINK} = 2 mA	V_{VANA} – 0.4		V_{VANA}	V
V_{PU}	Supply voltage for external pullup resistor, configured to open-drain				V_{VANA}	V
R_{PU}	External pullup resistor, configured to open-drain			10		kΩ
ALL DIGITAL INPUTS						
I_{LEAK}	Input current	All logic inputs over pin voltage range	−1		1	µA

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6.6 I²C Serial Bus Timing Parameters

These specifications are ensured by design. Unless otherwise noted, V_{IN_Bx} = 3.7 V. See (1) and Figure 1.

			MIN	MAX	UNIT
f_{SCL}	Serial clock frequency	Standard mode		100	kHz
		Fast mode		400	
		Fast mode+		1	MHz
		High-speed mode, C_b = 100 pF		3.4	
		High-speed mode, C_b = 400 pF		1.7	
t_{LOW}	SCL low time	Standard mode	4.7		µs
		Fast mode	1.3		
		Fast mode+	0.5		
		High-speed mode, C_b = 100 pF	0.16		
		High-speed mode, C_b = 400 pF	0.32		
t_{HIGH}	SCL high time	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode+	0.26		
		High-speed mode, C_b = 100 pF	0.06		
		High-speed mode, C_b = 400 pF	0.12		
$t_{SU;DAT}$	Data setup time	Standard mode	250		ns
		Fast mode	100		
		Fast mode+	50		
		High-speed mode	10		
$t_{HD;DAT}$	Data hold time	Standard mode	10	3450	ns
		Fast mode	10	900	
		Fast mode+	10		
		High-speed mode, C_b = 100 pF	10	70	
		High-speed mode, C_b = 400 pF	10	150	
$t_{SU;STA}$	Setup time for a start or a repeated start condition	Standard mode	4.7		µs
		Fast mode	0.6		
		Fast mode+	0.26		
		High-speed mode	0.16		
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode+	0.26		
		High-speed mode	0.16		
t_{BUF}	Bus free time between a stop and start condition	Standard mode	4.7		µs
		Fast mode	1.3		
		Fast mode +	0.5		
$t_{SU;STO}$	Setup time for a stop condition	Standard mode	4		µs
		Fast mode	0.6		
		Fast mode+	0.26		
		High-speed mode	0.16		
t_{rDA}	Rise time of SDA signal	Standard mode		1000	ns
		Fast mode	20	300	
		Fast mode+		120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	20	160	

(1) C_b refers to the capacitance of one bus line.

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I²C Serial Bus Timing Parameters (continued)

These specifications are ensured by design. Unless otherwise noted, V_{IN_Bx} = 3.7 V. See (1) and Figure 1.

			MIN	MAX	UNIT
t_{fDA}	Fall time of SDA signal	Standard mode		300	ns
		Fast mode	20 × (V_{DD} / 5.5 V)	300	
		Fast mode+	20 × (V_{DD} / 5.5 V)	120	
		High-speed mode, C_b = 100 pF	10	80	
		High-speed mode, C_b = 400 pF	30	160	
t_{rCL}	Rise time of SCL signal	Standard mode		1000	ns
		Fast mode	20	300	
		Fast mode+		120	
		High-speed mode, C_b = 100 pF	10	40	
		High-speed mode, C_b = 400 pF	20	80	
t_{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	High-speed mode, C_b = 100 pF	10	80	ns
		High-speed mode, C_b = 400 pF	20	160	
t_{fCL}	Fall time of a SCL signal	Standard mode		300	ns
		Fast mode	20 × (V_{DD} / 5.5 V)	300	
		Fast mode+	20 × (V_{DD} / 5.5 V)	120	
		High-speed mode, C_b = 10 – 100 pF	10	40	
		High-speed mode, C_b = 400 pF	20	80	
C_b	Capacitive load for each bus line (SCL and SDA)			400	pF
t_{SP}	Pulse width of spike suppressed (SCL and SDA spikes that are less then the indicated width are suppressed)	Standard mode, fast mode, and fast mode+		50	ns
		High-speed mode		10	

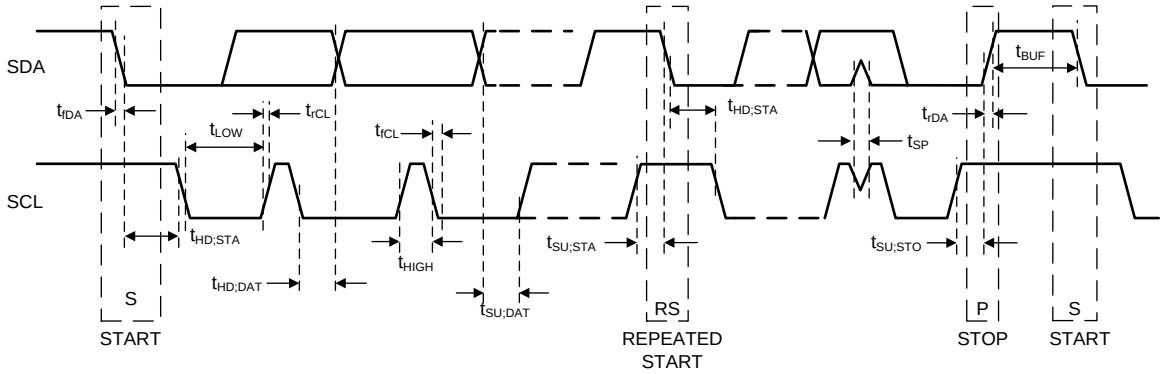

Figure 1. I²C Timing

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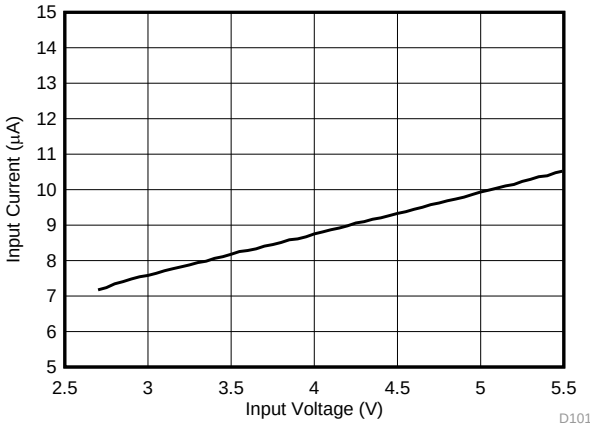
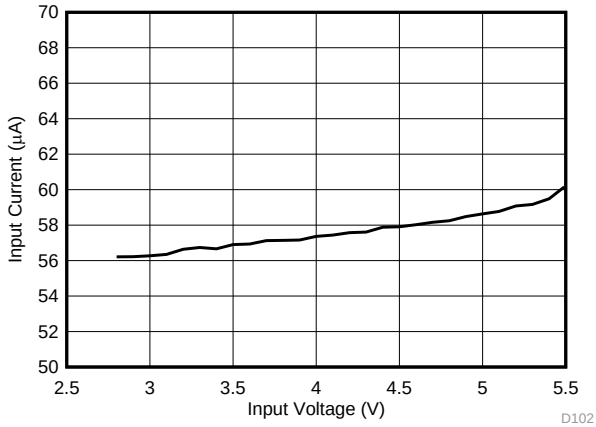
6.7 Typical Characteristics

Unless otherwise specified: $V_{(VIN\_Bx)} = V_{(VANA)} = 3.7$ V, $V_{OUT\_Bx} = 1$ V, $T_A = 25°C$, L = 0.47 µH (Murata DFE252012PD-R47M), $C_{OUT\_BUCK} = 22$ µF, and $C_{POL\_BUCK} = 22$ µF



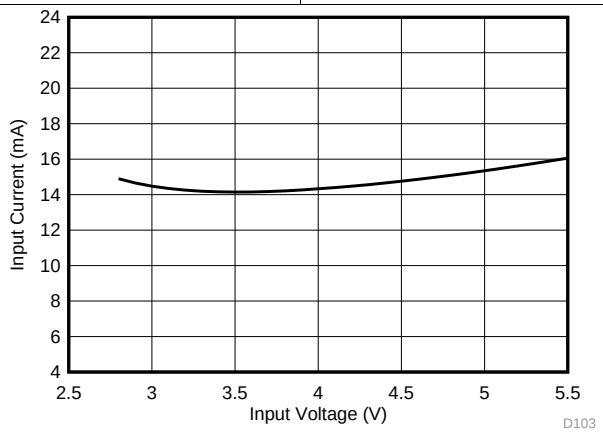
Regulators disabled

Figure 2. Standby Current Consumption vs Input Voltage



$V_{OUT\_Bx} = 1$ V Load = 0 mA

Figure 3. Active State Current Consumption vs Input Voltage, One Buck Regulator Enabled in PFM Mode



$V_{OUT\_Bx} = 1$ V Load = 0 mA

Figure 4. Active State Current Consumption vs Input Voltage, One Buck Regulator Enabled in Forced PWM Mode

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7 Detailed Description

7.1 Overview

The TPS65653-Q1 is a high-efficiency, high-performance flexible power supply device with two step-down DC/DC converter cores (Buck0 and Buck1) for automotive applications. Table 1 lists the output characteristics of the regulators.

Table 1. Supply Specification

SUPPLY	OUTPUT		
	V_{OUT} RANGE (V)	RESOLUTION (mV)	I_{MAX} MAXIMUM OUTPUT CURRENT (mA)
Buck0	1 to 3.36	5 (1 V to 1.4 V) 20 (1.4 V to 3.36 V)	3000
Buck1	1 to 3.36	5 (1 V to 1.4 V) 20 (1.4 V to 3.36 V)	3000

The TPS65653-Q1 also supports switching clock synchronization to an external clock (CLKIN pin). The nominal frequency of the external clock can be from 1 MHz to 24 MHz with 1-MHz steps.

Additional features include:

- Soft-start
- Input voltage protection:
  - Undervoltage lockout
  - Overvoltage protection
- Output voltage monitoring and protection:
  - Overvoltage monitoring
  - Undervoltage monitoring
  - Overload protection
- Thermal warning
- Thermal shutdown

The TPS65653-Q1 has one dedicated general purpose digital output (GPO) signal. CLKIN pin can be programmed as a second GPO signal (GPO2) if external clock is not needed. The output type (open-drain or push-pull) is programmable for the GPOs.

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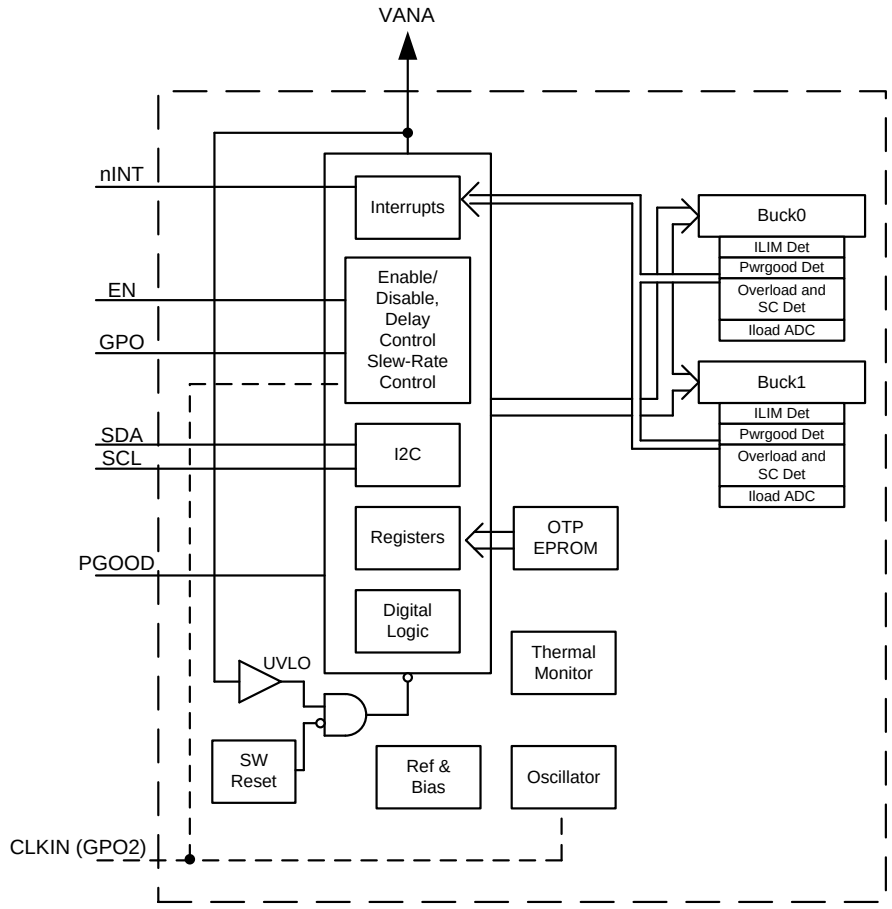
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 DC/DC Converters

7.3.1.1 Overview

The TPS65653-Q1 includes two step-down DC/DC converter cores. The cores are designed for flexibility; most of the functions are programmable, thus giving a possibility to optimize the regulator operation for each application. The buck regulators deliver 1-V to 3.36-V regulated voltage rails from a 2.8-V to 5.5-V supply voltage.

The TPS65653-Q1 has the following features:

- DVS support with programmable slew rate
- Automatic mode control based on the loading (PFM or PWM mode)
- Forced PWM mode option
- Optional external clock input to minimize crosstalk
- Optional spread-spectrum technique to reduce EMI
- Phase control for optimized EMI
- Synchronous rectification
- Current mode loop with PI compensator

Feature Description (continued)

- Soft start
- Power Good flag with maskable interrupt
- Power Good signal (PGOOD) with selectable sources
- Average output current sensing (for PFM entry and load current measurement)

The following parameters can be programmed via registers, the default values are set by OTP bits:

- Output voltage
- Forced PWM operation
- Switch current limit
- Output voltage slew rate
- Enable and disable delays

There are two modes of operation for the buck converter, depending on the output current required: pulse-width modulation (PWM) and pulse-frequency modulation (PFM). The converter operates in PWM mode at high load currents of approximately 600 mA or higher. Lighter output current loads cause the converter to automatically switch into PFM mode for reduced current consumption when forced PWM mode is disabled. The forced PWM mode can be selected to maintain fixed switching frequency at all load current levels.

A block diagram of a single core is shown in Figure 5.

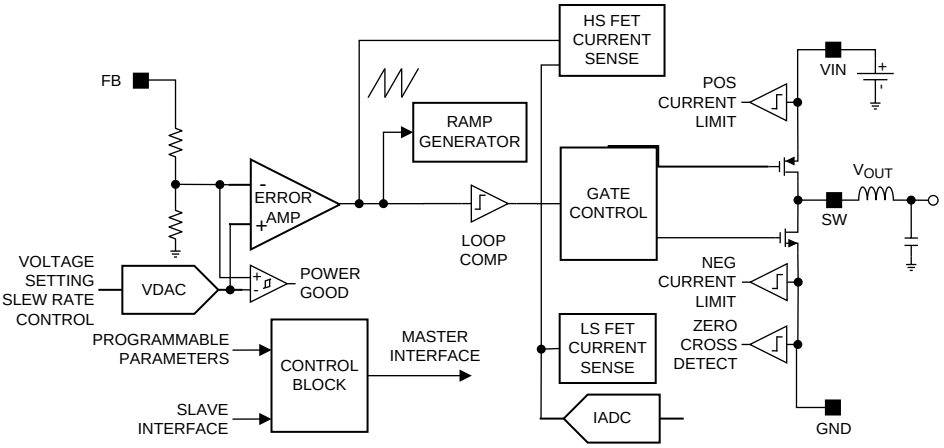


Figure 5. Detailed Block Diagram Showing One Core

7.3.1.2 Transition Between PWM and PFM Modes

PWM mode operation optimizes efficiency at mid to full load at the expense of light-load efficiency. The TPS65653-Q1 converter operates in PWM mode at load current of about 600 mA or higher. At lighter load current levels the device automatically switches into PFM mode for reduced current consumption when forced PWM mode is disabled (AUTO mode operation). By combining the PFM and the PWM modes a high efficiency is achieved over a wide output-load current range.

7.3.1.3 Buck Converter Load Current Measurement

Buck load current can be monitored via I^2C registers. The monitored buck converter is selected with the LOAD_CURRENT_BUCK_SELECT bit in SEL_I_LOAD register. A write to this selection register starts a current measurement sequence. The regulator is automatically forced to PWM mode for the measurement period. The measurement sequence is 50 µs long, maximum.

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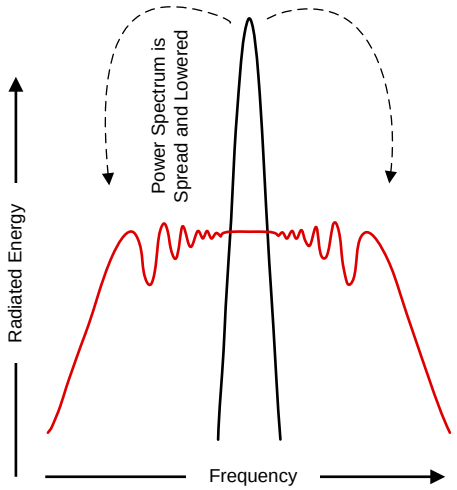
Feature Description (continued)

TPS65653-Q1 can be configured to give out an interrupt (I_MEAS_INT bit in INT_TOP_1 register) after the load current measurement sequence is finished. Load current measurement interrupt can be masked with I_MEAS_MASK bit (TOP_MASK_1 register). The measurement result can be read from registers I_LOAD_1 and I_LOAD_2. Register I_LOAD_1 bits BUCK_LOAD_CURRENT[7:0] give out the LSB bits and register I_LOAD_2 bit BUCK_LOAD_CURRENT[8] the MSB bit. The measurement result BUCK_LOAD_CURRENT[8:0] LSB is 20 mA, and maximum code value of the measurement corresponds to 10.22 A.

7.3.1.4 Spread-Spectrum Mode

Systems with periodic switching signals may generate a large amount of switching noise in a set of narrowband frequencies (the switching frequency and its harmonics). The usual solution to reduce noise coupling is to add EMI-filters and shields to the boards. The TPS65653-Q1 has register selectable spread-spectrum mode which minimizes the need for output filters, ferrite beads, or chokes. In spread spectrum mode, the switching frequency varies around the center frequency, reducing the EMI emissions radiated by the converter and associated passive components and PCB traces (see Figure 6). This feature is available only when internal RC oscillator is used (EN_PLL bit is 0 in PLL_CTRL register), and it is enabled with the EN_SPREAD_SPEC bit in CONFIG register, and it affects both buck cores.



Where a fixed frequency converter exhibits large amounts of spectral energy at the switching frequency, the spread spectrum architecture of the TPS65653-Q1 spreads that energy over a large bandwidth.

Figure 6. Spread-Spectrum Modulation

7.3.2 Sync Clock Functionality

The TPS65653-Q1 device contains a CLKIN input to synchronize the switching clock of the buck regulators with the external clock. The block diagram of the clocking and PLL module is shown in Figure 7. Depending on the EN_PLL bit in PLL_CTRL register and the external clock availability, the external clock is selected and interrupt is generated as shown in Table 2. The interrupt can be masked with SYNC_CLK_MASK bit in TOP_MASK_1 register. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[4:0] bits in PLL_CTRL register, and it can be from 1 MHz to 24 MHz with 1-MHz steps. The external clock must be inside accuracy limits (–10%/+10%) of the selected frequency for valid clock detection.

The SYNC_CLK_INT interrupt in INT_TOP_1 register is also generated in cases where the external clock is expected but it is not available. These cases are start-up (read OTP-to-standby transition) when EN_PLL is 1 and Buck regulator enable (standby-to-active transition) when EN_PLL is 1.

Feature Description (continued)

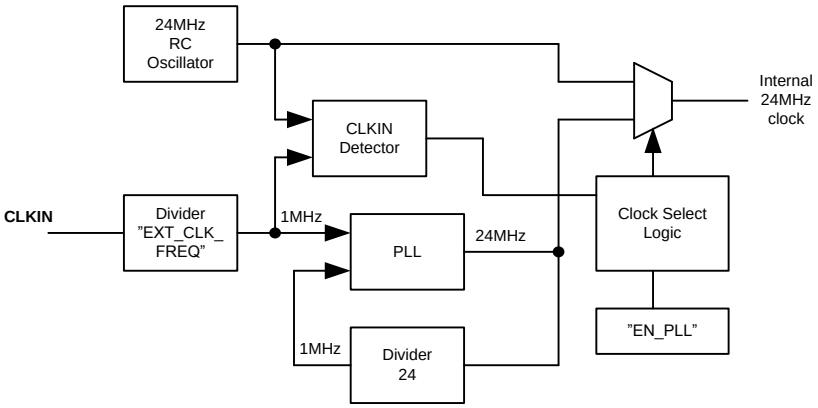


Figure 7. Clock and PLL Module

Table 2. PLL Operation

DEVICE OPERATION MODE	EN_PLL	PLL AND CLOCK DETECTOR STATE	INTERRUPT FOR EXTERNAL CLOCK	CLOCK
STANDBY	0	Disabled	No	Internal RC
ACTIVE	0	Disabled	No	Internal RC
STANDBY	1	Enabled	When external clock appears or disappears	Automatic change to external clock when available
ACTIVE	1	Enabled	When external clock appears or disappears	Automatic change to external clock when available

7.3.3 Power-Up

The power-up sequence for the TPS65653-Q1 is as follows:

- VANA (and VIN_Bx) reach minimum recommended levels (V_{VANA} > $VANA_{UVLO}$). This initiates power-on-reset (POR), OTP reading, and enables the system I/O interface. The I^2C host should allow at least 1.2 ms before writing or reading data to the TPS65653-Q1.
- Device enters standby mode.
- The host can change the default register setting by I^2C if needed.
- The regulators can be enabled/disabled and the GPO signals can be controlled by EN pin and by I^2C interface.

Transitions between the operating modes are shown in *Modes of Operation*.

7.3.4 Regulator Control

7.3.4.1 Enabling and Disabling Regulators

The regulators can be enabled when the device is in STANDBY or ACTIVE state. There are two ways for enable and disable the buck regulators:

- Using BUCKx_EN bit in BUCKx_CTRL_1 register (BUCKx_EN_PIN_CTRL bit is 0 in BUCKx_CTRL_1 register)
- Using EN control pin (BUCKx_EN bit is 1 **AND** BUCKx_EN_PIN_CTRL bit is 1)

If the EN control pin is used for enable and disable then the delay from the control signal rising edge to start-up is set by BUCKx_STARTUP_DELAY[3:0] bits in BUCKx_DELAY register and the delay from control signal falling edge to shutdown is set by BUCKx_SHUTDOWN_DELAY[3:0] bits in BUCKx_DELAY register. The delays are valid only for EN signal transitions and not for control with I^2C writings to the BUCKx_EN bit.

The control of the regulator (with 0-ms delays) is shown in Table 3.

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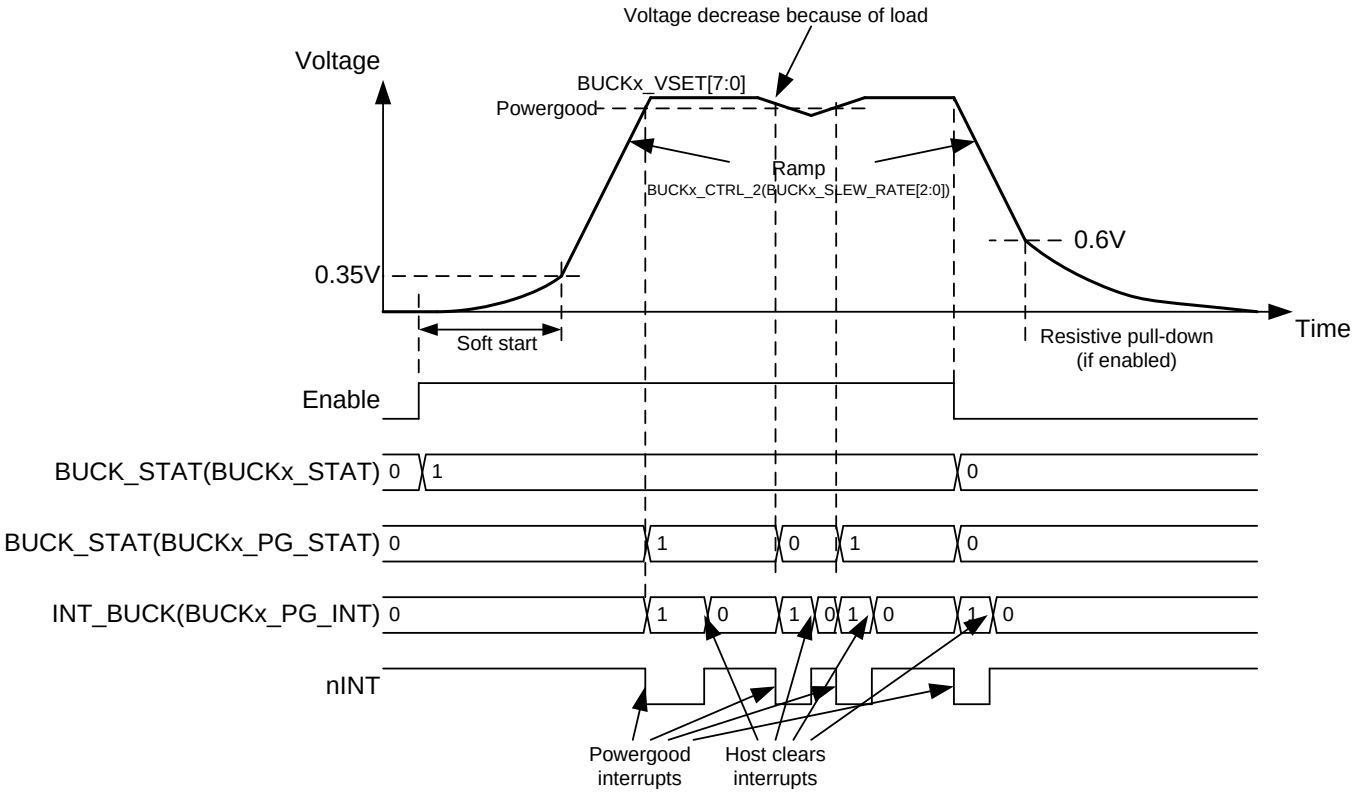
Table 3. Regulator Control

	BUCKx_EN	BUCKx_EN_PIN_CTRL	EN PIN	BUCKx OUTPUT VOLTAGE
Enable/disable control with BUCKx_EN bit	0	Don't Care	Don't Care	Disabled
	1	0	Don't Care	BUCKx_VSET[7:0]
Enable/disable control with EN pin	1	1	Low	Disabled
	1	1	High	BUCKx_VSET[7:0]

The buck regulator is enabled by the EN pin or by I^2C writing as shown in Figure 8. The soft-start circuit limits the in-rush current during start-up. When the output voltage rises to a 0.35-V level, the output voltage becomes slew-rate controlled. If there is a short circuit at the output, and the output voltage does not increase above the 0.35-V level in 1 ms or the output voltage drops below 0.35-V level during operation (for minimum of 1 ms), the regulator is disabled, and BUCKx_SC_INT interrupt in INT_BUCK register is set. When the output voltage reaches the Power-Good threshold level the BUCKx_PG_INT interrupt flag in INT_BUCK register is set. The Power-Good interrupt flag when reaching valid output voltage can be masked using BUCKx_PGR_MASK bit in BUCK_MASK register. The Power-Good interrupt flag can be also generated when the output voltage becomes invalid. The interrupt mask for invalid output voltage detection is set by BUCKx_PGF_MASK bit in BUCK_MASK register. A BUCKx_PG_STAT bit in BUCK_STAT register shows always the validity of the output voltage: 1 means valid and 0 means invalid output voltage. A PGOOD_WINDOW_BUCK bit in PGOOD_CTRL_1 register sets the detection method for the valid buck output voltage, either undervoltage detection or undervoltage and overvoltage detection.



BUCK_MASK(BUCKx_PGF_MASK) = 0
BUCK_MASK(BUCKx_PGR_MASK) = 0

Figure 8. Buck Regulator Enable and Disable

The EN input pin has an integrated pulldown resistor. The pulldown resistor is controlled with EN_PD bit in CONFIG register.

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7.3.4.2 Changing Output Voltage

The output voltage of the regulator can be changed by writing to the BUCKx_VOUT register. The voltage change for buck regulator is always slew-rate controlled, and the slew-rate is defined by the BUCKx_SLEW_RATE[2:0] bits in BUCKx_CTRL_2 register. During voltage change the forced PWM mode is used automatically. When the programmed output voltage is achieved, the mode becomes the one defined by load current, and the BUCKx_FPWM bit in BUCKx_CTRL_1 register.

The voltage change and Power-Good interrupts are shown in Figure 9.

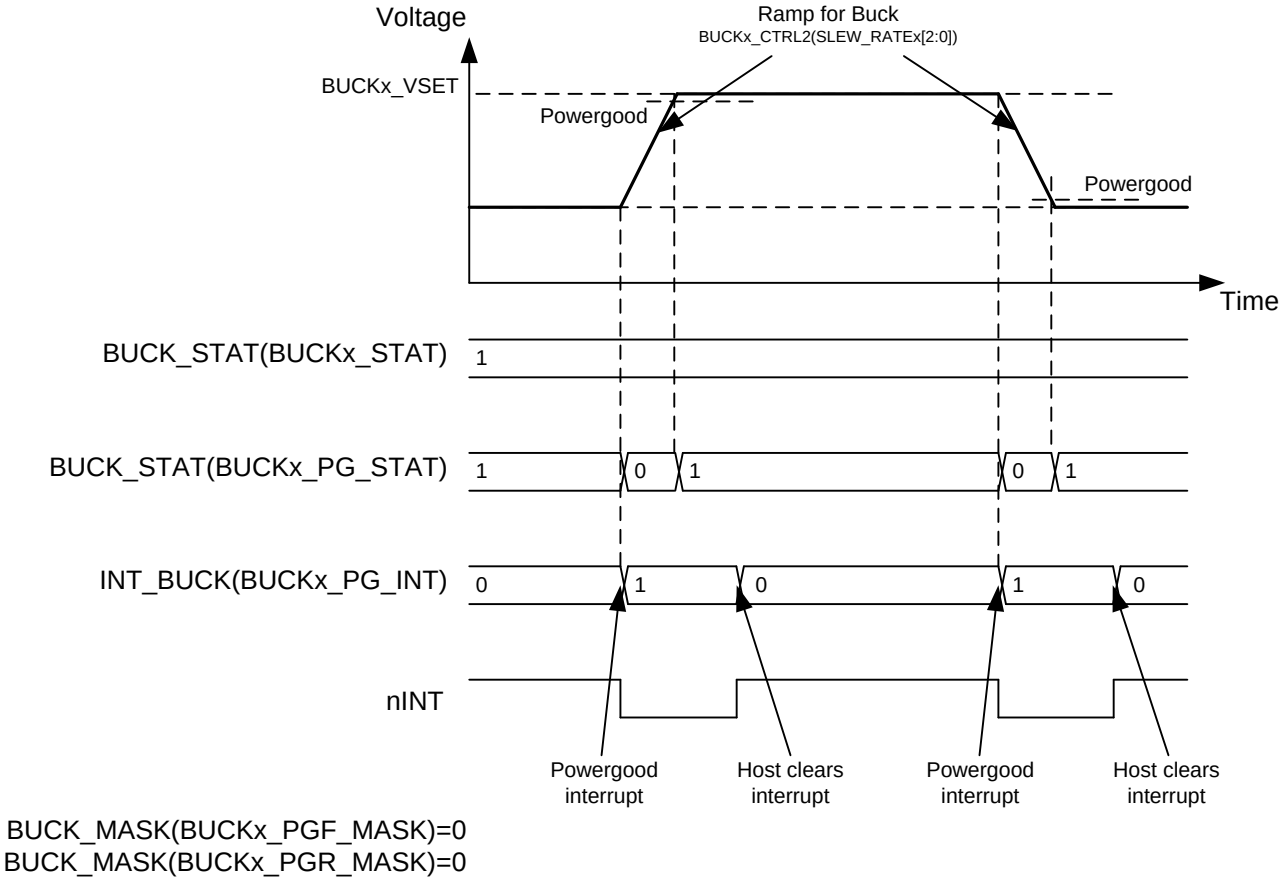

Figure 9. Regulator Output Voltage Change

7.3.5 Enable and Disable Sequences

The TPS65653-Q1 device supports start-up and shutdown sequencing with programmable delays for different regulator outputs using single EN control signal. The Buck regulator is selected for delayed control with:

- BUCKx_EN = 1 in BUCKx_CTRL_1 register
- BUCKx_EN_PIN_CTRL = 1 in BUCKx_CTRL_1 register
- BUCKx_VSET[7:0] bits in BUCKx_VOUT register defines the voltage when EN pin is high
- The delay from rising edge of EN pin to the regulator enable is set by BUCKx_STARTUP_DELAY[3:0] bits in BUCKx_DELAY register and
- The delay from falling edge of EN pin to the regulator disable is set by BUCKx_SHUTDOWN_DELAY[3:0] bits in BUCKx_DELAY register.

The GPO (and GPO2) digital output signals can be also controlled as a part of start-up and shutdown sequencing with the following settings:

- GPOx_EN = 1 in GPO_CTRL register
- GPOx_EN_PIN_CTRL = 1 in GPO_CTRL register
- The delay from rising edge of EN pin to the rising edge of GPO/GPO2 signal is set by

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GPOx_STARTUP_DELAY[3:0] bits in GPOx_DELAY register and

- The delay from falling edge of EN pin to the falling edge of GPO/GPO2 signal is set by GPOx_SHUTDOWN_DELAY[3:0] bits in GPOx_DELAY register.

An example of the start-up and shutdown sequences for the buck regulators are shown in Figure 10. The start-up and shutdown delays for the Buck0 regulator are 1 ms and 4 ms; for the Buck1 regulator start-up and shutdown delays are 3 ms and 1 ms. The delay settings are used only for enable/disable control with EN signal.

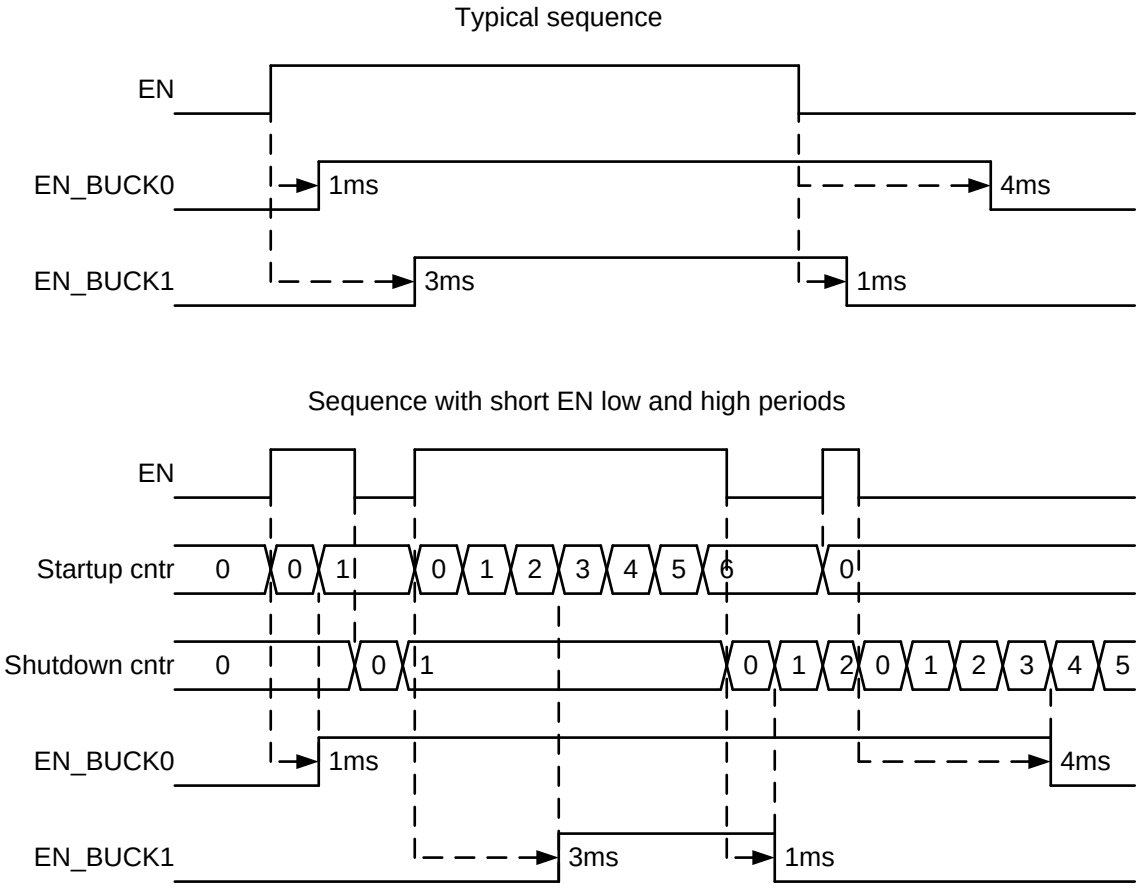

Figure 10. Start-Up and Shutdown Sequencing

7.3.6 Device Reset Scenarios

There are two reset methods implemented on the TPS65653-Q1:

- Software reset with SW_RESET bit in RESET register
- Undervoltage lockout (UVLO) reset from VANA supply

An SW reset occurs when SW_RESET bit is written 1. The bit is automatically cleared after writing. This event disables all the regulators immediately, drives GPO and GPO2 signals low, resets all the register bits to the default values and OTP bits are loaded (see Figure 15). I^2C interface is not reset during software reset.

If VANA supply voltage falls below the UVLO threshold level then all the regulators are disabled immediately, GPO and GPO2 signals are driven low, and all the register bits are reset to the default values. When the VANA supply voltage transition above UVLO threshold level an internal POR occurs. OTP bits are loaded to the registers and a startup is initiated according to the register settings.

7.3.7 Diagnosis and Protection Features

The TPS65653-Q1 is capable of providing four levels of protection features:

- Information of valid regulator output voltage which sets interrupt or PGOOD signal;
- Warnings for diagnosis which sets interrupt;
- Protection events which are disabling the regulators; and
- Faults which are causing the device to shutdown.

The TPS65653-Q1 sets the flag bits indicating what protection or warning conditions have occurred, and the nINT pin is pulled low. nINT is released again after a clear of flags is complete. The nINT signal stays low until all the pending interrupts are cleared.

When a fault is detected or software requested reset, it is indicated by a RESET_REG_INT interrupt flag in INT_TOP_2 register after next start-up. If the RESET_REG_MASK is set to masked in the OTP, the interrupt is not generated. The mask bit change with I^2C does not affect, because the RESET_REG_MASK bit is loaded from OTP during reset sequence.

Table 4. Summary of Interrupt Signals

EVENT	OUTCOME	INTERRUPT BIT	INTERRUPT MASK BIT	STATUS BIT	RECOVERY/INTERRUPT CLEAR
Buck current limit triggered	No effect	BUCK_INT BUCKx_ILIM_INT	BUCKx_ILIM_MASK	BUCKx_ILIM_STAT	Write 1 to BUCKx_ILIM_INT bit Interrupt is not cleared if current limit is active
Buck short circuit (V_{OUT} < 0.35 V at 1 ms after enable) or overload (V_{OUT} decreasing below 0.35 V during operation, 1-ms debounce)	Regulator disable	BUCK_INT BUCKx_SC_INT	N/A	N/A	Write 1 to BUCKx_SC_INT bit
Thermal warning	No effect	TDIE_WARN_INT	TDIE_WARN_MASK	TDIE_WARN_STAT	Write 1 to TDIE_WARN_INT bit Interrupt is not cleared if temperature is above thermal warning level
Thermal shutdown	All regulators disabled immediately and GPO and GPO2 are set to low	TDIE_SD_INT	N/A	TDIE_SD_STAT	Write 1 to TDIE_SD_INT bit Interrupt is not cleared if temperature is above thermal shutdown level
VANA overvoltage ($VANA_{OVP}$)	All regulators disabled immediately and GPO and GPO2 are set to low	OVP_INT	N/A	OVP_STAT	Write 1 to OVP_INT bit Interrupt is not cleared if VANA voltage is above $VANA_{OVP}$ level
Buck power good, output voltage becomes valid	No effect	BUCK_INT BUCKx_PG_INT	BUCKx_PGR_MASK	BUCKx_PG_STAT	Write 1 to BUCKx_PG_INT bit
Buck power good, output voltage becomes invalid	No effect	BUCK_INT BUCKx_PG_INT	BUCKx_PGF_MASK	BUCKx_PG_STAT	Write 1 to BUCKx_PG_INT bit
PGOOD pin changing from active to inactive state(1)	No effect	PGOOD_INT	PGOOD_MASK	PGOOD_STAT	Write 1 to PGOOD_INT bit
External clock appears or disappears	No effect to regulators	SYNC_CLK_INT(2)	SYNC_CLK_MASK	SYNC_CLK_STAT	Write 1 to SYNC_CLK_INT bit
Load current measurement ready	No effect	I_MEAS_INT	I_MEAS_MASK	N/A	Write 1 to I_MEAS_INT bit
Supply voltage $VANA_{UVLO}$ triggered (VANA falling)	Immediate shutdown, registers reset to default values	N/A	N/A	N/A	N/A
Supply voltage $VANA_{UVLO}$ triggered (VANA rising)	Startup, registers reset to default values and OTP bits loaded	RESET_REG_INT	RESET_REG_MASK	N/A	Write 1 to RESET_REG_INT bit
Software requested reset	Immediate shutdown followed by power up, registers reset to default values	RESET_REG_INT	RESET_REG_MASK	N/A	Write 1 to RESET_REG_INT bit

(1) PGOOD_STAT bit is 1 when the PGOOD pin shows valid voltages. PGOOD_POL bit in PGOOD_CTRL_1 register affects only PGOOD pin polarity, not Power Good and PGOOD_INT interrupt polarity.
(2) Interrupt is generated during clock-detector operation and if clock is not available when clock detector is enabled.

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7.3.7.1 Power-Good Information (PGOOD pin)

In addition to the interrupt-based indication of the current limit and the Power-Good level the TPS65653-Q1 device supports monitoring with PGOOD signal:

- Regulator output voltage,
- Input supply overvoltage,
- Thermal warning and
- Thermal shutdown.

Regulator output voltage monitoring (not current limit monitoring) can be selected for PGOOD indication. This selection is individual for both buck regulators and is set by EN_PGOOD_BUCKx bits in PGOOD_CTRL_1 register. When a regulator is disabled, the monitoring is automatically masked to prevent it forcing PGOOD inactive. A thermal warning can be also selected for PGOOD indication with EN_PGOOD_TWARN bit in PGOOD_CTRL_2 register. The monitoring from all the output rails, thermal warning (TDIE_WARN_STAT), input overvoltage interrupt (OVP_INT), and thermal shutdown interrupt (TDIE_SD_INT) are combined, and PGOOD pin is active only if all the selected sources shows a valid status.

The type of output voltage monitoring for PGOOD signal is selected by PGOOD_WINDOW_x bits in PGOOD_CTRL_1 register. If the bit is 0, only undervoltage is monitored; if the bit is 1, both undervoltage and overvoltage are monitored.

The polarity and the output type (push-pull or open-drain) are selected by the PGOOD_POL and PGOOD_OD bits in the PGOOD_CTRL_1 register.

PGOOD is only *active* or *asserted* when all enabled power resource output voltages are within specified tolerance for each requested/programmed output voltage.

PGOOD is *inactive* or *de-asserted* if any enabled power resource output voltages is outside specified tolerance for each requested/programmed output voltage.

The device OTP setting selects either gated (that is, *unusual*) or continuous (that is, *invalid*) mode of operation.

7.3.7.1.1 PGOOD Pin Gated mode

The gated (or *unusual*) mode of operation is selected by setting PGOOD_MODE bit to 0 in PGOOD_CTRL_2 register.

For the gated mode of operation, PGOOD behaves as follows:

- PGOOD is set to *active* or *asserted* state upon exiting OTP configuration as an initial default state.
- PGOOD status is suspended or unchanged during an 800-µs gated time period, thereby *gating-off* the status indication.
- During normal power-up sequencing and requested voltage changes, PGOOD state is not changed during an 800-µs gated time period. It typically remains *active* or *asserted* for normal conditions.
- During an *abnormal* power-up sequencing and requested voltage changes, PGOOD status could change to *inactive* or *de-asserted* after an 800-µs gated time period if any output voltage is outside of regulation range.
- Using the *gated mode of operation* could allow the PGOOD signal to initiate an immediate power shutdown sequence if the PGOOD signal is wired-OR with signal connected to EN input. This type of circuit configuration provides a smart PORz function for processor that eliminates the need for additional components to generate PORz upon start-up and to monitor voltage levels of key voltage domains.

The fault sets corresponding fault bit 1 in PG_FAULT register. The detected fault must be cleared to continue the PGOOD monitoring. The overvoltage and thermal shutdown are cleared by writing 1 to the OVP_INT and TDIE_SD_INT interrupt bits in INT_TOP_1 register. The regulator fault is cleared by writing 1 to the corresponding register bit in PG_FAULT register. The interrupts can be also cleared with VANA UVLO by toggling the input supply. An example of PGOOD pin operation in gated mode is shown in Figure 11.

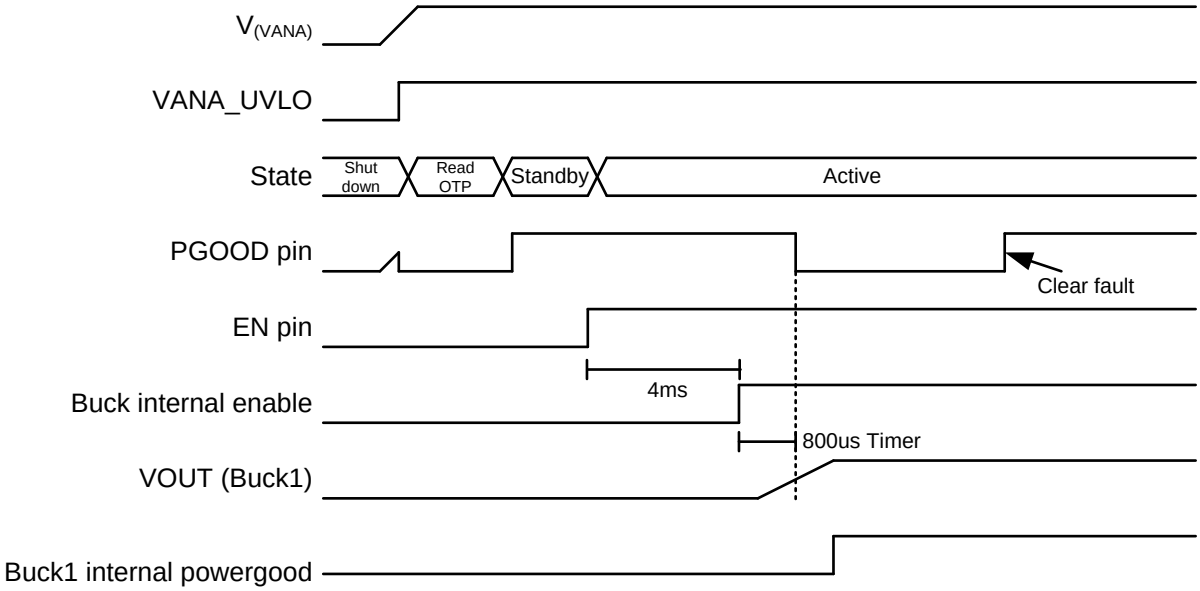

Figure 11. PGOOD Pin Operation in Gated Mode

7.3.7.1.2 PGOOD Pin Continuous Mode

The continuous (or *unvalid*) mode of operation is selected by setting PGOOD_MODE bit to 1 in PGOOD_CTRL_2 register.

For the continuous mode of operation, PGOOD behaves as follows:

- PGOOD is set to *active* or *asserted* state upon exiting OTP configuration.

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- PGOOD is set to *inactive* or *de-asserted* as soon as regulator is enabled.
- PGOOD status begins indicating output voltage regulation status immediately and continuously.
- During power-up sequencing and requested voltage changes, PGOOD will toggle between *inactive* or *de-asserted* while output voltages are outside of regulation ranges and *active* or *asserted* when inside of regulation ranges.

The PG_FAULT register bits are latched and maintain the fault information until host clears the fault bit by writing 1 to the bit. The PGOOD signal indicates also a thermal shutdown and input overvoltage interrupts, which are cleared by clearing the interrupt bits.

When regulator voltage is transitioning from one target voltage to another, the PGOOD signal is set inactive.

When the PGOOD signal becomes inactive, the source for the fault can be read from PG_FAULT register. If the invalid output voltage becomes valid again the PGOOD signal becomes active. Thus the PGOOD signal shows all the time if the monitored output voltages are valid. The block diagram for this operation is shown in Figure 12 and an example of operation is shown in Figure 13.

The PGOOD signal can be also configured so that it maintains inactive state even when the monitored outputs are valid but there are PG_FAULT_x bits in PG_FAULT register pending clearance. This type of operation is selected by setting PGFAULT_GATES_PGOOD bit to 1 in PGOOD_CTRL_2 register.

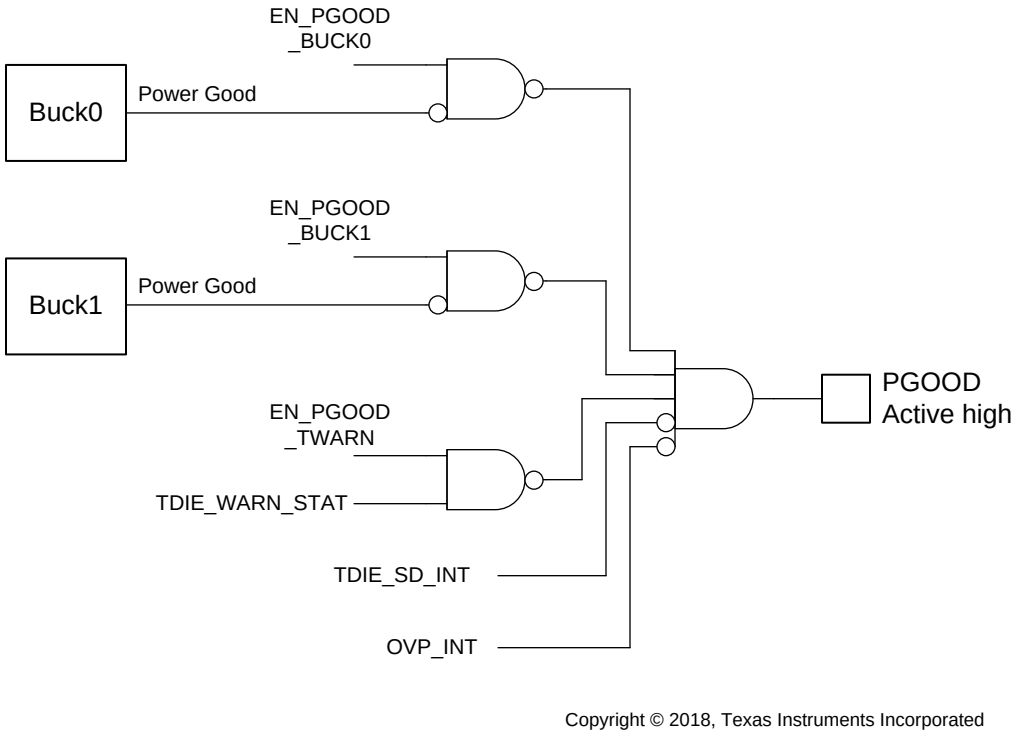

Figure 12. PGOOD Block Diagram (Continuous Mode)

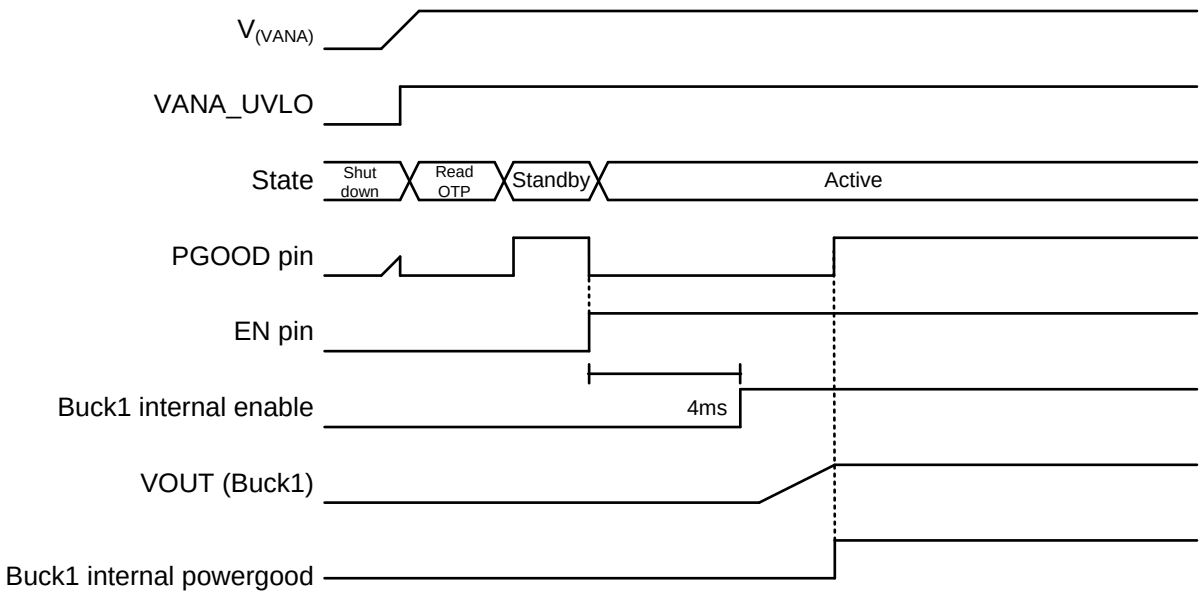

Figure 13. PGOOD Pin Operation in Continuous Mode

7.3.7.2 Warnings for Diagnosis (Interrupt)

7.3.7.2.1 Output Power Limit

The Buck regulators have programmable output peak current limits. The limits are individually programmed for both regulators with BUCKx_ILIM[2:0] bits in BUCKx_CTRL_2 register. If the load current is increased so that the current limit is triggered, the regulator continues to regulate to the limit current level (peak current regulation). The voltage may decrease if the load current is higher than limit current. If the current regulation continues for 20 µs, the TPS65653-Q1 device sets the BUCKx_ILIM_INT bit in INT_BUCK register and pulls the nINT pin low. The host processor can read BUCKx_ILIM_STAT bits in BUCK_STAT register to see if the regulator is still in peak current regulation mode and the interrupt is cleared by writing 1 to BUCKx_ILIM_INT bit. The current limit interrupt can be masked by setting BUCKx_ILIM_MASK bit in BUCK_MASK register to 1. The Buck overload situation is shown in Figure 14.

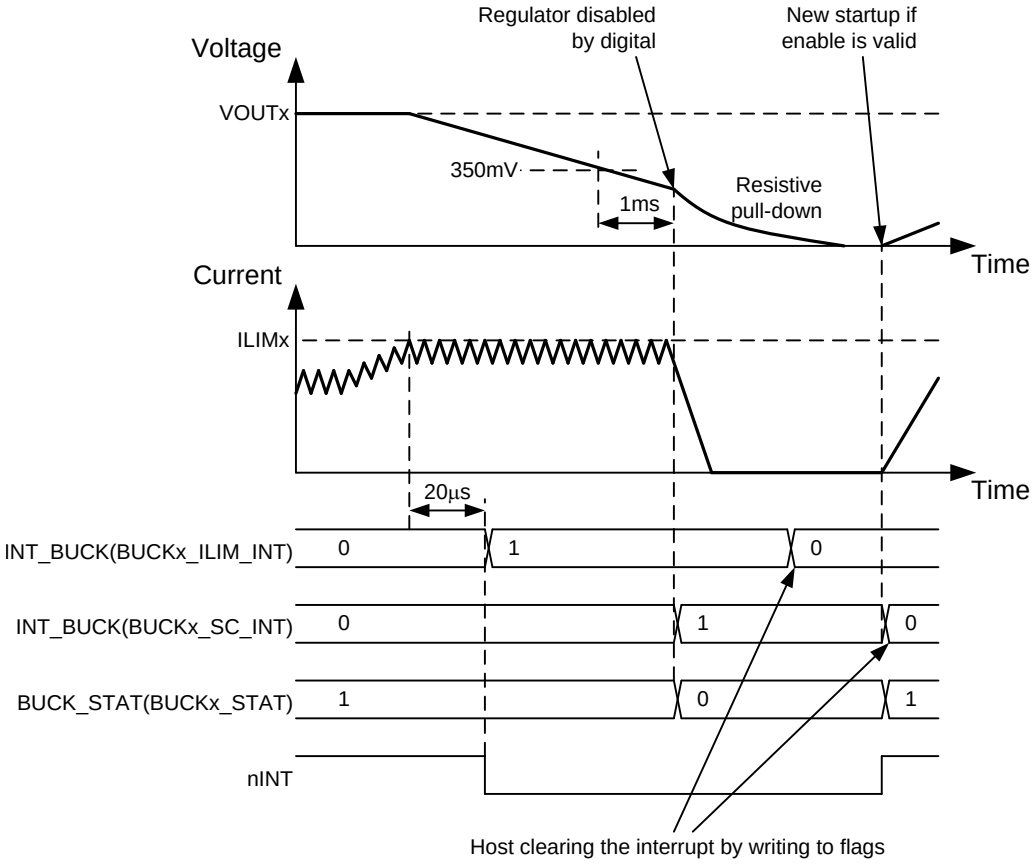

Figure 14. Buck Regulator Overload Situation

7.3.7.2.2 Thermal Warning

The TPS65653-Q1 device includes a protection feature against overtemperature by setting an interrupt for host processor. The threshold level of the thermal warning is selected with TDIE_WARN_LEVEL bit in CONFIG register.

If the TPS65653-Q1 device temperature increases above thermal warning level the device sets TDIE_WARN_INT bit in INT_TOP_1 register and pulls the nINT pin low. The status of the thermal warning can be read from TDIE_WARN_STAT bit in TOP_STAT register, and the interrupt is cleared by writing 1 to TDIE_WARN_INT bit. The thermal warning interrupt can be masked by setting TDIE_WARN_MASK bit in TOP_MASK_1 register to 1.

7.3.7.3 Protection (Regulator Disable)

If the regulator is disabled because of protection or fault (short-circuit protection, overload protection, thermal shutdown, input overvoltage protection, or UVLO), the output power FETs are set to high-impedance mode, and the output pulldown resistor is enabled (if enabled with BUCKx_RDIS_EN bit in BUCKx_CTRL_1 register). The turnoff time of the output voltage is defined by the output capacitance, load current, and the resistance of the integrated pull-down resistor. The pulldown resistors are active as long as VANA voltage is above approximately a 1.2-V level.

7.3.7.3.1 Short-Circuit and Overload Protection

A short-circuit protection feature allows the TPS65653-Q1 to protect itself and external components against short circuit at the output or against overload during start-up. For buck regulators the fault thresholds are about 350 mV, and the protection is triggered and the regulator is disabled if the output voltage is below the threshold level 1 ms after the regulator is enabled.

In a similar way the overload situation is protected during normal operation. If the output voltage falls below 0.35 V and 0.3 V and remains below the threshold level for 1 ms the regulator is disabled.

In buck regulator short-circuit and overload situations the BUCKx_SC_INT bit in INT_BUCK register and the INT_BUCKx bit in INT_TOP_1 register are set to 1, the BUCKx_STAT bit in BUCK_STAT register is set to 0, and the nINT signal is pulled low. The host processor clears the interrupt by writing 1 to the BUCKx_SC_INT bit. Upon clearing the interrupt the regulator makes a new start-up attempt if the regulator is in an enabled state.

7.3.7.3.2 Overvoltage Protection

The TPS65653-Q1 device monitors the input voltage from the VANA pin in standby and active operation modes. If the input voltage rises above $VANA_{OVP}$ voltage level, all the regulators are disabled immediately (without switching ramp, no shutdown delays), pulldown resistors discharge the output voltages if they are enabled (BUCKx_RDIS_EN = 1 in BUCKx_CTRL_1 register), GPOs are set to logic low level, nINT signal is pulled low, OVP_INT bit in INT_TOP_1 register is set to 1, and BUCKx_STAT bit in BUCK_STAT register is set to 0. The host processor clears the interrupt by writing 1 to the OVP_INT bit. If the input voltage is above overvoltage detection level the interrupt is not cleared. The host can read the status of the overvoltage from the OVP_STAT bit in TOP_STAT register. Regulators cannot be enabled as long as the input voltage is above overvoltage detection level or the overvoltage interrupt is pending.

7.3.7.3.3 Thermal Shutdown

The TPS65653-Q1 has an overtemperature protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the regulators are disabled immediately (without switching ramp, no shutdown delays), the TDIE_SD_INT bit in INT_TOP_1 register is set to 1, the nINT signal is pulled low, and the device enters STANDBY. nINT is cleared by writing 1 to the TDIE_SD_INT bit. If the temperature is above thermal shutdown level the interrupt is not cleared. The host can read the status of the thermal shutdown from the TDIE_SD_STAT bit in TOP_STAT register. Regulators cannot be enabled as long as the junction temperature is above thermal shutdown level or the thermal shutdown interrupt is pending.

7.3.7.4 Fault (Power Down)

7.3.7.4.1 Undervoltage Lockout

When the input voltage falls below $VANA_{UVLO}$ at the VANA pin, the buck regulators are disabled immediately (without switching ramp, no shutdown delays), and the output capacitor is discharged using the pulldown resistor, and the TPS65653-Q1 device enters SHUTDOWN. When $V_{(VANA)}$ voltage is above $VANA_{UVLO}$ threshold level, the device powers up to STANDBY state.

If the reset interrupt is unmasked by default (OTP bit for RESET_REG_MASK is 0 in TOP_MASK_2 register) the RESET_REG_INT interrupt bit in INT_TOP_2 register indicates that the device has been in SHUTDOWN. The host processor must clear the interrupt by writing 1 to the RESET_REG_INT bit. If the host processor reads the RESET_REG_INT interrupt bit after detecting an nINT low signal, it knows that the input supply voltage has been below $VANA_{UVLO}$ level (or the host has requested reset with SW_RESET bit in RESET register), and the registers are reset to default values.

7.3.8 Operation of the GPO Signals

The TPS65653-Q1 device supports up to 2 general purpose output signals, GPO and GPO2. The GPO2 signal is multiplexed with CLKIN signal. The selection between CLKIN and GPO2 pin function is set with CLKIN_PIN_SEL bit in CONFIG register.

The GPO pins are configured with the following bits:

- GPOx_OD bit in GPO_CTRL register defines the type of the output, either push-pull with $V_{(VANA)}$ level or open drain

The logic level of the GPOx pin is set by EN_GPOx bit in GPO_CTRL register.

The control of the GPOs can be included to start-up and shutdown sequences. The GPO control for a sequence with EN pin is selected by GPOx_EN_PIN_CTRL bit in GPO_CTRL register. For start-up and shutdown sequence control see *Enable and Disable Sequences*.

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7.3.9 Digital Signal Filtering

The digital signals have a debounce filtering. The signal or supply is sampled with a clock signal and a counter. This results as an accuracy of one clock period for the debounce window.

Table 5. Digital Signal Filtering

EVENT	SIGNAL/SUPPLY	RISING EDGE LENGTH	FALLING EDGE LENGTH
Enable/disable for BUCKx or GPOx	EN	3 µs(1)	3 µs(1)
VANA UVLO	VANA	3 µs(1) (VANA voltage rising)	Immediate (VANA voltage falling)
VANA overvoltage	VANA	1 µs (VANA voltage rising)	20 µs (VANA voltage falling)
Thermal warning	TDIE_WARN_INT	20 µs	20 µs
Thermal shutdown	TDIE_SD_INT	20 µs	20 µs
Current limit	VOUTx_ILIM	20 µs	20 µs
Overload	FB_B0, FB_B1	1 ms	N/V
PGOOD pin and power-good interrupt	PGOOD / FB_B0, FB_B1	6 µs	6 µs

(1) No glitch filtering, only synchronization.

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7.4 Device Functional Modes

7.4.1 Modes of Operation

SHUTDOWN: The $V_{(VANA)}$ voltage is below $VANA_{UVLO}$ threshold level. All switch, reference, control, and bias circuitry of the TPS65653-Q1 device are turned off.

READ OTP: The main supply voltage $V_{(VANA)}$ is above $VANA_{UVLO}$ level. The regulators are disabled, and the reference and bias circuitry of the TPS65653-Q1 are enabled. The OTP bits are loaded to registers.

STANDBY: The main supply voltage $V_{(VANA)}$ is above $VANA_{UVLO}$ level. The regulators are disabled, and the reference, control and bias circuitry of the TPS65653-Q1 are enabled. All registers can be read or written by the host processor via the system serial interface. The regulators can be enabled if needed.

ACTIVE: The main supply voltage $V_{(VANA)}$ is above $VANA_{UVLO}$ level. At least one regulator is enabled. All registers can be read or written by the host processor via the system serial interface.

The operating modes and transitions between the modes are shown in Figure 15.

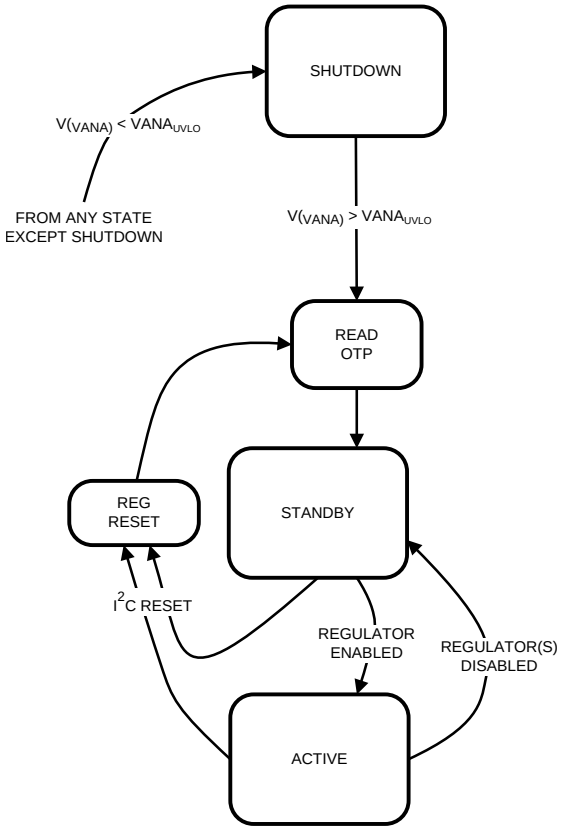

Figure 15. Device Operation Modes

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7.5 Programming

7.5.1 I²C-Compatible Interface

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed on the line and remain HIGH even when the bus is idle. The TPS65653-Q1 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz).

7.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

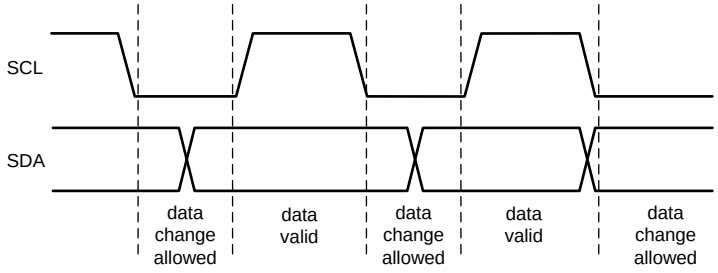

Figure 16. Data Validity Diagram

7.5.1.2 Start and Stop Conditions

The TPS65653-Q1 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as SDA transitions from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transition from LOW to HIGH while SCL is HIGH. The I²C master always generates the START and STOP conditions.

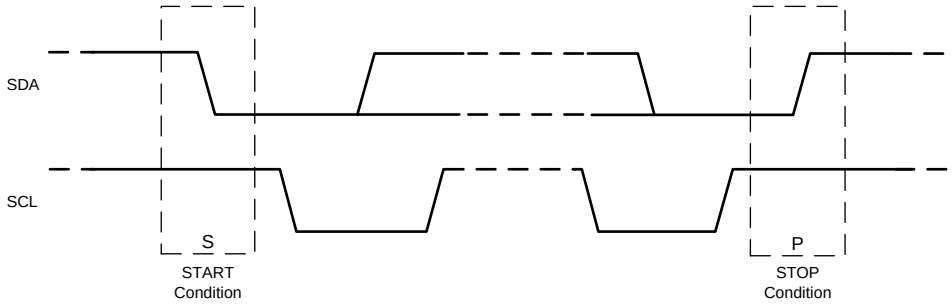

Figure 17. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW. Figure 18 shows the SDA and SCL signal timing for the I²C-compatible bus. See the Figure 1 for timing values.

Programming (continued)

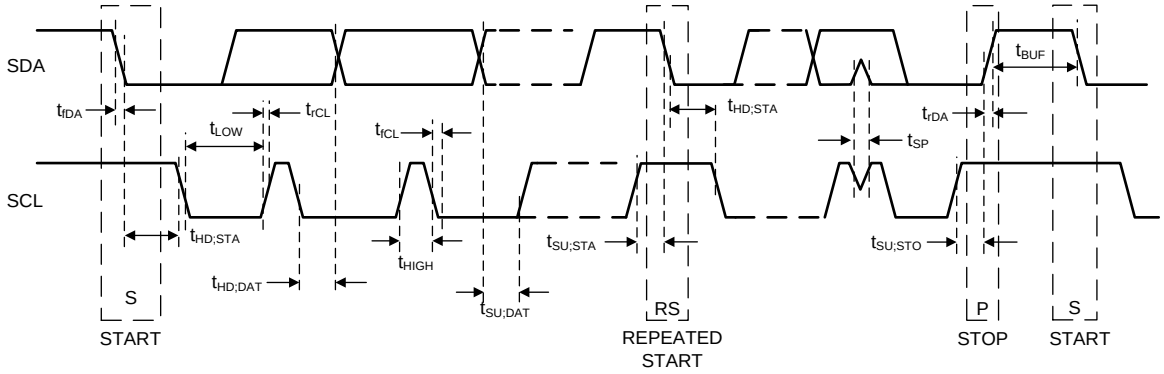

Figure 18. I²C-Compatible Timing

7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The TPS65653-Q1 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The TPS65653-Q1 generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the slave. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

NOTE

If the $V_{(VANA)}$ voltage is below $VANA_{UVLO}$ threshold level during I²C communication the TPS65653-Q1 device does not drive SDA line. The ACK signal and data transfer to the master is disabled at that time.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE, and a 1 indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

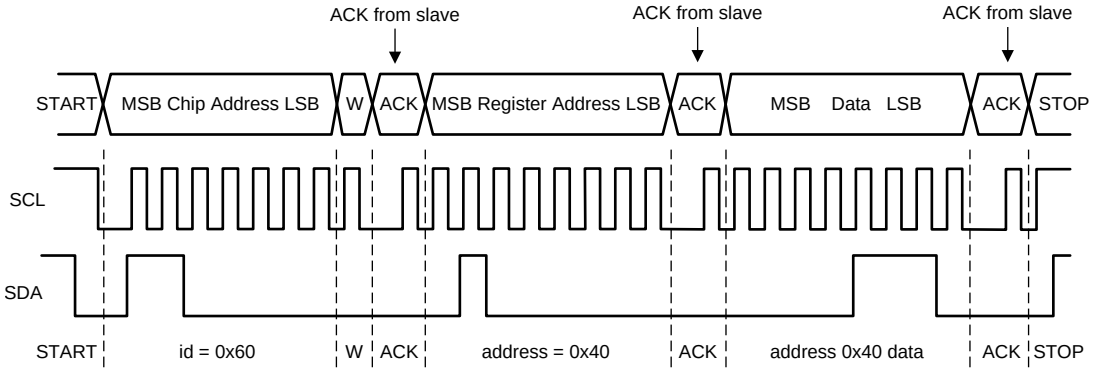

Figure 19. Write Cycle (w = write; SDA = 0). Example Device Address = 0x60

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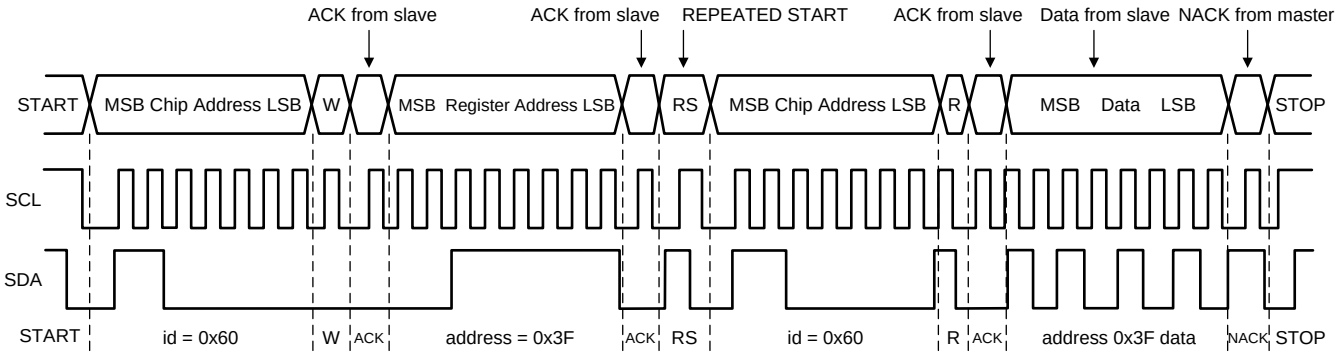
Programming (continued)



When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

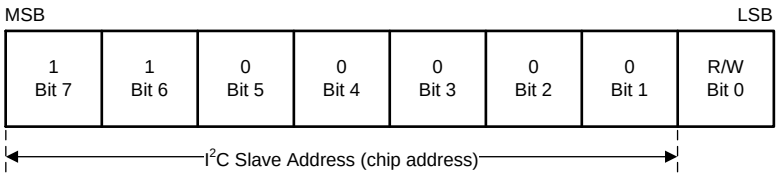
Figure 20. Read Cycle (r = read; SDA = 1). Example Device Address = 0x60

7.5.1.4 I^2C-Compatible Chip Address

NOTE

The device address for the TPS65653-Q1 is 0x61.

After the START condition, the I^2C master sends the 7-bit address followed by an eighth bit, read or write (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data is written. The third byte contains the data for the selected register.



Here in an example with device address of 1100000Bin = 60Hex.

Figure 21. Device Address Example

7.5.1.5 Auto-Increment Feature

The auto-increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the TPS65653-Q1, the internal address index counter is incremented by one and the next register is written. Table 6 shows writing sequence to two consecutive registers. Note that auto-increment feature does not work for read.

Table 6. Auto-Increment Example

MASTER ACTION	START	DEVICE ADDRESS = 0x61	WRITE		REGISTER ADDRESS		DATA		DATA		STOP
TPS65653-Q1				ACK		ACK		ACK		ACK	

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7.6 Register Maps

7.6.1 Register Descriptions

The TPS65653-Q1 is controlled by a set of registers through the I²C-compatible interface. The device registers, their addresses and their abbreviations are listed in Table 7. A more detailed description is given in the *DEV_REV* to I_LOAD_1 sections.

An "X" indicates register bits which are updated from OTP memory during READ OTP state.

Table 7. Summary of TPS65653-Q1 Control Registers

Addr	Register	Read / Write	D7	D6	D5	D4	D3	D2	D1	D0
0x00	DEV_REV	R	DEVICE_ID[1:0]		Reserved					
0x01	OTP_REV	R	OTP_ID[7:0]							
0x02	BUCK0_CTRL_1	R/W	Reserved				BUCK0_FPWM	BUCK0_RDIS_EN	BUCK0_EN_PIN_CTRL	BUCK0_EN
0x03	BUCK0_CTRL_2	R/W	Reserved		BUCK0_ILIM[2:0]			BUCK0_SLEW_RATE[2:0]		
0x04	BUCK1_CTRL_1	R/W	Reserved				BUCK1_FPWM	BUCK1_RDIS_EN	BUCK1_EN_PIN_CTRL	BUCK1_EN
0x05	BUCK1_CTRL_2	R/W	Reserved		BUCK1_ILIM[2:0]			BUCK1_SLEW_RATE[2:0]		
0x06	BUCK0_VOUT	R/W	BUCK0_VSET[7:0]							
0x07	BUCK1_VOUT	R/W	BUCK1_VSET[7:0]							
0x0C	BUCK0_DELAY	R/W	BUCK0_SHUTDOWN_DELAY[3:0]				BUCK0_STARTUP_DELAY[3:0]			
0x0D	BUCK1_DELAY	R/W	BUCK1_SHUTDOWN_DELAY[3:0]				BUCK1_STARTUP_DELAY[3:0]			
0x10	GPO_DELAY	R/W	GPO_SHUTDOWN_DELAY[3:0]				GPO_STARTUP_DELAY[3:0]			
0x11	GPO2_DELAY	R/W	GPO2_SHUTDOWN_DELAY[3:0]				GPO2_STARTUP_DELAY[3:0]			
0x12	GPO_CTRL	R/W	Reserved	GPO2_OD	GPO2_EN_PIN_CTRL	GPO2_EN	Reserved	GPO_OD	GPO_EN_PIN_CTRL	GPO_EN
0x13	CONFIG	R/W	Reserved	STARTUP_DELAY_SEL	SHUTDOWN_DELAY_SEL	CLKIN_PIN_SEL	CLKIN_PD	EN_PD	TDIE_WARN_LEVEL	EN_SPREAD_SPEC
0x14	PLL_CTRL	R/W	Reserved	EN_PLL	Reserved	EXT_CLK_FREQ[4:0]				
0x15	PGOOD_CTRL_1	R/W	PGOOD_POL	PGOOD_OD	Reserved	PGOOD_WINDOW_BUCK	Reserved		EN_PGOOD_BUCK1	EN_PGOOD_BUCK0
0x16	PGOOD_CTRL_2	R/W	Reserved					EN_PGOOD_TWARN	PG_FAULT_GATES_PGOOD	PGOOD_MODE
0x17	PG_FAULT	R	Reserved						PG_FAULT_BUCK1	PG_FAULT_BUCK0
0x18	RESET	R/W	Reserved							SW_RESET
0x19	INT_TOP_1	R/W	PGOOD_INT	Reserved	INT_BUCK	SYNC_CLK_INT	TDIE_SD_INT	TDIE_WARN_INT	OVP_INT	I_MEAS_INT
0x1A	INT_TOP_2	R/W	Reserved							RESET_REG_INT
0x1B	INT_BUCK	R/W	Reserved	BUCK1_PG_INT	BUCK1_SC_INT	BUCK1_ILIM_INT	Reserved	BUCK0_PG_INT	BUCK0_SC_INT	BUCK0_ILIM_INT
0x1D	TOP_STAT	R	PGOOD_STAT	Reserved		SYNC_CLK_STAT	TDIE_SD_STAT	TDIE_WARN_STAT	OVP_STAT	Reserved
0x1E	BUCK_STAT	R	BUCK1_STAT	BUCK1_PG_STAT	Reserved	BUCK1_ILIM_STAT	BUCK0_STAT	BUCK0_PG_STAT	Reserved	BUCK0_ILIM_STAT

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Register Maps (continued)

Table 7. Summary of TPS65653-Q1 Control Registers (continued)

Addr	Register	Read / Write	D7	D6	D5	D4	D3	D2	D1	D0
0x20	TOP_ MASK_1	R/W	PGOOD_ INT_MASK	Reserved		SYNC_CLK _MASK	Reserved	TDIE_WAR N_MASK	Reserved	I_MEAS_ MASK
0x21	TOP_ MASK_2	R/W	Reserved							RESET_ REG_MASK
0x22	BUCK_MAS K	R/W	BUCK1_PG F_MASK	BUCK1_PG R_MASK	Reserved	BUCK1_ ILIM_ MASK	BUCK0_PG F_MASK	BUCK0_PG R_MASK	Reserved	BUCK0_ ILIM_ MASK
0x24	SEL_I_ LOAD	R/W	Reserved							LOAD_CUR RENT_ BUCK_SEL ECT
0x25	I_LOAD_2	R	Reserved							BUCK_LOA D_CURREN T[8]
0x26	I_LOAD_1	R	BUCK_LOAD_CURRENT[7:0]							

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7.6.1.1 DEV_REV

Address: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
DEVICE_ID[1:0]		Reserved					

Bits	Field	Type	Default	Description
7:6	DEVICE_ID[1:0]	R	X	Device specific ID code.
5:0	Reserved	R	00 0010	

7.6.1.2 OTP_REV

Address: 0x01

D7	D6	D5	D4	D3	D2	D1	D0
OTP_ID[7:0]							

Bits	Field	Type	Default	Description
7:0	OTP_ID[7:0]	R	X	Identification Code of the OTP EPROM Version.

7.6.1.3 BUCK0_CTRL_1

Address: 0x02

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				BUCK0_FPWM	BUCK0_RDIS_EN	BUCK0_EN_PIN_CTRL	BUCK0_EN

Bits	Field	Type	Default	Description
7:4	Reserved	R/W	0000	
3	BUCK0_FPWM	R/W	X	Buck0 mode selection: 0 - Automatic transitions between PFM and PWM modes (AUTO mode) 1 - Forced to PWM operation.
2	BUCK0_RDIS_EN	R/W	1	Enable output discharge resistor (R_{DIS_Bx}) when Buck0 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled.
1	BUCK0_EN_PIN_CTRL	R/W	X	Enable control for Buck0: 0 - only BUCK0_EN bit controls Buck0 1 - BUCK0_EN bit AND EN pin control Buck0.
0	BUCK0_EN	R/W	X	Enable Buck0 regulator: 0 - Buck0 regulator is disabled 1 - Buck0 regulator is enabled.

7.6.1.4 BUCK0_CTRL_2

Address: 0x03

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			BUCK0_ILIM[2:0]			BUCK0_SLEW_RATE[2:0]	

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Bits	Field	Type	Default	Description
7:6	Reserved	R/W	00	
5:3	BUCK0_ILIM[2:0]	R/W	X	Sets the switch current limit of Buck0. Can be programmed at any time during operation: 0x0 - 1.5 A 0x1 - 2.0 A 0x2 - 2.5 A 0x3 - 3.0 A 0x4 - 3.5 A 0x5 - 4.0 A 0x6 - Reserved 0x7 - Reserved
2:0	BUCK0_SLEW_RATE[2:0]	R/W	X	Sets the output voltage slew rate for Buck0 regulator (rising and falling edges): 0x0 - Reserved 0x1 - Reserved 0x2 - 10 mV/µs 0x3 - 7.5 mV/µs 0x4 - 3.8 mV/µs 0x5 - 1.9 mV/µs 0x6 - 0.94 mV/µs 0x7 - 0.47 mV/µs

7.6.1.5 BUCK1_CTRL_1

Address: 0x04

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				BUCK1_FPWM	BUCK1_RDIS_EN	BUCK1_EN_PIN_CTRL	BUCK1_EN

Bits	Field	Type	Default	Description
7:4	Reserved	R/W	0000	
3	BUCK1_FPWM	R/W	X	Buck1 mode selection: 0 - Automatic transitions between PFM and PWM modes (AUTO mode) 1 - Forced to PWM operation.
2	BUCK1_RDIS_EN	R/W	1	Enable output discharge resistor (R_{DIS_Bx}) when Buck1 is disabled: 0 - Discharge resistor disabled 1 - Discharge resistor enabled.
1	BUCK1_EN_PIN_CTRL	R/W	X	Enable control for Buck1: 0 - only BUCK1_EN bit controls Buck1 1 - BUCK1_EN bit AND EN pin control Buck1.
0	BUCK1_EN	R/W	X	Enable Buck1 regulator: 0 - Buck1 regulator is disabled 1 - Buck1 regulator is enabled.

7.6.1.6 BUCK1_CTRL_2

Address: 0x05

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			BUCK1_ILIM[2:0]			BUCK1_SLEW_RATE[2:0]	

Bits	Field	Type	Default	Description
7:6	Reserved	R/W	00	
5:3	BUCK1_ILIM[2:0]	R/W	X	Sets the switch current limit of Buck1. Can be programmed at any time during operation: 0x0 - 1.5 A 0x1 - 2.0 A 0x2 - 2.5 A 0x3 - 3.0 A 0x4 - 3.5 A 0x5 - 4.0 A 0x6 - Reserved 0x7 - Reserved
2:0	BUCK1_SLEW_RATE[2:0]	R/W	X	Sets the output voltage slew rate for Buck1 regulator (rising and falling edges): 0x0 - Reserved 0x1 - Reserved 0x2 - 10 mV/µs 0x3 - 7.5 mV/µs 0x4 - 3.8 mV/µs 0x5 - 1.9 mV/µs 0x6 - 0.94 mV/µs 0x7 - 0.47 mV/µs

7.6.1.7 BUCK0_VOUT

Address: 0x06

D7	D6	D5	D4	D3	D2	D1	D0
BUCK0_VSET[7:0]							

Bits	Field	Type	Default	Description
7:0	BUCK0_VSET[7:0]	R/W	X	Sets the output voltage of Buck0 regulator **Reserved, DO NOT USE** 0x00 ... 0x4C **1 V - 1.4 V, 5 mV steps** 0x4C - 1 V ... 0x9D - 1.4 V **1.4 V - 3.36 V, 20 mV steps** 0x9E - 1.42 V ... 0xFF - 3.36 V

7.6.1.8 BUCK1_VOUT

Address: 0x07

D7	D6	D5	D4	D3	D2	D1	D0
BUCK1_VSET[7:0]							

Bits	Field	Type	Default	Description
7:0	BUCK1_VSET[7:0]	R/W	X	Sets the output voltage of Buck1 regulator **Reserved, DO NOT USE** 0x00 ... 0x4C **1 V - 1.4 V, 5 mV steps** 0x4C - 1 V ... 0x9D - 1.4 V **1.4 V - 3.36 V, 20 mV steps** 0x9E - 1.42 V ... 0xFF - 3.36 V

7.6.1.9 BUCK0_DELAY

Address: 0x0C

D7	D6	D5	D4	D3	D2	D1	D0
BUCK0_SHUTDOWN_DELAY[3:0]				BUCK0_STARTUP_DELAY[3:0]			

Bits	Field	Type	Default	Description
7:4	BUCK0_ SHUTDOWN_ DELAY[3:0]	R/W	X	Shutdown delay of Buck0 from falling edge of EN signal: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register) ... 0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register)
3:0	BUCK0_ STARTUP_ DELAY[3:0]	R/W	X	Startup delay of Buck0 from rising edge of EN signal: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in CONFIG register) ... 0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in CONFIG register)

7.6.1.10 BUCK1_DELAY

Address: 0x0D

D7	D6	D5	D4	D3	D2	D1	D0
BUCK1_SHUTDOWN_DELAY[3:0]				BUCK1_STARTUP_DELAY[3:0]			

Bits	Field	Type	Default	Description
7:4	BUCK1_ SHUTDOWN_ DELAY[3:0]	R/W	X	Shutdown delay of Buck1 from falling edge of EN signal: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register) ... 0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register)
3:0	BUCK1_ STARTUP_ DELAY[3:0]	R/W	X	Startup delay of Buck1 from rising edge of EN signal: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in CONFIG register) ... 0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in CONFIG register)

7.6.1.11 GPO_DELAY

Address: 0x10

D7	D6	D5	D4	D3	D2	D1	D0
GPO_SHUTDOWN_DELAY[3:0]				GPO_STARTUP_DELAY[3:0]			

Bits	Field	Type	Default	Description
7:4	GPO_ SHUTDOWN_ DELAY[3:0]	R/W	X	Delay for GPO falling edge from falling edge of EN signal: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register) ... 0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register)
3:0	GPO_ STARTUP_ DELAY[3:0]	R/W	X	Delay for GPO rising edge from rising edge of EN signal: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in CONFIG register) ... 0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in CONFIG register)

7.6.1.12 GPO2_DELAY

Address: 0x11

D7	D6	D5	D4	D3	D2	D1	D0
GPO2_SHUTDOWN_DELAY[3:0]				GPO2_STARTUP_DELAY[3:0]			

Bits	Field	Type	Default	Description
7:4	GPO2_ SHUTDOWN_ DELAY[3:0]	R/W	X	Delay for GPO2 falling edge from falling edge of EN signal: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register) ... 0xF - 7.5 ms (15 ms if SHUTDOWN_DELAY_SEL=1 in CONFIG register)
3:0	GPO2_ STARTUP_ DELAY[3:0]	R/W	X	Delay for GPO2 rising edge from rising edge of EN signal: 0x0 - 0 ms 0x1 - 0.5 ms (1 ms if STARTUP_DELAY_SEL=1 in CONFIG register) ... 0xF - 7.5 ms (15 ms if STARTUP_DELAY_SEL=1 in CONFIG register)

7.6.1.13 GPO_CTRL

Address: 0x12

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	GPO2_OD	GPO2_EN_PIN _CTRL	GPO2_EN	Reserved	GPO_OD	GPO_EN_PIN_ CTRL	GPO_EN

Bits	Field	Type	Default	Description
7	Reserved	R	0	
6	GP02_OD	R/W	X	GPO2 signal type when configured as General Purpose Output (CLKIN pin): 0 - Push-pull output (VANA level) 1 - Open-drain output
5	GPO2_EN_PIN_C TRL	R/W	X	Control for GPO2: 0 - Only GPO2_EN bit controls GPO2 1 - GPO2_EN bit AND EN pin control GPO2.
4	GPO2_EN	R/W	X	Output level of GPO2 signal (when configured as General Purpose Output): 0 - Logic low level 1 - Logic high level
3	Reserved	R	0	
2	GPO_OD	R/W	X	GPO signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output
1	GPO_EN_PIN_CT RL	R/W	X	Control for GPO: 0 - Only GPO_EN bit controls GPO 1 - GPO_EN bit AND EN pin control GPO.
0	GPO_EN	R/W	X	Output level of GPO signal: 0 - Logic low level 1 - Logic high level

7.6.1.14 CONFIG

Address: 0x13

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	STARTUP_DE LAY_SEL	SHUTDOWN_ DELAY_SEL	CLKIN_PIN_SE L	CLKIN_PD	EN2_PD	TDIE_WARN_ LEVEL	EN_SPREAD _SPEC

Bits	Field	Type	Default	Description
7	Reserved	R/W	0	
6	STARTUP_DELAY _SEL	R/W	X	Startup delay range from EN signals. 0 - 0 ms - 7.5 ms with 0.5 ms steps 1 - 0 ms - 15 ms with 1 ms steps
5	SHUTDOWN_DEL AY_SEL	R/W	X	Shutdown delay range from EN signals. 0 - 0 ms - 7.5 ms with 0.5 ms steps 1 - 0 ms - 15 ms with 1 ms steps
4	CLKIN_PIN_SEL	R/W	X	CLKIN pin function: 0 - GPO2 1 - CLKIN

PRODUCT PREVIEW

Bits	Field	Type	Default	Description
3	CLKIN_PD	R/W	X	Selects the pull down resistor on the CLKIN input pin. (valid also when selected as GPO2) 0 - Pull-down resistor is disabled. 1 - Pull-down resistor is enabled.
2	EN_PD	R/W	X	Selects the pull down resistor on the EN input pin. 0 - Pull-down resistor is disabled. 1 - Pull-down resistor is enabled.
1	TDIE_WARN_ LEVEL	R/W	X	Thermal warning threshold level. 0 - 125°C 1 - 137°C.
0	EN_SPREAD _SPEC	R/W	X	Enable spread spectrum feature: 0 - Disabled 1 - Enabled

7.6.1.15 PLL_CTRL

Address: 0x14

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	EN_PLL	Reserved	EXT_CLK_FREQ[4:0]				

Bits	Field	Type	Default	Description
7	Reserved	R/W	0	
6	EN_PLL	R/W	X	Selection of external clock and PLL operation: 0 - Forced to internal RC oscillator. PLL disabled. 1 - PLL is enabled in STANDBY and ACTIVE modes. Automatic external clock use when available, interrupt generated if external clock appears or disappears.
5	Reserved	R/W	0	**This bit must be set to '0'.**
4:0	EXT_CLK_FREQ[4 :0]	R/W	X	Frequency of the external clock (CLKIN): 0x00 - 1 MHz 0x01 - 2 MHz 0x02 - 3 MHz ... 0x16 - 23 MHz 0x17 - 24 MHz 0x18...0x1F - Reserved See electrical specification for input clock frequency tolerance.

7.6.1.16 PGOOD_CTRL_1

Address: 0x15

D7	D6	D5	D4	D3	D2	D1	D0
PGOOD_POL	PGOOD_OD	Reserved	PGOOD_ WINDOW_BUC K	Reserved		EN_PGOOD_B UCK1	EN_PGOOD_B UCK0

Bits	Field	Type	Default	Description
7	PGOOD_POL	R/W	X	PGOOD signal polarity. 0 - PGOOD signal high when monitored outputs are valid 1 - PGOOD signal low when monitored outputs are valid
6	PGOOD_OD	R/W	X	PGOOD signal type: 0 - Push-pull output (VANA level) 1 - Open-drain output
5	Reserved	R/W	0	
4	PGOOD_ WINDOW_BUCK	R/W	X	Buck Output voltage monitoring method for PGOOD signal: 0 - Only undervoltage monitoring 1 - Overvoltage and undervoltage monitoring.
3:2	Reserved	R/W	00	

PRODUCT PREVIEW

Bits	Field	Type	Default	Description
1	EN_PGOOD_BUCK1	R/W	X	PGOOD signal source control from Buck1 0 - Buck1 is not monitored 1 - Buck1 Power-Good threshold voltage monitored
0	EN_PGOOD_BUCK0	R/W	X	PGOOD signal source control from Buck0 0 - Buck0 is not monitored 1 - Buck0 Power-Good threshold voltage monitored

7.6.1.17 PGOOD_CTRL_2

Address: 0x16

D7	D6	D5	D4	D3	D2	D1	D0
Reserved					EN_PGOOD_TWARN	PG_FAULT_GATES_PGOOD	PGOOD_MODE

Bits	Field	Type	Default	Description
7:3	Reserved	R/W	0 0000	
2	EN_PGOOD_TWARN	R/W	X	Thermal warning control for PGOOD signal: 0 - Thermal warning not monitored 1 - PGOOD inactive if thermal warning flag is active.
1	PG_FAULT_GATES_PGOOD	R/W	X	Type of operation for PGOOD signal: 0 - Indicates live status of monitored voltage outputs. 1 - Indicates status of PG_FAULT register, inactive when at least one PG_FAULT_x bit is inactive.
0	PGOOD_MODE	R/W	X	Operating mode for PGOOD signal: 0 - Gated mode 1 - Continuous mode

7.6.1.18 PG_FAULT

Address: 0x17

D7	D6	D5	D4	D3	D2	D1	D0
Reserved						PG_FAULT_BUCK1	PG_FAULT_BUCK0

Bits	Field	Type	Default	Description
7:2	Reserved	R/W	00 0000	
1	PG_FAULT_BUCK1	R/W	0	Source for PGOOD inactive signal: 0 - Buck1 has not set PGOOD signal inactive. 1 - Buck1 is selected for PGOOD signal and it has set PGOOD signal inactive. This bit can be cleared by writing '1' to this bit when Buck1 output is valid.
0	PG_FAULT_BUCK0	R/W	0	Source for PGOOD inactive signal: 0 - Buck0 has not set PGOOD signal inactive. 1 - Buck0 is selected for PGOOD signal and it has set PGOOD signal inactive. This bit can be cleared by writing '1' to this bit when Buck0 output is valid.

7.6.1.19 RESET

Address: 0x18

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							SW_RESET

Bits	Field	Type	Default	Description
7:1	Reserved	R/W	000 0000	
0	SW_RESET	R/W	0	Software commanded reset. When written to 1, the registers will be reset to default values, OTP memory is read, and the I^2C interface is reset. The bit is automatically cleared.

7.6.1.20 INT_TOP_1

Address: 0x19

D7	D6	D5	D4	D3	D2	D1	D0
PGOOD_INT	Reserved	BUCK_INT	SYNC_CLK_INT	TDIE_SD_INT	TDIE_WARN_INT	OVP_INT	I_MEAS_INT

Bits	Field	Type	Default	Description
7	PGOOD_INT	R/W	0	Latched status bit indicating that the PGOOD pin has changed from active to inactive. Write 1 to clear interrupt.
6	Reserved	R	0	
5	BUCK_INT	R	0	Interrupt indicating that Buck1 and/or Buck0 have a pending interrupt. The reason for the interrupt is indicated in INT_BUCK register. This bit is cleared automatically when INT_BUCK register is cleared to 0x00.
4	SYNC_CLK_INT	R/W	0	Latched status bit indicating that the external clock has appeared or disappeared. Write 1 to clear interrupt.
3	TDIE_SD_INT	R/W	0	Latched status bit indicating that the die junction temperature has exceeded the thermal shutdown level. The regulators have been disabled if they were enabled and GPO and GPO2 signals are driven low. The regulators cannot be enabled if this bit is active. The actual status of the thermal shutdown is indicated by TDIE_SD_STAT bit in TOP_STAT register. Write 1 to clear interrupt.
2	TDIE_WARN_INT	R/W	0	Latched status bit indicating that the die junction temperature has exceeded the thermal warning level. The actual status of the thermal warning is indicated by TDIE_WARN_STAT bit in TOP_STAT register. Write 1 to clear interrupt.
1	OVP_INT	R/W	0	Latched status bit indicating that the input voltage has exceeded the over-voltage detection level. The regulators have been disabled if they were enabled and GPO and GPO2 signals are driven low. The actual status of the over-voltage is indicated by OVP_STAT bit in TOP_STAT register. Write 1 to clear interrupt.
0	I_MEAS_INT	R/W	0	Latched status bit indicating that the load current measurement result is available in I_LOAD_1 and I_LOAD_2 registers. Write 1 to clear interrupt.

7.6.1.21 INT_TOP_2

Address: 0x1A

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							RESET_REG_INT

Bits	Field	Type	Default	Description
7:1	Reserved	R/W	000 0000	
0	RESET_REG_INT	R/W	0	Latched status bit indicating that either VANA supply voltage has been below undervoltage threshold level or the host has requested a reset using SW_RESET bit in RESET register. The regulators have been disabled, and registers are reset to default values and the normal startup procedure is done. Write 1 to clear interrupt.

7.6.1.22 INT_BUCK

Address: 0x1B

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	BUCK1_PG_INT	BUCK1_SC_INT	BUCK1_ILIM_INT	Reserved	BUCK0_PG_INT	BUCK0_SC_INT	BUCK0_ILIM_INT

Bits	Field	Type	Default	Description
7	Reserved	R/W	0	
6	BUCK1_PG_INT	R/W	0	Latched status bit indicating that Buck1 Power-Good event has been detected. Write 1 to clear.
5	BUCK1_SC_INT	R/W	0	Latched status bit indicating that the Buck1 output voltage has been over 1 ms below short-circuit threshold level. Write 1 to clear.
4	BUCK1_ILIM_INT	R/W	0	Latched status bit indicating that the Buck1 output current limit has been active. Write 1 to clear.
3	Reserved	R/W	0	
2	BUCK0_PG_INT	R/W	0	Latched status bit indicating that Buck0 Power-Good event has been detected. Write 1 to clear.
1	BUCK0_SC_INT	R/W	0	Latched status bit indicating that the Buck0 output voltage has been over 1 ms below short-circuit threshold level. Write 1 to clear.
0	BUCK0_ILIM_INT	R/W	0	Latched status bit indicating that the Buck0 output current limit has been active. Write 1 to clear.

7.6.1.23 TOP_STAT

Address: 0x1D

D7	D6	D5	D4	D3	D2	D1	D0
PGOOD_STAT	Reserved		SYNC_CLK_STAT	TDIE_SD_STAT	TDIE_WARN_STAT	OVP_STAT	Reserved

Bits	Field	Type	Default	Description
7	PGOOD_STAT	R	0	Status bit indicating the status of PGOOD pin: 0 - PGOOD pin is inactive 1 - PGOOD pin is active
6:5	Reserved	R	00	
4	SYNC_CLK_STAT	R	0	Status bit indicating the status of external clock (CLKIN): 0 - External clock frequency is valid 1 - External clock frequency is not valid.
3	TDIE_SD_STAT	R	0	Status bit indicating the status of thermal shutdown: 0 - Die temperature below thermal shutdown level 1 - Die temperature above thermal shutdown level.
2	TDIE_WARN_STAT	R	0	Status bit indicating the status of thermal warning: 0 - Die temperature below thermal warning level 1 - Die temperature above thermal warning level.
1	OVP_STAT	R	0	Status bit indicating the status of input overvoltage monitoring: 0 - Input voltage below overvoltage threshold level 1 - Input voltage above overvoltage threshold level.
0	Reserved	R	0	

7.6.1.24 BUCK_STAT

Address: 0x1E

D7	D6	D5	D4	D3	D2	D1	D0
BUCK1_STAT	BUCK1_PG_STAT	Reserved	BUCK1_ILIM_STAT	BUCK0_STAT	BUCK0_PG_STAT	Reserved	BUCK0_ILIM_STAT

Bits	Field	Type	Default	Description
7	BUCK1_STAT	R	0	Status bit indicating the enable/disable status of Buck1: 0 - Buck1 regulator is disabled 1 - Buck1 regulator is enabled.
6	BUCK1_PG_STAT	R	0	Status bit indicating Buck1 output voltage validity (raw status) 0 - Buck1 output voltage is valid. 1 - Buck1 output voltage is invalid.

Bits	Field	Type	Default	Description
5	Reserved	R	0	
4	BUCK1_ILIM _STAT	R	0	Status bit indicating Buck1 current limit status (raw status) 0 - Buck1 output current is below current limit level 1 - Buck1 output current limit is active.
3	BUCK0_STAT	R	0	Status bit indicating the enable/disable status of Buck0: 0 - Buck0 regulator is disabled 1 - Buck0 regulator is enabled.
2	BUCK0_PG_STAT	R	0	Status bit indicating Buck0 output voltage validity (raw status) 0 - Buck0 output voltage is valid. 1 - Buck0 output voltage is invalid.
1	Reserved	R	0	
0	BUCK0_ILIM _STAT	R	0	Status bit indicating Buck0 current limit status (raw status) 0 - Buck0 output current is below current limit level 1 - Buck0 output current limit is active.

7.6.1.25 TOP_MASK_1

Address: 0x20

D7	D6	D5	D4	D3	D2	D1	D0
PGOOD_INT_ MASK	Reserved		SYNC_CLK _MASK	Reserved	TDIE_WARN _MASK	Reserved	I_LOAD_ READY_MASK

Bits	Field	Type	Default	Description
7	PGOOD_INT _MASK	R/W	X	Masking for Power-Good interrupt (PGOOD_INT in INT_TOP_1 register): 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect PGOOD_STAT status bit in TOP_STAT register.
6:5	Reserved	R/W	00	
4	SYNC_CLK _MASK	R/W	X	Masking for external clock detection interrupt (SYNC_CLK_INT in INT_TOP_1 register): 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect SYNC_CLK_STAT status bit in TOP_STAT register.
3	Reserved	R/W	0	
2	TDIE_WARN _MASK	R/W	X	Masking for thermal warning interrupt (TDIE_WARN_INT in INT_TOP_1 register): 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect TDIE_WARN_STAT status bit in TOP_STAT register.
1	Reserved	R/W	0	
0	I_MEAS _MASK	R/W	X	Masking for load current measurement ready interrupt (MEAS_INT in INT_TOP_1 register). 0 - Interrupt generated 1 - Interrupt not generated.

7.6.1.26 TOP_MASK_2

Address: 0x21

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							RESET_REG _MASK

Bits	Field	Type	Default	Description
7:1	Reserved	R/W	000 0000	
0	RESET_REG _MASK	R/W	X	Masking for register reset interrupt (RESET_REG_INT in INT_TOP_2 register): 0 - Interrupt generated 1 - Interrupt not generated. This change of this bit by I^2C writing has no effect because it will be read from OTP memory during reset.

7.6.1.27 BUCK_MASK

Address: 0x22

D7	D6	D5	D4	D3	D2	D1	D0
BUCK1_PGF_MASK	BUCK1_PGR_MASK	Reserved	BUCK1_ILIM_MASK	BUCK0_PGF_MASK	BUCK0_PGR_MASK	Reserved	BUCK0_ILIM_MASK

Bits	Field	Type	Default	Description
7	BUCK1_PGF_MASK	R/W	X	Masking of Power Good invalid detection for Buck1 power good interrupt (BUCK1_PG_INT in INT_BUCK register): 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK1_PG_STAT status bit in BUCK_STAT register.
6	BUCK1_PGR_MASK	R/W	X	Masking of Power Good valid detection for Buck1 Power Good interrupt (BUCK1_PG_INT in INT_BUCK register): 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK1_PG_STAT status bit in BUCK_STAT register.
5	Reserved	R	0	
4	BUCK1_ILIM_MASK	R/W	X	Masking for Buck1 current limit detection interrupt (BUCK1_ILIM_INT in INT_BUCK register): 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK1_ILIM_STAT status bit in BUCK_STAT register.
3	BUCK0_PGF_MASK	R/W	X	Masking of Power Good invalid detection for Buck0 power good interrupt (BUCK0_PG_INT in INT_BUCK register): 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STAT register.
2	BUCK0_PGR_MASK	R/W	X	Masking of Power Good valid detection for Buck0 power good interrupt (BUCK0_PG_INT in INT_BUCK register): 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK0_PG_STAT status bit in BUCK_STAT register.
1	Reserved	R	0	
0	BUCK0_ILIM_MASK	R/W	X	Masking for Buck0 current limit detection interrupt (BUCK0_ILIM_INT in INT_BUCK register): 0 - Interrupt generated 1 - Interrupt not generated. This bit does not affect BUCK0_ILIM_STAT status bit in BUCK_STAT register.

7.6.1.28 SEL_I_LOAD

Address: 0x24

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							LOAD_CURRENT_BUCK_SELECT

Bits	Field	Type	Default	Description
7:1	Reserved	R/W	000 0000	
0	LOAD_CURRENT_BUCK_SELECT	R/W	0	Start the current measurement on the selected regulator: 0 - Buck0 1 - Buck1 The measurement is started when register is written.

7.6.1.29 I_LOAD_2

Address: 0x25

D7	D6	D5	D4	D3	D2	D1	D0
Reserved							BUCK_LOAD_CURRENT[8]

PRODUCT PREVIEW

Bits	Field	Type	Default	Description
7:1	Reserved	R	000 0000	
0	BUCK_LOAD_ CURRENT[8]	R	0	This register describes the MSB bit of the average load current on selected regulator with a resolution of 20 mA per LSB and maximum 10.22-A current.

7.6.1.30 I_LOAD_1

Address: 0x26

D7	D6	D5	D4	D3	D2	D1	D0
BUCK_LOAD_CURRENT[7:0]							

Bits	Field	Type	Default	Description
7:0	BUCK_LOAD_ CURRENT[7:0]	R	0000 0000	This register describes 8 LSB bits of the average load current on selected regulator with a resolution of 20 mA per LSB and maximum 10.22-A current.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65653-Q1 is a power management unit including two step-down regulators and two general-purpose digital output signals.

8.2 Typical Application

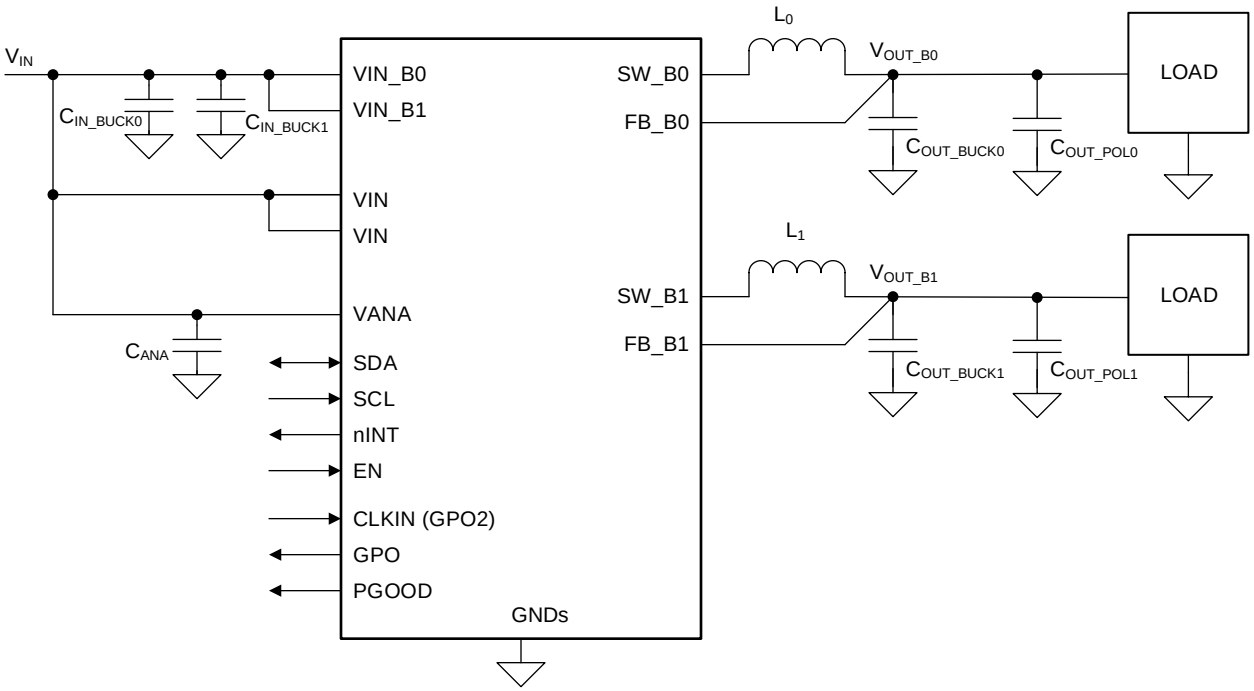


Figure 22. TPS65653-Q1 Typical Application

8.2.1 Design Requirements

8.2.1.1 Inductor Selection

The inductors L_0 and L_1 are shown in the *Typical Application*. The inductance and DCR of the inductor affects the control loop of the buck regulator. TI recommends using inductors similar to those listed in Table 8. Pay attention to the saturation current and temperature rise current of the inductor. Check that the saturation current is higher than the peak current limit and the temperature rise current is higher than the maximum expected rms output current. For the minimum effective inductance to ensure good performance at maximum peak output current over the operating temperature range refer to Electrical Characteristics. DC resistance of the inductor must be less than 0.05 Ω for good efficiency at high-current condition. The inductor AC loss also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle load. Shielded inductors are preferred as they radiate less noise.

Typical Application (continued)

Table 8. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	DIMENSIONS L × W × H (mm)	RATED DC CURRENT I_{SAT} maximum (typical) / I_{TEMP} maximum (typical) (A)	DCR typical / maximum (mΩ)
Murata	DFE252012PD-R47M	0.47 µH (20%)	2.5 × 2 × 1.2	5.2 (–) / 4 (–)(1)	— / 27
Tayo Yuden	MDMK2020TR47MMV	0.47 µH (20%)	2 × 2 ×1.2	4.2 (4.8) / 2.3 (2.45)	40 / 46

(1) Operating temperature range is up to 125°C including self temperature rise.

8.2.1.2 Buck Input Capacitor Selection

The input capacitors C_{IN_BUCK0} and C_{IN_BUCK1} are shown in the *Typical Application*. A ceramic input bypass capacitor of 10 µF is required for each phase of the regulator. Place the input capacitor as close as possible to the VIN_Bx pin and PGND_Bx pin of the device. A larger value or higher voltage rating improves the input voltage filtering. Use X7R type of capacitors, not Y5V or F. Also the DC bias characteristics capacitors must be considered. Minimum effective input capacitance to ensure good performance is 1.9 µF per buck input at maximum input voltage including tolerances, ambient temperature range and aging. This is assuming that there are at least 22 µF of additional capacitance common for all the power input pins on the system power rail. See Table 9.

The input filter capacitor supplies current to the high-side FET switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating. In addition ferrite can be used in front of the input capacitor to reduce the EMI.

Table 9. Recommended Buck Input Capacitor (X7R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L × W × H (mm)	VOLTAGE RATING
Murata	GCM21BR71A106KE22	10 µF (10%)	0805	2 × 1.25 × 1.25	10 V

8.2.1.3 Buck Output Capacitor Selection

The output capacitor C_{OUT_BUCK0} and C_{OUT_BUCK1} are shown in *Typical Application*. A ceramic local output capacitor of 22 µF is required per buck. Use ceramic capacitors, X7R type; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. Minimum effective output capacitance to ensure good performance is 10 µF per buck including the DC voltage rolloff, tolerances, aging, and temperature effects.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR}. The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part. See Table 10.

POL capacitors can be used to improve load transient performance and to decrease the ripple voltage. A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreases the PFM switching frequency. However, output capacitance higher than 100 µF per buck is not necessarily of any benefit. Note that the output capacitor may be the limiting factor in the output voltage ramp, see Specifications for maximum output capacitance for different slew-rate settings. For large output capacitors, the output voltage might be slower than the programmed ramp rate at voltage transitions, because of the higher energy stored on the output capacitance. Also at start-up, the time required to charge the output capacitor to target value might be longer. At shutdown the output voltage is discharged to 0.6 V level using forced-PWM operation. This can increase the input voltage if the load current is small and the output capacitor is large compared to input capacitor. Below 0.6 V level the output capacitor is discharged by the internal discharge resistor and with large capacitor more time is required to settle V_{OUT} down as a consequence of the increased time constant.

Table 10. Recommended Buck Output Capacitors (X7R Dielectric)

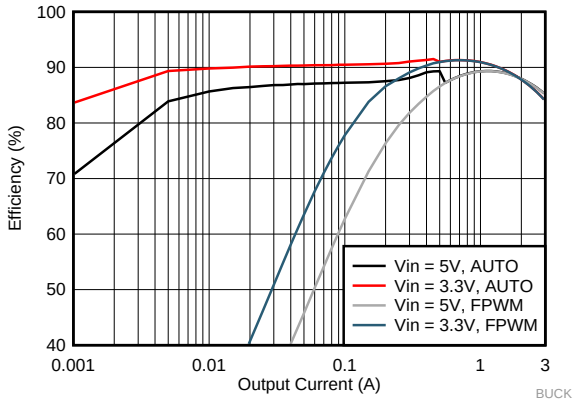
MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS L × W × H (mm)	VOLTAGE RATING
Murata	GCM31CR71A226KE02	22 µF (10%)	1206	3.2 × 1.6 × 1.6	10 V

8.2.2 Detailed Design Procedure

The performance of the TPS65653-Q1 device depends greatly on the care taken in designing the printed circuit board (PCB). The use of low-inductance and low serial-resistance ceramic capacitors is strongly recommended, while proper grounding is crucial. Attention must be given to decoupling the power supplies. Decoupling capacitors must be connected close to the device and between the power and ground pins to support high peak currents being drawn from system power rail during turnon of the switching MOSFETs. Keep input and output traces as short as possible, because trace inductance, resistance, and capacitance can easily become the performance limiting items. The separate buck regulator power pins VIN_Bx are not connected together internally. Connect the VIN_Bx power connections together outside the package using power plane construction.

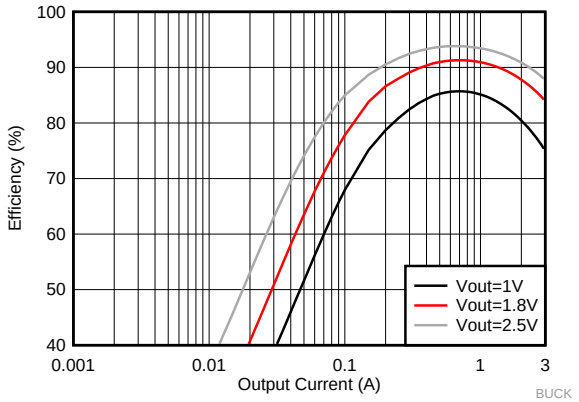
8.2.3 Application Curves

Measurements are done using typical application set up with connections shown in Figure 22. Graphs may not reflect the OTP default settings. Unless otherwise specified: $V_{(VIN\_Bx)} = V_{(VANA)} = 3.7$ V, $V_{OUT\_Bx} = 1$ V, $T_A = 25°C$, L = 0.47 µH (Murata DFE252012PD-R47M), $C_{OUT\_BUCK} = 22$ µF, and $C_{POL\_BUCK} = 22$ µF.



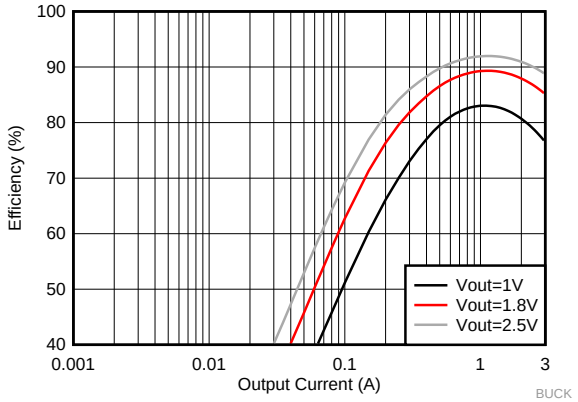
V_{OUT} = 1.8 V

Figure 23. Buck Efficiency in PFM/PWM and Forced PWM Mode



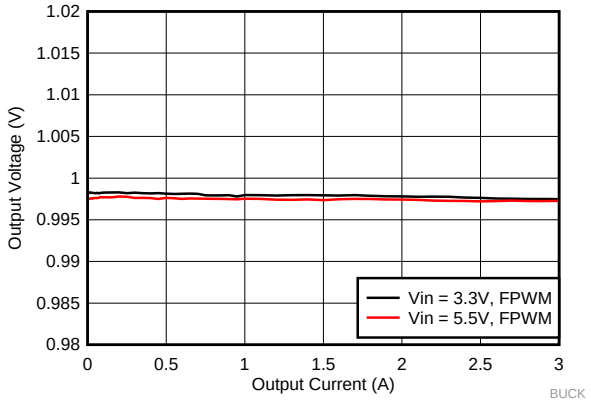
V_{IN} = 3.3 V

Figure 24. Buck Efficiency in Forced PWM Mode



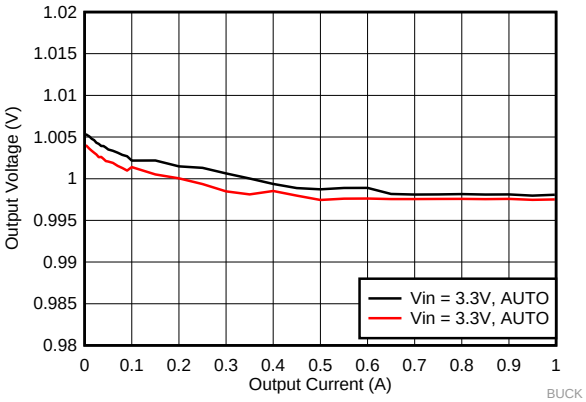
V_{IN} = 5 V

Figure 25. Buck Efficiency in Forced PWM Mode



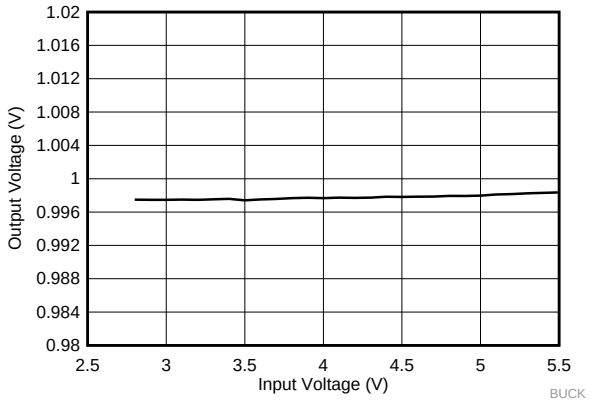
V_{OUT} = 1 V

Figure 26. Buck Output Voltage vs Load Current in Forced PWM Mode



V_{OUT} = 1 V

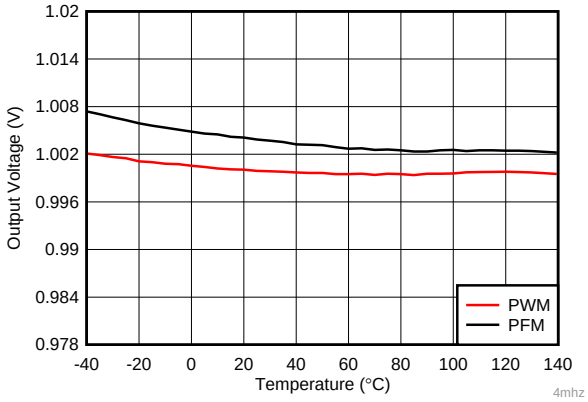
Figure 27. Buck Output Voltage vs Load Current in PFM/PWM Mode



V_{OUT} = 1 V Load = 1 A

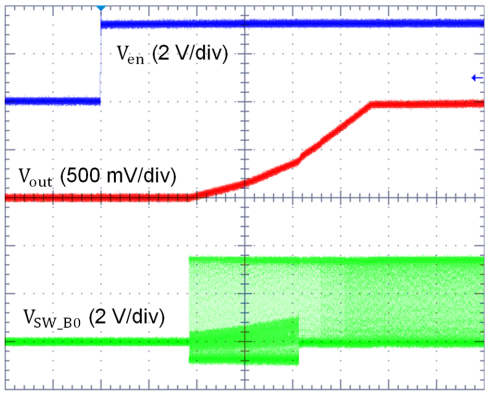
Figure 28. Buck Output Voltage vs Input Voltage in PWM Mode

PRODUCT PREVIEW



Load = 1 A (PWM) and 0.1 A (PFM)

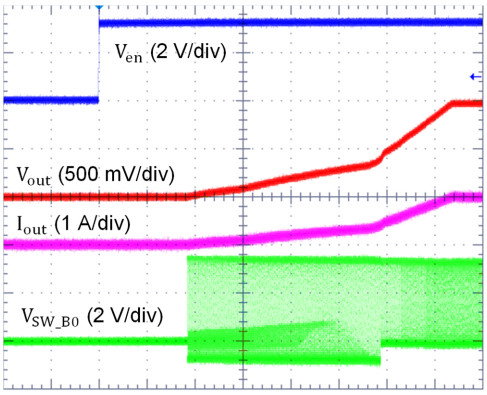
Figure 29. Buck Output Voltage vs Temperature



Time (40 µs/div)

Slew-rate = 10 mV/µs I_{LOAD} = 0 A V_{OUT} = 1 V

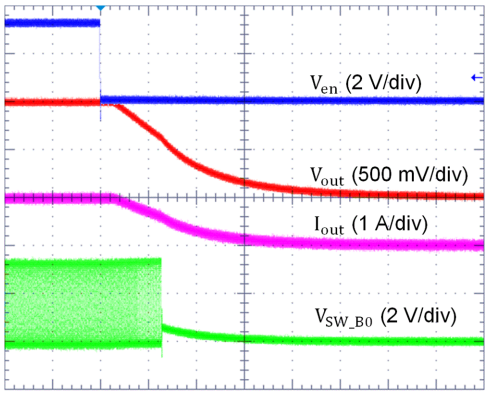
Figure 30. Buck Start-Up With EN1, Forced PWM Mode



Time (40 µs/div)

Slew-rate = 10 mV/µs R_{LOAD} = 1 Ω V_{OUT} = 1 V

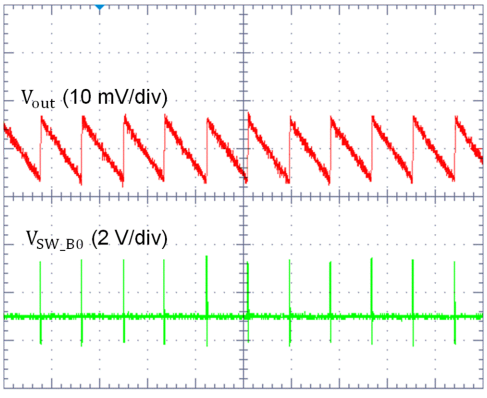
Figure 31. Buck Start-Up with EN1, Forced PWM Mode



Time (40 µs/div)

Slew-rate = 10 mV/µs R_{LOAD} = 1 Ω V_{OUT} = 1 V

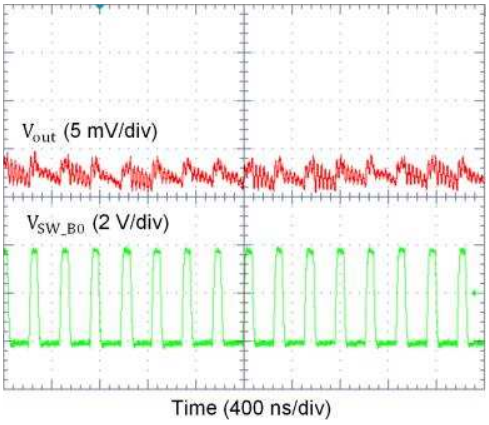
Figure 32. Buck Shutdown With EN1, Forced PWM Mode



Time (40 µs/div)

I_{OUT} = 10 mA

Figure 33. Buck Output Voltage Ripple, PFM Mode



Time (400 ns/div)

I_{OUT} = 500 mA

Figure 34. Buck Output Voltage Ripple, Forced PWM Mode

PRODUCT PREVIEW

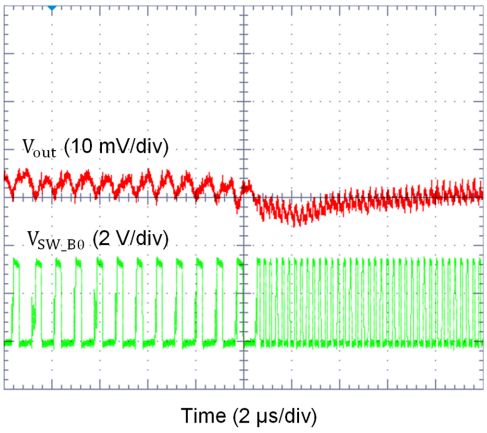


Figure 35. Buck Transient From PFM-to-PWM Mode

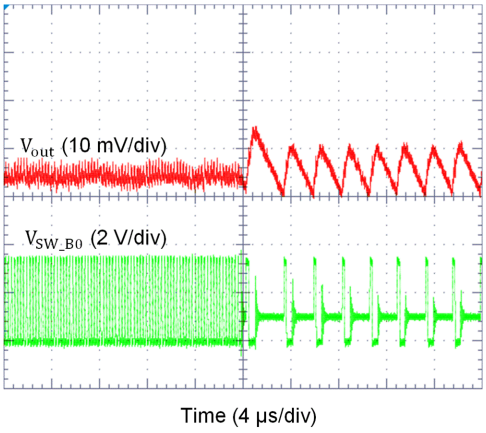
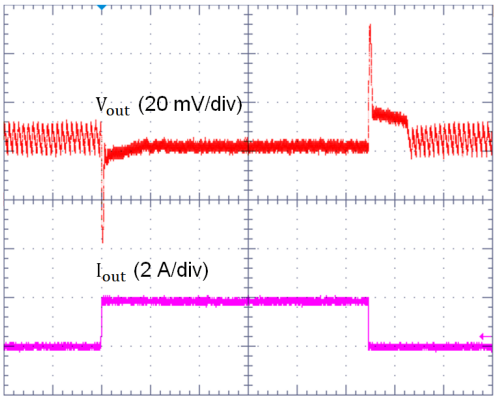
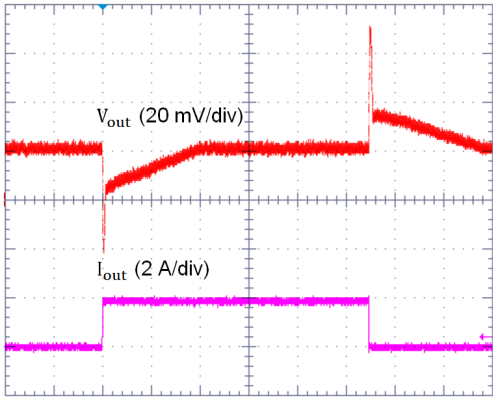


Figure 36. Buck Transient From PWM-to-PFM Mode



I_{OUT} = 0.1 A → 2 A → 0.1 A $T_R = T_F$ = 400 ns

Figure 37. Buck Transient Load Step Response, AUTO Mode



I_{OUT} = 0.1 A → 2 A → 0.1 A $T_R = T_F$ = 400 ns

Figure 38. Buck Transient Load Step Response, Forced PWM Mode

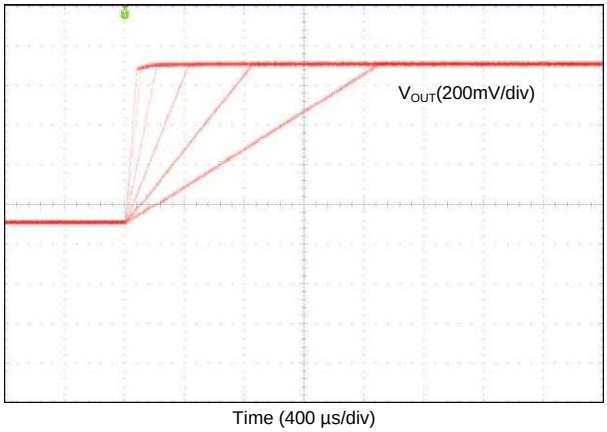


Figure 39. Buck V_{OUT} Transition from 0.6 V to 1.4 V With Different Slew Rate Settings

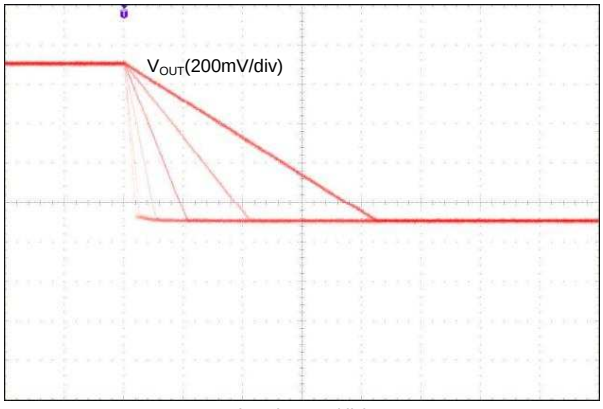


Figure 40. Buck V_{OUT} Transition from 1.4 V to 0.6 V With Different Slew Rate Settings

PRODUCT PREVIEW

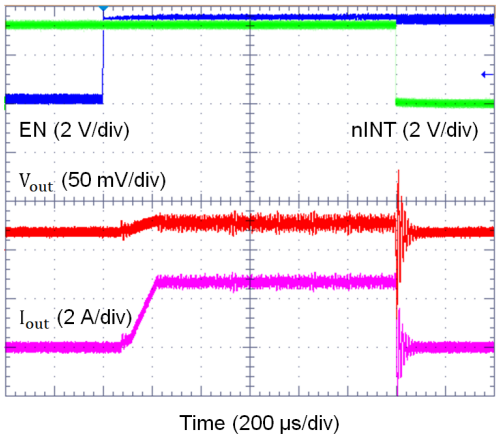


Figure 41. Buck Start-up With Short on Output

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.8 V and 5.5 V. The VANA input and VIN_Bx buck inputs must be connected together, and they must use the same input supply. This input supply must be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail must be low enough that the input current transient does not cause too high a drop in the TPS65653-Q1 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the TPS65653-Q1 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The high frequency and large switching currents of the TPS65653-Q1 make the choice of layout important. Good power supply results only occur when care is given to proper design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to several amps, good power supply layout is much more difficult than most general PCB design. Use the following steps as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

1. Place C_{IN} as close as possible to the VIN_Bx pin and the PGND_Bx pin. Route the V_{IN} trace wide and thick to avoid IR drops. The trace between the positive node of the input capacitor and the VIN_Bx pin(s) of TPS65653-Q1, as well as the trace between the negative node of the input capacitor and power PGND_Bx pin(s), must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor — parasitic inductance on these traces must be kept as small as possible for proper device operation. The parasitic inductance can be reduced by using a ground plane as close as possible to top layer by using thin dielectric layer between top layer and ground plane.
2. The output filter, consisting of L and COUT, converts the switching signal at SW_Bx to the noiseless output voltage. It must be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Route the traces between the output capacitors of the TPS65653-Q1 and the input capacitors of the load direct and wide to avoid losses due to the IR drop.
3. Input for analog blocks (VANA and AGND) must be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close as possible to the VANA pin.
4. If remote voltage sensing can be used for the load, connect the TPS65653-Q1 feedback pins FB_Bx to the respective sense pins on the load capacitor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND_Bx, VIN_Bx, and SW_Bx, as well as high bandwidth signals such as

PRODUCT PREVIEW

Layout Guidelines (continued)

the I^2C. Avoid both capacitive and inductive coupling by keeping the sense lines short and direct, and close to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. If series resistors are used for load current measurement, place them after connection of the voltage feedback.

5. PGND_Bx, VIN_Bx and SW_Bx must be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND_Bx, VIN_Bx and SW_Bx.

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient ($R_{\theta JA}$) and junction-to-board ($R_{\theta JB}$) thermal resistances, thereby reducing the device junction temperature, T_J. TI strongly recommends performance of a careful system-level 2D or full 3D dynamic thermal analysis at the beginning product design process by using a thermal modeling analysis software.

10.2 Layout Example

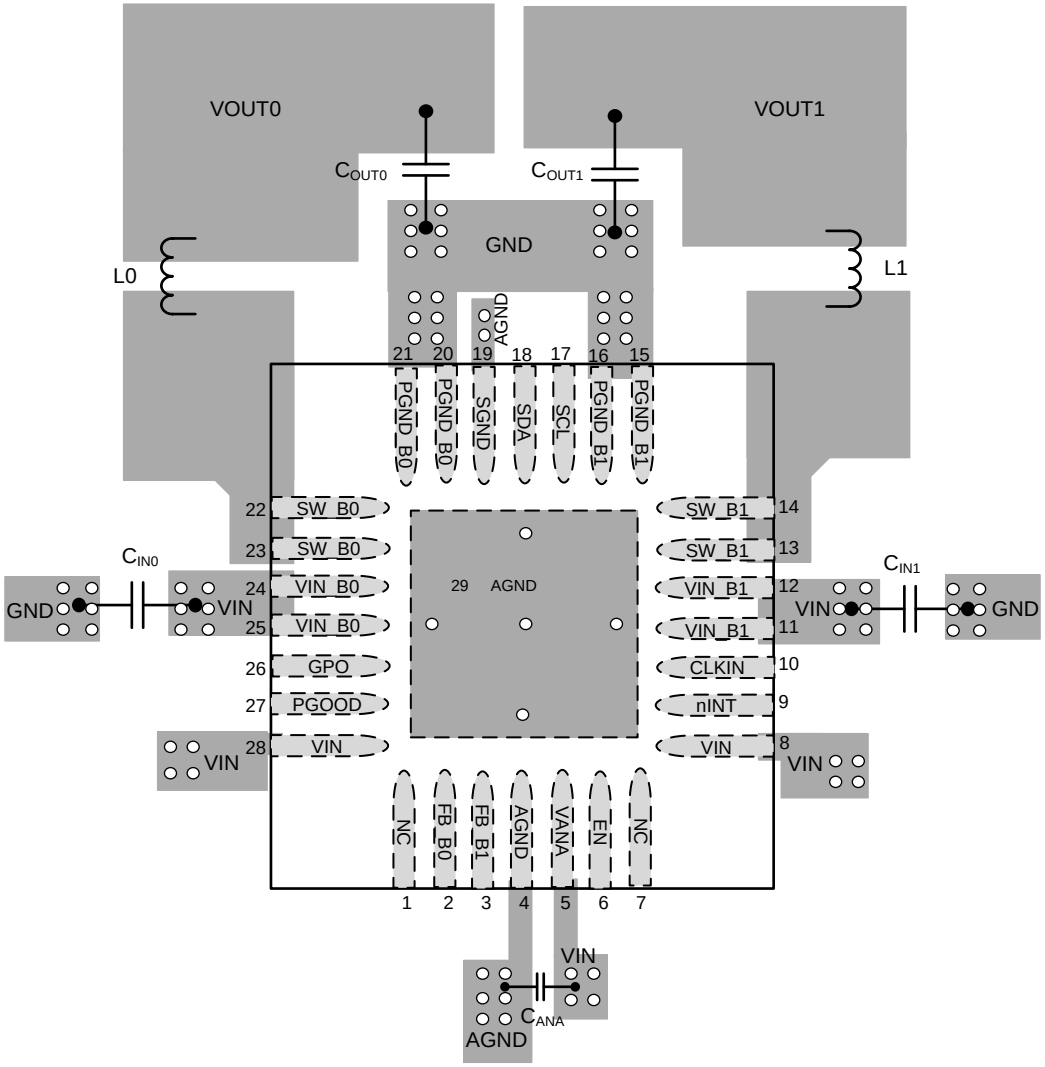


Figure 42. TPS65653-Q1 Board Layout

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

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要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

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11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS6565342RHDRQ1	ACTIVE	VQFN	RHD	28	3000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TPS6565 342-Q1	Samples
TPS6565342RHDTQ1	ACTIVE	VQFN	RHD	28	250	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TPS6565 342-Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

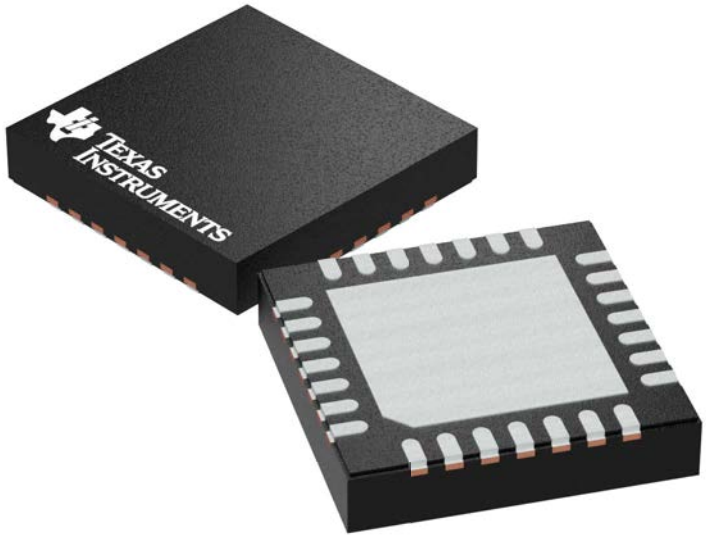
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

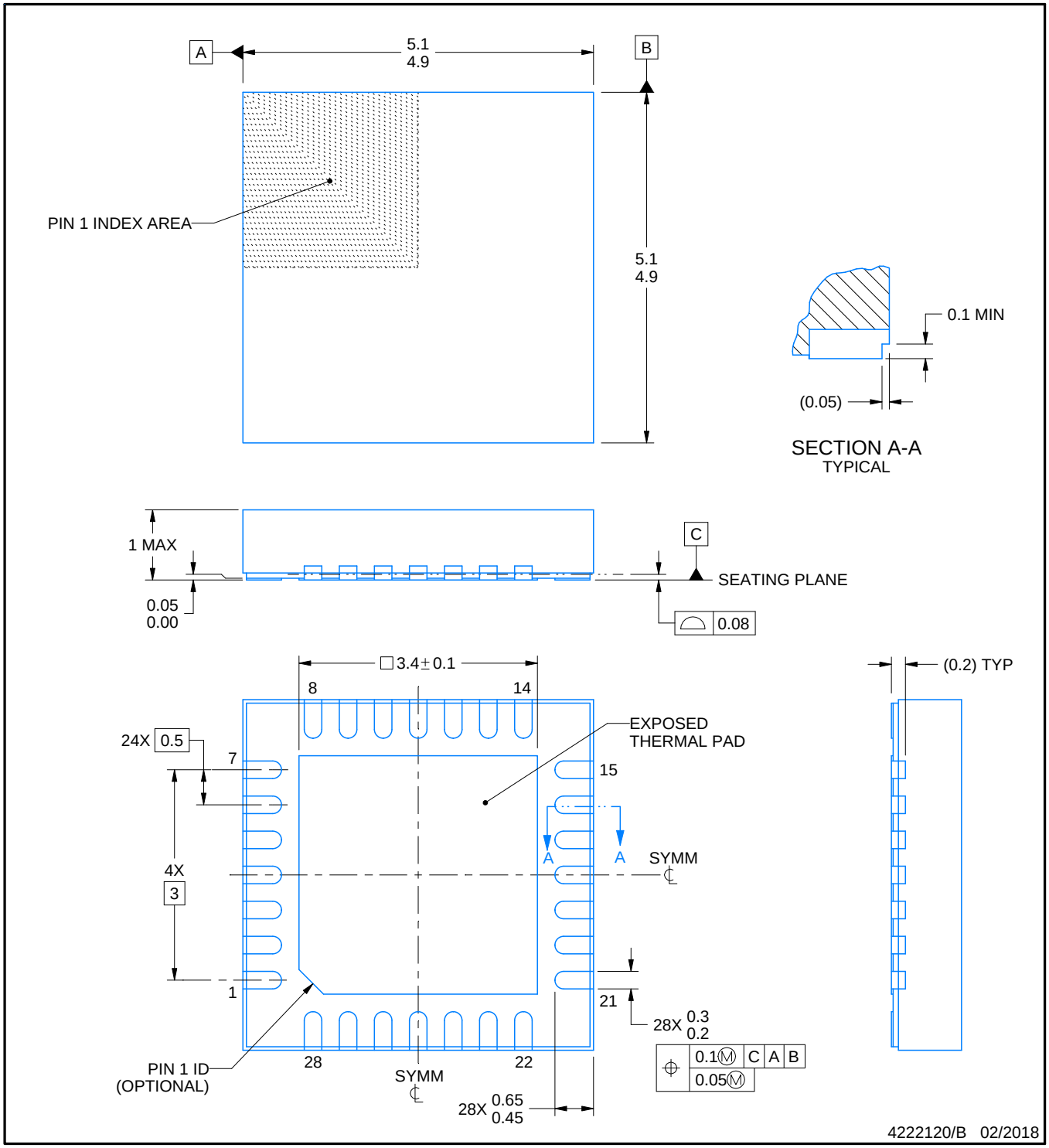
4204400/G

RHD0028W

PACKAGE OUTLINE

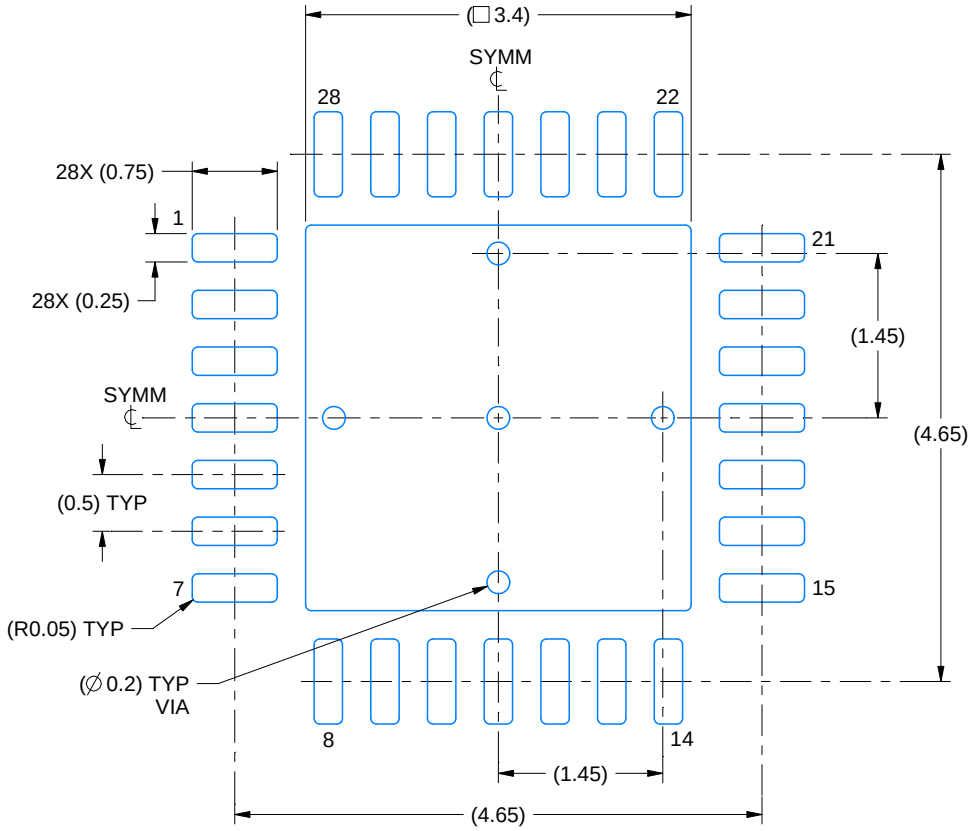
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

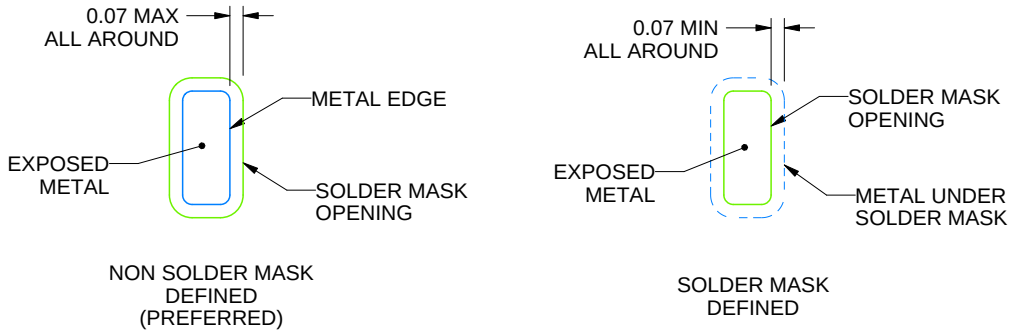


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

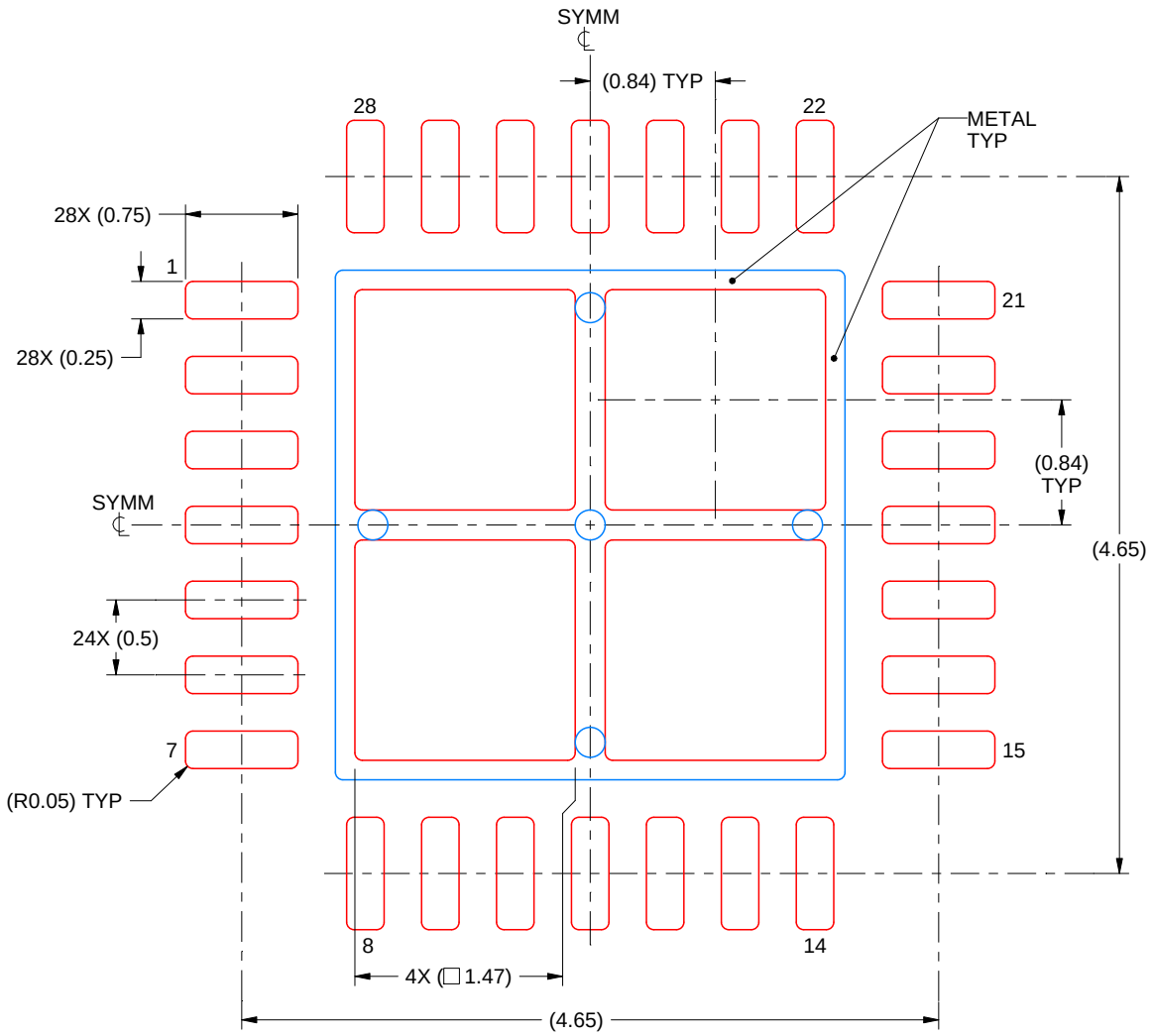


SOLDER MASK DETAILS

4222120/B 02/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4222120/B 02/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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