具有集成场效应晶体管 **(FET)**，**USB** 开关和按钮控制的 **4.5V** 至 **16V** 输入，高电流，同步降压 **3** 个直流 **-** 直流转换器

查询样片: **TPS65257**

特性

- 宽输入电源电压范围：
  4.5V - 16V
- **0.8V**，**1%** 精度基准
- 持续加载：
  3A（降压 **1**），**2A**（降压 **2** 和降压 **3**）
- 最大电流：
  3.5A（降压 **1**），**2.5A**（降压 **2** 和降压 **3**）
- 同步操作，由外部电阻设置的 **300kHz - 2.2MHz** 开关频率
- 具有内置电流源的外部使能引脚以实现简便排序
- 外部软启动引脚
- 外部电阻设置的可调节逐周期电源限制
- 具有简单补偿电路的电流模式控制
- 自动低脉冲跳跃 **(PSM)** 电源模式，可实现一个优于 **2%** 的输出纹波
- 支持预偏置输出
- 电源正常监控器和复位发生器
- 具有过流和热保护的 **1A USB** 电源开关
- 用于智能系统加电**/**断电操作的按钮（针对 **PB_IN** 的额定 **10kV** 静电放电 **(ESD)**）控制
- 小型，高效散热的 **40** 引脚 **6mm x 6mm RHA**（四方扁平无引线 **(QFN)**）封装
- **-40°C** 至 **125°C** 的结温范围

说明/订购信息

TPS65257 是一款具有 3 个逐降降压转换器的电源管理集成电路 (IC)。 集成了高侧和低侧金属氧化物半导体场效应晶体管 (MOSFET) 以提供效率更高的完全同步转换。 这个转换器被设计成在使设计人员能够根据目标应用来优化他们的用法的同时，简化它的应用。

此转换器可运行在 5V，9V，12V 或 15V 系统中。 此输出电压可在外部由一个电阻分压器设定为 0.8V 至输入电压减去转换器路径上阻性压降所得值之间的任一电压值。 每个转换器特有使能引脚，此引脚允许一个针对排序用途的延迟启动，通过选择软启动电容来实现可调软启动时间的软启动引脚，和一个电流限制 (RLIM) 引脚，此引脚使得设计人员能够通过选择一个外部电阻器来调整电流限值，并且优化电感器的选择。 所有转换器运行在“断续模式”中：一旦在任何一个转换器中感测到持续时间超过 10ms 的过流情况，它们将被关断 10ms，然后将重试启动序列。 如果过载已经被移除，此转换器将斜升并且正常运转。 如果情况不是这样，此转换器将感测到另外一个过流事件，再次关断，并且在此故障被消除前，重复此循环（断续）。 如果过载情况持续时间少于 10ms，那么只关断并重启动受到影响的相关转换器，而不会出现全局断续模式。

这些转换器的开关频率由一个连接至 ROSC 引脚的外部电阻器设定。 开关稳压器被设计成在 300kHz 至 2.2MHz 的频率范围内运行。 于是，这些转换器以 180°相位差运行，以大大减少输入滤波需求。

所有转换器具有峰值电流模式控制，此控制可简化外部频率补偿。 此器件具有一个内置斜率补偿斜坡。 斜率补偿能够防止峰值电流模式控制中的次谐波振荡。 一个传统类型 II 补偿网络能够稳定系统并实现快速瞬态响应。 此外，一个与反馈分压器的上层电阻并联的可选电容器多提供一个零值，并使得分频频率超过 100kHz。

所有转换器特有一个自动低功率脉冲频率调制 (PFM) 跳跃模式，此模式提升了轻负载和待机运行期间的效率，而与此同时又保证一个极低的输出纹波，从而在低输出电压上实现一个少于 2% 的值。

此器件组装有一个过压瞬态保护电路来最大限度地减少电压过冲。 过压保护 (OVP) 特性通过执行一个电路来最大限度地减少输出过冲，此电路将 FB 引脚电压与 OVP 阀值（内部电压基准的 109%）相比较。 如果 FB 引脚电压大于 OVTP 阀值，高侧 MOSFET 被禁用，从而防止电流流入输出，并且大大减少输出过冲。 当 FB 电压下降至低于 OVP 较低阀值（为内部电压基准的 107%）时，高侧 MOSFET 可接通下一个时钟周期。

English Data Sheet: SLVSB32

TPS65257 特有一个监控电路，此电路监控每个降压转换器的输出，而 PGOOD 引脚在排序完成时置位。 PGOOD 引脚是一个开漏输出。 这个 PGOOD 引脚在任一降压转换器被下拉至低于标称输出电压值的 85% 时下拉为低电平。 当所有转换器输出大于其标称输出电压值的 90% 以上时，PGOOD 被上拉。 缺省复位时间为 100ms。PGOOD 的极性为高电平有效。

此按钮操作被已经被设计成在施加输入电源时实现自动系统启动，或者在无需额外的外部组件的情况下提供集成型接通/关闭系统管理。 此器件的运行方式将取决于 INT 引脚的状态（请见启动信号）。

此 USB 开关提供下游 USB 器件所需的高达 1A 电流。 当输出负载超过电流限制阀值或者出现短路时，电源管理单元 (PMU) 通过切换至恒定电流模式，并将过流逻辑输出下拉至低电平来将输出电流限制在安全水平上。 当持续重负载和短路增加了开关内的功率耗散，而导致结温上升时，一个过热报警保护电路关闭此 USB 开关并使得这些降压转换器继续运行。

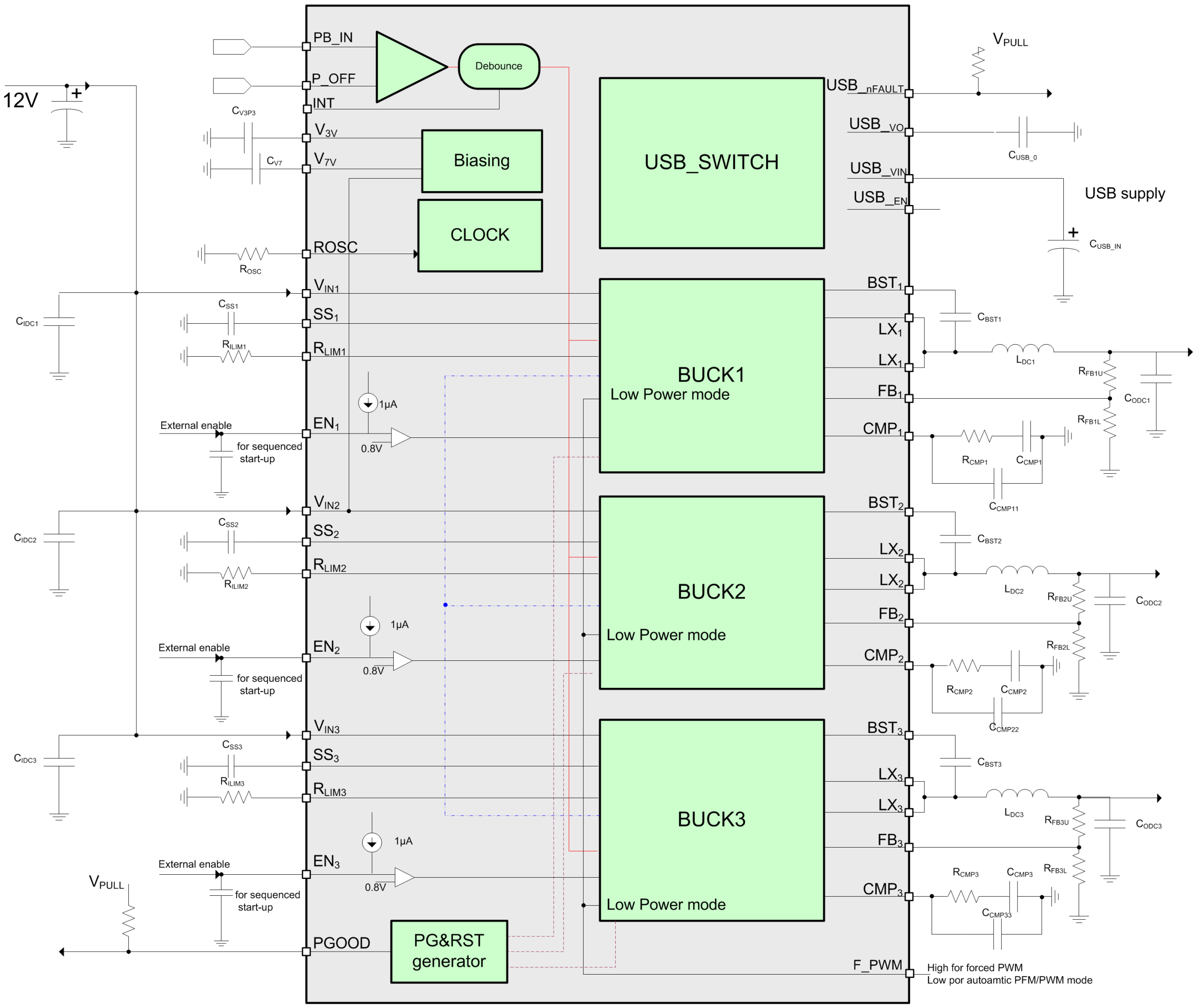
此器件执行一个内部热关断来在结温超过 160°C 时保护其自身不受损坏。 当结温超过热跳变阀值时，此热关断强制器件停止运行。 一旦裸片温度减少至低于 140°C，此器件重新启动加电序列。 热关断滞后值为 20°C。

订购信息 (1)

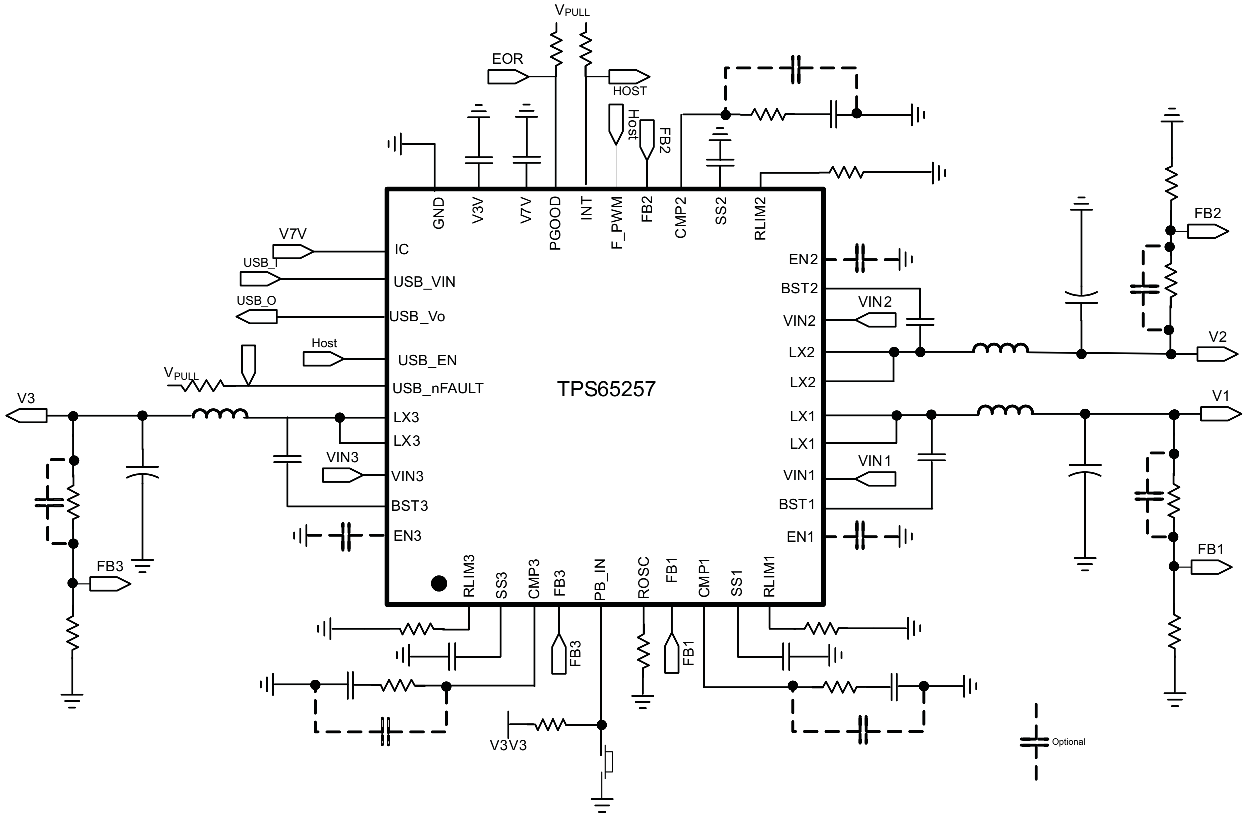
T_A	封装 (2)		部件号	正面标记
-40°C 至 125°C	40 引脚 (QFN) - RHA	2500 卷带	TPS65257RHAR	TPS65257
		250 卷	TPS65257RHAT	

(1) 如需了解最新的封装和订购信息，敬请参阅本文档末尾的封装选项附录，或者查看 TI 网站 www.ti.com。
(2) 封装图样、散热数据和符号可从网站 www.ti.com/packaging 中获取。

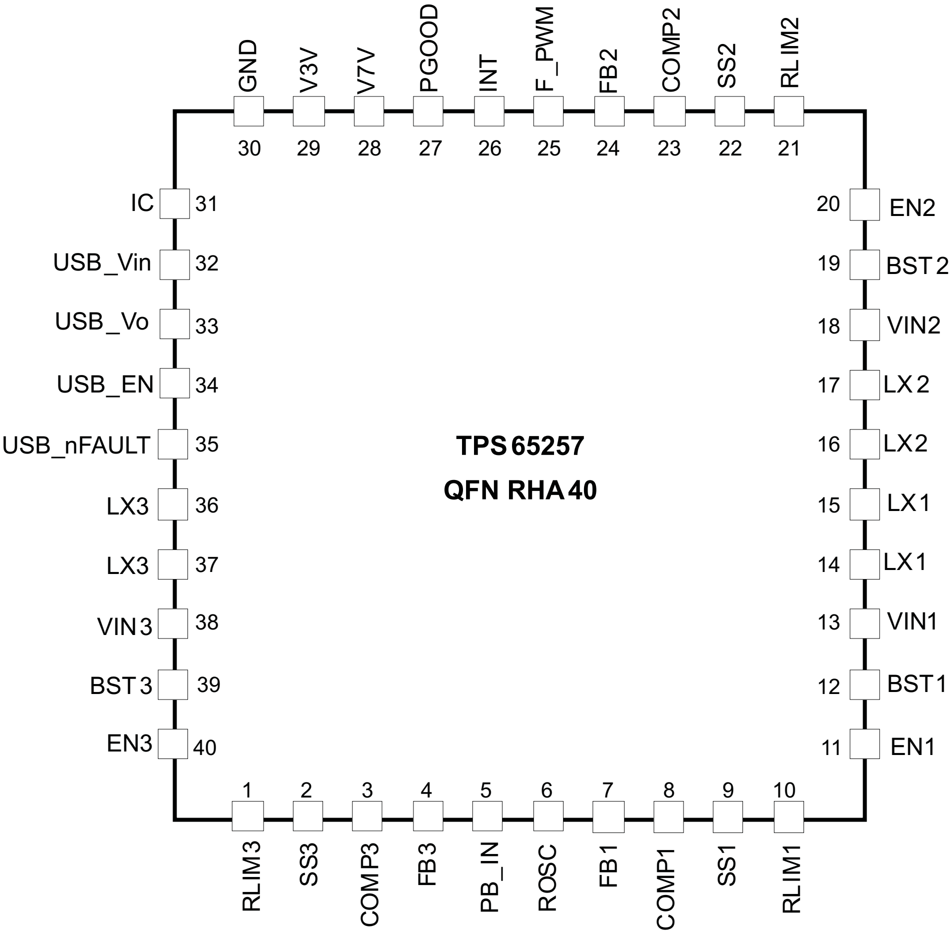
FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION



PIN OUT


TPS65257
QFN RHA40
1 RLIM3
2 SS3
3 COMP3
4 FB3
5 PB_IN
6 ROSC
7 FB1
8 COMP1
9 SS1
10 RLIM1
11 EN1
12 BST1
13 VIN1
14 LX1
15 LX1
16 LX2
17 LX2
18 VIN2
19 BST2
20 EN2
21 RLIM2
22 SS2
23 COMP2
24 FB2
25 F_PWM
26 INT
27 PGOOD
28 V7V
29 V3V
30 GND
31 IC
32 USB_Vin
33 USB_Vo
34 USB_EN
35 USB_nFAULT
36 LX3
37 LX3
38 VIN3
39 BST3
40 EN3

TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
RLIM3	1	I	Current limit setting for Buck3. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS3	2	I	Soft start pin for Buck3. Fit a small ceramic capacitor to this pin to set the converter soft start time.
COMP3	3	O	Compensation for Buck3. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB3	4	I	Feedback pin for Buck3. Connect a divider set to 0.8 V from the output of the converter to ground.
PB_IN	5	I	Push button input (active low)
ROSC	6	I	Oscillator set. This resistor sets the frequency of internal autonomous clock.
FB1	7	I	Feedback pin for Buck1. Connect a divider set to 0.8 V from the output of the converter to ground.
COMP1	8	O	Compensation pin for Buck1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
SS1	9	I	Soft-start pin for Buck1. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
RLIM1	10	I	Current limit setting pin for Buck1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
EN1	11	I	Enable pin for Buck1. A high signal on this pin enables the regulator Buck. For a delayed start-up add a small ceramic capacitor from this pin to ground.
BST1	12		Bootstrap capacitor for Buck1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
VIN1	13	I	Input supply for Buck1. Fit a 10-µF ceramic capacitor close to this pin.
LX1	14, 15	O	Switching node for Buck1
LX2	16, 17	O	Switching node for Buck2
VIN2	18	I	Input supply for Buck2. Fit a 10-µF ceramic capacitor close to this pin.
BST2	19		Bootstrap capacitor for Buck2. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN2	20	I	Enable pin for Buck2. A high signal on this pin enables the regulator. For a delayed start-up add a small ceramic capacitor from this pin to ground.
RLIM2	21	I	Current limit setting pin for Buck2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS2	22	I	Soft-start pin for Buck2. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
COMP2	23	O	Compensation pin for Buck2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB2	24	I	Feedback input for Buck2. Connect a divider set to 0.8 V from the output of the converter to ground.
F_PWM	25		Forces PWM operation in all converters when set high. If low converters will operate in automatic PFM/PWM mode.
INT	26	O	Open drain interrupt output
PGOOD	27	O	Power good. Open drain output asserted low after all converters and sequenced and within regulation. Polarity is factory selectable (active high default).
V7V	28	O	Internal supply. Connect a 4.7-µF to 10-µF ceramic capacitor from this pin to ground.
V3V	29	O	Internal supply. Connect a 3.3-µF to 10-µF ceramic capacitor from this pin to ground.
GND	30		Ground
IC	31	I	This pin should be connected to V7V pin
USB_VIN	32	I	USB switch Input supply
USB_Vo	33		USB switch output
USB_EN	34	I	Enable input, high turns on the switch

TERMINAL FUNCTIONS (continued)

NAME	NO.	I/O	DESCRIPTION
USB_nFAULT	35	I	USB1 fault flag output, open drain, active low. Asserted when overcurrent or overtemperature condition is detected in the switch.
LX3	36, 37	O	Switching node for Buck3
VIN3	38	I	Input supply for Buck3. Fit a 10-µF ceramic capacitor close to this pin.
BST3	39	I	Bootstrap capacitor for Buck3. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN3	40	I	Enable pin for Buck3. A high signal on this pin enables the converter. For a delayed start-up add a small ceramic capacitor from this pin to ground.
PowerPAD			PowerPAD. Connect to system ground for electrical and thermal connection.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted, all voltages are with respect to GND)

	Voltage range at VIN1,VIN2, VIN3, LX1, LX2, LX3	–0.3 to 18	V
	Voltage range at LX1, LX2, LX3 (maximum withstand voltage transient < 10 ns)	–3 to 18	V
	Voltage at BST1, BST2, BST3 referenced to LX pin	–0.3 to 7	V
	Voltage at V7V, COMP1, COMP2, COMP3, USB_Vin, USB_Vo	–0.3 to 7	V
	Voltage at V3V, RLIM1, RLIM2, RLIM3, EN1,EN2, EN3, SS1, SS2, SS3, FB1, FB2, FB3 , PGOOD, ROSC, PB_IN INT, USB_EN, USB_ILIM, F_PWM	–0.3 to 3.6	V
	Voltage at GND	–0.3 to 0.3	V
T_J	Operating junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		16	V
T_A	Junction temperature	–40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model (HBM), PB_IN pin to ground	10000		V
Any other pin	2000		
Charge device model (CDM)	500		V

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} (°C/W)	$T_A = 25°C$ POWER RATING (W)	$T_A = 55°C$ POWER RATING (W)	$T_A = 85°C$ POWER RATING (W)
RHA	30	3.33	2.3	1.3

(1) Based on JEDEC 51.5 HIGH K environment measured on a 76.2 x 114 x 0.6-mm board with the following layer arrangement:
(a) Top layer: 2 Oz Cu, 6.7% coverage
(b) Layer 2: 1 Oz Cu, 90% coverage
(c) Layer 3: 1 Oz Cu, 90% coverage
(d) Bottom layer: 2 Oz Cu, 20% coverage

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE						
V_{IN}	Input voltage range		4.5		16	V
IDD_{SDN}	Shutdown	EN pin = low for all converters		170		µA
IDD_Q	Quiescent (push-button pull-up current not included)	Converters enabled, no load Buck1 = 1.2 V Buck2 = 1.8 V Buck3 = 3.3 V T_A = 25°C, F_PWM = Low		600		µA
	Quiescent, forced PWM	Converters enabled, no load F_PWM = High		18		mA
UVLO	V_{IN} under voltage lockout	Rising V_{IN}		4.22		V
		Falling V_{IN}		4.1		
$UVLO_{DEGLITCH}$		Both edges		110		µs
V3p3	Internal biasing supply			3.3		V
I_{3V}	Biasing supply output current	V_{IN} = 12 V			10	mA
V7V	Internal biasing supply			6.25		V
I_{7V}	Biasing supply output current	V_{IN} = 12 V			10	mA
$V7V_{UVLO}$	UVLO for internal V7V rail	Rising V7V		3.8		V
		Falling V7V		3.6		
$V7V_{UVLO\_DEGLITCH}$		Falling edge		110		µs
BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT-START AND SWITCHING FREQUENCY)						
V_{IH}	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENx} rising	1.55		1.82	V
	Enable high level	External GPIO, V_{ENX} rising	0.66 x V3p3			
V_{IL}	Enable threshold low	V3p3 = 3.2 V - 3.4 V, V_{ENx} falling	0.98		1.24	V
	Enable low level	External GPIO, VENX falling			0.33 x V3p3	
$V_{IH\_F\_PWM}$	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENx} rising	0.66 x V3p3			V
$V_{IL\_F\_PWM}$	Enable treshold low	V3p3 = 3.2 V - 3.4 V, V_{ENx} falling			0.33 x V3p3	V
ICH_{EN}	Pull up current enable pin			1		µA
t_D	Discharge time enable pins	Power-up		10		ms
I_{SS}	Soft-start pin current source			5		µA
F_{SW_BK}	Converter switching frequency range	Set externally with resistor	0.3		2.2	MHz
R_{FSW}	Frequency setting resistor		50		600	kΩ
f_{SW_TOL}	Internal oscillator accuracy	f_{SW} = 800 kHz	-10		10	%
FEEDBACK, REGULATION, OUTPUT STAGE						
V_{FB}	Feedback voltage	V_{IN} = 12 V , T_A = 25°C	-1%	0.8	1%	V
		V_{IN} = 4.5 V to 16 V	-2%	0.8	2%	
t_{ON_MIN}	Minimum on time (current sense blanking)				135	ns
MOSFET (BUCK 1)						
H.S. Switch	On resistance of high side FET on CH1	25°C, BOOT = 6.5 V		95		mΩ
L.S. Switch	On resistance of low side FET on CH1	25°C, VIN = 12 V		50		mΩ

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET (BUCK 2)						
H.S. Switch	On resistance of high side FET on CH2	25°C, BOOT = 6.5 V		120		mΩ
L.S. Switch	On resistance of low side FET on CH2	25°C, VIN = 12 V		80		mΩ
MOSFET (BUCK 3)						
H.S. Switch	On resistance of high side FET on CH3	25°C, BOOT = 6.5 V		120		mΩ
L.S. Switch	On resistance of low side FET on CH3	25°C, VIN = 12 V		80		mΩ
ERROR AMPLIFIER						
g_M	Error amplifier transconductance	-2 µA < ICOMP < 2 µA		130		µ℧
gm_{PS}	COMP to ILX gm	I_{LX} = 0.5 A		10		A/V
POWER GOOD RESET GENERATOR						
VUV_{BUCKX}	Threshold voltage for buck under voltage	Output falling		85		%
		Output rising (PG will be asserted)		90		
$t_{UV\_deglitch}$	Deglitch time (both edges)			11		ms
t_{ON_HICCUP}	Hiccup mode ON time	VUV_{BUCKX} asserted		12		ms
t_{OFF_HICCUP}	Hiccup mode OFF time	All converters disabled. Once t_{OFF_HICCUP} elapses, all converters will go through sequencing again.		20		ms
VOV_{BUCKX}	Threshold voltage for buck over voltage	Output rising (high side FET will be forced off)		109		%
		Output falling (high side FET will be allowed to switch)		107		
t_{RP}	minimum reset period	Measured after the later of Buck1 or Buck3 power-up successfully		100		ms
PB_IN						
V_{PB}	PB_IN, P_OFF , threshold	Low, V3p3 = 3.2-3.4V			0.33x V3p3	V
		High, V3p3 = 3.2-3.4V	0.66x V3p3			
$T_{PB\_DEGLITCH}$	P_{OFF} Internal de-bounce time turn_on and turn_off			20		ms
USB SWITCH						
VIN_{USB}	USB input voltage range		3		6	V
$V_{IH\_USB\_EN}$	USB_EN high level input voltage	V3p3 = 3.2-3.4 V, V_{USB_EN} rising	0.66x V3p3			V
$V_{IL\_USB\_EN}$	USB_EN low level input voltage	V3p3 = 3.2-3.4 V, V_{USB_EN} falling			0.33x V3p3	V
R_{DS_USB}	Static drain-source on-state resistance	USB_VIN = 5 V and Io_USB = 0.5 A, T_J = 2 5°C		120		mΩ
I_{CS_USB}	USB current limit	Increasing USB_Vo current di/dt<1 A/s	-20%	1.2	20%	A
$K_{OVERCURRENT}$	Overcurrent detection factor Ratio of I_{LIM_START}/I_{CS_USB}	Increasing USB_Vo current di/dt< 1A/s, VIN_{USB} = 6 V VIN_{USB} = 5 V		1.5		
V_{USBx_nFAULT}	USBx_nFAULT output voltage low	I_{USB_ILIM} = 3 mA			0.4	V
T_{CS_USB}	USB over current fault deglitch	Fault assertion due to over current protection		5		ms

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{USB_TRIP}	USB thermal trip point	Rising temperature		130		°C
T_{USB_HYST}	USB thermal trip hysteresis	Falling temperature		20		°C
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shut down trip point	Rising temperature		160		°C
T_{HYST}	Thermal shut down hysteresis	Device re-starts		20		°C
$T_{TRIP\_DEGLITCH}$	Thermal shut down deglitch			110		µs
CURRENT LIMIT PROTECTION						
$RLIM_x$	Limit resistance range		75		300	kΩ
$ILIM_1$	Buck 1 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 44	1.2		5.05	A
$ILIM_2$	Buck 2 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 45	1.2		4.7	A
$ILIM_3$	Buck 3 adjustable current limit range	V_{IN} = 12 V, f_{SW} = 500 kHz, see Figure 46	1.3		4.7	A

TYPICAL CHARACTERISTICS

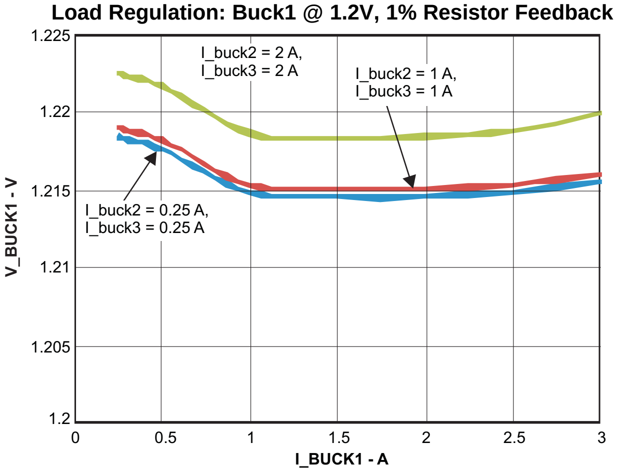

Load Regulation: Buck1 @ 1.2V, 1% Resistor Feedback

Figure 1.

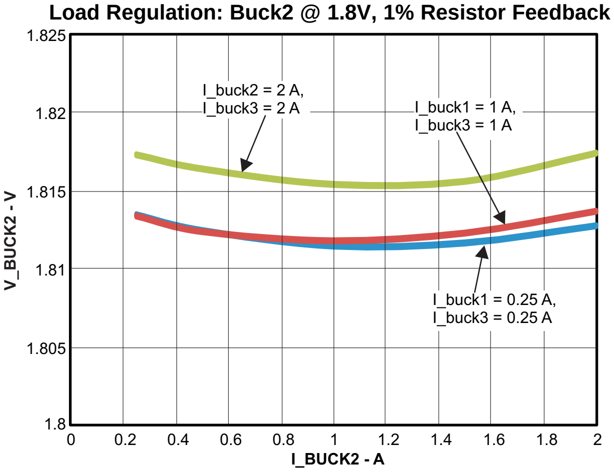

Load Regulation: Buck2 @ 1.8V, 1% Resistor Feedback

Figure 2.

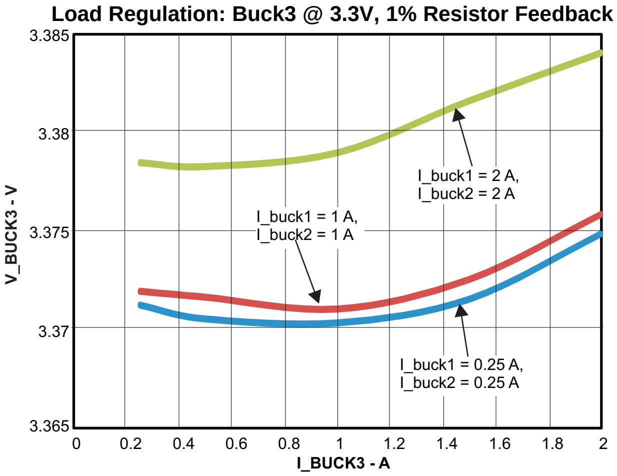

Load Regulation: Buck3 @ 3.3V, 1% Resistor Feedback

Figure 3.

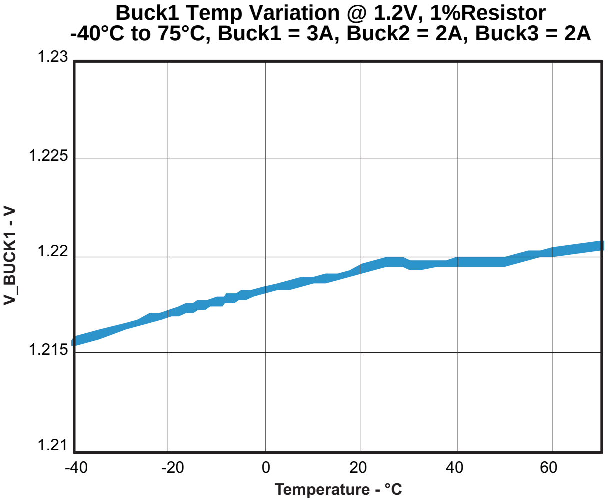

Buck1 Temp Variation @ 1.2V, 1%Resistor
-40°C to 75°C, Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

Figure 4.

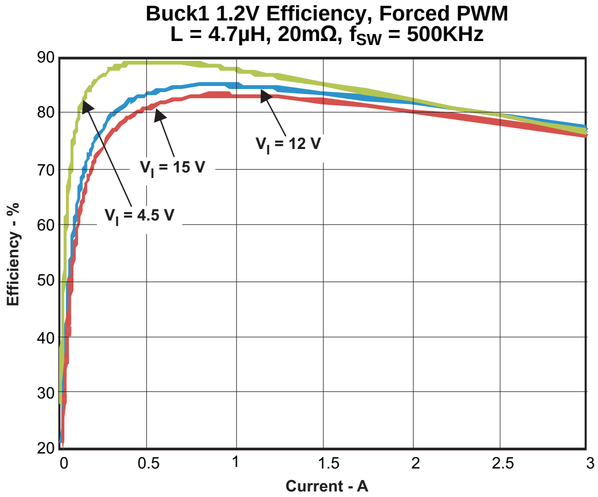

Buck1 1.2V Efficiency, Forced PWM
L = 4.7µH, 20mΩ, f_{SW} = 500KHz

Figure 5.

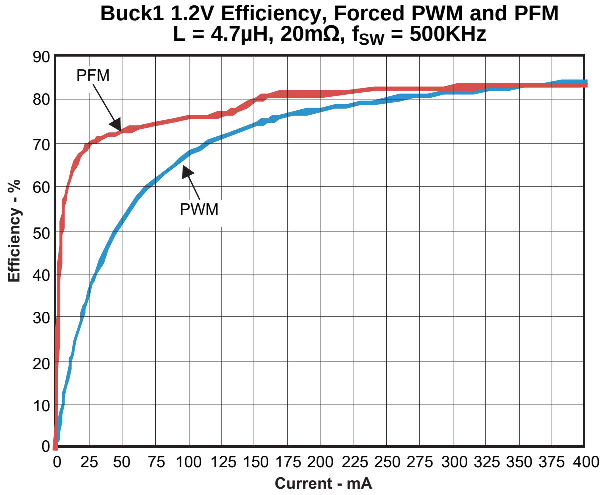
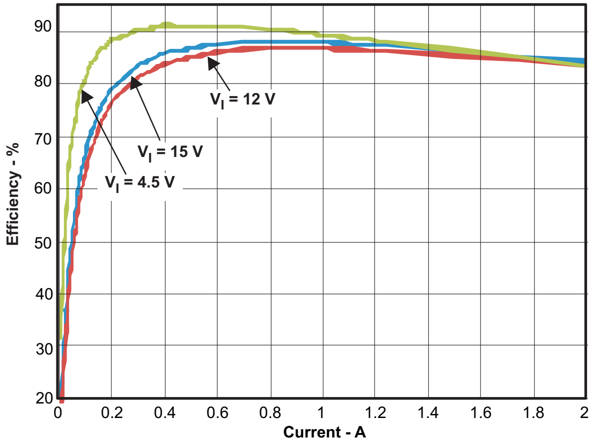

Buck1 1.2V Efficiency, Forced PWM and PFM
L = 4.7µH, 20mΩ, f_{SW} = 500KHz

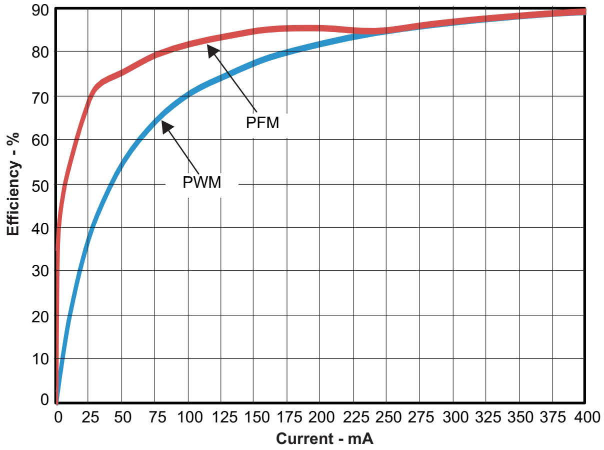
Figure 6.

TYPICAL CHARACTERISTICS (continued)



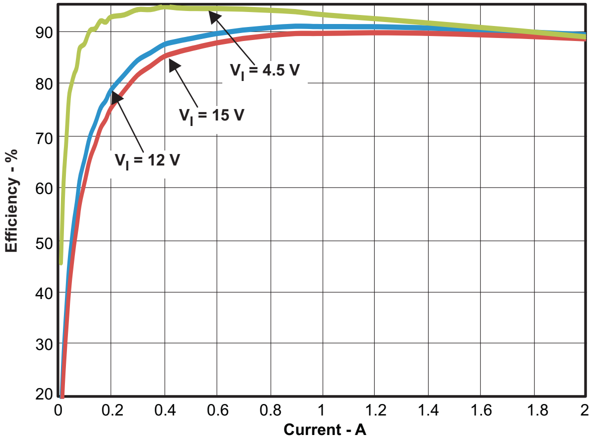
Buck2 1.8V Efficiency, Forced PWM
L = 4.7µH, 20mΩ, f_{SW} = 500KHz

Figure 7.



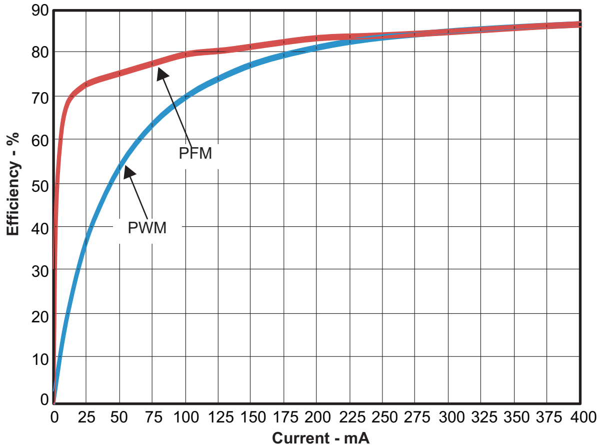
Buck2 1.8V Efficiency, Forced PWM and PFM
L = 4.7µH, 20mΩ, f_{SW} = 500KHz

Figure 8.



Buck3 3.3V Efficiency, Forced PWM
L = 4.7µH, 20mΩ, f_{SW} = 500KHz

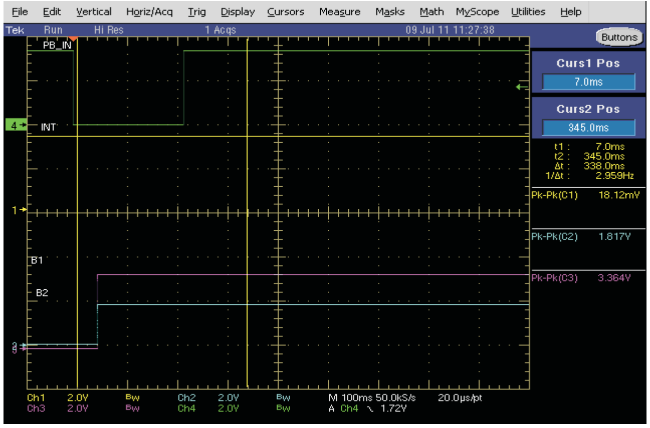
Figure 9.



Buck3 3.3V Efficiency, Forced PWM and PFM
L = 4.7µH, 20mΩ, f_{SW} = 500KHz

Figure 10.

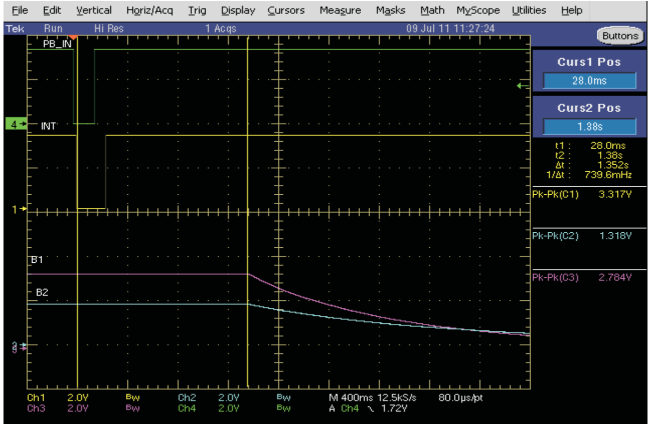
Push-Button Operation Power-Up



Curs1 Pos 7.0ms
Curs2 Pos 345.0ms
t1 : 7.0ms
t2 : 345.0ms
Δt : 338.0ms
1/Δt : 2.959Hz
Pk-Pk(C1) 18.12mV
Pk-Pk(C2) 1.817V
Pk-Pk(C3) 3.364V
Ch1 2.0V Bw Ch2 2.0V Bw M 100ms 50.0kS/s 20.0µs/pt
Ch3 2.0V Bw Ch4 2.0V Bw A Ch4 ↘ 1.72V

Figure 11.

Push-bButton Operation Power-Down



Curs1 Pos 28.0ms
Curs2 Pos 1.38s
t1 : 28.0ms
t2 : 1.38s
Δt : 1.352s
1/Δt : 739.6mHz
Pk-Pk(C1) 3.317V
Pk-Pk(C2) 1.318V
Pk-Pk(C3) 2.784V
Ch1 2.0V Bw Ch2 2.0V Bw M 400ms 12.5kS/s 80.0µs/pt
Ch3 2.0V Bw Ch4 2.0V Bw A Ch4 ↘ 1.72V

Figure 12.

TYPICAL CHARACTERISTICS (continued)

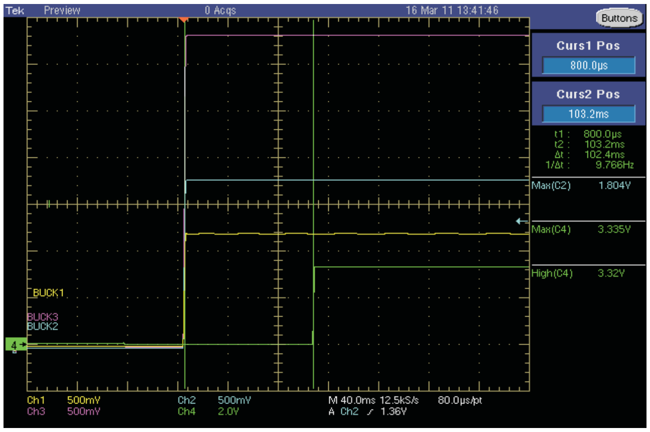

Power-Up All Converters and PGOOD (Green), No Load

Figure 13.

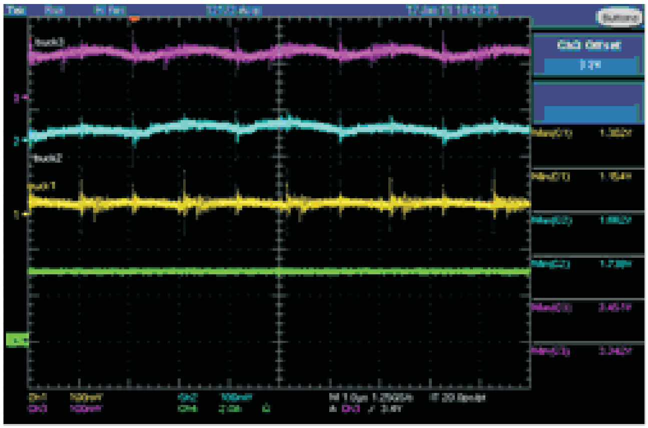

Ripple T_A = 25°C Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

Figure 14.

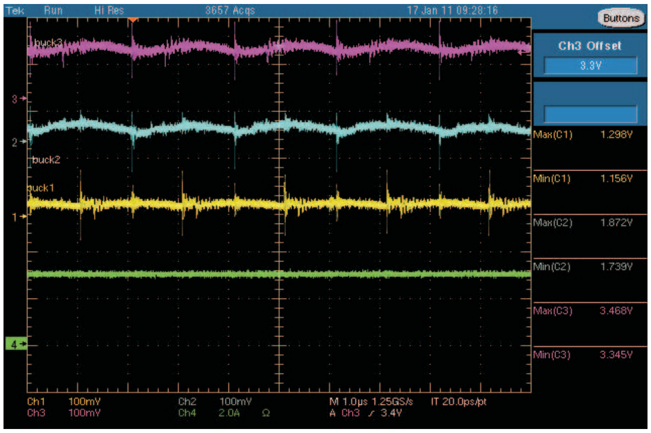

Ripple T_A = 70°C, Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

Figure 15.

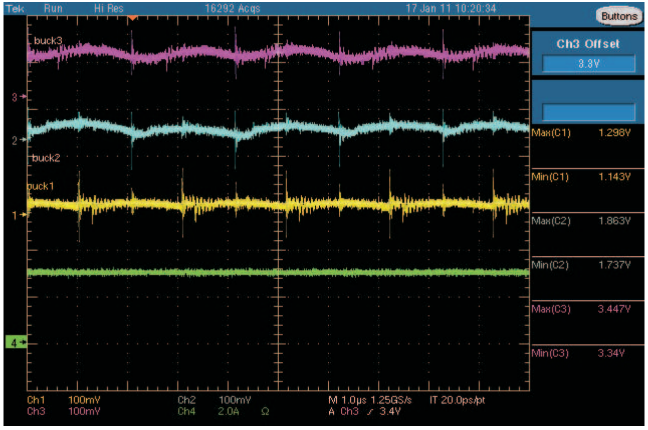

Ripple T_A = 10°C, Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

Figure 16.

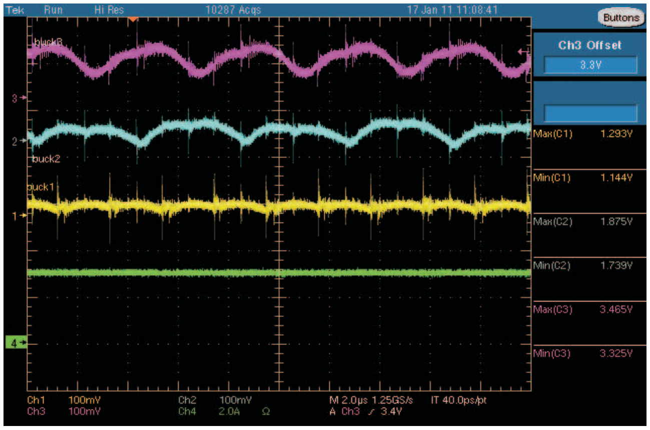

Ripple T_A = 40°C, Buck1 = 3A, Buck2 = 2A, Buck3 = 2A

Figure 17.

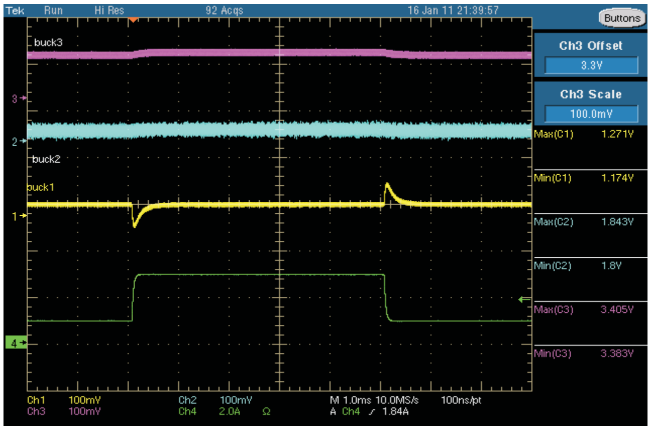

Transient Response Buck1
1.2V, 1-3A Step, Co = 22µF,L = 4.7µH, f_{SW} = 500KHz

Figure 18.

TYPICAL CHARACTERISTICS (continued)

Transient Response Buck2
1.8V, 1-2A Step, Co = 22µF,L = 4.7µH, f_{SW} = 500KHz

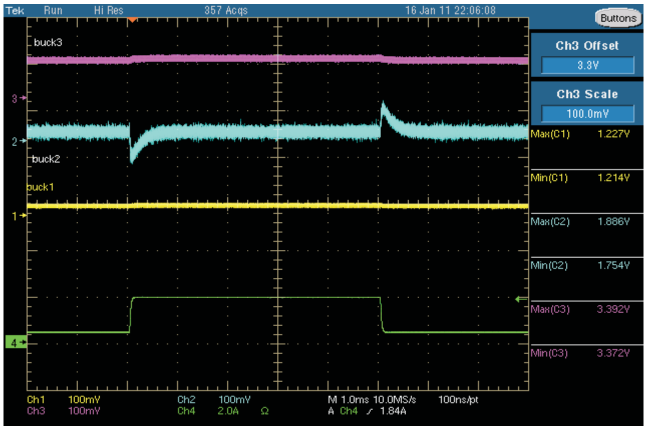


Figure 19.

Buck3 3.3V Efficiency Measured With
L = 4.7µH, 20mΩ, f_{SW} = 500kHz

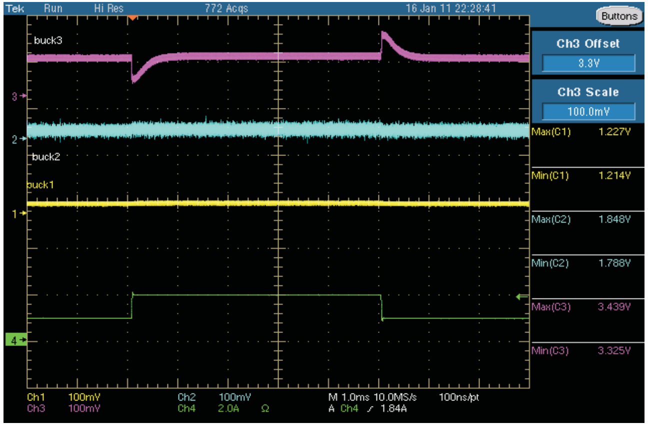


Figure 20.

PFM Operation 1.2V, 1.8V, 3.3V

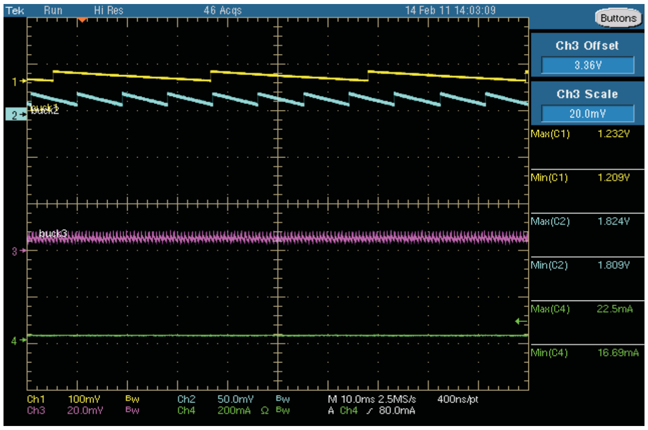


Figure 21.

PFM/PWM Transition (Pin 25 Pulled High)

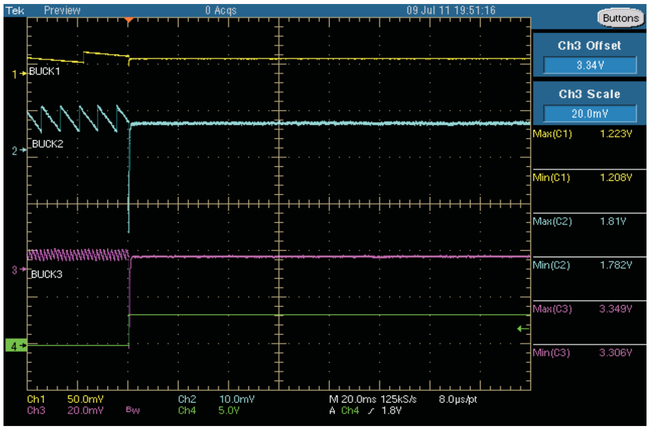


Figure 22.

PWM/PFM Transition (Pin 25 Pulled Low)

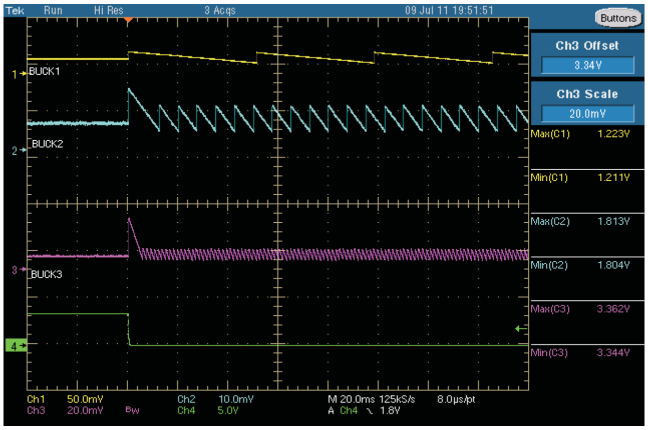


Figure 23.

Buck1 Dynamic Transition from PFM to PWM
4.7µH, 68µF, 500 kHz

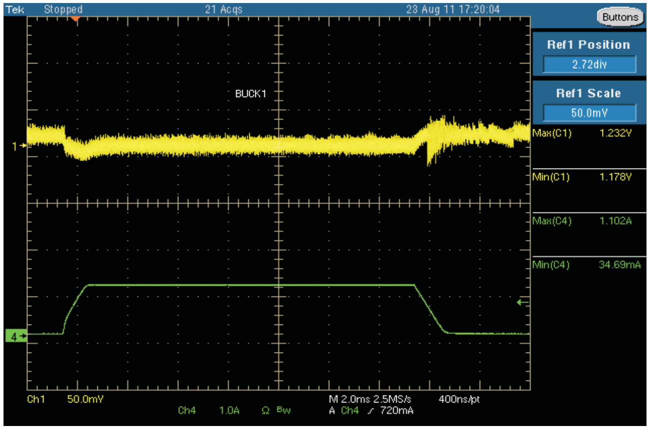


Figure 24.

TYPICAL CHARACTERISTICS (continued)

**Buck2 Dynamic Transition from PFM to PWM
4.7μH, 44μF, 500 kHz**

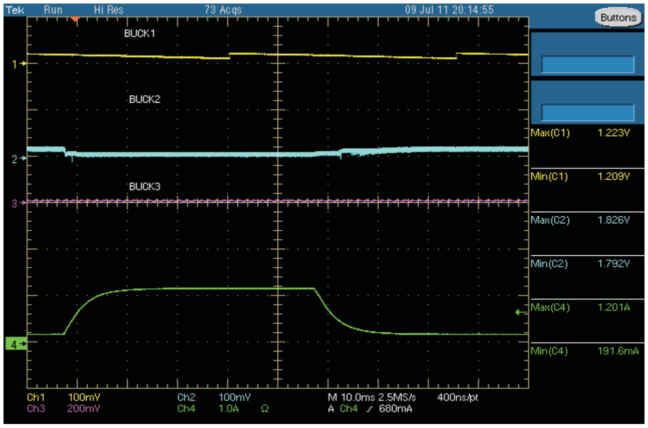


Figure 25.

**Buck3 Dynamic Transition from PFM to PWM
4.7μH, 22μF, 500 kHz**

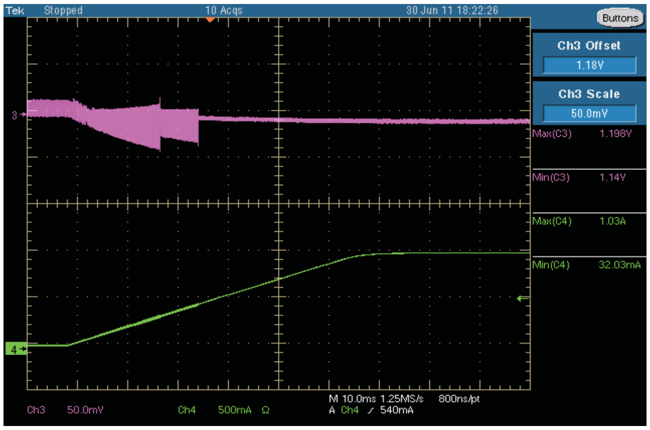


Figure 26.

USB Switch Start-Up, No Load

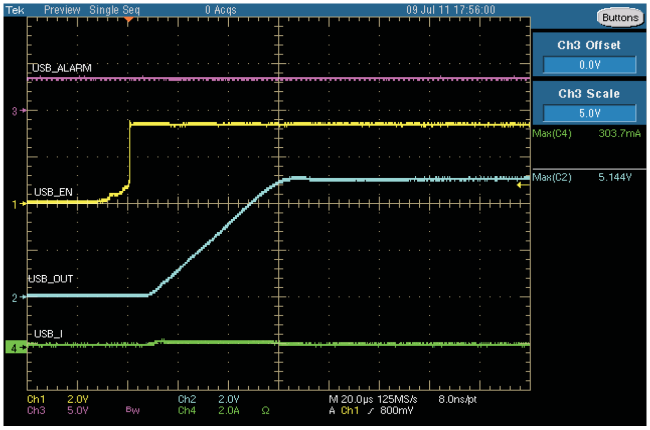


Figure 27.

USB Switch Start-Up, No Load

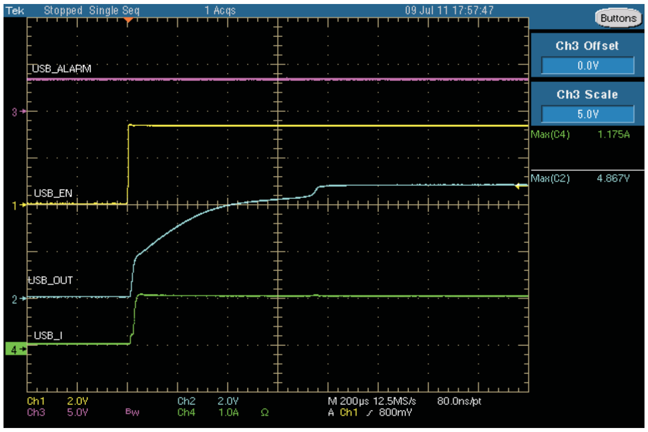


Figure 28.

USB Current Limit Operation (3.3V)

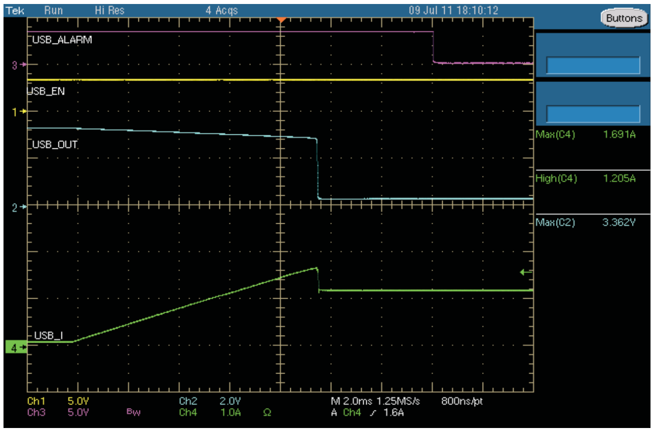


Figure 29.

USB Current Limit Recovery (3.3V)

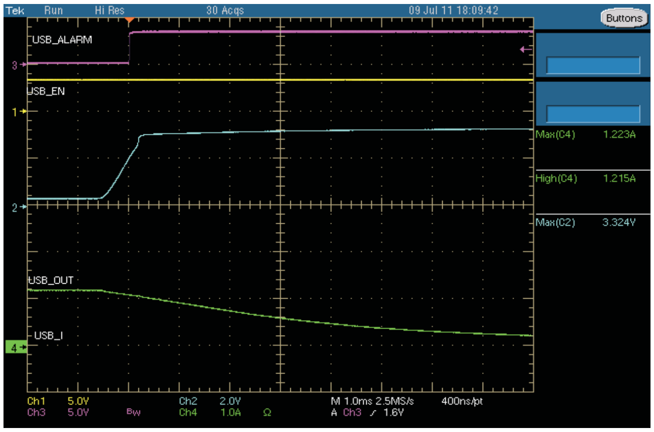


Figure 30.

TYPICAL CHARACTERISTICS (continued)

USB Current Limit Operation (5V)

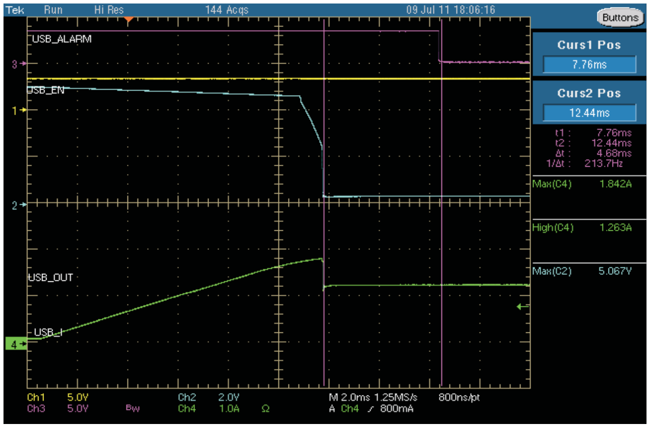


Figure 31.

USB Current Limit Recovery (5V)

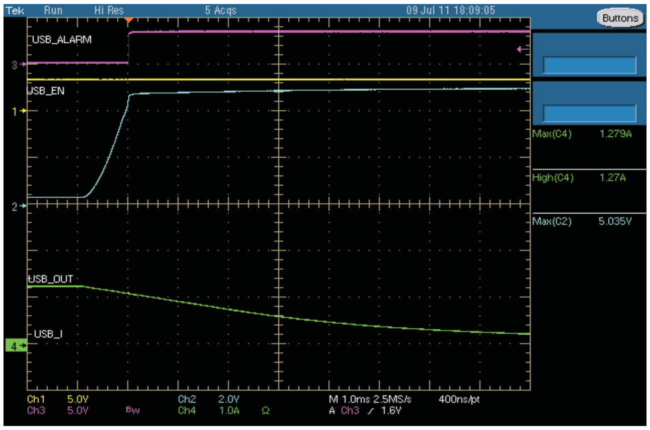
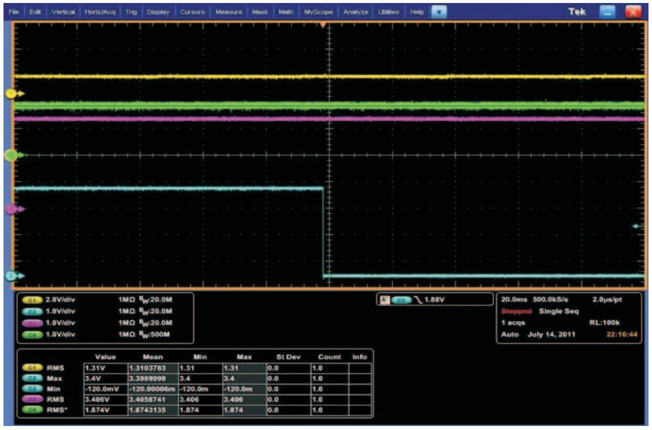


Figure 32.

Bucks Operation (Top 3 Traces) and USB Alarm Operation



	Value	Mean	Min	Max	St Dev	Count	Info
C1 RMS	1.31V	1.3103783	1.31	1.31	0.0	1.0	
C2 Max	3.4V	3.3999999	3.4	3.4	0.0	1.0	
C2 Min	-120.0mV	-120.00006m	-120.0m	-120.0m	0.0	1.0	
C3 RMS	3.406V	3.4058741	3.406	3.406	0.0	1.0	
C4 RMS*	1.874V	1.8743135	1.874	1.874	0.0	1.0	

Figure 33.

EVM Layout

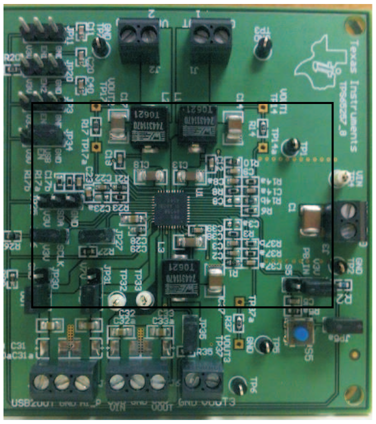


Figure 34.

T_A = 25°, V_{IN} = 12V, f_{SW} = 500kHz
B1 = 3A, B2 = 2A, B3 = 2A

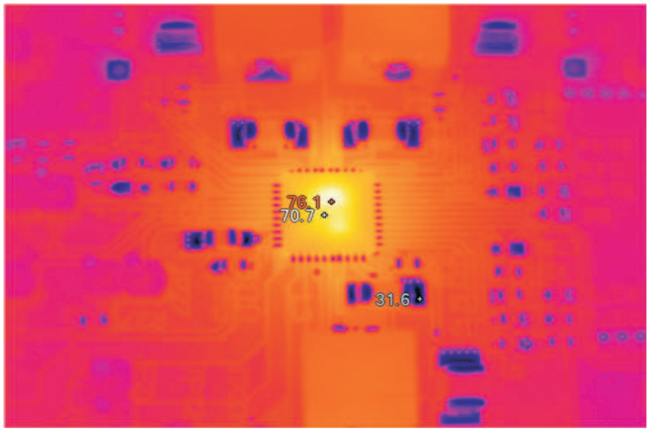


Figure 35.

T_A = 25°, V_{IN} = 5V, f_{SW} = 500kHz
B1 = 3A, B2 = 2A, B3 = 2A

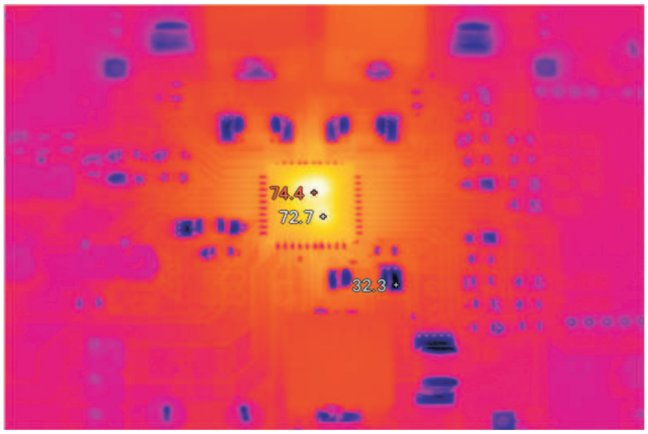


Figure 36.

TYPICAL CHARACTERISTICS (continued)

T_A = 25°, V_{IN} = 5V, f_{SW} = 1000kHz
B1 = 3A, B2 = 2A, B3 = 2A

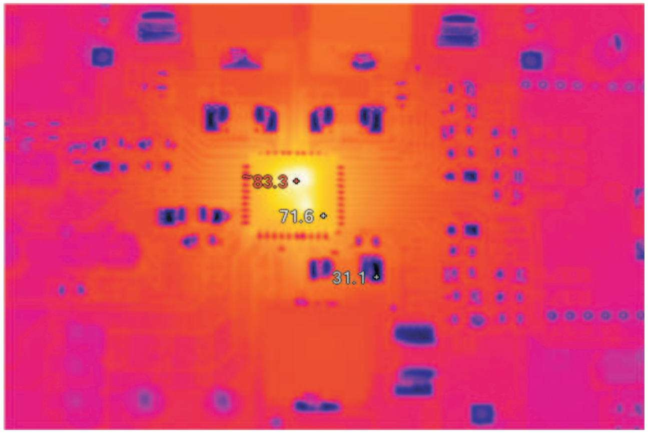


Figure 37.

DETAILED DESCRIPTION

Adjustable Switching Frequency

To select the internal switching frequency, connect a resistor from ROSC to ground. Figure 38 shows the required resistance for a given switching frequency.

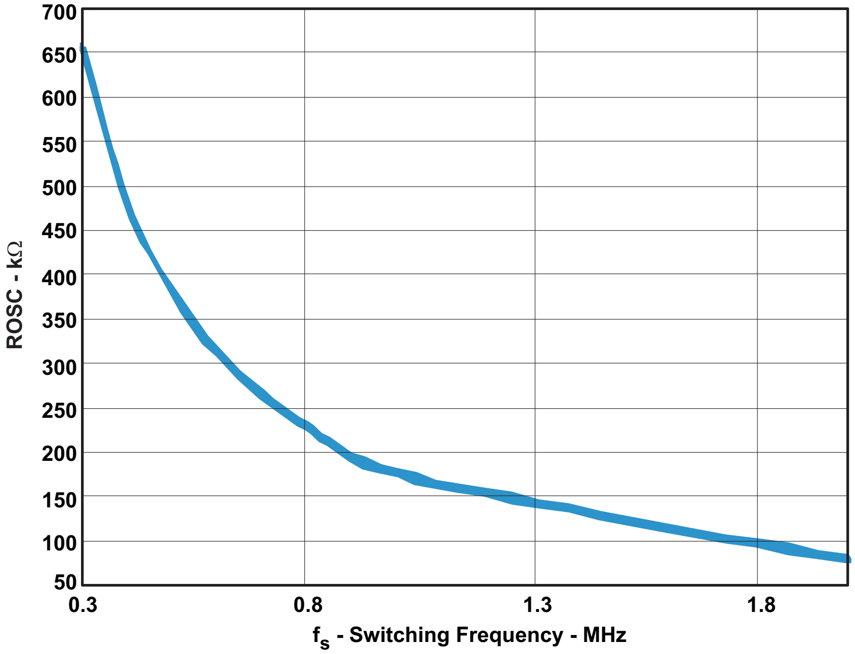


Figure 38. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 174 \bullet f_{SW}^{-1.122} \quad (1)$$

Output Inductor Selection

To calculate the value of the output inductor, use Equation 2.

$$Lo = \frac{Vin - Vout}{Io \cdot K_{ind}} \cdot \frac{Vout}{Vin \cdot fsw} \tag{2}$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. In general, K_{IND} is normally from 0.1 to 0.3 for the majority of applications. A value of 0.1 will improve the efficiency at light load, while a value of 0.3 will provide the lowest possible cost solution. The ripple current is:

$$Iripple = \frac{Vin - Vout}{Lo} \cdot \frac{Vout}{Vin \cdot fsw} \tag{3}$$

Output Capacitor

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements. If a minimum transient specification is required use the following equation:

$$Co > \frac{\Delta I_{OUT}{}^{2} \cdot L_o}{V_{out} \cdot \Delta Vout} \tag{4}$$

The following equation calculates the minimum output capacitance needed to meet the output voltage ripple specification.

$$Co > \frac{1}{8 \cdot fsw} \cdot \frac{1}{\frac{V_{RIPPLE}}{I_{RIPPLE}}} \tag{5}$$

Where f_{SW} is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and V_{RIPPLE} is the inductor ripple current.

Input Capacitor

A minimum 10-µF X7R/X5R ceramic input capacitor is recommended to be added between VIN and GND of each converter. The input capacitor must handle the RMS ripple current shown in the following equation.

$$Icirms = Iout \cdot \sqrt{\frac{Vout}{Vin\min} \cdot \frac{(Vin\min - Vout)}{Vin\min}} \tag{6}$$

Bootstrap Capacitor

The device has two integrated boot regulators and requires a small ceramic capacitor between the BST and LX pins to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.047 µF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

Push Button

The push button control is an optional feature. The user can power on and off the PMU without push button by connecting the PB pin to GND. Alternatively, the user can power on and off the PMU by using a push button on/off controller. When the 3.3V LDO's output is more than 2.6V, the internal logic will detect the voltage at PB to determine whether the PB pin is used. When the voltage at PB is zero, the PMU will be activated after detecting PB staying low for at least 20ms. On the other hand, if the voltage at PB is high, the PMU will keep off until the first solid push button signal. After a valid push button signal is asserted, the PMU will follow each dc/dc converter's EN and power up from a valid push button signal.

During power off, once the PB has been pressed, INT is switched low. This warns the system to shut down all housekeeping tasks. During the off period, the PMU will keep off until a new PB signal is received. This “off” state can be overridden by recycling the input power.

Turn On Through Push Button

When the PB pin is not tied to GND, a high to low transition on PB initiates the power on sequence. PB must stay low for a period of 20ms. Once completing this 20mS, the internal EN is asserted and the PMU is turned on.

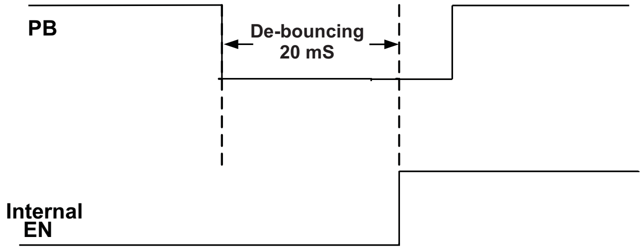


Figure 39. Push Button Turn On

Turn Off Through Push Button

A high to low transition on PB initiates the power off sequence. PB must stay low for a period of 20ms. After completing 20ms, the PMU pulls down the INT to alert the system that the PMU will be shut down within 1024ms. After 1024ms, the PMU will be disabled through an internal EN, which can override the individual EN of each power converter. The PMU will keep off unless there is another from high to low transition on PB or the input power is recycled.

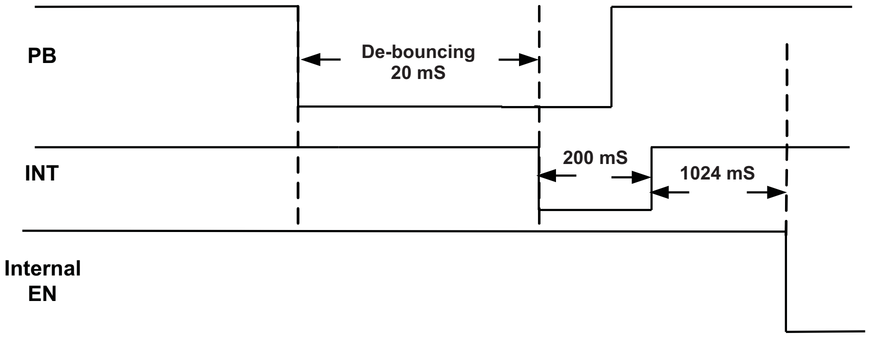


Figure 40. Push Button Trun Off

Delayed Start-Up After pb_in

If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is ~1.67 ms per nF connected to the pin. Note that the EN pins have a weak 1 MΩ pull-up to the 3V3 rail.

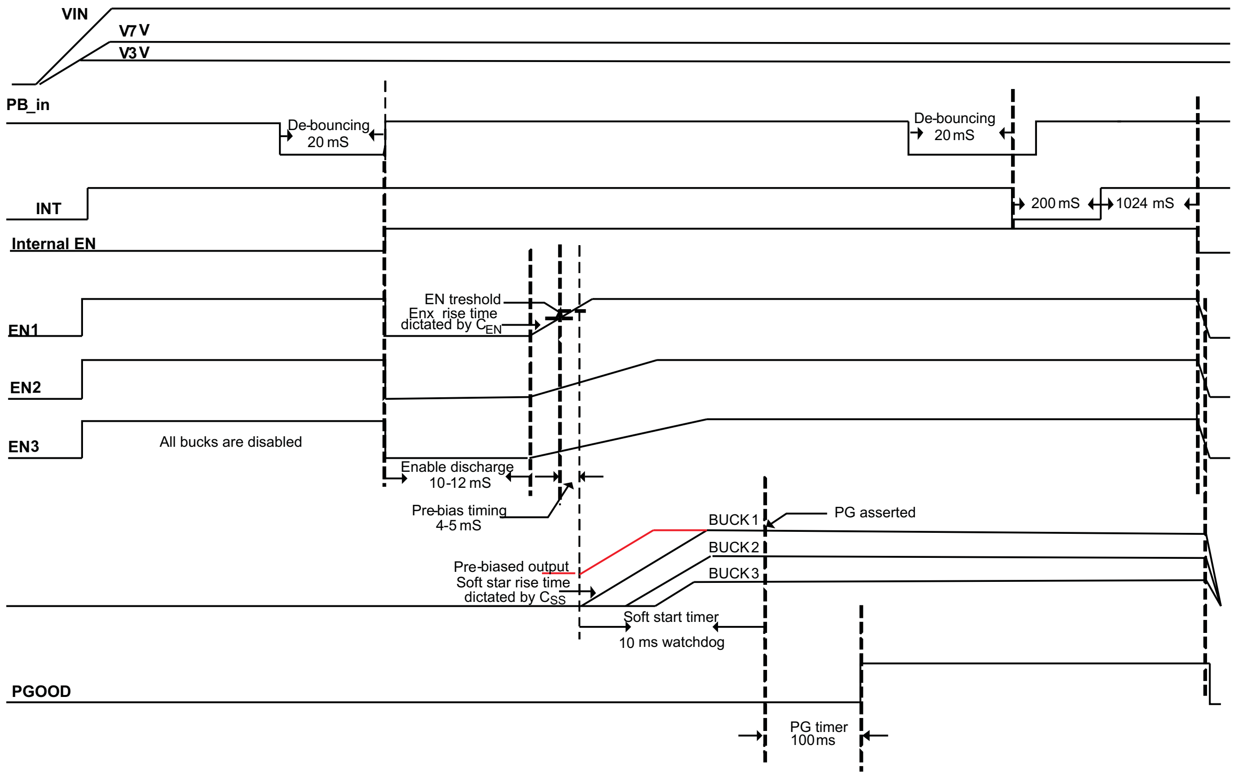


Figure 41. Delayed Start-Up

Out-of-Phase Operation

In order to reduce input ripple current, buck 1 and buck 2 operate 180 degree out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

Soft-Start Time

The device has an internal pull-up current source of 5 µA that charges an external soft-start capacitor to implement a slow start time. Equation 7 shows how to select a soft-start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8 V and the soft-start charge current (I_{SS}) is 5 µA. The soft-start circuit requires 1 nF per around 167 µs to be connected at the SS pin. A 0.8-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant SS pin.

$$T_{ss}(ms) = V_{REF}(V) \bullet \left(\frac{C_{ss}(nF)}{I_{ss}(\mu A)}\right) \tag{7}$$

The Power Good circuit for the bucks has a 10-ms watchdog. Therefore the soft-start time should be lower than this value. It is recommended not to exceed 5 ms.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with a value close to 40 kΩ for the R1 resistor and use Equation 8 to calculate R2.

$$R2 = R1 \cdot \left(\frac{0.8V}{V_O - 0.8V} \right) \tag{8}$$

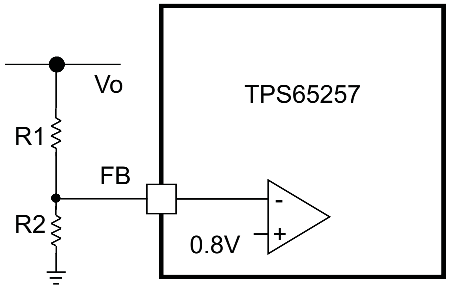


Figure 42. Voltage Divider Circuit

Loop Compensation

TPS65257 is a current mode control DC/DC converter. The error amplifier is a transconductance amplifier with a g_M of 130 µA/V. A typical compensation circuit could be type II (R_c and C_c) to have a phase margin between 60° and 90°, or type III (R_c and C_c and C_{ff} to improve the converter transient response. C_{Roll} adds a high frequency pole to attenuate high-frequency noise when needed. It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

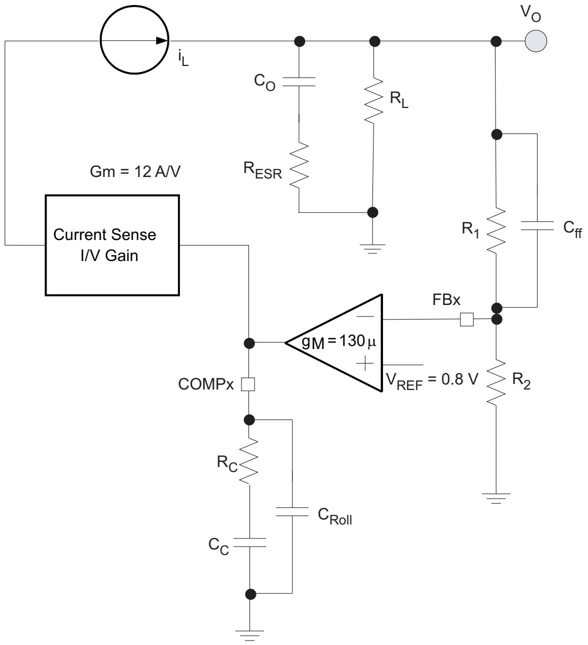


Figure 43. Loop Compensation Scheme

To calculate the external compensation components follow the following steps:

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies around 500 kHz yield best trade off between performance and cost. When using smaller L and C, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Type III circuit recommended for switching frequencies higher than 500 kHz.
Select cross over frequency (f_c) to be at least 1/5 to 1/10 of switching frequency (f_S).	Suggested $f_c = f_S/10$	Suggested $f_c = f_S/10$
Set and calculate R_c.	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$	$R_C = \frac{2\pi \cdot fc \cdot Co}{g_M \cdot gm_{ps}}$
Calculate C_c by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}$	$C_c = \frac{R_L \cdot Co}{R_c}$	$C_c = \frac{R_L \cdot Co}{R_c}$
Add C_{Roll} if needed to remove large signal coupling to high impedance CMP node. Make sure that $fp_{Roll} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_{Roll}}$ is at least twice the cross over frequency.	$C_{Roll} = \frac{\mathrm{Re}\, sr \cdot Co}{R_C}$	$C_{Roll} = \frac{\mathrm{Re}\, sr \cdot Co}{R_C}$
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff}) is smaller than equivalent soft-start frequency ($1/T_{ss}$).	NA	$C_{ff} = \frac{1}{2 \cdot \pi \cdot fz_{ff} \cdot R_1}$

Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control.

Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when both buck converters' outputs are more than 90% of its nominal output voltage.

The default reset time is 100 ms. The polarity of the PGOOD is active high.

Current Limit Protection

Figure 44 shows the (peak) inductor current limit for Buck 1. The typical limit can be approximated with the following graph.

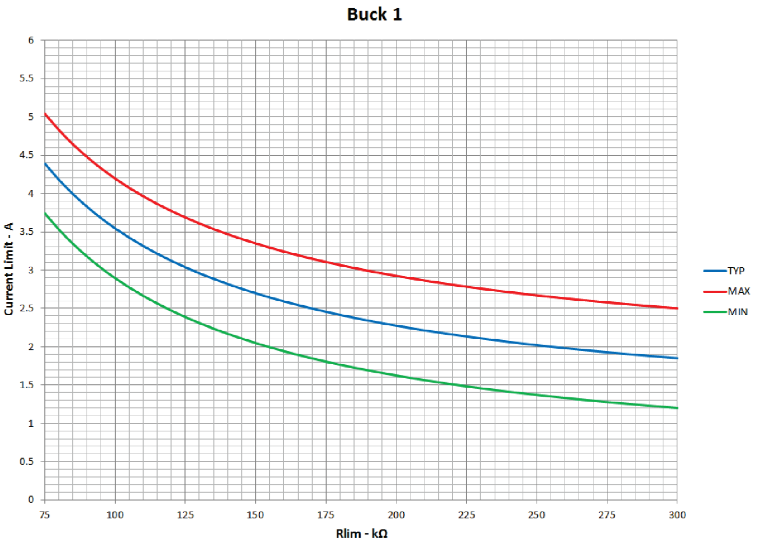


Figure 44. Buck 1

Figure 45 shows the (peak) inductor current limit for Buck 2. The typical limit can be approximated with the following graph.

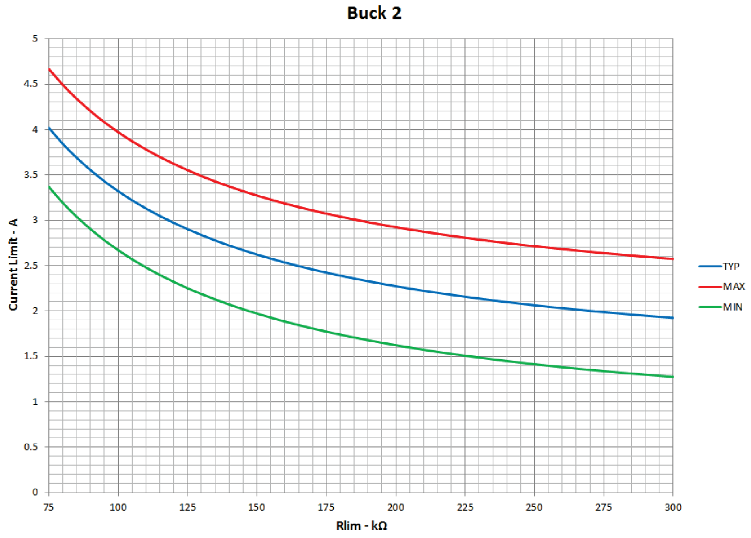


Figure 45. Buck 2

Figure 46 shows the (peak) inductor current limit for Buck 3. The typical limit can be approximated with the following graph.

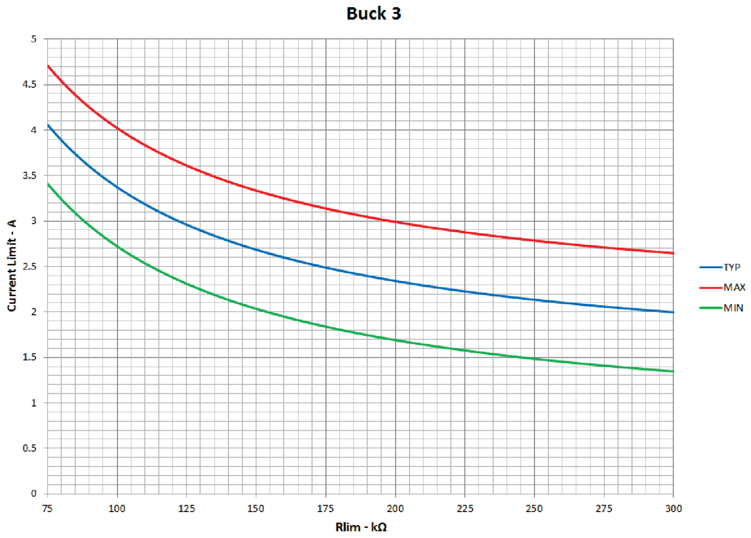


Figure 46. Buck 3

The current limit should be set by using either the TYP or MIN line. If using the TYP line, ensure that limit trips at the MIN line are acceptable for your application. When setting high-side current limit to large current values, ensure that the additional load immediately prior to an overcurrent condition will not cause the switching node voltage to exceed 20 V. Additionally, ensure during worst case operation, with all bucks loaded immediately prior to current limit, the maximum virtual junction temperature of the device does not exceed 125°C.

All converters operate in hiccup mode: Once an over-current lasting more than 10 ms is sensed in any of the converters, they will shut down for 10 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

If an overload condition lasts for less than 10 ms, only the relevant converter affected will shut-down and re-start and no global hiccup mode will occur.

Overvoltage Transient Protection

The device incorporates an overvoltage transient protection (OVP) circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold which is 107%, the high side MOSFET is allowed to turn on the next clock cycle.

Low Power/Pulse Skipping Operation

When a buck synchronous converter operates at light load or standby conditions, the switching losses are the dominant source of power losses. Under these load conditions, TPS65257 uses a pulse skipping modulation technique to reduce the switching losses by keeping the power transistors in the off-state for several switching cycles, while maintaining a regulated output voltage. Figure 47 shows the output voltage and load plus the inductor current.

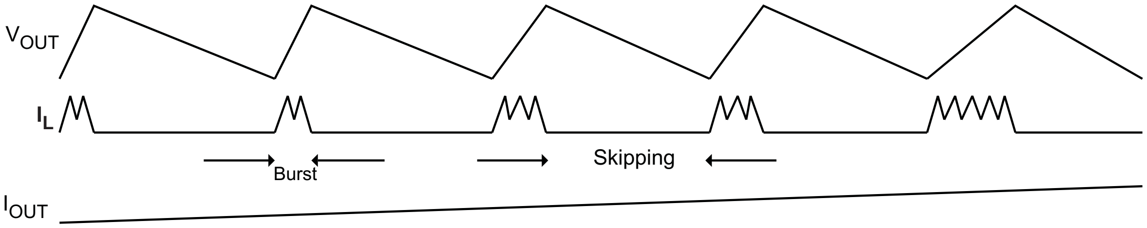


Figure 47. Low Power/Pulse Skipping

During the burst mode, the converter continuously charges up the output capacitor until the output voltage reaches a certain limit threshold. The operation of the converter in this interval is equivalent to the peak inductor current mode control. In each switch period, the main switch is turned on until the inductor current reaches the peak current limit threshold. As the load increases the number of pulses increases to make sure that the output voltage stays within regulation limits. When the load is very light the low power controller has a zero crossing detector to allow the low side mosfet to operate even in light load conditions. The transistor is not disabled at light loads. A zero crossing detection circuit will disable it when inductor current reverses. During the whole process the body diode does not conduct but is used as blocking diode only.

During the skipping interval, the upper and lower transistors are turned off and the converter stays in idle mode. The output capacitors are discharged by the load current until the moment when the output voltage drops to a low threshold.

The choice of output filter will influence the performance of the low power circuit. The maximum ripple during low power mode can be calculated as:

$$V_{OUT\_RIPPLE} = \frac{K_{RIP} T_S}{C_{OUT}} \tag{9}$$

Where K_{RIP} is 1.4 for Buck1 and 0.7 for Buck2 and Buck3. TS can be calculated as:

$$T_S = \frac{0.35}{\left[\left(\frac{V_{IN} - V_{OUT}}{L}\right)\frac{V_{OUT}}{V_{IN}}\right]} \tag{10}$$

USB Switch

The USB switch is enabled (active high) with the USB_EN pin. The switch has a typical resistance of 100mΩ and has a fold-back current limit that is typically 25% lower than the overcurrent detection point. If a continuous short-circuit condition is applied to the USB switch output, the USB switch will shut-down once its temperature reaches 130°C, allowing for the buck converters to operate unaffected. Once the USB switch cools down it will restart automatically.

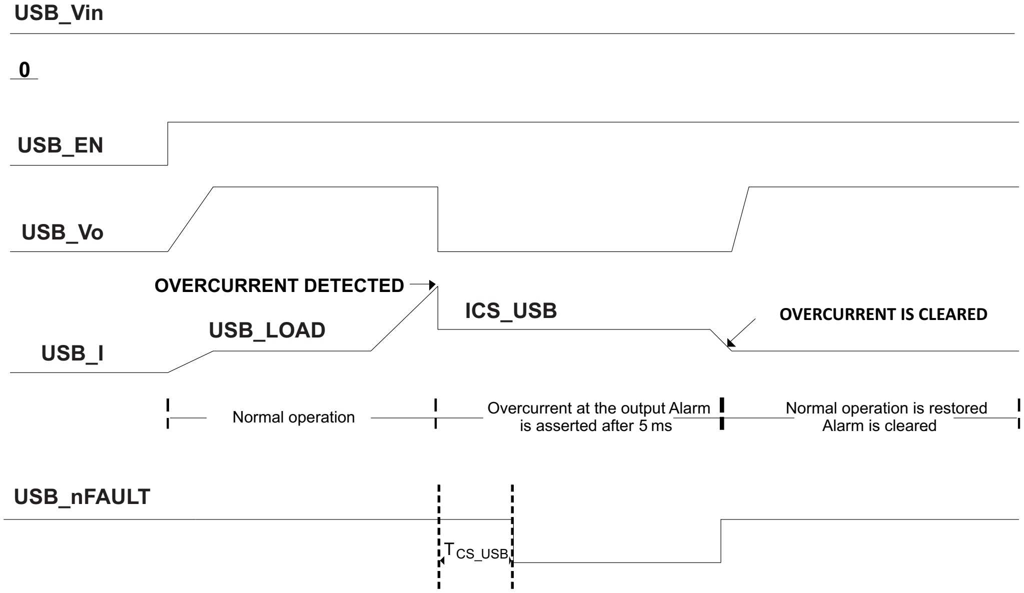
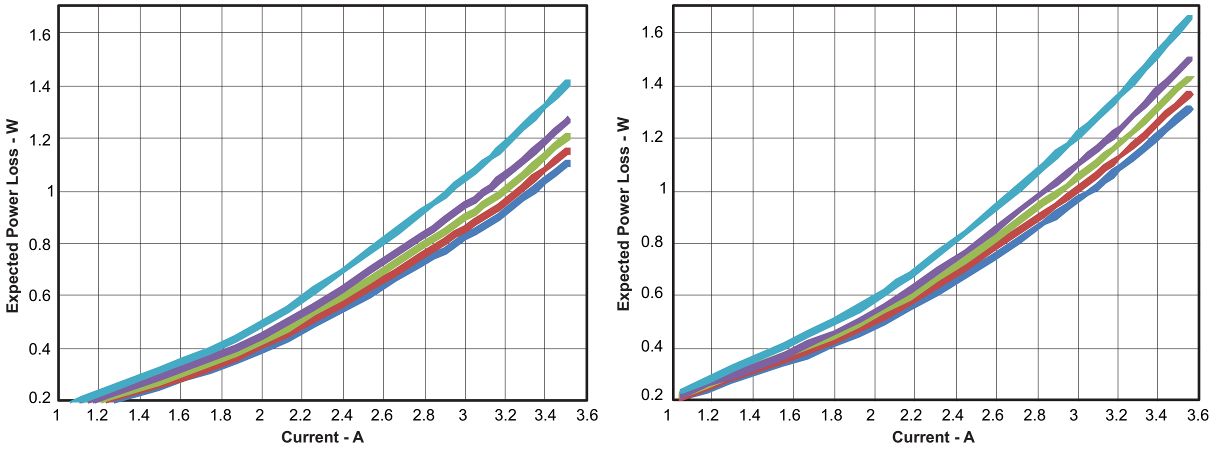


Figure 48. USB Switch

Power Dissipation

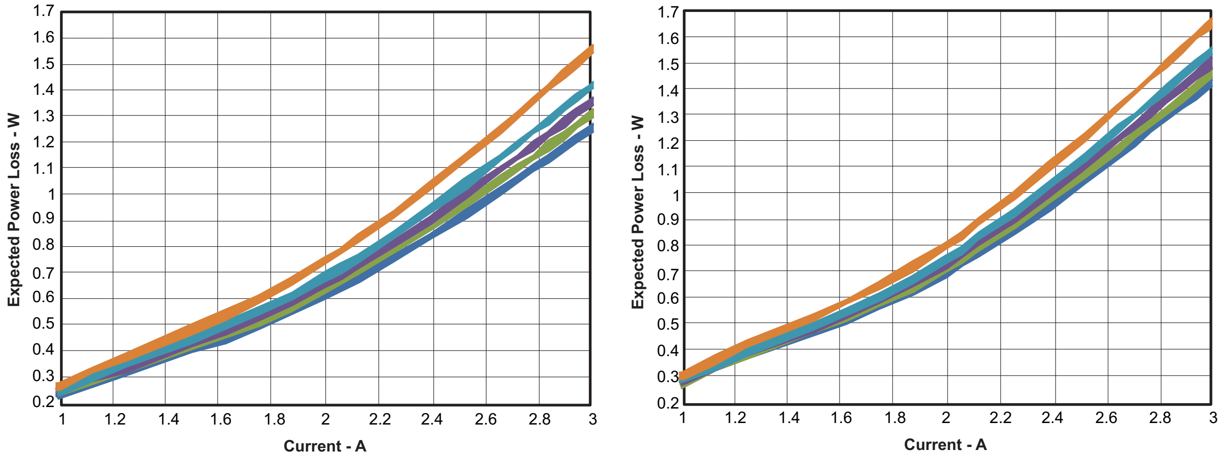
The total power dissipation inside TPS65257 should not to exceed the maximum allowable junction temperature of 125°C. The maximum allowable power dissipation is a function of the thermal resistance of the package (R_{JA}) and ambient temperature. To calculate the temperature inside the device under continuous loading use the following procedure:

1. Define the set voltage for each converter.
2. Define the continuous loading on each converter. Make sure do not exceed the converter maximum loading..
3. Determine from the graphs below the expected losses in watts per converter inside the device. The losses depend on the input supply, the selected switching frequency, the output voltage and the converter chosen.



Buck1 Vin = 12 V, fsw = 500 kHz,
Vo (from top to bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

Buck1 Vin = 12 V, fsw = 1.1 MHz,
Vo (from top to bottom) = 5, 3.3, 2.5, 1.8, 1.2 V



Buck2&3 Vin = 12 V, fsw = 500 kHz,
Vo (from top to bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

Buck2&3 Vin = 12 V, fsw = 1.1 MHz,
Vo (from top to bottom) = 5, 3.3, 2.5, 1.8, 1.2 V

Figure 49. Power Dissipation Curves

4. To calculate the maximum temperature inside the IC use the following formula:

$$T_{HOT\_SPOT} = T_A + P_{DIS} \text{ x } \Theta_{JA} \quad (11)$$

Where:

T_A is the ambient temperature

P_{DIS} is the sum of losses in all converters

Θ_{JA} is the junction to ambient thermal impedance of the device and it is heavily dependant on board layout

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

3.3-V and 6.5 LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 4.7 µF to 10 µF for V7V pin 28
- 3.3 µF to 10 µF for V3V pin 29

Layout Recommendation

Layout is a critical portion of PMIC designs.

- Place tracing for output voltage and LX on the top layer and an inner power plane for VIN.
- Fit also on the top layer connections for the remaining pins of the PMIC and a large top side area filled with ground.
- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65257 device to provide a thermal path from the PowerPad land to ground.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the CMPx pins. The CMPx and ROSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65257RHAR	ACTIVE	VQFN	RHA	40	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65257	Samples
TPS65257RHAT	ACTIVE	VQFN	RHA	40	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR		TPS 65257	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

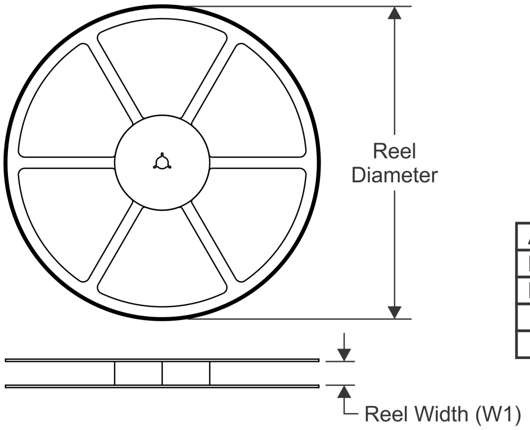
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

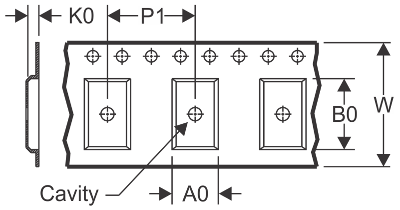
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

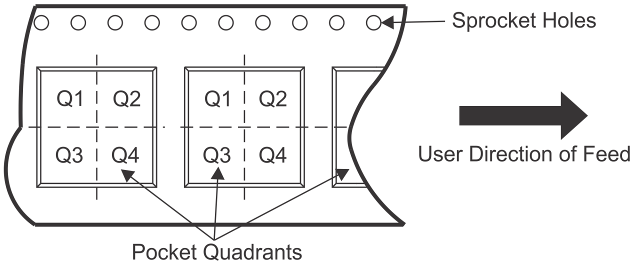


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

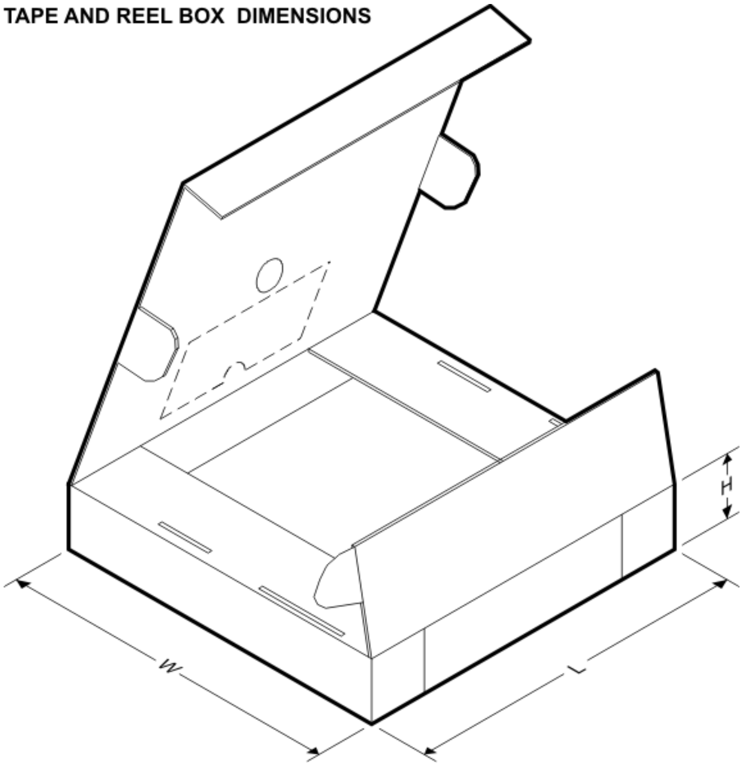
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65257RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65257RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65257RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
TPS65257RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

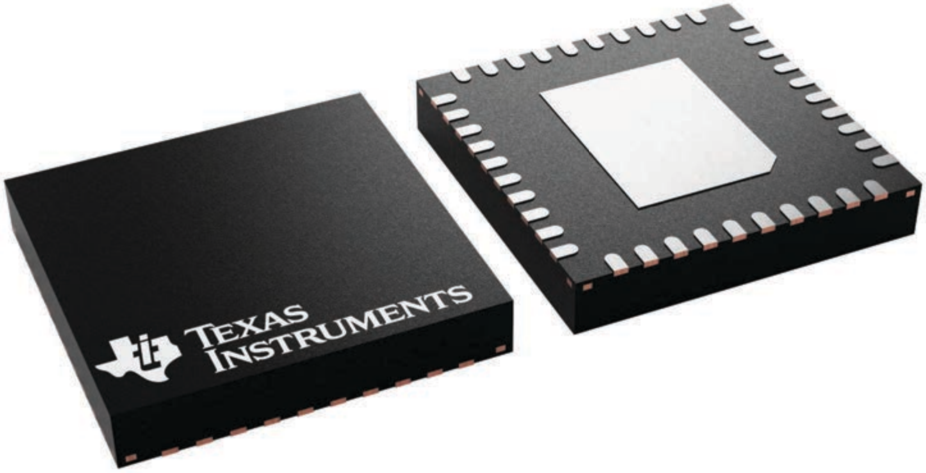
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

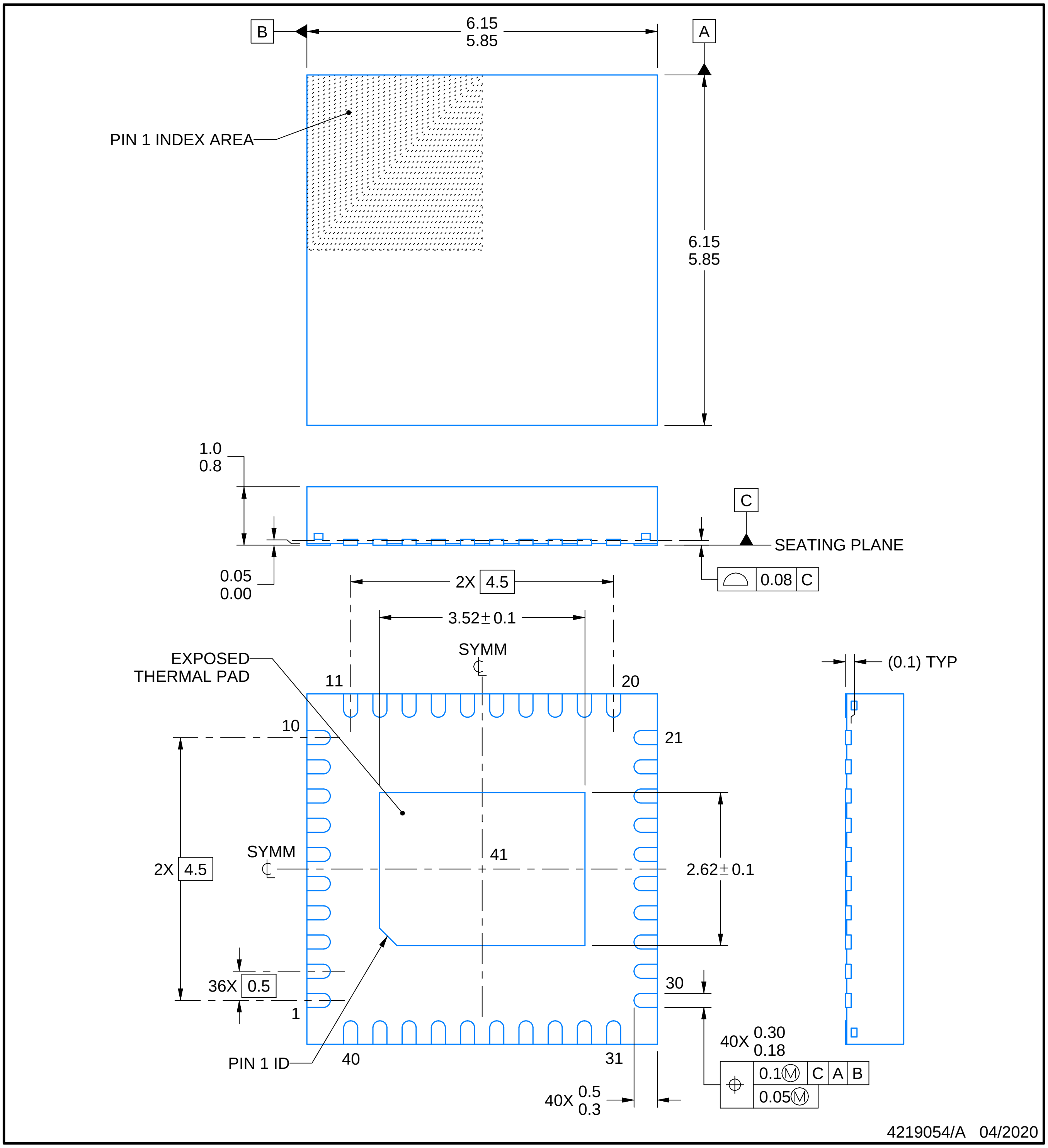


PACKAGE OUTLINE

RHA0040E

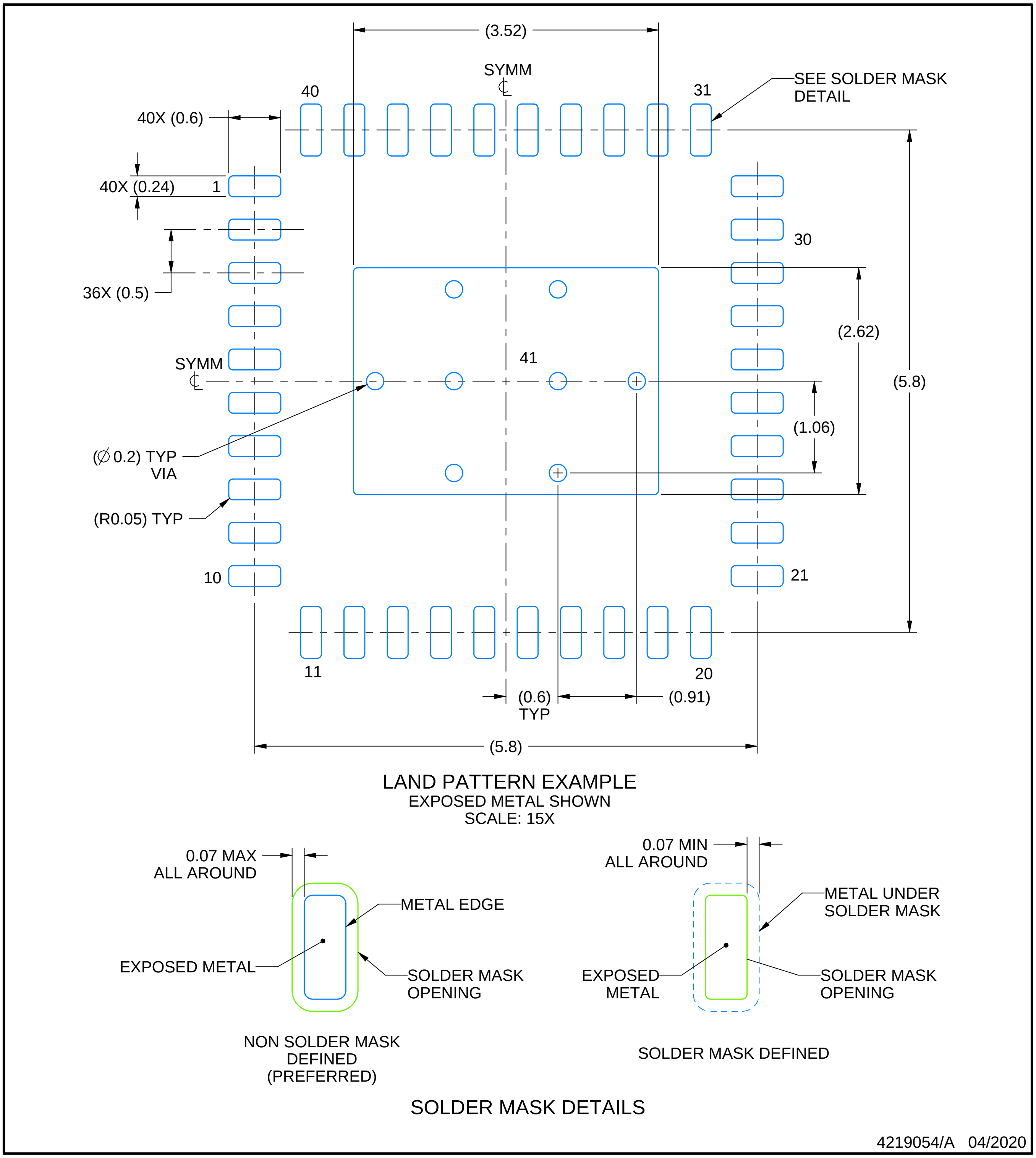
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



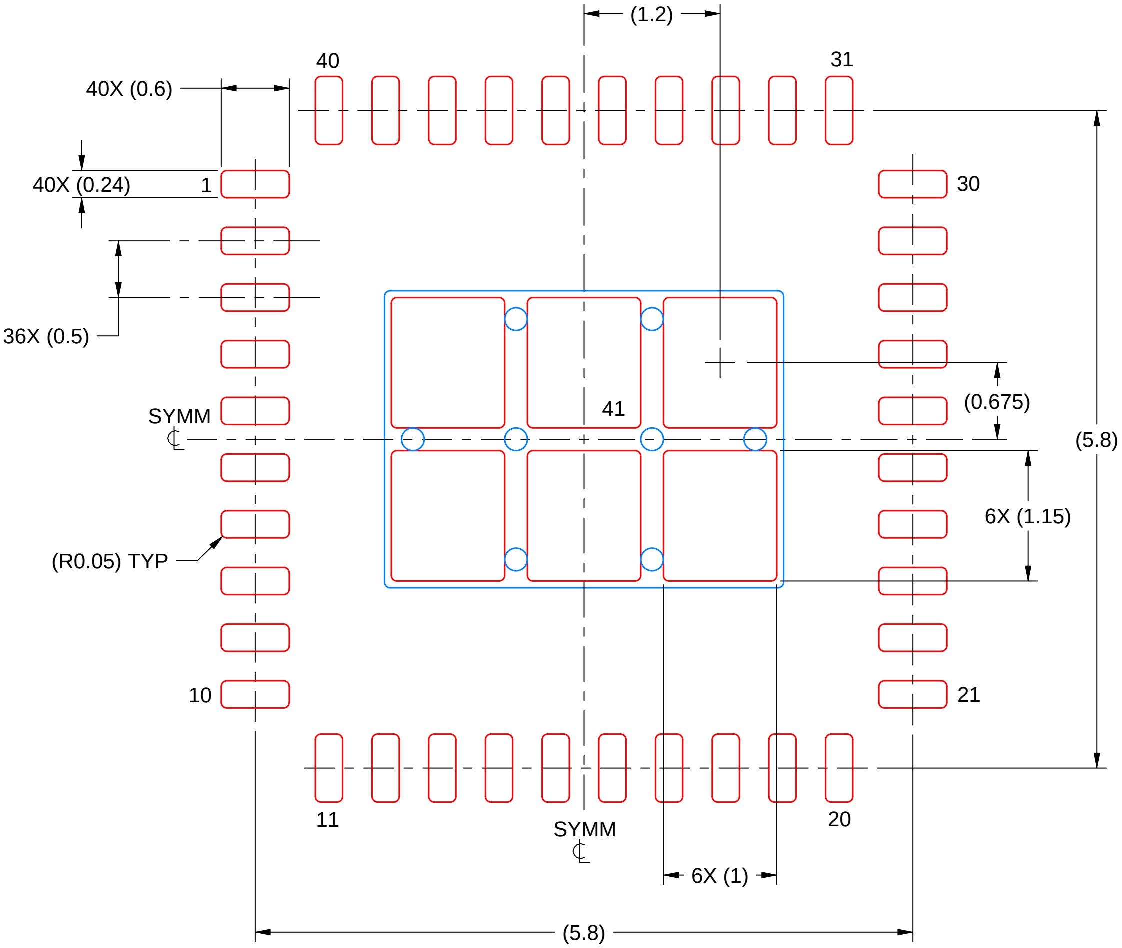
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

SOLDER MASK DETAILS

4219054/A 04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122