TPS536C9T 具有 TLVR 支持、PMBus 和 VR14 SVID 接口的双 channel（N + M ≤ 12 相）D-CAP+™ 降压多相控制器

1 特性

- 输入电压范围：4.5V 至 17V
- 输出电压范围：0.25V 至 5.5V
- 支持 N+M 相位配置（N+M ≤ 12，M ≤ 6）的双路输出
- 自带跨电感稳压器 (TLVR) 拓扑支持，具有 L_C 开路和短路保护
- 与 TI 智能功率级完全兼容
- 支持电压源和电流源 IMON 功率级，具有内部 1kΩ 电阻器
- 支持传统模式和跛行模式功率级故障识别
- 支持布线长度大于 12 英寸的双侧电力输送
- 符合 Intel® VR14 SVID 标准且支持 PSYS
- 向后兼容 VR13.HC/VR13.0 SVID
- 自动 NVM 故障状态记录
- 增强型 D-CAP+ 控制可提供卓越的瞬态性能和出色的动态电流共享
- 可通过可编程阈值实现动态切相，从而提高轻负载和重负载下的效率
- 可通过非易失性存储器 (NVM) 进行配置，从而减少外部组件数量
- 单独的每相位 IMON 校准，具有多斜率增益校准以提高系统精度
- 具有可编程超时的二极管制动，可减少瞬态过冲
- 可编程的每相位谷值电流限制 (OCL)
- PMBus™ v1.3.1 系统接口，用于遥测电压、电流、功率、温度和故障条件
- 可通过 PMBus 对环路补偿进行编程
- 6.00 mm × 6.00 mm，48 引脚，QFN 封装

2 应用

- 数据中心和企业计算 机架式服务器
- 硬件加速器
- 网络接口卡 (NIC)
- ASIC 和 高性能客户端

3 说明

TPS536C9T 是一款符合 VR14 SVID 标准的降压控制器，具有跨电感稳压器 (TLVR) 拓扑支持、双通道、内置非易失性存储器 (NVM) 和 PMBus™ 接口，而且与 TI 智能功率级完全兼容。D-CAP+ 架构等高级控制特性可提供快速瞬态响应、低输出电容和良好的动态电流共享。还本地支持输出电压转换率和自适应电压定位的可调控制。此外，该器件还支持 PMBus 通信接口，可向主机系统报告遥测的电压、电流、功率、温度和故障状况。所有可编程参数均可通过 PMBus 接口进行配置，而且可作为新的默认值存储在 NVM 中，以尽可能减少外部组件数量。

封装信息

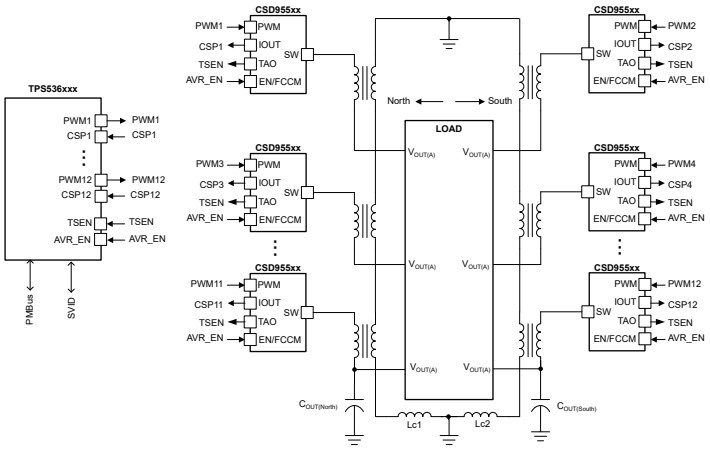
器件型号	封装(1)	封装尺寸(2)
TPS536C9T	RSL（QFN，48）	6.00 mm × 6.00 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。

器件信息

器件型号(1)	相位数
TPS536C9T	12 相位

(1) 请参阅*器件比较表*



简化版应用（交错式 TLVR）

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
September 2023	*	Initial Release

5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

5.1 Documentation Support

5.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

5.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Intel® is a registered trademark of Intel Corporation.
所有商标均为其各自所有者的财产。

5.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 Package Option Addendum

6.2 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (5) (6)
TPS536C9TRSLR	ACTIVE	VQFN	RSL	48	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	–40 to 125	TPS 536C9T

1. The marketing status values are defined as follows:
   ACTIVE: Product device recommended for new designs.
   LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
   PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
   OBSOLETE: TI has discontinued the production of the device.

2. Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
   TBD: The Pb-Free/Green conversion plan has not been defined.
   Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
   Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
   Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

3. MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

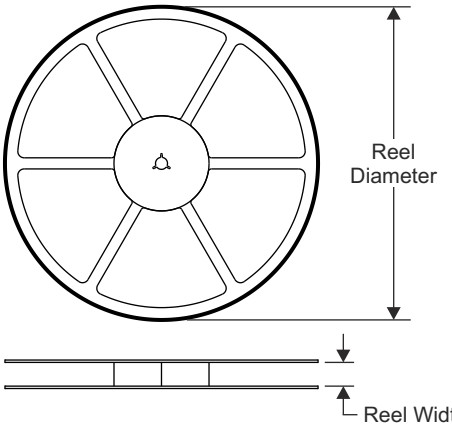
4. Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

5. There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

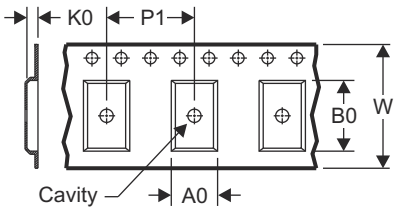
6. Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

6.3 Tape and Reel Information

REEL DIMENSIONS

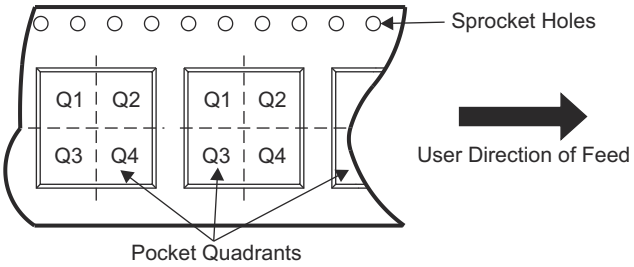


TAPE DIMENSIONS



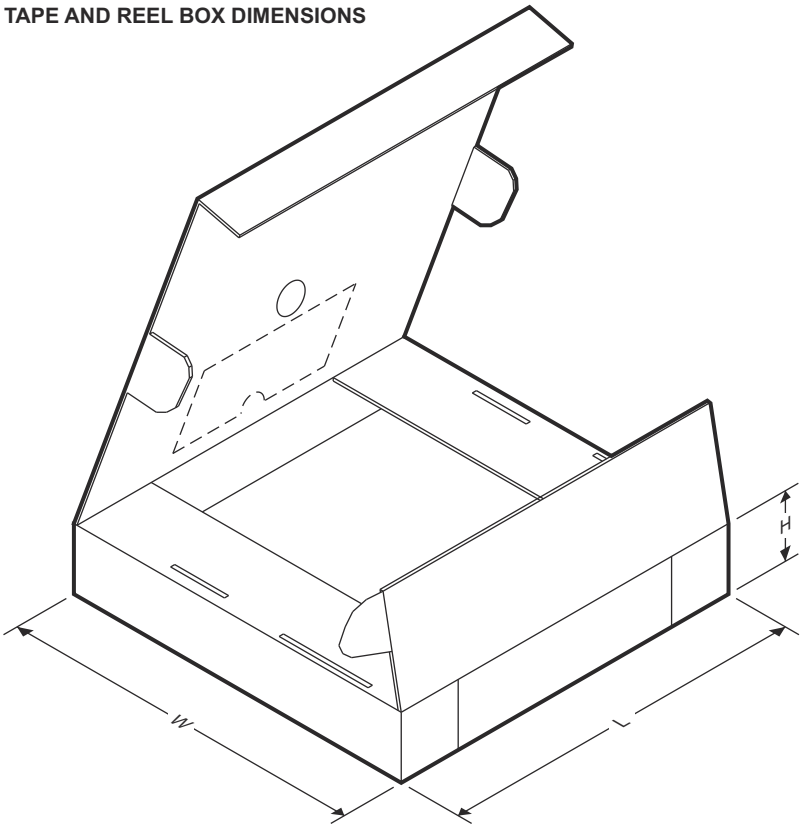
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS536C9TRSLR	VQFN	RSL	48	3000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

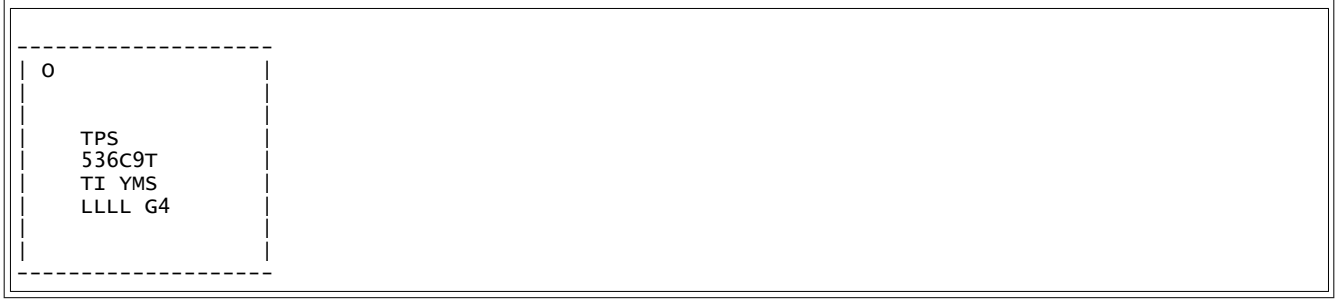
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS536C9TRSLR	VQFN	RSL	48	3000	367.0	367.0	38.0

Top Side Markings

Top-Side Markings
TPS536C9T



TI = The letters "TI" for Texas Instruments

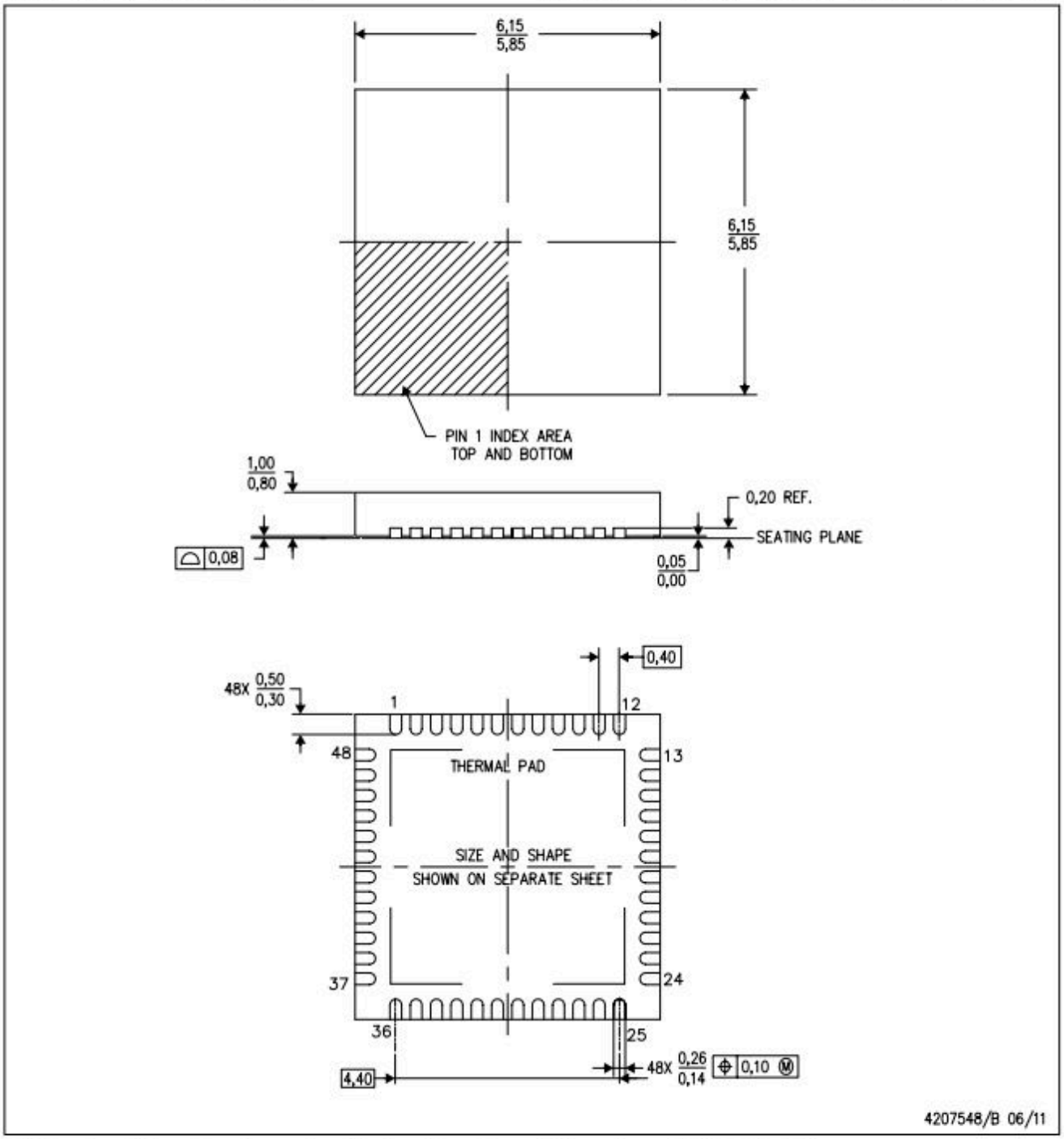
Y = Year (Last digit of the year assembled, 0=2020, 1=2021, ...)

M = Month (1=Jan, 2=Feb, … A=Oct, B=Nov, C=Dec)

S = Assembly Site Code

LLLL = Assembly Lot Trace Code

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

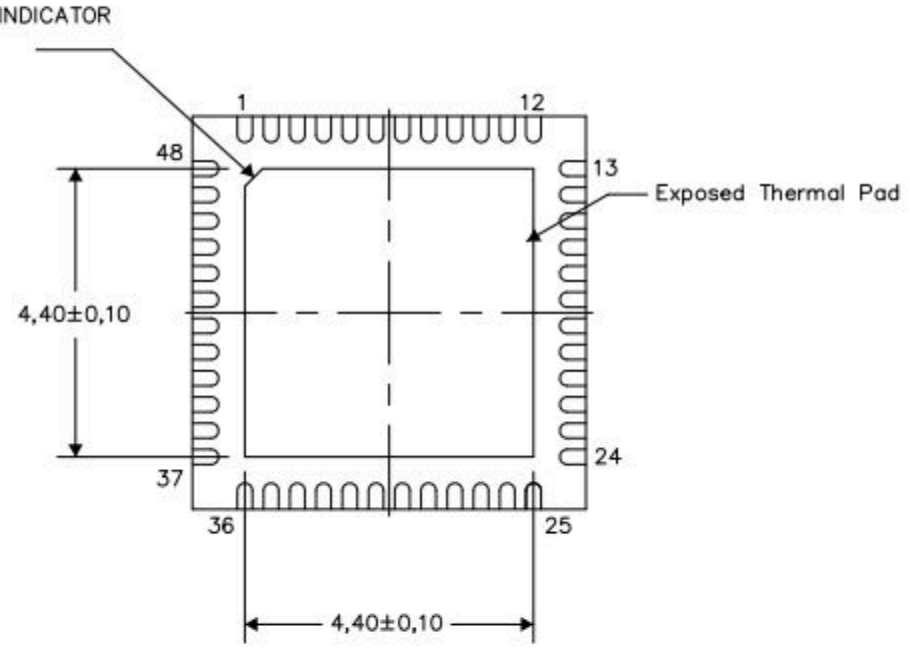
RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



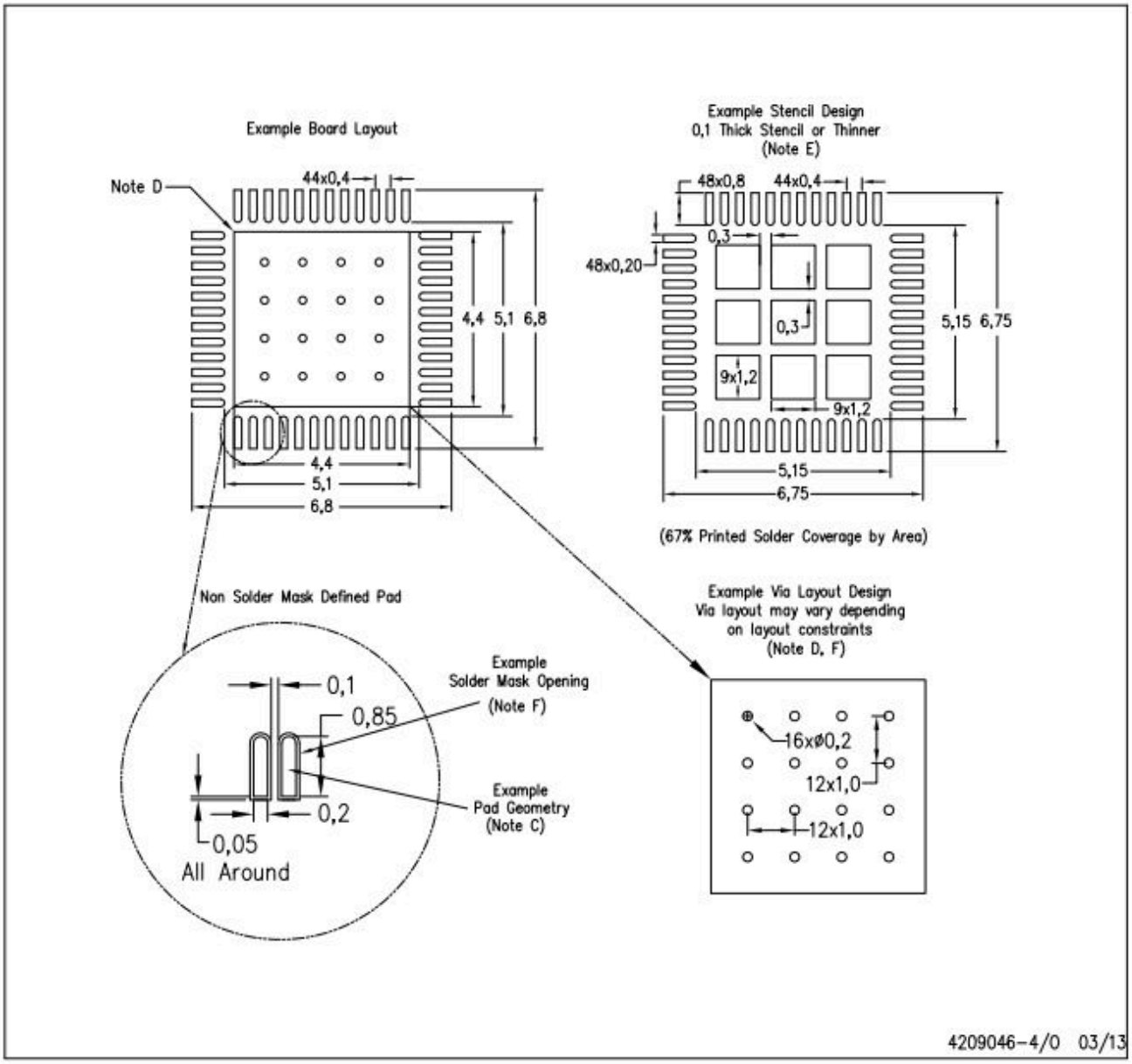
Bottom View

Exposed Thermal Pad Dimensions

4207841–2/P 03/13

NOTE: All linear dimensions are in millimeters

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS536C9TRSLR	ACTIVE	VQFN	RSL	48	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 536C9T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

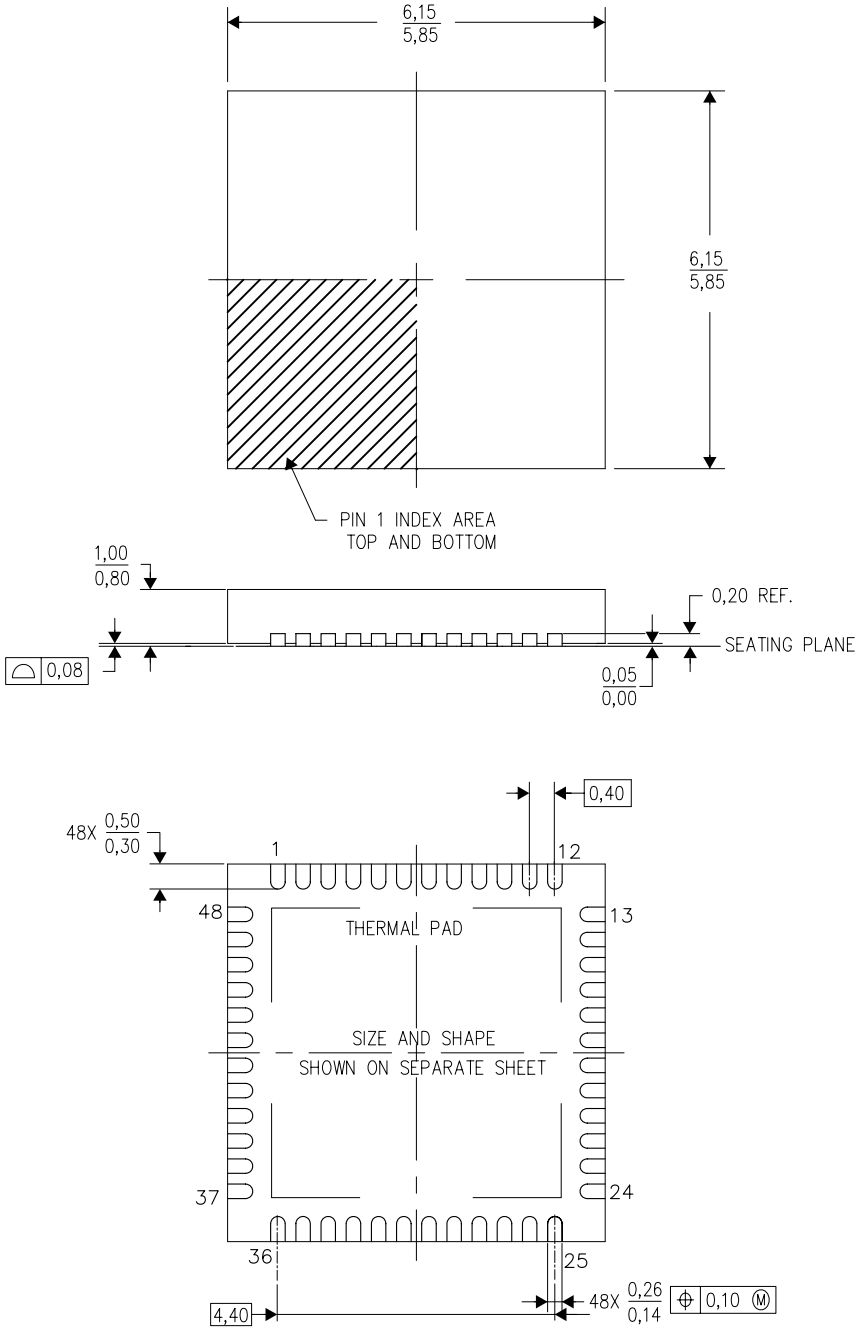
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



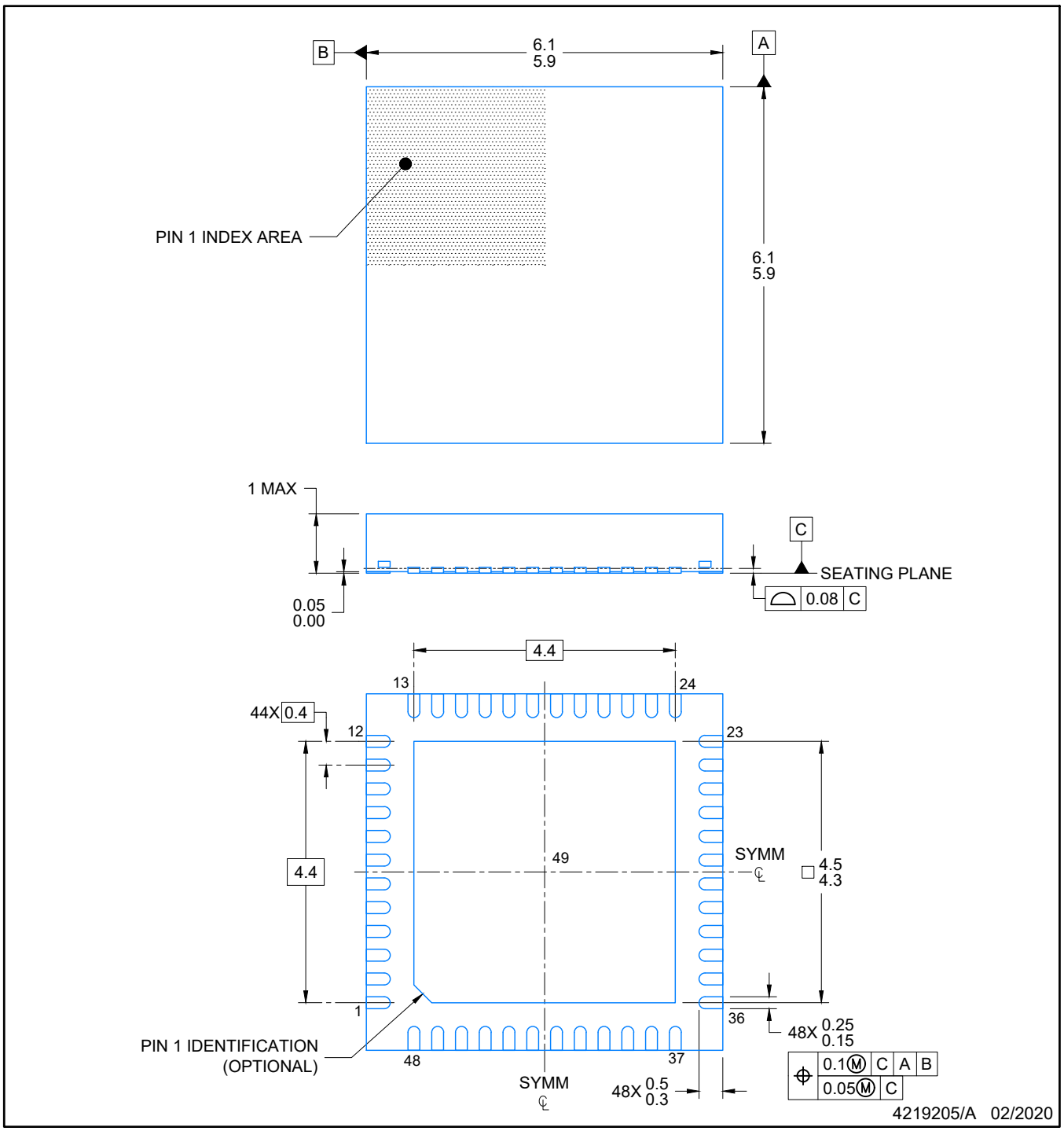
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

PACKAGE OUTLINE

RSL0048B

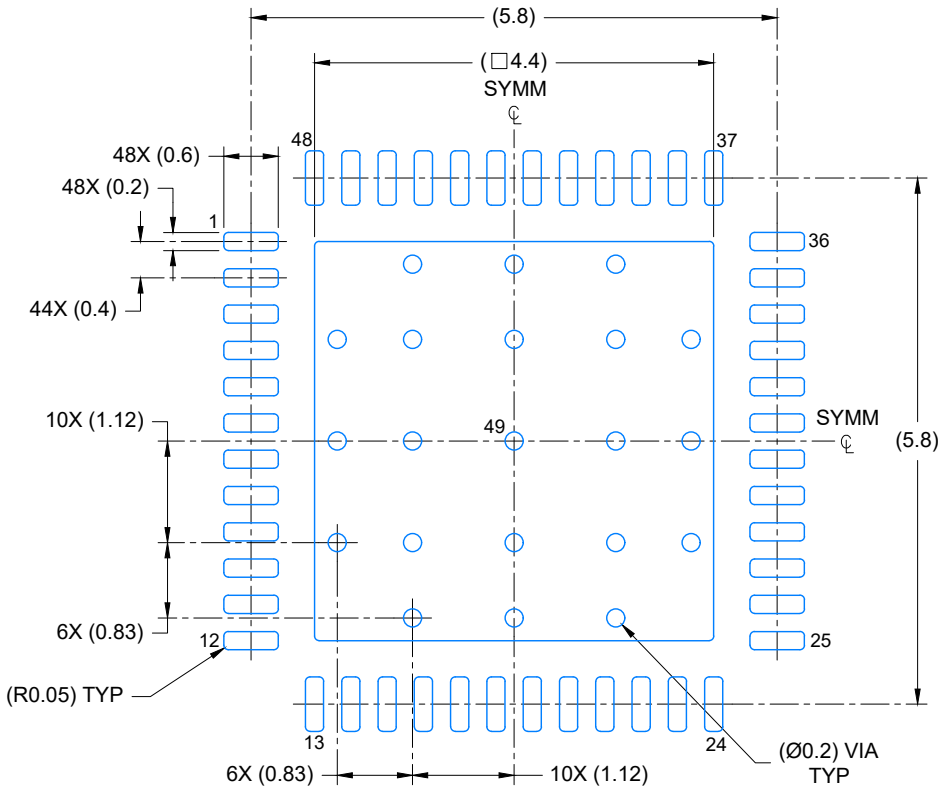
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

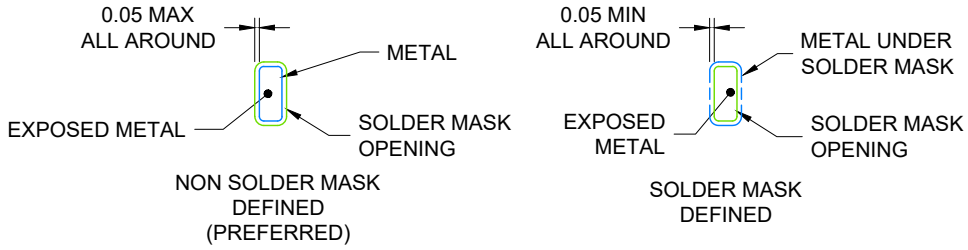


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

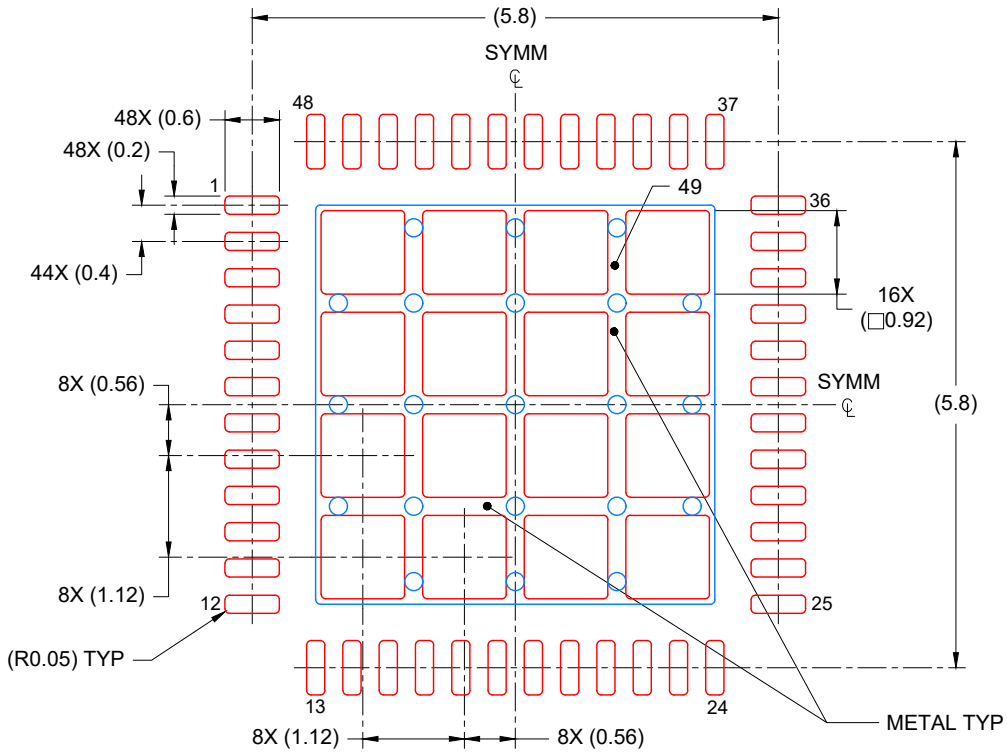


SOLDER MASK DETAILS

4219205/A 02/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
70% PRINTED COVERAGE BY AREA
SCALE: 12X

4219205/A 02/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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