TPS51604用于高频 CPU 内核功率的同步降压 FET 驱动器

1 特性

- 针对已优化连续传导模式 (CCM) 的精简死区时间驱动电路
- 针对已优化断续传导模式 (DCM) 效率的自动零交叉检测
- 针对已优化轻负载效率的多个低功耗模式
- 为了实现高效运行的经优化信号路径延迟
- 针对超级本 (Ultrabook) FET 的集成 BST 开关驱动强度
- 针对 5V FET 驱动而进行了优化
- 转换输入电压范围 (V_{IN})：4.5V 至 28V
- 2mm × 2mm 8 引脚 WSON 散热垫封装

2 应用

- 使用高频 CPU 且具有以下电源输入的平板电脑：
  - 适配器
  - 电池
  - NVDC
  - 5V 至 12V 电源轨

3 说明

TPS51604 驱动器针对高频 CPU V_{CORE} 应用 进行了优化。具有 降低 死区时间驱动和自动零交越等高级特性，可用于在整个负载范围内优化效率。

$\overline{\text{SKIP}}$ 引脚提供 CCM 操作选项，以支持输出电压的受控管理。此外，TPS51604 支持两种低功耗模式。借助于脉宽调制 (PWM) 输入三态，静态电流被减少至 130µA，并支持立即响应。当 $\overline{\text{SKIP}}$ 被保持在三态时，电流被减少至 8µA（恢复切换通常需要 20µs）。此驱动器与合适的德州仪器 (TI) 控制器配对使用，能够成为出色的高性能电源系统。

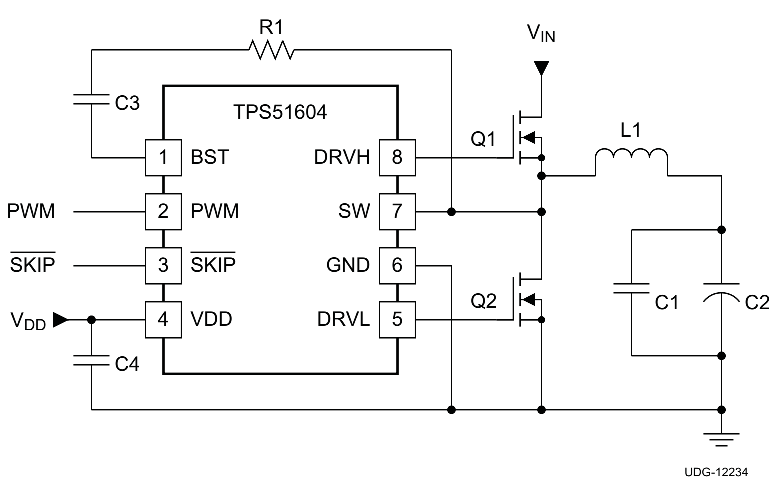
TPS51604 器件采用节省空间的耐热增强型 8 引脚 2mm x 2mm WSON 封装，工作温度范围为 -40°C 至 105°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS51604	WSON (8)	2.00mm x 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

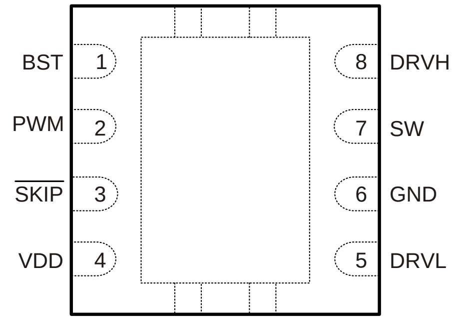
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (August 2013) to Revision B | **Page**

- *添加了 ESD 额定值 表、特性 说明部分，器件功能模式部分，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分* 1

5 Pin Configuration and Functions

DSG Package
8-Pin WSON
Top View



Pin Functions

PIN		I/O [(1)]	DESCRIPTION
NAME	**NO.**		
BST	1	I	High-side N-channel FET bootstrap voltage input; power supply for high-side driver
DRVH	8	O	High-side N-channel gate drive output
DRVL	5	O	Synchronous low-side N-channel gate drive output
GND	6	G	Synchronous low-side N-channel gate drive return and device reference
PWM	2	I	PWM input. A tri-state voltage on this pin turns off both the high-side (DRVH) and low-side drivers (DRVL)
$\overline{\text{SKIP}}$	3	I	When $\overline{\text{SKIP}}$ is LO, the zero crossing comparator is active. The power chain enters discontinuous conduction mode when the inductor current reaches zero. When $\overline{\text{SKIP}}$ is HI, the zero crossing comparator is disabled, and the driver outputs follow the PWM input. A tri-state voltage on $\overline{\text{SKIP}}$ puts the driver into a very-low power state.
SW	7	I/O	High-side N-channel gate drive return. Also, zero-crossing sense input
VDD	4	I	5-V power supply input; decouple to GND with a ceramic capacitor with a value of 1 µF or greater
Thermal Pad		G	Tie to system GND plane with multiple vias

(1) I = Input, O = Output, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings[(1)] [(2)]

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VDD	–0.3	6	V
	PWM, $\overline{\text{SKIP}}$	–0.3	6	
Output voltage	BST	–0.3	35	V
	BST (transient <20 ns)	–0.3	38	
	BST to SW; DRVH to SW	–0.3	6	
	SW	–2	30	
	DRVH, SW (transient <20 ns)	–5	38	
	DRVL	–0.3	6	
Ground pins	GND to PAD	–0.3	0.3	V
Operating junction temperature, T_J		–40	125	°C
Storage temperature range, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VDD	4.5	5	5.5	V
	PWM, $\overline{\text{SKIP}}$	–0.1		5.5	
Output voltage	BST	–0.1		34	V
	BST to SW; DRVH to SW	–0.1		5.5	
	SW	–1		28	
	DRVL	–0.1		5.5	
Ground pins	GND to PAD	–0.1		0.1	V
Operating junction temperature, T_J		–40		105	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS51604 WSON (DSG) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.7	°C/W

(1) 有关传统和新热指标的更多信息，请参见应用报告《*半导体和 IC 封装热指标*》（文献编号：SPRA953）。

6.5 Electrical Characteristics

These specifications apply for –40°C ≤ T_J ≤ 105°C, and V_{VDD} = 5 V unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD INPUT SUPPLY						
I_{CC}	Supply current (operating)	$V_{\overline{SKIP}}$ = V_{VDD} or $V_{\overline{SKIP}}$ = 0 V, PWM = High		160	600	µA
		$V_{\overline{SKIP}}$ = V_{VDD} or $V_{\overline{SKIP}}$ = 0 V, PWM = Low		250		
		$V_{\overline{SKIP}}$ = V_{VDD} or $V_{\overline{SKIP}}$ = 0 V, PWM = Float		130		
		$V_{\overline{SKIP}}$ = Float		8		
VDD UNDERVOLTAGE LOCKOUT (UVLO)						
V_{UVLO}	UVLO threshold	Rising threshold			4.15	V
		Falling threshold	3.7			
V_{UVHYS}	UVLO hysteresis			0.2		V
PWM AND $\overline{SKIP}$ I/O SPECIFICATIONS						
R_I	Input impedance	Pullup to VDD		1.7		MΩ
		Pulldown (to GND)		800		kΩ
V_{IL}	Low-level input voltage				0.6	V
V_{IH}	High-level input voltage		2.65			V
V_{IHH}	Hysteresis			0.2		V
V_{TS}	Tri-state voltage		1.3		2.0	V
$t_{THOLD(off1)}$	Tri-state activation time (falling) PWM			60		ns
$t_{THOLD(off2)}$	Tri-state activation time (rising) PWM			60		ns
t_{TSKF}	Tri-state activation time (falling) $\overline{SKIP}$			1		µs
t_{TSKR}	Tri-state activation time (rising) $\overline{SKIP}$			1		µs
$t_{3RD(PWM)}$	Tri-state exit time PWM				100	ns
$t_{3RD(\overline{SKIP})}$	Tri-state exit time $\overline{SKIP}$				50	µs
HIGH-SIDE GATE DRIVER (DRVH)						
$t_{R(DRVH)}$	Rise time	DRVH rising, C_{DRVH} = 3.3 nF; 20% to 80%		30		ns
$t_{RPD(DRVH)}$	Rise time propogation delay	C_{DRVH} = 3.3 nF		40		ns
R_{SRC}	Source resistance	Source resistance, (V_{BST}– V_{SW}) = 5 V, high state, (V_{BST} – V_{DRVH}) = 0.1 V		4	8	Ω
$t_{F(DRVH)}$	Fall time	DRVH falling, C_{DRVH} = 3.3 nF		8		ns
$t_{FPD(DRVH)}$	Fall-time propagation delay	C_{DRVH} = 3.3 nF		25		ns
R_{SNK}	Sink resistance	Sink resistance, (V_{BST} – V_{SW}) forced to 5 V, low state (V_{DRVH} – V_{SW}) = 0.1 V		0.5	1.6	Ω
R_{DRVH}	DRVH to SW resistance (1)			100		kΩ

(1) Specified by design. Not production tested.

Electrical Characteristics (接下页)

These specifications apply for –40°C ≤ T_J ≤ 105°C, and V_{VDD} = 5 V unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-SIDE GATE DRIVER (DRVL)						
$t_{R(DRVL)}$	Rise time	DRVL rising, C_{DRVL} = 3.3 nF; 20% to 80%		15		ns
$t_{RPD(DRVL)}$	Rise time propagation delay	C_{DRVL} = 3.3 nF		35		ns
R_{SRC}	Source resistance	Source resistance, (V_{VDD}–GND) = 5 V, high state, (V_{VDD} – V_{DRVL}) = 0.1 V		1.5	3	Ω
$t_{F(DRVL)}$	Fall time	DRVL falling, C_{DRVL} = 3.3 nF		10		ns
$t_{FPD(DRVL)}$	Fall-time propagation delay	C_{DRVL}= 3.3 nF		15		ns
R_{SNK}	Sink resistance	Sink resistance, (V_{VDD}– GND) = 5 V, low state, (V_{DRVL} – GND) = 0.1 V		0.4	1.6	Ω
R_{DRVL}	DRVL to GND resistance(1)			100		kΩ
GATE DRIVER DEAD-TIME						
$t_{R(DT)}$	Rising edge		0	20	35	ns
$t_{F(DT)}$	Falling edge		0	10	25	ns
ZERO CROSSING COMPARATOR						
V_{ZX}	Zero crossing offset	SW voltage rising	–2.25	0	2.00	mV
BOOTSTRAP SWITCH						
V_{FBST}	Forward voltage	I_F = 10 mA		120	240	mV
I_{RLEAK}	Reverse leakage	(V_{BST} – V_{VDD}) = 25 V			2	µA
$R_{DS(on)}$	On-resistance			12	24	Ω

6.6 Typical Characteristics

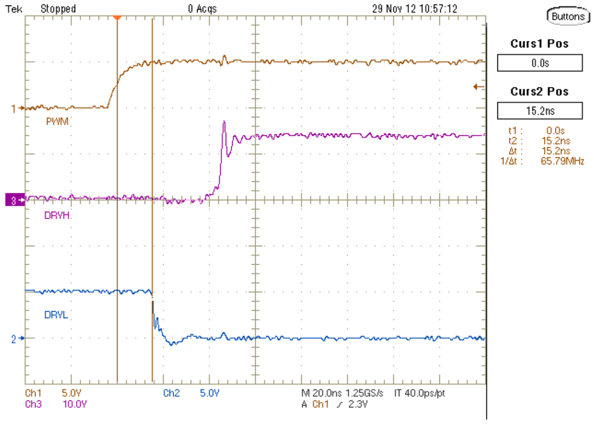


图 1. PWM High to DRVL Low

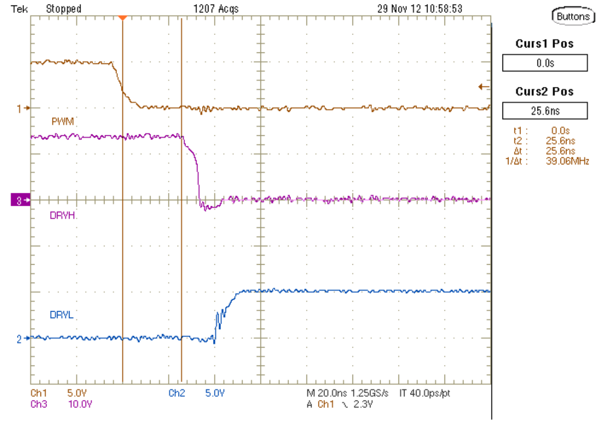


图 2. PWM Low to DRVH Low

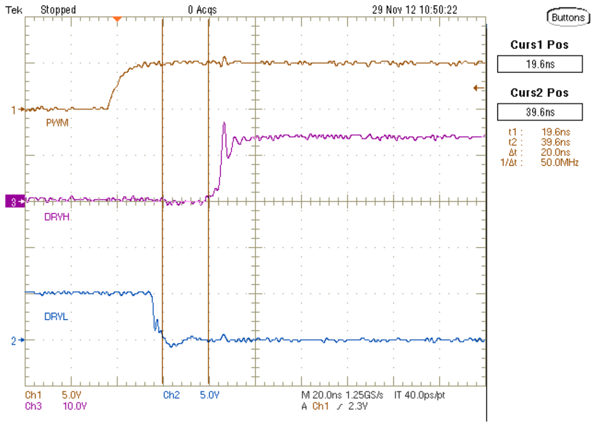


图 3. DRVL Low to DRVH High

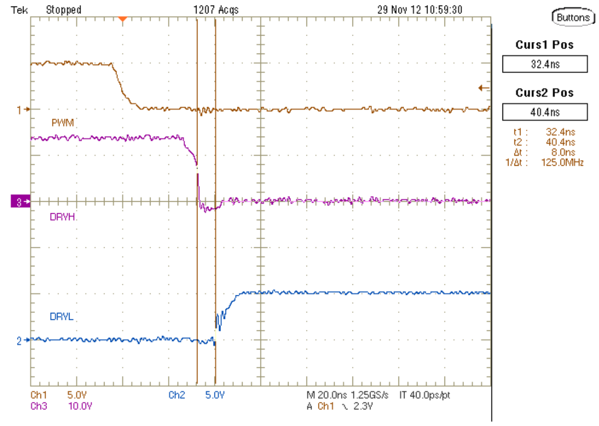


图 4. DRVH Low to DRVL High

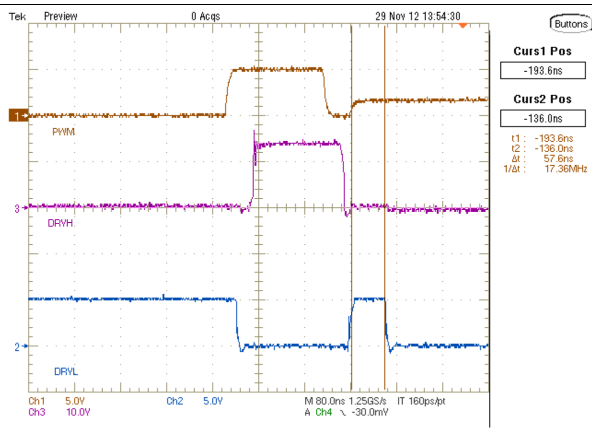


图 5. PWM Low to Tri-State

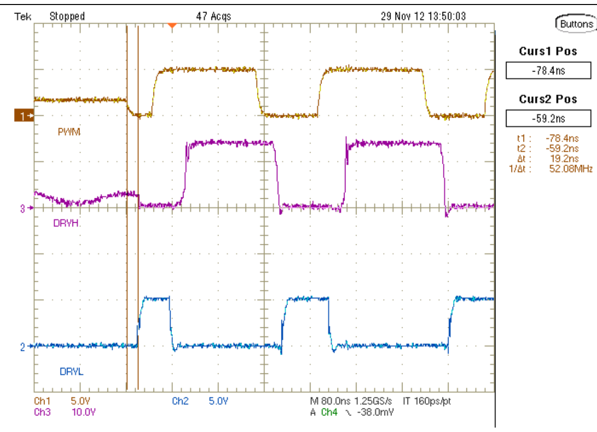


图 6. PWM Tri-State to Low

Typical Characteristics (接下页)

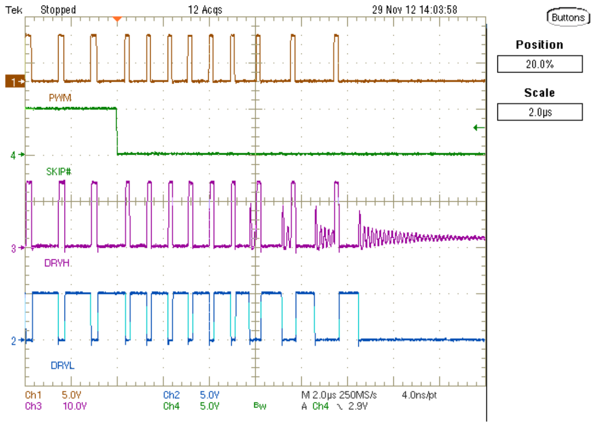


图 7. SKIP Mode Entry

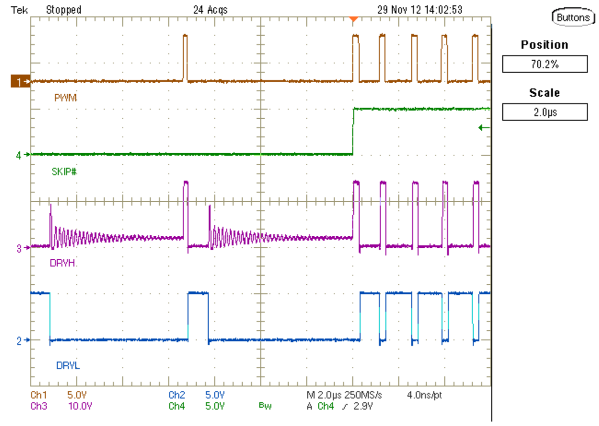


图 8. SKIP Mode Exit

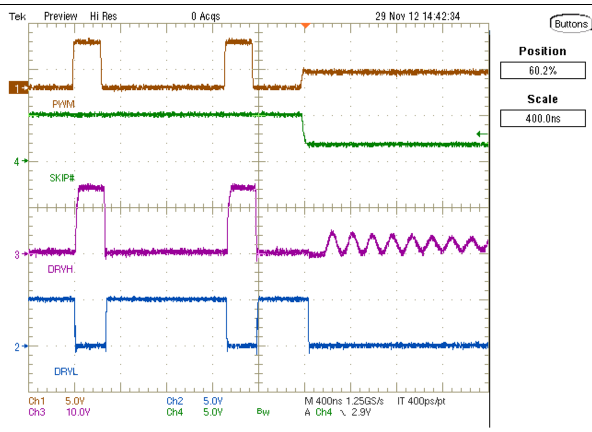


图 9. Very-Low-Power Mode Entry

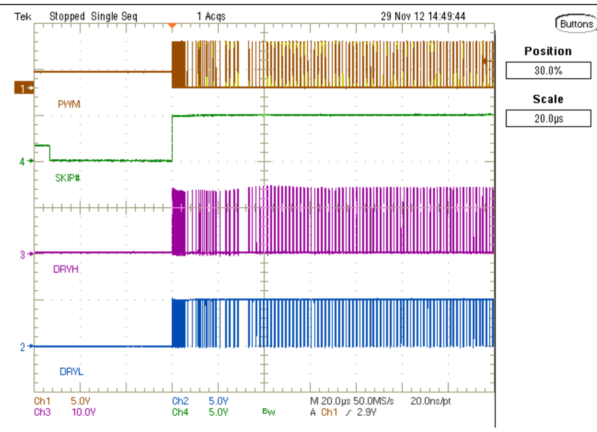
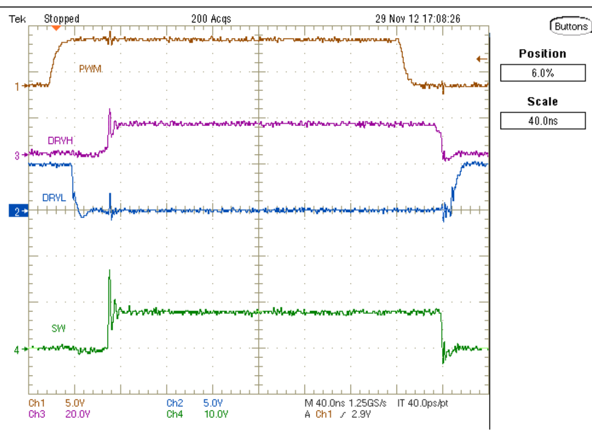
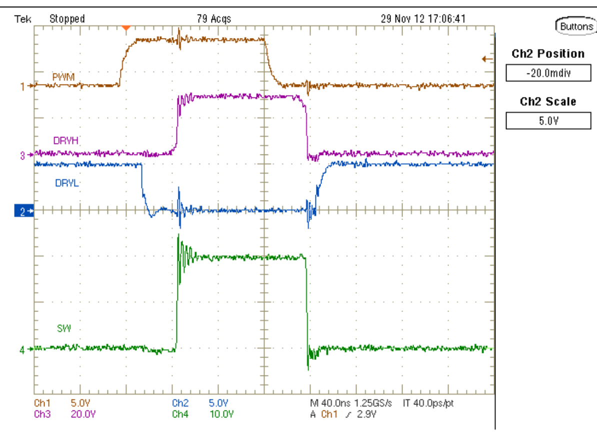


图 10. Very-Low-Power Mode Exit



V_{IN} = 8 V

图 11. SW Node-Ringing

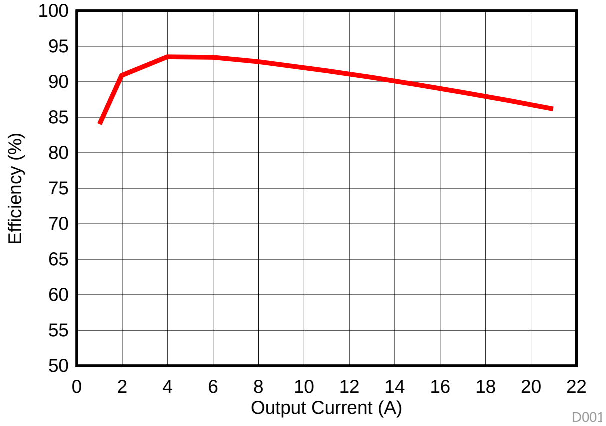


V_{IN} = 20 V

图 12. SW Node-Ringing

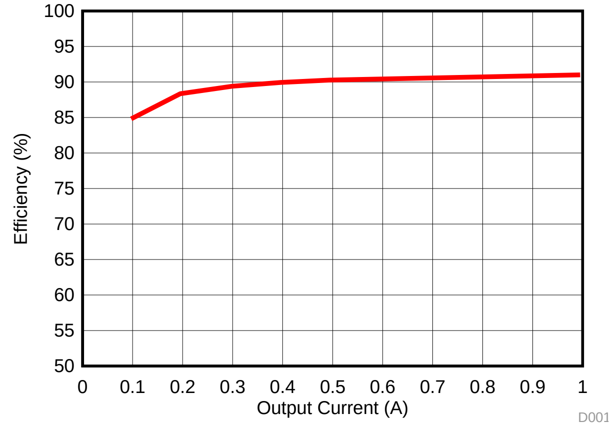
6.7 Typical Power Block MOSFET Characteristics

Power block MOSFET: CSD87330, Inductor: 0.22 µF, 1.1-mΩ DCR



FCCM
V_{IN} = 7.4 V
V_{OUT} = 1.8 V
f_{SW} = 800 kHz

图 13. Efficiency vs Output Current, FCCM



Skip Mode
V_{IN} = 7.4 V
V_{OUT} = 1.8 V
f_{SW} = 800 kHz

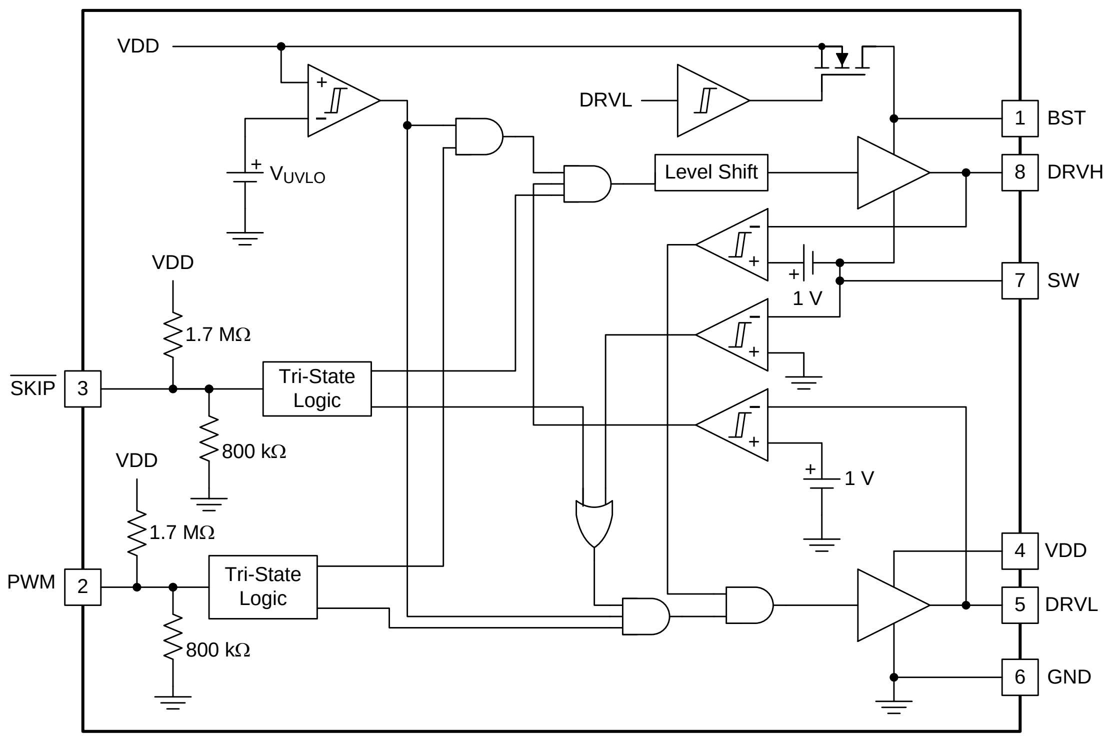
图 14. Efficiency vs Output Current, SKIP Mode

7 Detailed Description

7.1 Overview

The TPS51604 device is a synchronous-buck MOSFET driver designed to drive both high-side and low-side MOSFETs. It allows high-frequency operation with current driving capability matched to the application. The integrated boost switch is internal. The TPS51604 device employs dead-time reduction control and shoot-through protection, which helps avoid simultaneous conduction of high-side and low-side MOSFETs. Also, the drivers improve light-load efficiency with integrated DCM-mode operation using adaptive crossing detection. Typical applications yield a steady-state duty cycle of 60% or less. For high steady-state duty cycle applications, including a small external Schottky diode may help to ensure sufficient charging of the bootstrap capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 UVLO Protection

The UVLO comparator evaluates the VDD voltage level. As V_{VDD} rises, both DRVH and DRVL hold actively low at all times until V_{VDD} reaches the higher UVLO threshold (V_{UVLO_H}). Then, the driver becomes operational and responds to PWM and $\overline{\text{SKIP}}$ commands. If VDD falls below the lower UVLO threshold ($V_{UVLO\_L} = V_{UVLO\_H}$ – Hysteresis), the device disables the driver and drives the outputs of DRVH and DRVL actively low. 图 15 shows this function.

CAUTION

Do not start the driver in the very low power mode ($\overline{\text{SKIP}}$ = Tri-state).

Feature Description (接下页)

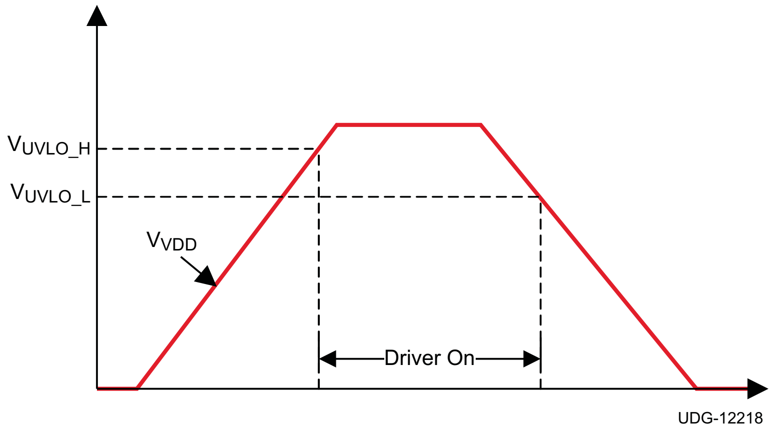


图 15. UVLO Operation

7.3.2 PWM Pin

The PWM pin incorporates an input tri-state function. The device forces the gate driver outputs to low when PWM is driven into the tri-state window and the driver enters a low power state with zero exit latency. The pin incorporates a weak pullup to maintain the voltage within the tri-state window during low-power modes. Operation into and out of a tri-state condition follows the timing diagram outlined in 图 16.

When VDD reaches the UVLO_H level, a tri-state voltage range (window) is set for the PWM input voltage. The window is defined as the PWM voltage range between PWM logic high (V_{IH}) and logic low (V_{IL}) thresholds. The device sets high-level input voltage and low-level input voltage threshold levels to accommodate both 3.3-V (typical) and 5-V (typical) PWM drive signals.

When the PWM exits the tri-state condition, the driver enters CCM for a period of 4 µs, regardless of the state of the SKIP pin. Typical operation requires this time period in order for the auto-zero comparator to resume.

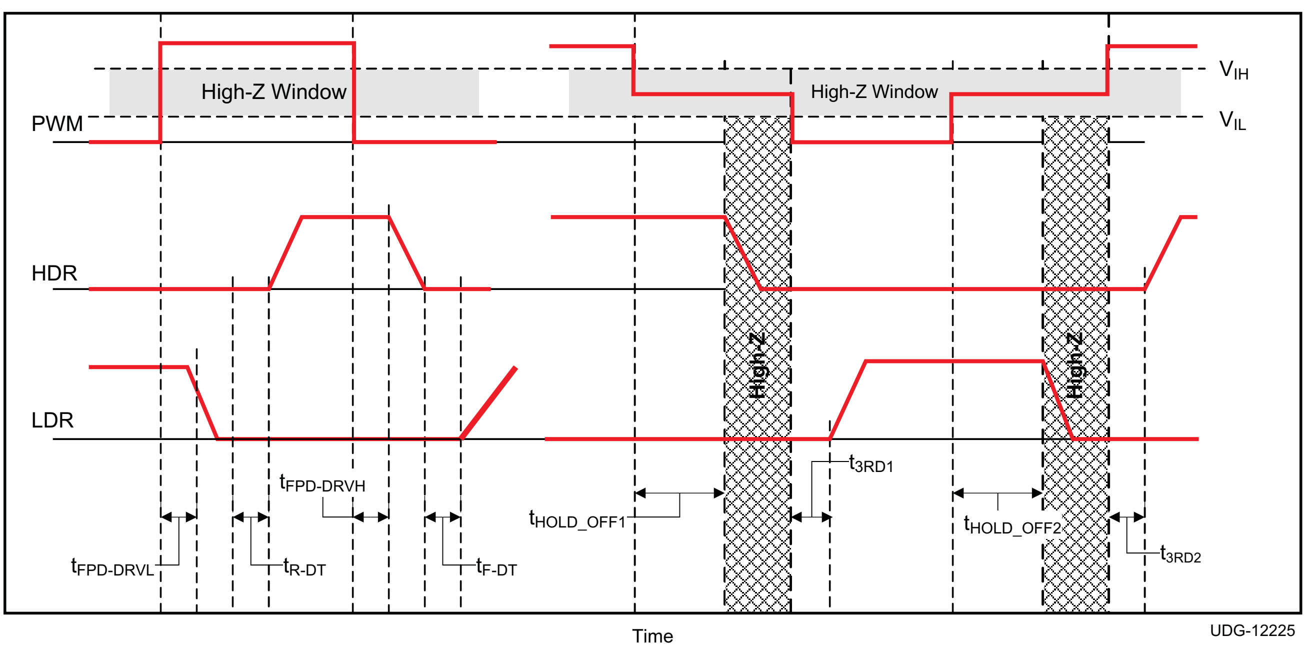


图 16. PWM Tri-State Timing Diagram

Feature Description (接下页)

7.3.3 $\overline{\text{SKIP}}$ Pin

The $\overline{\text{SKIP}}$ pin incorporates the input tri-state buffer as PWM. The function is somewhat different. When $\overline{\text{SKIP}}$ is low, the zero crossing (ZX) detection comparator is enabled, and DCM mode operation occurs if the load current is less than the critical current. When $\overline{\text{SKIP}}$ is high, the ZX comparator disables, and the converter enters FCCM mode. When the $\overline{\text{SKIP}}$ pin is in a tri-state condition, typical operation forces the gate driver outputs low and the driver enters a very-low-power state. In the low-power state, the UVLO comparator remains off to reduce quiescent current. When the $\overline{\text{SKIP}}$ pin voltage is pulled either low or high, the driver wakes up and is able to accept PWM pulses in less than 50 µs.

表 1 shows the logic functions of UVLO, PWM, $\overline{\text{SKIP}}$, DRVH, and DRVL.

表 1. Logic Functions of the TPS51604

UVLO	PWM	$\overline{\text{SKIP}}$	DRVL	DRVH	MODE
Active	—	—	Low	Low	Disabled
Inactive	Low	Low	High (1)	Low	DCM (1)
Inactive	Low	High	High	Low	FCCM
Inactive	High	H or L	Low	High	
Inactive	Tri-state	H or L	Low	Low	Low power
Inactive	—	Tri-state	Low	Low	Very-low power

(1) Until zero crossing protection occurs.

7.3.3.1 Zero Crossing (ZX) Operation

The zero crossing comparator is adaptive for improved accuracy. As the output current decreases from a heavy load condition, the inductor current also reduces and eventually arrives at a *valley*, where it touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The SW pin detects the zero-current condition. When this zero inductor current condition occurs, the ZX comparator turns off the rectifying MOSFET.

7.3.4 Adaptive Dead-Time Control and Shoot-Through Protection

The driver utilizes an anti-shoot-through and adaptive dead-time control to minimize low-side body diode conduction time and maintain high efficiency. When the PWM input voltage becomes high, the low-side MOSFET gate voltage begins to fall after a propagation delay. At the same time, DRVL voltage is sensed, and high-side driving voltage starts to increase after DRVL voltage is lower than a proper threshold.

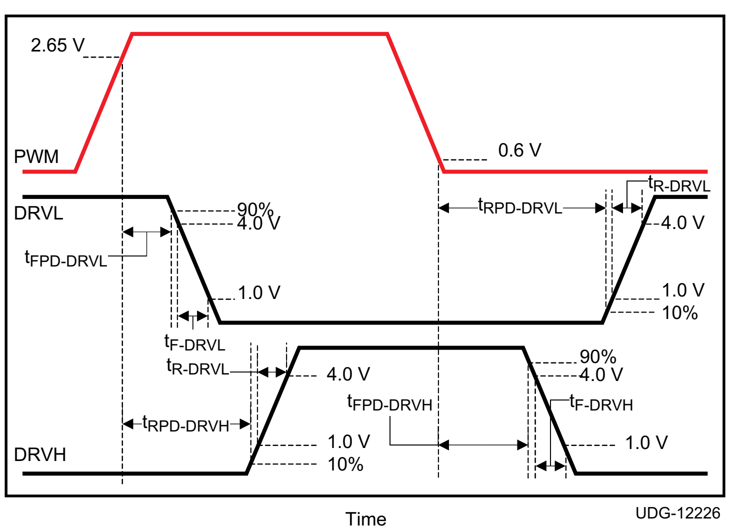


图 17. Rise and Fall Timing and Propagation Delay Definitions

Typical operation manages to near zero the dead-time between the low-side gate turn-off to high-side gate voltage turn-on, and high-side gate turn-off to low-side gate turn-on, in order to avoid simultaneous conduction of both MOSFETs, as well as to reduce body diode conduction and recovery losses. This operation also reduces ringing on the leading edge of the SW waveform.

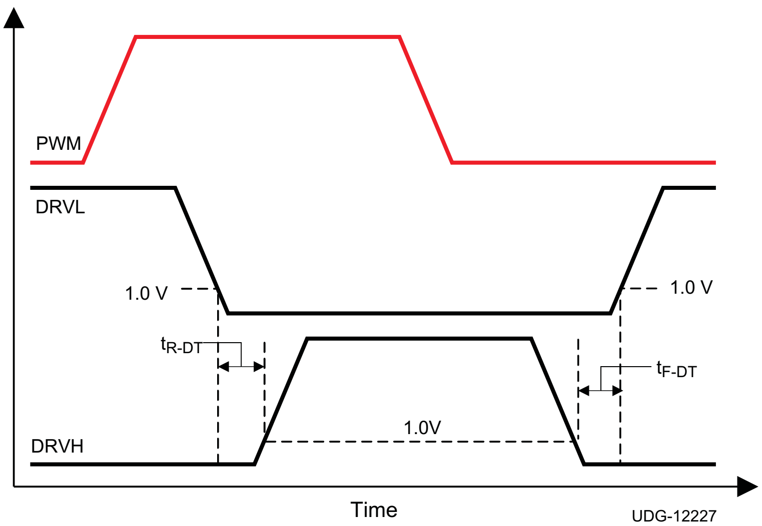


图 18. Dead-Time Definitions

7.3.5 Integrated Boost-Switch

To maintain a BST-SW voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode between the VDD pin and BST pin is replaced by a FET, which is gated by the DRVL signal.

7.4 Device Functional Modes

The TPS51604 device operates in CCM mode when the $\overline{SKIP}$ pin is high, and it enters DCM mode when the $\overline{SKIP}$ pin is low. When both the $\overline{SKIP}$ pin and the PWM pin are in a tri-state condition, it forces the gate driver outputs low and the driver enters a very-low-power state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS51604 driver is optimized for high-frequency CPU V_{CORE} applications. Advanced features such reduced dead-time drive and Auto Zero Crossing are used to optimize efficiency over the entire load range.

8.2 Typical Application

Figure 19 and Figure 20 show a 2-phase design example where TPS51604 device works with the TPS51632 controller and the CSD87381 power block.

Typical Application (continued)

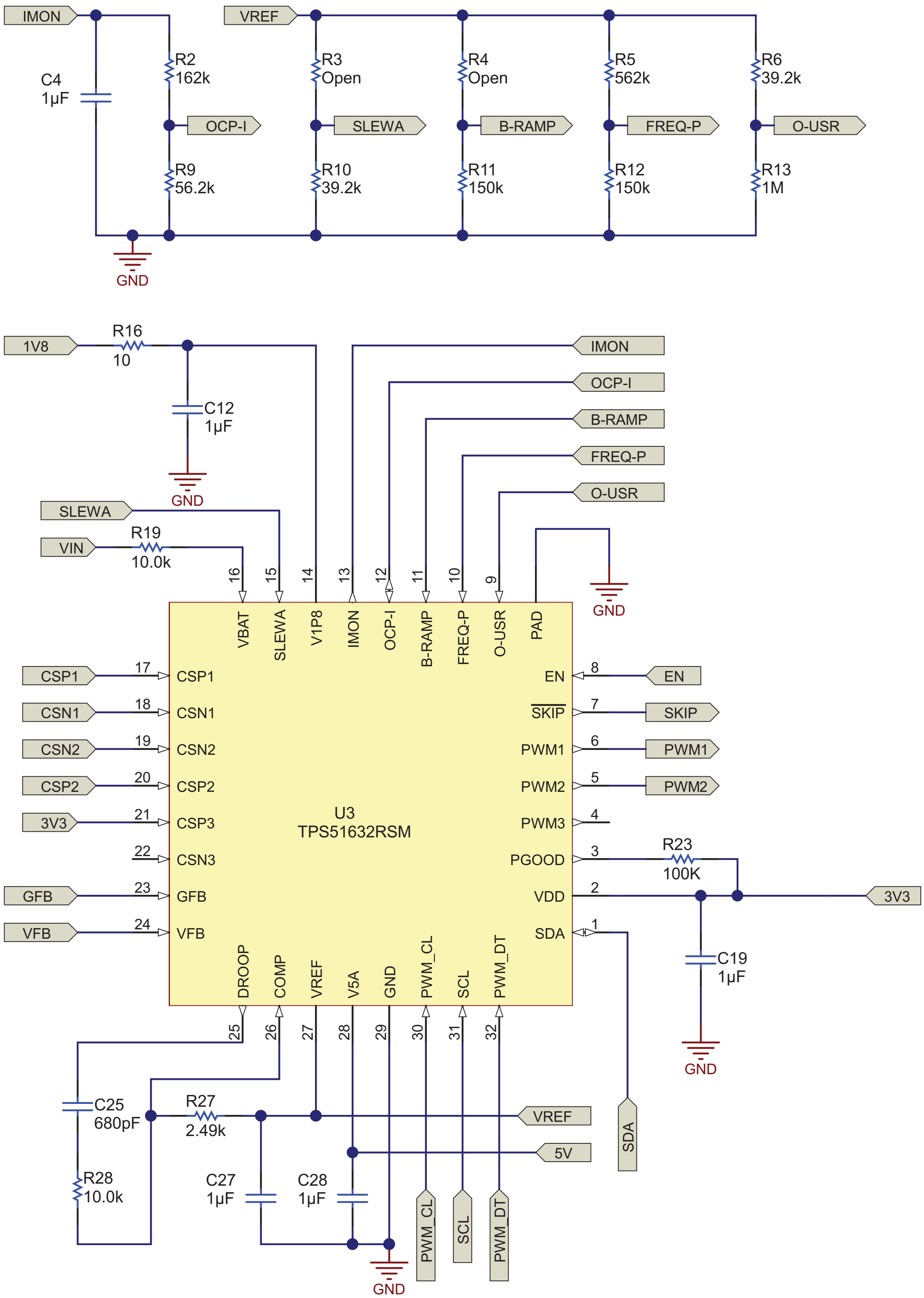


Figure 19. Controller Schematic

Typical Application (continued)

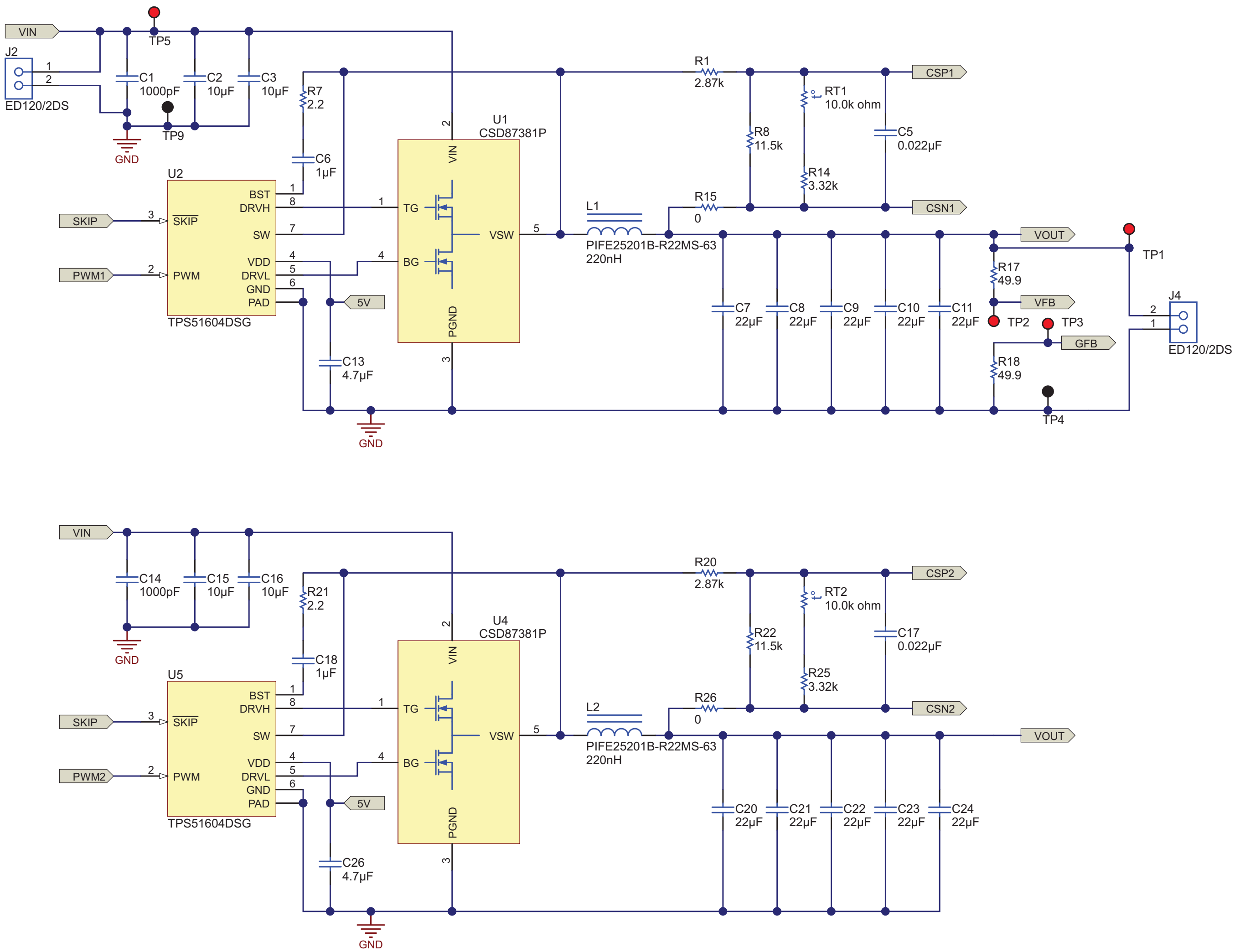


Figure 20. Driver, Power Block, and Output Stage Schematic

Typical Application (continued)

8.2.1 Design Requirements

The design example uses the input parameters summarized in Table 2.

Table 2. Design Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		6	12	20	V
V_{OUT}	Output voltage			1.2		V
V_{P_P}	Output ripple voltage	I_{OUT} = 12 A		20		mV
I_{OUT}	Output current		0		12	A
η	Efficiency	I_{OUT} = 12 A, V_{IN} - 12 V		80%		
f_{SW}	Switching frequency			1000		kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Step 1: Select the Input (VDD) Capacitor

A 5-V power supply is suggested for VDD. Placed a ceramic capacitor with a value of 1 uF or greater between VDD and GND.

8.2.2.2 Step 2: Select Boot Capacitor and Boot Resistor

The boot capacitor is the power supply for high-side driver. Place a ceramic capacitor with a value of 0.1 µF or greater between the BST pin and the SW pin.

To reduce the voltage spike on switch node, use a boot resistor with a value of several Ohms in series with boot capacitor to slow the turn-on of high-side FET.

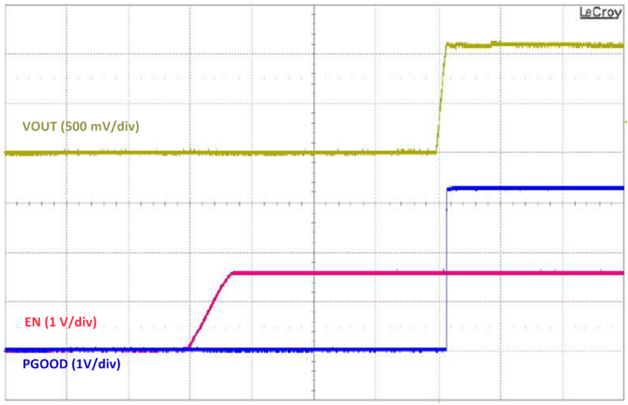
8.2.2.3 Step 3: Establish Connection Between TPS51604 and Controller

Connect the PWM pin of the TPS51604 device to the PWM pin of the controller. The TRIP pins can be used for DCM mode or very-low-power state. Leave the TRIP pin floating if it is not in use.

8.2.2.4 Step 4: Establish Connection Between TPS51604 and the Power Block

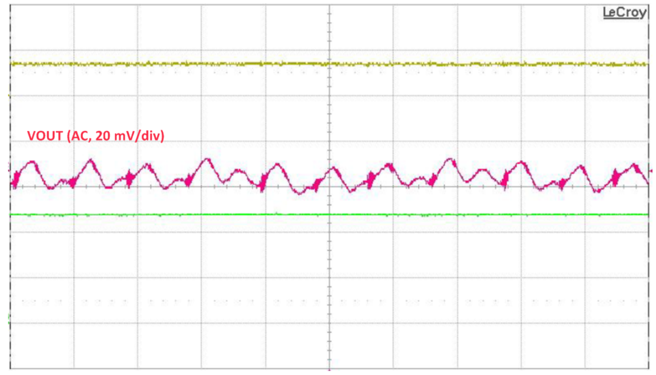
Connect the DRVH pin of the TPS51604 device to the gate of the high-side FET of the power block. Connect the DRVL pin of the TPS51604 device to the gate of the low-side FET of the power block. Connect the SW pins of the TPS51604 device to the switch node as required by the high-side driver fo the power block.

8.2.3 Application Curves



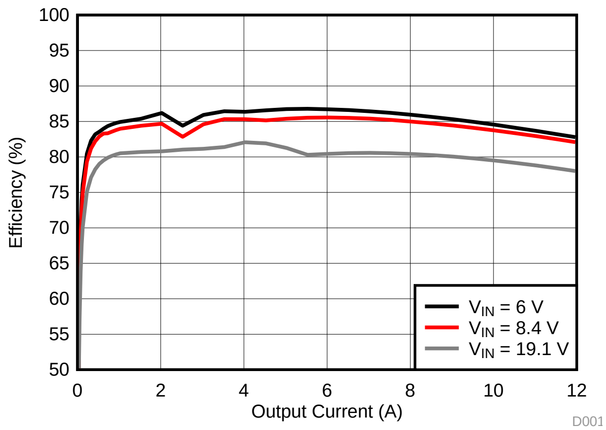
V_{IN} = 12 V I_{OUT} = 0 A

Figure 21. Enable Turn-on



V_{IN} = 7.2 V I_{OUT} = 12 A

Figure 22. Output Ripple



f_{SW} = 1 MHz

Figure 23. Efficiency vs. Load

9 Power Supply Recommendations

The voltage range for the VDD pin is between 4.5 V and 5.5 V. A 5-V power supply is recommended for the VDD pin of the TPS51604 device.

10 Layout

10.1 Layout Guidelines

To improve the switching characteristics and design efficiency, these layout rules must be considered:

- Locate the driver as close as possible to the MOSFETs.
- Locate the VDD and bootstrap capacitors as close as possible to the driver.
- Pay special attention to the GND trace. Use the thermal pad of the package as the GND by connecting it to the GND pin. The GND trace or pad from the driver goes directly to the source of the MOSFET, but should not include the high current path of the main current flowing through the drain and source of the MOSFET.
- Use a similar rule for the switch-node as for the GND.
- Use wide traces for DRVH and DRVL closely following the related SW and GND traces. A width of between 80 and 100 mils is preferable where possible.
- Place the bypass capacitors as close as possible to the driver.
- Avoid PWM and enable traces going close to the SW and pad where high dV/dT voltage can induce significant noise into the relatively high-impedance leads.

A poor layout can decrease the reliability of the entire system.

10.2 Layout Example

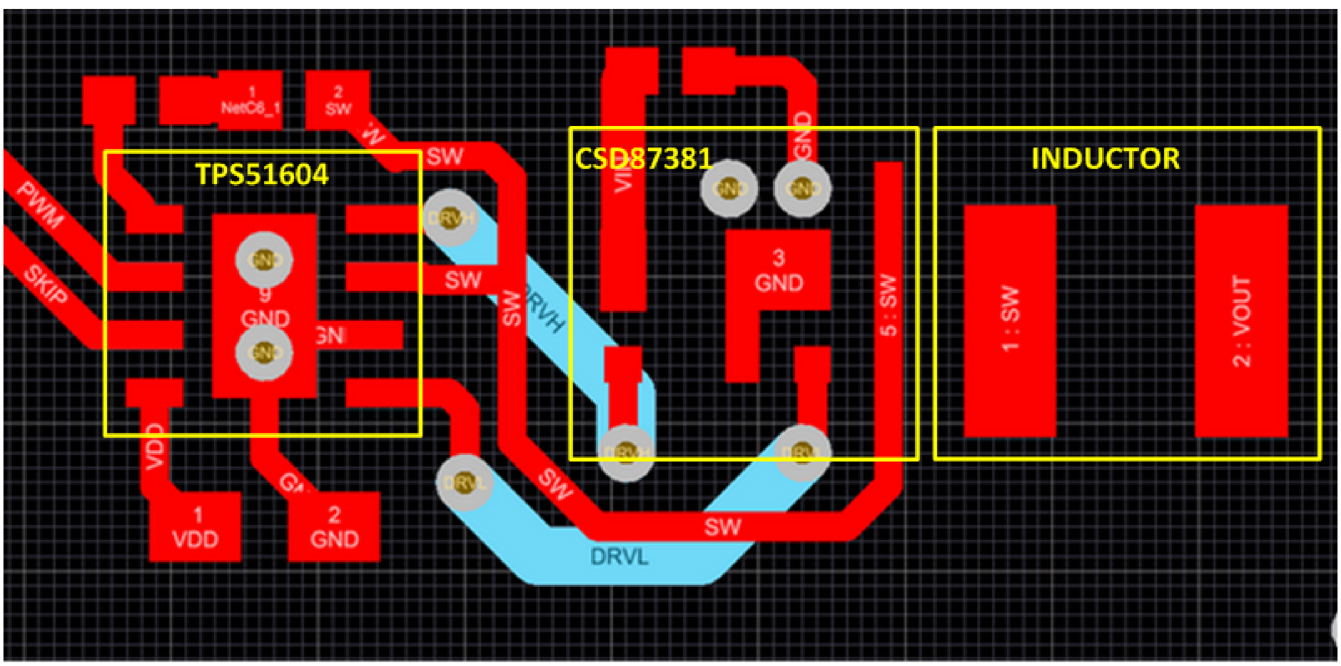


图 24. Layout Recommendation

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

如需 Power Stage Designer，请访问 www.ti.com.cn/tool/cn/powerstage-designer。

11.2 文档支持

11.2.1 相关文档

- 用于 Tegra® CPU 的 TPS51632 *3-2-1 相 D-Cap+ ™降压无驱动器控制器* SLUSBM3
- CSD87330 *30V 同步降压 NexFET™ 电源块* SLPS284

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

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11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51604DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1604	Samples
TPS51604DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	1604	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS51604 :

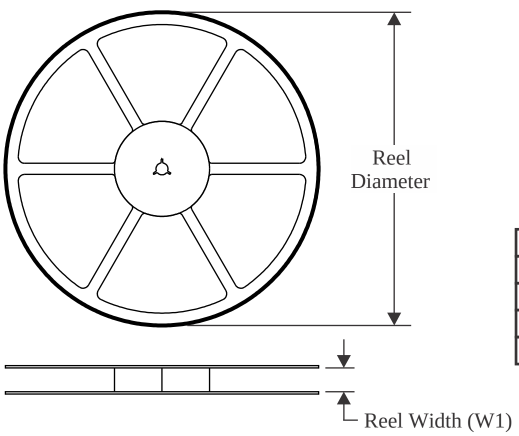
- Automotive : TPS51604-Q1

NOTE: Qualified Version Definitions:

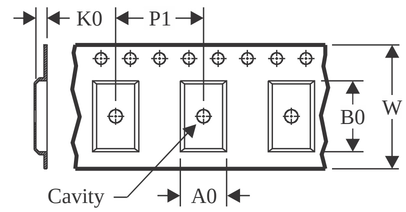
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

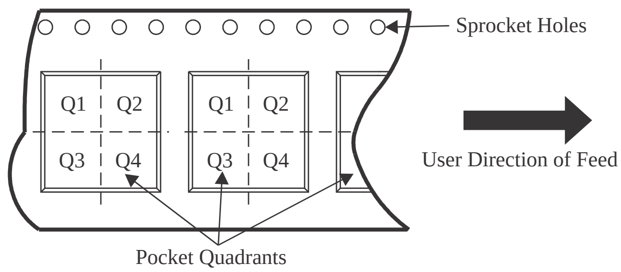


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

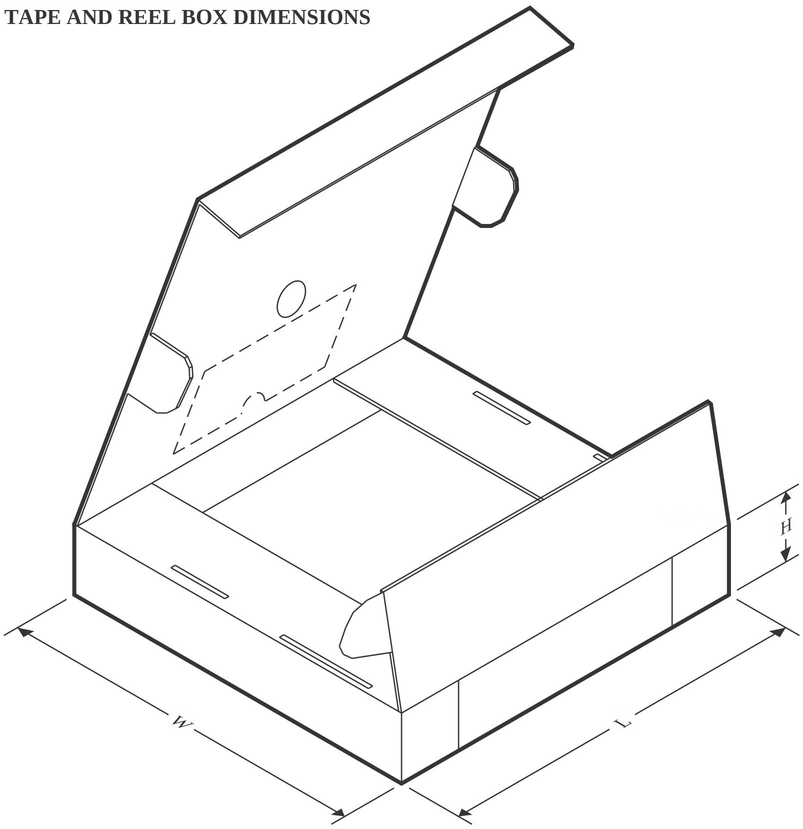
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51604DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51604DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51604DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
TPS51604DSGT	WSON	DSG	8	250	182.0	182.0	20.0

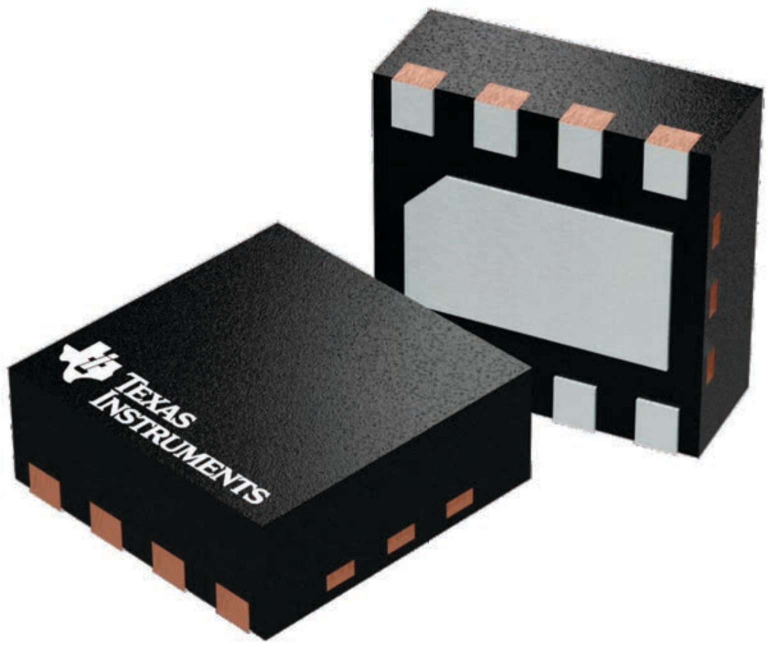
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

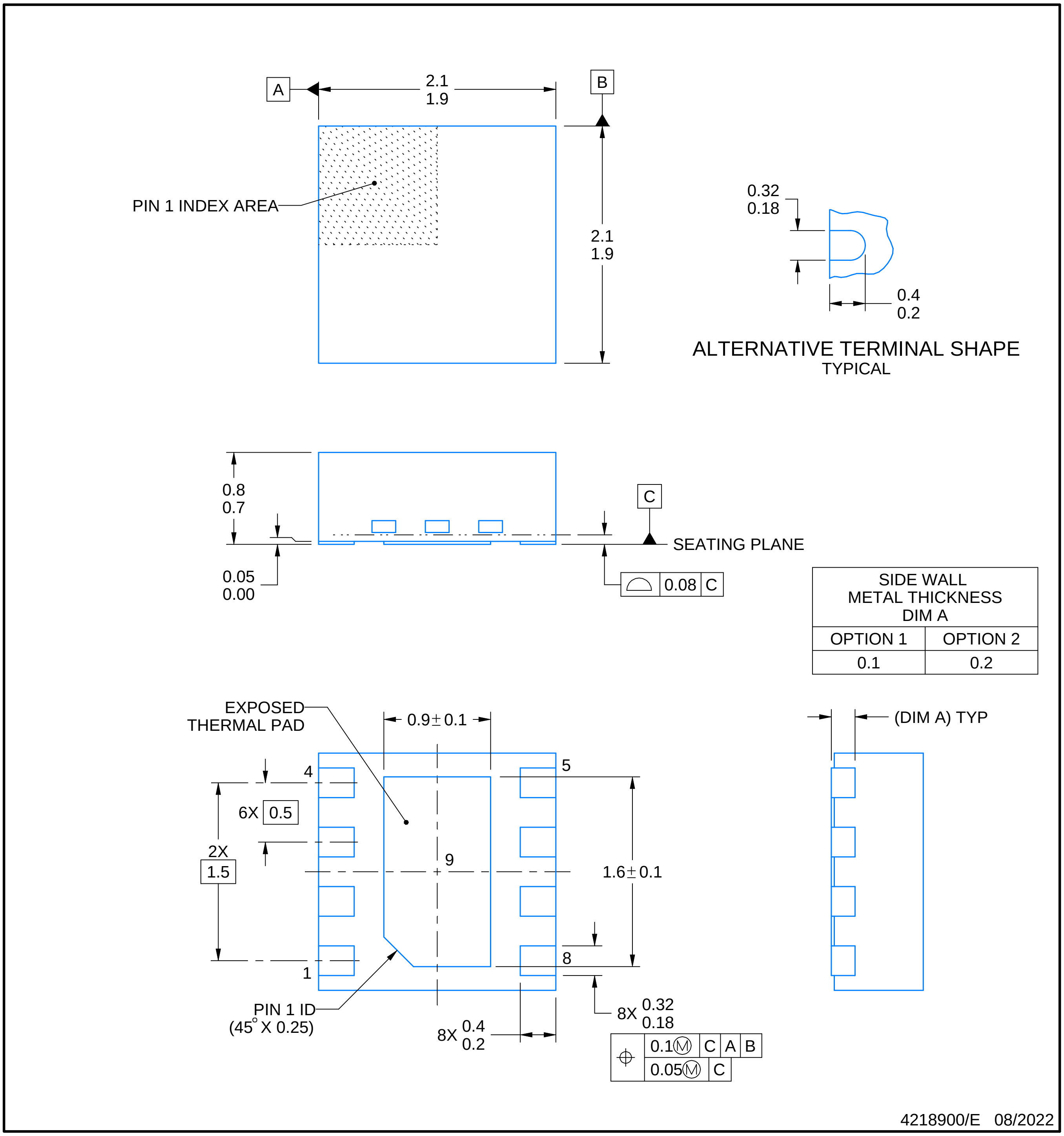
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

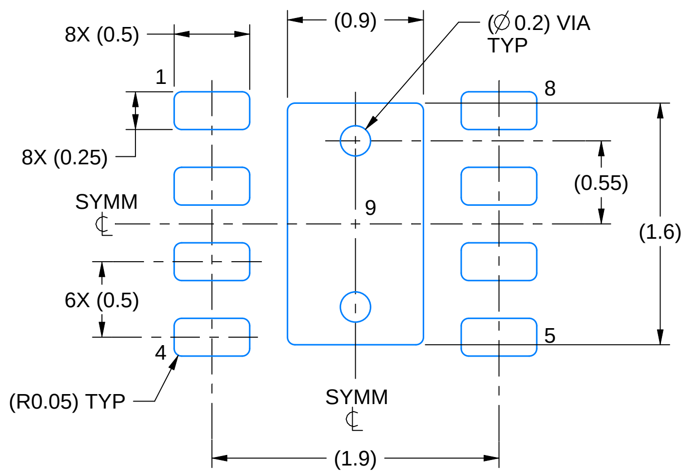
PLASTIC SMALL OUTLINE - NO LEAD



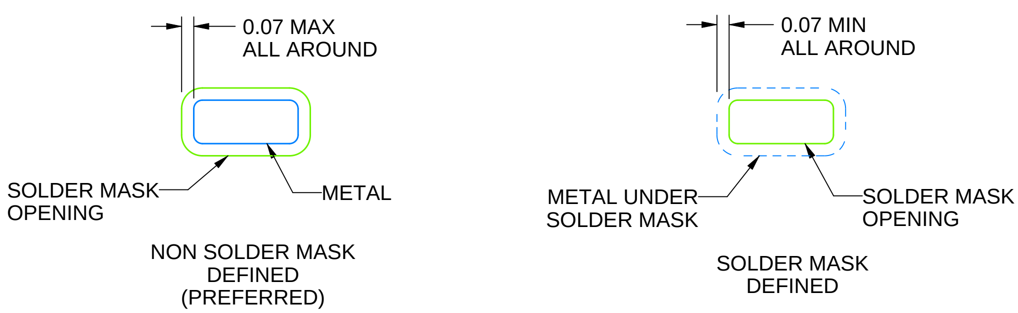
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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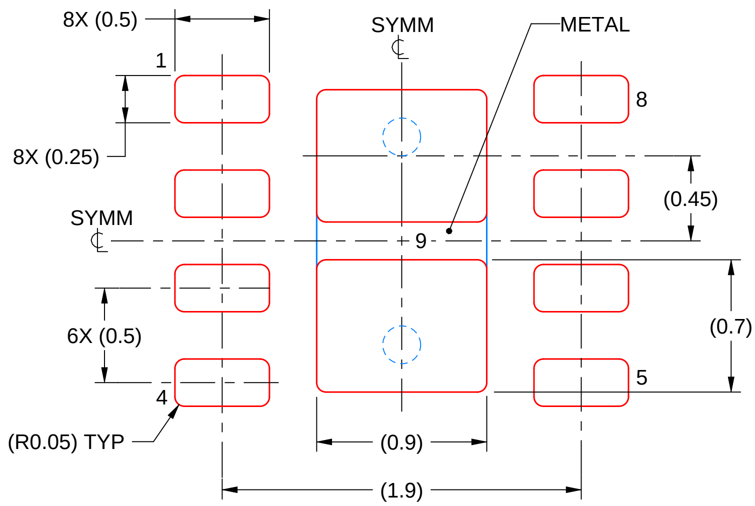
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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